GaSb nanowire transistors with process induced strain

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Abstract

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With the constant downscaling of Si transistors reaching its limits, other alternatives have been actively researched the past decades. Group III-V semiconductors are excellent materials with generally high carrier mobilities that can replace Si in transistors. Strain has been used for some years to improve silicon technology, and it can also be applied to III-V materials to make them perform even better. In this work, GaSb nanowire transistors were strained using PECVD to deposit a stressing film of Si₃N₄ and the effects on the electrical characteristics investigated.

The deposited films ranged between thicknesses of 40-104 nm, with stresses in the range 300-2000 MPa. Raman spectroscopy measurements showed a strain in the nanowires up to 0.5%. The effect on the threshold voltage from the Si₃N₄ films containing positive charges made it challenging to separate the effects from this and the effects from strain. All samples exhibited a reduction in current but a significant increase in the on/off-ratio, making the strained devices turn off much better than untreated devices, with an on/off-ratio increase of up to 70 times observed. The results obtained here show that this method of process induced strain could see uses in order to reduce power consumption.
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Abbreviations

Al₂O₃  Aluminum Oxide
ALD  Atomic Layer Deposition
CVD  Chemical Vapor Deposition
GaSb  Gallium Arsenide
GaSb  Gallium Antimonide
HH  Heavy Hole
LH  Light Hole
LO  Longitudinal Optical
InAs  Indium Arsenide
MOCVD  Metal Organic Chemical Vapor Deposition
MOS  Metal-Oxide-Semiconductor
MOSFET  Metal-Oxide-Semiconductor Field-Effect Transistor
N  Nitrogen
PECVD  Plasma Enhanced Chemical Vapor Deposition
RF  Radio Frequency
RIE  Reactive Ion Etch
SEM  Scanning Electron Microscopy
SF₆  Sulfur hexafluoride
Si  Silicon
SiO₂  Silicon dioxide
Si₃N₄  Silicon Nitride
TMA  Trimethyl Aluminium
TO  Transverse Optical
UVL  Ultra Violet Lithography
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Chapter 1

Introduction

It has been 70 years since the first transistor was invented, in 1947. Without this invention, modern electronics would appear very different, as the rapid technological advancements the world has experienced for the past decades would not have been feasible. In fact, the possibilities that this device allowed were quickly realized and research to improve this new technology took off immediately. A few years later, in 1965, one of the founders of Intel, Gordon E. Moore, observed a pattern in the advancement of transistors and proposed a method to predict future progress. This became famous as Moore’s Law, and states that every two years, the density of transistors in integrated circuits will double. Moore’s law proved surprisingly accurate and has been used to predict the advancement of transistors until very recently[1].

Silicon (Si) has been the dominant material in semiconductor technology for a long time due to its high abundance on earth, making it an easy obtainable and cheap material while still having good electrical and chemical properties. The most common type of transistor has been the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), with silicon as the semiconductor and silicon dioxide SiO$_2$ as the oxide. Following Moore’s Law has simply been done by downscaling this structure, which has many advantages. A transistor behaves as a switch that can be turned on or off, and as a result of downscaling, the switching time decreases due to lower number of charges that have to be moved from or to the channel in each switching event, and the switching energy for each individual transistor is reduced[2].

However, Moore’s law can not continue endlessly. With no other drawbacks, it will eventually hit a stop as a result of natural limitations due to the finite size of molecules that the devices are comprised of. There is still a long way to go
before this limit is reached, and other drawbacks do appear. The most significant drawback that has been highly relevant over the past years is the dissipation of power due to quantum mechanical tunneling that allow current to escape through the thin oxide, leading to overheating. To continue the trend of developing faster and more energy efficient transistors, the issue with leakage current needs to be resolved.[3].

1.1 Alternatives to Si for MOSFETs

Over the more recent decades, the quest to find new semiconductor materials or design new transistor structures have seen a huge growth across the world. The research has provided results, and new technology is being released onto the market every year, such as Intel revealing their 22 nm tri-gate technology, as an evolution from planar geometry, back in 2011[4].

Carbon based technology like carbon nanotubes or graphene looked initially very promising, but seem to recently have fallen out of favor for more established approaches. The use of III-V materials instead of Si as semiconductor are seeing the most research currently. While Si is found in group IV in the periodic system, III-V materials are combinations of elements from groups III and V. A large amount of combinations of materials and compositions are possible, many of which have very good electrical properties, such as high carrier mobility which leads to a higher current than Si at the same dimensions[2].

Developers are still reluctant to transition to III-V however, and are trying to squeeze every last bit of potential possible out of Si. There are a couple of reasons for why the use of Si has been able to be extended for so long. The most obvious is the expensive costs of both the III-V materials compared to Si, and the cost of transitioning factories from Si production to III-V production.

Physically, the use of high-κ oxides rather than the intrinsic SiO₂ allow the same capacitance as SiO₂ but at a thicker layer, reducing the amount of leakage current from tunneling. Another reason why Si is still dominant is the introduction of strain. It has been found that by straining a semiconductor material, properties such as the carrier mobility can be improved significantly. For many years now, the most high-performing generations of logic technologies have utilized strained Si semiconductors to continue improving. This applies primarily to p-type transistors as the hole mobility is lower than the electron mobility due to the much higher mass of holes[5].
Nanowires are researched heavily as a replacement for the standard planar or fin structures. One big advantage of nanowires is that heterostructures with a large lattice mismatch can be grown into a stable nanowire which is very difficult or impossible in standard planar structures. Due to the shape of nanowires, it is possible to create gates that are wrapped around the wire for high control. Nanowires have many advantages like these, and also have high scalability and allow for tight packaging if designed vertically[6].

In this work, many of these technologies are combined, and nanowire transistors made from the high hole mobility III-V material GaSb are strained in order to try and improve its performance. This is done by depositing a stressing film on the devices by Plasma Enhanced Chemical Vapor Deposition (PECVD).
Chapter 2

Theory

This chapter will cover the relevant topics of theory needed to understand this report. It will assume that the reader has basic university knowledge of physics and electronics, but will have a brief repetition on the origin of band structure and the basic principles of a MOSFET. There will then be more detailed information about strain and its effects on materials, as well as an explanation of the film deposition method and measurement techniques used.

2.1 Band structure

As is known from the Pauli exclusion principle, no two identical fermions can be in the same quantum state simultaneously. In an atom, this gives rise to the various quantum numbers to describe each electron orbiting the nucleus, that must be different for each electron. When atoms are packed together as a crystal, the exclusion principle still applies. As the atomic orbitals of atoms overlap, the energy levels that are identical in every individual atom of a material will now spread out over a larger energy range. These areas are called energy bands, and between them, where there are no allowed states for electrons, are energy gaps, see Fig. 2.1.
In Fig. 2.1, $E_F$ is the Fermi level. The Fermi level is defined as the energy level where there is a 50% chance of electron occupation[7]. Below the Fermi level, the majority of levels are occupied, and above it, the majority are unoccupied. If the Fermi level is in the midgap as in Fig. 2.1, the material is a semiconductor, with $E_C$ and $E_V$ corresponding to the edge of the conduction and valence bands respectively. $E_g$ is the size of the band gap.

In reality, the band structure is a bit more complicated than the simplification of conduction and valence bands. In a semiconductor, there is symmetry all across the crystal with atoms positioned periodically. A Brillouin zone has the definition that it is the region of reciprocal space that is closer to a given reciprocal lattice point than to any other[8]. It is shaped nearly as an octahedron in the zinc blende structure of the GaSb crystal, see Fig 2.2.
Figure 2.2: The first Brillouin zone of GaSb. The $\Gamma$-point is located in the center, with the $X$-point shown along the $x$-axis, and the $L$-point shown in the top frontal hexagonal area. In total there is one $\Gamma$-point, three $X$-points and four $L$-points. Image taken from [9].

Along the different directions in the Brillouin zone, the band structure looks different, see Fig. 2.3. The band gap $E_g$ shown here is the same band gap as in Fig. 2.1, corresponding to the distance between the lowest energy valley and the highest hole energy. The conduction and valence bands begins at these points and include the rest of the states around the Brillouin zone shown in this figure.

Figure 2.3: The band structure of GaSb. The lowest energy of the conduction band is located at the $\Gamma$-valley, with a direct band gap between this point and the peak of the states for heavy and light holes. Image adapted from [10].
2.2 MOSFET basics

A MOSFET consists, as the name suggests, of a metal layer, an oxide layer and a semiconductor layer. The devices used in this work use undoped nanowires for the channel, and are not top gated with the oxide and metal layers directly on top of the semiconductor, but back gated, where the gate voltage is normally applied to the metal chuck beneath the sample instead. The basic principles of this device will be introduced in this section.

A MOSFET has three terminals, at the source, drain and the gate. The gate terminal is the metal layer part of the MOS structure, and the source and drain terminals are connected to the semiconductor. The active region of the MOSFET is the channel, located between the source and drain regions[11], see Fig. 2.4.

Figure 2.4: An illustration of a MOSFET, showing the Si substrate, SiO$_2$ layer, nanowire (in red), source, and drain. The current flow, gate voltage and drain-source voltage are indicated.

The channel behavior is controlled by the gate terminal. When a voltage $V_g$ is applied to the gate, the resulting electric field attracts carriers in the semiconductor toward the oxide. If a voltage, $V_{ds}$ is applied between the drain and source regions, a current will flow through the channel, giving rise to the ON-state of the device. The current will increase linearly while $V_{ds}$ is low, until it reaches a saturation level after which the current is ideally constant regardless of $V_{ds}$. For higher $V_{ds}$, $V_g$ alone controls the current[12]. Fig. 2.5 shows the band structure difference between ON and OFF-states for a pFET, as used in this project, where $E_C$ is the conduction band, $E_V$ the valence band, $E_{f,S}$ the source Fermi level and $E_{f,D}$ the drain Fermi level. A positive $V_g$ gives a higher potential barrier that prohibits transport in the valence band.
The threshold voltage $V_T$ of a device is the minimum gate voltage required for conduction between the source and drain terminals. This parameter is usually linearly extracted from a transfer characteristics curve, where the drain current is plotted against the gate voltage. With $|V_g| < |V_T|$, the device is turned off, and with $|V_g| > |V_T|$, the device is turned on. In an enhancement mode p-type device as is used in this work, $V_T$ is ideally somewhat below zero so that the device is in its off-state without any gate bias applied\[12\].

The transconductance $g_m$ of a device relates the gate voltage to the current through the channel. It describes how effective the gate voltage is at altering the current through the channel. The transconductance can be calculated anywhere in a transfer characteristic curve using

$$g_m = \frac{\Delta I_{ds}}{\Delta V_g},$$

(2.1)

where $\Delta I_{ds}$ is the change in source-drain current and $\Delta V_g$ the change in gate voltage, but usually only its maximum value is reported\[12\].

The total ON-state resistance $R_{\text{tot}}$ through the device is a sum of the wire resistance, $R_w$, the drain resistance $R_d$ and the source resistance, $R_s$. In this work, the resistance at the source and drain contacts are assumed to be equal, so that the total sum is

$$R_{\text{tot}} = R_w + 2R_c$$

(2.2)

where $R_c$ represents the contact resistance. To separate between the wire resistance and contact resistance, a four-probe method can be used. The nanowires used in this project each have four contacts along them, and a probe is attached to each contact for this method. By applying a voltage to the outer two probes, a current, $I$ will flow through the channel and the two inner probes will experience a voltage.
drop, $V$. The wire resistance is then simply calculated using an Ohmic equation $R_w = V/I$ and can thus be isolated from the total resistance\cite{13}.

### 2.3 Stress and strain

Stress $\sigma$ is defined as force $F$ per unit area $A$ that is perpendicular to the direction of the applied force. As such, it has the dimension $\text{Nm}^{-2}$, which is the same dimension as pressure, measured in Pascal, Pa. Stress can be either tensile or compressive depending on how it is applied, see Fig. 2.6. A solid material exposed to stress will deform from the pressure. This deformation is called strain, $\epsilon$, and is defined as $\Delta l/l$ where $l$ is the original length of the solid, and $\Delta l$ the change in length when exposed to stress\cite{8}.

![Figure 2.6: Images showing tensile (a) and compressive (b) strain and deformation of an object due to stress.](image)

The relation between stress and strain depends on the material, and is described by the Young’s modulus, $Y = \sigma/\epsilon$, with the same unit (Pa) as stress. $Y$ varies a lot for different materials, and has a value of 0.1 GPa for rubber, and 1000 GPa for carbon nanotubes, with metals and other materials in between\cite{8}. Young’s modulus and other parameters for materials used in this project will be discussed later in this chapter, in section 2.4.

At the atomic level, strain in a material occurs when the distance between atoms is changed from its equilibrium. With low external stress, the strain will change as the equilibrium distance $a$ between two atoms is altered, but when the stress is removed the atoms will return back to their equilibrium position, hence this is called elastic strain. With higher amounts of stress, the material may begin to
permanently deform as defects and dislocations arise, which is known as plastic deformation. Eventually, at a high enough stress the material will break, eg. through a chain of dislocations forming cracks through the object[8].

### 2.3.1 Stress in thin films

The stress in the thin films used in this work arises from the PECVD deposition technique. The stress does not favor any particular direction and is as such biaxial within the plane of the film. If the plane of the film is denoted as the $x$ and $y$ directions, then the stress is locked in these directions and no stress will push down on or away from the substrate in the $z$ direction. The substrate will however feel the opposite type of stress, tensile or compressive, than the film, due to Newton’s third law[14]. Fig. 2.7 is an illustration of the stresses in the film and substrate.

![Figure 2.7: An illustration of how the substrate bows due to the film stress. The dimension of the $z$-direction is exaggerated to show the radius of the curvature $r$, and where $t_s$ is the substrate thickness, $t_f$ the film thickness and $F$ the various forces.](image)

A compressed film will try to expand to its equilibrium, and a tensile stressed film will try to contract. If the stressed film is located on a thin substrate, the stress will cause the substrate to bow. A compressively stressed film will cause the
substrate to bow with the film on the convex side, as in Fig. 2.7, while a tensile stressed film will be on the concave side[15].

With the above knowledge, and if the Young’s modulus and Poisson ratio for the substrate are known, the stress in the film can be calculated. This was first done by G.G. Stoney in 1909, and the resulting equation

$$\sigma_f = \left( \frac{Y}{1-\nu} \right) \frac{t_s^2}{6rt_f}$$

(2.3)

is therefore named Stoney’s equation. If the film is compressively strained, the stress will be negative, and with tensile strain the stress will be positive.

In this equation, $\sigma_f$ is the film stress, $Y$ Young’s modulus for the substrate material, $\nu$ Poisson’s ratio for the substrate material, which relates the strain in the direction of the force and the perpendicular plane (as illustrated in Fig. 2.6), $t_s$ the substrate thickness, $t_f$ the film thickness, and $r$ the radius of curvature of the substrate due to the bowing. For Stoney’s equation to work, it is assumed that the film and substrate thicknesses are uniform, that the film and substrate have the same bowing, that the film and substrate are homogeneous, isotropic and linearly elastic, and that any any stress within the material is uniform[16].

The curvature $r$ is most commonly calculated by measuring the bowing of the substrate, which can be done by optical interferometry, laser beam reflection, the change of electrical capacitance between surfaces[15], or, as in this case, by measuring the height difference along a line between two points on the surface before and after deposition using a profilometer. In a profile measurement, the curvature $r$ can be calculated using

$$r = \frac{(L/2)^2}{2h_{\text{max}}},$$

(2.4)

where $L$ is the length of profile scan and $h_{\text{max}}$ the highest point of the scan. By scanning before and after film deposition, equations 2.3 and 2.4 can be combined into

$$\sigma_f = \frac{8Yt_s^2(h_{\text{pre}} - h_{\text{post}})}{6(1-\nu)L^2t_f},$$

(2.5)

where $h_{\text{pre}}$ is the maximum height of the scan before film deposition, and $h_{\text{post}}$ the maximum height of the scan after film deposition.

When the stress is too high, different effects occur in a thin film depending on the type of stress applied. With a tensile stress, the film will break by cracking. With
Chapter 2. Theory

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a compressively stressed film there are two main types of film failure, buckling-driven interface delamination and edge delamination. The high stress causes the entire film to buckle or twist in various ways, and the two types suggest bending away from the interface with the substrate or causing relief mainly at the edges[17].

2.3.2 Strain effects on band structure

Since the band structure depends heavily on the interaction between adjacent atoms in a crystal, it comes naturally that the band structure is affected by strain. A number of models have been developed throughout the years, and it’s been found that modeling the effects in the valence band is much more complicated than in the conduction band. While it is enough to model electron mobility change due to strain using only deformation potentials, different approaches are needed for the hole mobility, due to the overlapping of heavy and light hole bands[18].

The enhanced carrier mobility comes from a disruption of the crystal symmetry. As the strain in this work comes from a film that strains in the $x,y$-plane but not in the $z$-direction, it is biaxially strained. The total strain can be divided into a hydrostatic strain and shear strain, where the shear strain is what causes the change in crystal symmetry. Every group IV and III-V semiconductor has its valence band maxima at the Γ point, as in Figs. 2.2 and 2.3 for GaSb. GaAs, similar to GaSb, also has its conduction band edge at the Γ point and a direct band gap. In GaAs, the effect of this biaxial strain on the conduction band is simply to shift the energy of the band edge[18], and it is here assumed that the physics is similar for GaSb.

The Γ point maxima is degenerate with both heavy holes, HH, and light holes, LH, contributing to hole transport. The shear strain that is a result of there being no stress in the $z$-direction changes the angles of bonds between atoms in the crystal. These bonds consist of $p_x$, $p_y$, $p_z$ and $s$ states. The $p$ states are directional and their projections along the different crystal directions give rise to the LH states in one direction, and the HH states in the perpendicular direction. When the angles between these bonds is altered, the weight from each of these four bonds changes from being equal to being unevenly distributed. The result is that the degeneracy of the LH and HH bands is lifted. With biaxial tensile strain, the out-of-plane HH band energy decreases and the LH band energy increases, and in-plane, the opposite occurs. As such, the hole transport contribution is dominated by light holes out-of-plane, and by heavy holes in-plane. The shift in band energy thus leads to a change in the apparent hole mass[18].
While it is assumed that the strain in this work is biaxial, it is worth mentioning an additional effect that occurs when the strain is uniaxial. If the stress is only applied along the $x$-direction rather than in the $x,y$-plane, shear strain arises in an additional orientation. This added shear strain causes larger distortion of the symmetry than biaxial strain does. The result is that rather than only raising or lowering their energy, the LH and HH bands may also change their curvature, called warping. The additional shear strain typically makes uniaxial strain better for mobility enhancement than biaxial strain, but for both types of strain, the symmetry of the axes on which the stress is applied matters. If the stress is applied along an axis with low symmetry, it will have a higher effect on the crystal symmetry, and thus the band structure, than if it is applied along an axis with high symmetry[18]. Fig. 2.8 is a simulation by [18] of the LH and HH bands of Si under stress. Keep in mind that the physics of the bands in Si is different than the III-V materials due to different crystal structures, but it is an example of how bands may shift in energy and warp. Even without band warping, splitting of the bands is a good effect as it leads to less band-to-band scattering and a larger

![Figure 2.8: A simulation of the LH and HH bands in Si under varying amounts of stress. The left image is without stress, the center image with 1 GPa biaxial stress and the right image with 1 GPa uniaxial stress. When stress is applied, the LH and HH energies will separate, and the bands may begin to warp. Hole mobilities, $m^*$, for each case are also shown. Image adapted from [18].](image)

While tensile and compressive strain alter the bands differently, both types of strain increase hole mobility. With biaxial compressive stress, it has been simulated that up to 2.3x increased mobility is possible in GaSb, with biaxial tensile stress up to 1.4x, uniaxial compressive 4.3x and uniaxial tensile 2.3x. This is very dependent on the crystal direction[19].

Using PECVD to apply a film of Si$_3$N$_4$ as in this work has previously been done to show a 3.86x increase hole mobility in a planar GaSb MOSFET. A heavy hole
mass reduction from 0.32 to 0.24 at 2.0% biaxial strain was achieved[20]. A similar method has also been used to apply uniaxial stress to a quantum well FET with InGaSb which increased the transconductance by as much as 60%[21].

2.4 Material properties

Some of the material properties relevant for electronic applications of Si, GaSb, InAs and GaAs are listed in Table 2.1. Si is included since it is the most common semiconductor material and used for comparison. The nanowire material used in this work is GaSb. It is grown on top of an InAs segment however, which could be relevant during the Raman measurements. GaAs is also shown since it is mentioned in this chapter.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaSb</th>
<th>InAs</th>
<th>GaAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal structure</td>
<td>Diamond</td>
<td>Zinc Blende</td>
<td>Zinc Blende</td>
<td>Zinc Blende</td>
</tr>
<tr>
<td>Young’s modulus (GPa)</td>
<td>130</td>
<td>63.1</td>
<td>51.4</td>
<td>85.9</td>
</tr>
<tr>
<td>Poisson ratio</td>
<td>0.28</td>
<td>0.31</td>
<td>0.35</td>
<td>0.31</td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>1.12</td>
<td>0.726</td>
<td>0.354</td>
<td>1.424</td>
</tr>
<tr>
<td>Electron mobility (cm²V⁻¹s⁻¹)</td>
<td>1.4 · 10³</td>
<td>3 · 10³</td>
<td>4 · 10⁴</td>
<td>8.5 · 10⁴</td>
</tr>
<tr>
<td>Hole mobility (cm²V⁻¹s⁻¹)</td>
<td>4.5 · 10²</td>
<td>1 · 10³</td>
<td>5 · 10²</td>
<td>4 · 10²</td>
</tr>
<tr>
<td>Refractive index</td>
<td>3.42</td>
<td>3.8</td>
<td>3.51</td>
<td>3.3</td>
</tr>
<tr>
<td>TO phonon energy (cm⁻¹)</td>
<td>508.1</td>
<td>224.1</td>
<td>~218</td>
<td>267.8</td>
</tr>
<tr>
<td>LO phonon energy (cm⁻¹)</td>
<td>508.1</td>
<td>233.0</td>
<td>~234</td>
<td>291.2</td>
</tr>
</tbody>
</table>

2.5 Plasma Enhanced Chemical Vapor Deposition

Plasma-Enhanced Chemical Vapor Deposition (PECVD) is, as the name suggests, a type of Chemical Vapor Deposition (CVD) where the reaction process between reactants occur in a plasma. PECVD is generally used to deposit SiO₂ or Si₃N₄ films but can also be used to deposit high-κ materials used for e.g. gate dielectrics.
The biggest advantage of PECVD over other methods of CVD is its ability to operate at low temperatures, down to 100 °C, and as such can be used on sensitive samples[7].

Another advantage of CVD processes in general is their excellent step coverage. After being adsorbed on the sample surface, reactants will quickly migrate, causing uniform film buildup regardless of the topography of the surface, unlike methods with low migration where certain areas will lag behind due to difficulty for reactants to reach. Fig. 2.9 shows a comparison between good and bad step coverage.

Fig. 2.9: Film step coverage, a) conformal step coverage, b) nonconformal step coverage.

A PECVD chamber is designed with a grounded electrode at the bottom on which the sample is placed, and which can be heated. A parallel electrode is positioned above to which a Radio Frequency (RF) voltage is applied. Gas inlets allow the reactant gases to enter the chamber, and a vacuum pump keeps the pressure low[7]. See Fig. 2.10 for a schematic.

Fig. 2.10: A simple schematic of a PECVD chamber, showing gas inlets, vacuum pump, top and bottom electrodes and the sample holder which is heated.
When the reacting gases have entered the chamber and the RF voltage is applied, a plasma discharge between the electrodes appear. In a plasma discharge, a fraction of the gas molecules are ionized into charged reactive species. These positively charged ions travel towards the cathode, and the electrons towards the anode. On their path they collide with neutral particles and ionize them, causing a chain reaction. Since an RF bias is applied, it is important that the electrons move much faster than ions, who will not get far before the electric field turns, causing a DC bias to arise. This process is sustained as long as the RF voltage is applied. The particles that become excited from collisions quickly lose their energy, most importantly through the release of a photon, causing the plasma to glow[23].

The drift of ions towards the cathode where the sample is located is what causes the film growth. The active species will react on the surface during the arrival of charged particles that affect the deposited materials. As a result, films deposited by PECVD tend to be amorphous or polycrystalline due to the random impact locations of the bombardment, and they are also often charged due to charged species from the plasma being embedded in the films. Plasma-deposited films generally contain a high concentration of impurities. A 20-25% composition of hydrogen is typical in silicon nitride films, and other impurities such as carbon or halide atoms are also common. These effects on the film can be a big limitation to plasma deposition, depending on what the film will be used for[7].

The deposition rate and quality heavily depends on input parameters such as temperature, pressure and gas flow. A silicon nitride film as is used in this project, is typically grown using silane (SiH$_4$) and either ammonia (NH$_3$) or nitrogen (N$_2$).

### 2.6 Raman spectroscopy

Raman spectroscopy is a method commonly utilized to measure the strain in an object. In Raman spectroscopy, an intense laser beam is focused on an object and detectors are used to observe the resulting outgoing signals, see Fig. 2.11 for a schematic. The basic theory of what happens in the material in a Raman measurement is explained in this section.
Atoms are never still, but they constantly vibrate. In classical mechanics, the bond between two atoms can be viewed as a spring that follows Hooke’s law which states that the force is proportional to the extension of the spring. The vibrational modes in atoms and crystals are quantized, with the energy and momentum taking the form of a phonon, similar to how a photon represents the energy and momentum in electromagnetic radiation. In a crystal, phonons are described as either acoustic or optical. For each acoustic and optical phonon, there is also the option of longitudinal or transverse vibrations, in three dimensions[24].

When the sample is irradiated by laser light in the UV, IR or visible region, scattered light will be influenced by the vibrational modes. The scattered light consists of both Rayleigh scattering and Raman scattering. The majority of the scattered intensity is from Rayleigh scattering, with typically only $10^{-5}$ of the incident beam from Raman scattering. The inelastic scattering where light obtains or emits energy as phonons has frequencies $v_0 \pm v_m$ where $v_0$ is the incident beam energy, and $v_m$ is a vibration frequency. As such, the frequency measured is the difference between the incident beam and vibrational frequencies in the sample[25].

Many parameters can affect the Raman scattering efficiency, such as defects, electric field and carrier density. The shape of the lines and the full width half maximum (FWHM) can therefore yield information about the quality of a crystal. When an object is exposed to stress, the Raman frequency will shift proportionally to the strain, depending on the deformation potential of the material[26].

The Raman frequency shift with strain for bulk GaSb has previously been measured[27], and the result (Fig. 2.12) is used in this work to determine the strain in single GaSb nanowires.
Figure 2.12: The Raman energy of GaSb with relation to strain for the longitudinal optical (LO) and transverse optical (TO) phonons. This image is adapted from [27].
Chapter 3

Method

For my experiments GaSb nanowires previously grown using metalorganic chemical vapor deposition (MOCVD) from gold (Au) seed particles were used. The nanowires were grown on an Si substrate with an indium arsenide (InAs) layer of 250 nm. First, an InAs nanowire segment was grown, before the growth of a GaSb segment. The nanowires were then transferred to a 4x6 mm Si chip with 24 pairs of gold pads, using a sharp piece of paper to scratch the wires off their original substrate and release them onto the chip. Between each pair of gold pads, a suitable nanowire was chosen to be connected to the pads with individually designed Pd/Zn/Pd electrodes using electron beam lithography (EBL).

Figure 3.1 is a scanning electron microscopy (SEM) image of one wire and its contacts. The wires are roughly 50 nm in diameter, the contact width is set to 150 nm, and the distance between each pair of contacts is 200 nm. The center gap distance will depend on the length of each individual nanowire. These steps were previously performed by Johannes Svensson and Aein Shiri Babadi at the Nanoelectronics group at EIT. The rest of this chapter will discuss the subsequent processing steps conducted throughout this project on these samples.
3.1 Electrical characterization

The chips with the contacted GaSb nanowires transistors, fabricated up to a year ago, were first annealed on a hotplate at 100 °C. This step was done to reduce the amount of absorbed molecules in the sample that may have formed over time. A heating similar to this is later part of the film depositing process, so by annealing the samples at this stage it would also be easier to distinguish between effects caused by the heating, and effects caused by the film depositing process.

Before depositing any film, thorough electrical measurements were performed on the samples. Transfer characteristics and resistances were investigated using a probe station. Transfer characteristics were measured between the two center contacts with a drain voltage of 50 or 500 mV. A measurement sweep was then performed between gate voltages -10 V and 10 V, with 401 measurement points in each direction.

The nanowire resistance was measured using a four-probe setup where a current sweep between -100 and 100 nA was done between the two outer contacts. The voltage drop was then measured using two different probes between the two center contacts. This allowed the extraction of the nanowire resistance. A separate two-probe measurement was then done between the center contacts, sweeping between voltages of -0.5 and 0.5 V. By measuring the current and calculating the
Ohmic resistance, the total resistance through the nanowire and the two contacts is obtained. The contact resistance could then be deduced from the difference between the four-probe and two-probe measurements.

These measurements were performed prior to film deposition, and after each deposition, with the same settings for a systematic process.

3.2 Film deposition

In order to measure the results of the deposition, a 2” Si wafer was placed next to the sample throughout the entire process. Two small markers were first carefully placed 30 mm apart on the Si wafer, using a diamond tip pen. The topography between these markers was then measured using the profilometer Dektak 6M profiler, which has a maximum lateral measurement distance of 30 mm.

3.2.1 Atomic Layer Deposition

Before depositing a stressed \( \text{Si}_3\text{N}_4 \) film using PECVD, a film of \( \text{Al}_2\text{O}_3 \) was deposited using Atomic Layer Deposition (ALD) on one of the samples. The deposition was done at 100 °C with the aluminium precursor Trimethyl Aluminium (TMA) and the oxygen precursor \( \text{H}_2\text{O} \).

The recipe used consisted of 5 cycles with 0.015 s pulses of TMA and a 40 s wait time after each pulse. After this initial preparation step, 20 cycles were done with 0.015 s pulses of TMA and 0.015 s pulses of \( \text{H}_2\text{O} \) with 40 s and 60 s wait time after each pulse respectively.

3.2.2 Plasma Enhanced Chemical Vapor Deposition

After the thorough electrical investigation of a sample, and the preparation of an Si wafer, they were placed together in the loading chamber of the PECVD tool MicroSys 200. Every deposition was done at 100 °C with a plasma formed of the gases argon (Ar), silane (\( \text{SiH}_4 \)) and nitrogen (\( \text{N}_2 \)). Duration, gas flows and pressure varied for each sample, and is indicated in the results when necessary.

The film is expected to cover the surface conformly. To measure the thickness and refractive index of the film, ellipsometry was used on the control sample. The sample was placed on the ellipsometer table and a model of materials and thicknesses
was done based on previous PECVD test runs, to obtain the film thickness. The control sample was once again measured in the profilometer, between the same two markings as before. The height difference prior to, and after, deposition was then used to calculate the film stress using Stoney’s equation 2.3.

3.3 Film etching

Since the entire surface of the substrate is covered with the Si$_3$N$_4$ film after deposition, including the gold pads, the probes cannot access these pads for electrical measurements. Therefore the film covering these areas had to be etched away. This was done using ultra violet lithography (UVL) and reactive ion etching (RIE), detailed in this section.

In order to etch the film only on top of the gold pads to clear for the probes, and leave the film covering the wires untouched as to not affect the strain, a photolithographic process was implemented. The sample was first covered in a few drops of photoresist S1813 in a spin coater, and was then accelerated to 1500 rpm over 3 seconds, and then spun at 4000 rpm for 45 seconds. To evaporate the solvent and solidify the resist, the sample was baked on a hotplate for 90s at 115°C. The resist was then exposed to UV light for 5 seconds, using the same mask as was originally used to define the gold pads on the substrate. This way, only resist in the areas of the gold pads is affected by the exposure. To develop the exposed resist, the sample was gently stirred in developer MF319 for 90 seconds, and then rinsed in distilled water for 60 seconds. Finally, it was baked at 120°C for 10 minutes.

When the resist had been opened up, the film on the gold pads was clear to be etched away. This was done using Reactive Ion Etching (RIE), which is a dry etching process where a chemically reactive plasma etches the undesired material. The plasma was in this case created from SF$_6$, which will react with Si$_3$N$_4$ with strong selectivity over Si and not at all with Au[28].

The RIE recipe used had the pressure set to 160 mT, the power to 140 W, a flow of Ar to 5 sccm, a flow of SF$_6$ to 45 sccm, and a process time depending on the film thickness. A dummy run determined the etch rate to be 3.75 nm/s on the Si$_3$N$_4$ films, and the etch time was always set to a few seconds more than would be required to etch away the film on the gold pads, just to be sure. If the mask was slightly misaligned during the UV lithography, the extra etch time would only etch
a small part of the SiO$_2$ layer in close proximity to the gold pads, which should have no effect on the final result.

To clean the sample from fluoro carbon contamination that are a result of the RIE process, the sample was placed in a Plasma Preen etcher and exposed to an O$_2$ plasma at 5 mbar for 30 seconds. Finally, the sample was cleaned in acetone for 90 seconds, followed by IPA for 90 seconds to remove any remaining residues.

### 3.4 Raman spectroscopy

Every sample was measured using Raman spectroscopy. The setup used had a laser wavelength of 633 nm and used a reflective diffraction grating with 1800 lines/mm. The resolution of the Raman shift was 1.25 cm$^{-1}$ between each measuring point. Measurement data on single GaSb nanowires was acquired over 5 min to obtain a good signal-to-noise ratio.
Chapter 4

Results and discussion

In this chapter all the results from this work will be presented and discussed. At first, stress results from various PECVD dummy runs are given and trends discussed. Then there will be a brief section with a Raman analysis that was performed to study the impact of the deposition of the stressed film. Finally, the electrical characteristics and Raman signal results of the three main nanowire samples will be presented. The three samples will be presented individually and in order of production, with a summary at the end.

4.1 Si$_3$N$_4$ film properties

To get an understanding of how varying deposition parameters affect the film, a number of dummy runs were construed where Si$_3$N$_4$ films were deposited on 2” silicon wafers. Table 4.1 shows the input parameters and film stress of a large number of these dummy runs. All depositions were done at a temperature of 100 °C.
Table 4.1: PECVD runs on Si wafers. Table shows the input parameters flow of the gases Ar, SiH$_4$ and N$_2$ in sccm, pressure in mbar and time in s. Resulting thickness in nm, stress in GPa and refractive index. The additional note indicates if the recipe was used for any of the nanowire samples.

<table>
<thead>
<tr>
<th>Ar/SiH$_4$/N$_2$ (sccm)</th>
<th>Press. (mbar)</th>
<th>Time (s)</th>
<th>Thick. (nm)</th>
<th>Stress (GPa)</th>
<th>Ref. index</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>300</td>
<td>122.2</td>
<td>-1.94</td>
<td>1.989</td>
<td></td>
</tr>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>300</td>
<td>126.7</td>
<td>-1.62</td>
<td>1.976</td>
<td></td>
</tr>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>200</td>
<td>85.3</td>
<td>-1.83</td>
<td>1.970</td>
<td></td>
</tr>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>140</td>
<td>52.1</td>
<td>-2.35</td>
<td>2.036</td>
<td></td>
</tr>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>100</td>
<td>40.8</td>
<td>-2.42</td>
<td>1.970</td>
<td></td>
</tr>
<tr>
<td>0/10/10</td>
<td>0.025</td>
<td>100</td>
<td>41.3</td>
<td>-1.94</td>
<td>1.962</td>
<td>Sample 1</td>
</tr>
<tr>
<td>90/5/4</td>
<td>0.010</td>
<td>420</td>
<td>125.2</td>
<td>-0.71</td>
<td>2.058</td>
<td></td>
</tr>
<tr>
<td>60/5/4</td>
<td>0.025</td>
<td>300</td>
<td>111.4</td>
<td>-1.35</td>
<td>2.011</td>
<td></td>
</tr>
<tr>
<td>60/5/4.5</td>
<td>0.015</td>
<td>40</td>
<td>20.2</td>
<td>-1.02</td>
<td>1.828</td>
<td></td>
</tr>
<tr>
<td>60/5/4.5</td>
<td>0.015</td>
<td>20</td>
<td>9.1</td>
<td>-2.19</td>
<td>2.06</td>
<td>Sample 2</td>
</tr>
<tr>
<td>60/5/4.5</td>
<td>0.015</td>
<td>60</td>
<td>25.1</td>
<td>-1.32</td>
<td>1.900</td>
<td>Sample 2</td>
</tr>
<tr>
<td>60/5/4.5</td>
<td>0.015</td>
<td>100</td>
<td>42.5</td>
<td>-0.70</td>
<td>1.898</td>
<td>Sample 2</td>
</tr>
<tr>
<td>60/10/10</td>
<td>0.015</td>
<td>180</td>
<td>118.3</td>
<td>-0.38</td>
<td>1.979</td>
<td></td>
</tr>
<tr>
<td>60/10/10</td>
<td>0.015</td>
<td>160</td>
<td>104.4</td>
<td>-0.35</td>
<td>1.950</td>
<td>Sample 3</td>
</tr>
<tr>
<td>60/10/10</td>
<td>0.015</td>
<td>160</td>
<td>104.1</td>
<td>-0.11</td>
<td>1.950</td>
<td>Sample 3</td>
</tr>
</tbody>
</table>

As is seen in the table, the resulting thickness, stress and refractive index varies considerably with the input parameters. The first two rows show the same recipe used twice, with a minor variation in film thickness and refractive index, but very different stress outcomes. This means that there is either a high variation in the deposition or the measurement techniques.

The measurement technique used to obtain the thickness and refractive index was ellipsometry, and the stress was obtained with profilometry. Out of the three processes, PECVD, ellipsometry and profilometry, the one with the smallest error is likely ellipsometry, since ellipsometry is commonly used to obtain film thicknesses and the ellipsometer used is of high quality. There might be variations in film thickness depending on where on the sample the measurement is done, but it is assumed that the PECVD films are applied uniformly.

The most likely culprit in the large stress variation is the profilometry. The longer a scan is, the more accurate the overall result will be, less prone to local topographical variations. Therefore, two markers 30 mm apart were placed on each wafer as to utilize the entire scan range and always measure along the same line of a wafer.
However, the initial topography of the wafers varied quite significantly. While the maximum peak height between the two markers ranged between -10 and 10 µm on any sample, a 10 µm height change after deposition of a 50 nm thick film represents a stress of ∼6 GPa. While 10 µm is only 0.03% of the scan length, if the wafer bending due to stress is only slightly affected by the initial warping of the wafer, it could cause a rather significant error when working with stresses around 1 GPa. Nevertheless, it is probably more likely that it is the shape of the surface that affects the result the most. Fig. 4.1 shows two variations of how a wafer surface might look. The left one has a single peak, while the right one has a more wavelike surface.

![Figure 4.1: Two examples of the topography of wafers measured with profilometry. The left example has one single peak while the right has a wavelike profile.](image)

In the right side example, it might be difficult to choose a reference point, as different points along the surface might be affected differently by the stress. To be as precise as possible with this measurement technique, wafers with wavy surfaces were mostly avoided. However, if using a wafer with a single peak surface, it is difficult to determine if it also has a single peak, or is wavy, in the direction perpendicular to the axis measured, which might affect how much the wafer bends.

In theory, these effects seem insignificant, but there is no denying that the first two rows in Table 4.1 are rather similar in thickness and refractive index but has a large variation in stress. Perhaps the difference originates from the atmosphere in the PECVD chamber affecting the plasma, but the similar refractive index of the films indicate that the composition is nearly the same in both films. After working with the profiler throughout this project, I conclude that the stress measurement process is the most likely culprit. A better way to measure the stress might be with Raman, which is being used on the nanowire samples.

The results in table 4.1 illustrate that the thickness increases with time, obviously, but that the stress is also reduced with thickness. This shows that the stress is strongest near the surface. However, this does not mean that the substrate is less strained with a thicker film, a thicker film always increases the strain on the
substrate, but since stress is defined as force per area, and the cross sectional area of the film increases with thickness, the stress is reduced. In other words, the force does not scale linearly with film thickness and as such the stress is reduced as the film grows.

Fig. 4.2 is a plot of the stress as a function of the film thickness of films applied with the 0/10/10 recipe shown in Table 4.1. Note that the absolute value of the stress is shown, and that the stress is negative, i.e. compressive. The conclusion is that the stress is steadily reduced, except for the lower and higher film thicknesses, where possible errors have already been discussed.

![Graph](image)

**Figure 4.2:** Film stress compared to film thickness for the 0 sccm Ar, 10 sccm SiH\(_4\) and 10 sccm N\(_2\) recipes given in Table 4.1.

The depositions presented in Fig. 4.2 are for separate samples. In contrast, the 60/5/4.5 recipes are done sequentially on the same substrates, a dummy Si wafer used to measure film thickness and stress, and the sample with nanowires called sample 2. Since the added film thickness with each step are 9.1, 25.1 and 42.5 nm as shown in Table 4.1, the total thickness is 9.1, 34.2 and 76.7 nm respectively. The stress and refractive index in relation to film thickness for this sample are shown in Fig. 4.3.
Chapter 4. Results and discussion

4.2 Raman measurements

The GaSb nanowires used were grown on a base of InAs. When the wires are cut off and transferred to the sample, this short section of InAs can remain on the wire and contribute to peaks in the Raman spectra. There will also be some remnants of In in the gold particle that will be incorporated into the GaSb section of the nanowires when the growth is changed from InAs to GaSb.

Since InAs has Raman peaks very near GaSb, as shown in Table 2.1, an InAs/Si substrate was studied in order to understand how the results are affected by the presence of InAs. Fig. 4.4 shows the results of Raman measurements on various substrates.
Figure 4.4: Raman spectroscopy data of samples with vertical GaSb wires, vertical GaSb wires covered with a 60 nm film of Si$_3$N$_4$, and the same vertical wires covered with the 60 nm film transferred to an Si substrate, and an Si wafer with a 250 nm layer of InAs. Image a) shows the full measured spectrum and b) is zoomed in on the GaSb peak.

It can be seen here that the GaSb and InAs peaks are at roughly the same position. When the GaSb segment is grown, a thin layer of GaSb will also form on the substrate which can contribute to the GaSb peaks in this figure (red and blue), since the laser spot size in this setup is a few times wider than the nanowires. When the wires were transferred to a Si substrate and the measurement done on an individual wire, the peak intensity is much lower (green). However, the peak has around the same intensity as the InAs peak (yellow) which originates from an entire layer of InAs.

The peak at 0 cm$^{-1}$ comes from the laser, with the Si substrate at $\sim$520 cm$^{-1}$ and Si$_3$N$_4$ at $\sim$590 cm$^{-1}$. It is therefore assumed that on the real samples of GaSb nanowires, the peak around 230 cm$^{-1}$ will originate mainly from GaSb. The very small amount of InAs should therefore only contribute some to the intensity to the GaSb peak, and not cause any confusion as to which material the signal originates from.

4.3 GaSb nanowires

This section will include results from the three samples in order, with a brief discussion about the results for each sample. A summary of the results will be given at the end with a more thorough analysis of the results.
4.3.1 High stress

The first sample has Si$_3$N$_4$ with a high film stress of -1.94 GPa, as seen in Table 4.1, denoted 'Sample 1'. The high stress was chosen in order to obtain a high strain for maximum results. However, the film delaminated from the surface due to too high stress as can be clearly seen when imaged in SEM, see Fig. 4.5. The Raman measurement still gave results however, which is seen in Fig. 4.6.

**Figure 4.5:** SEM image of the surface of the dummy wafer used in conjunction with sample 1, showing delamination of the Si$_3$N$_4$ film.

**Figure 4.6:** Raman shift measured on three uncoated reference wires (red) and three wires on sample 1 with 41.3 nm Si$_3$N$_4$. The peak position prior to and after deposition are indicated by vertical lines.
The reference used for the Raman measurements is the same for all three samples as the wires have the same growth conditions before deposition of the film. The peak position of the red lines representing the reference sample is difficult to determine due to the peak shape, but is equal for every wire, at 230.53 cm$^{-1}$, representing the LO line at 232.6 cm$^{-1}$ in Table 2.1. The second reference sample has an additional peak at 226.69 cm$^{-1}$, which could possibly come from the TO peak of GaSb, or InAs if the laser spot size was focused on the InAs part of the wire.

The Raman signal for sample 1 is shifted down to 226.69 cm$^{-1}$ for two wires and 225.44 cm$^{-1}$ for one wire. Due to the delamination from the surface, the film might have relaxed and reduced the strain in the wires, and perhaps the peak position would be different without the delamination.

In the Raman setup used, the spectral resolution was 1.25 cm$^{-1}$ so the different peak positions for one of the wires could be due to the bad resolution of the measurement, that the film did not exert the same stress uniformly across the sample, or that something caused this wire to be affected differently by the stress. The small bump around 236 cm$^{-1}$ could come from InAs LO peak. The change in the peak position after film deposit is 3.84 ± 1.25 cm$^{-1}$ due to the resolution, which corresponds to a strain of 0.46 ± 0.15% using the results in Fig. 2.12.

![Figure 4.7: Transfer characteristics of sample 1 before processing, after annealing, and after film deposition. A drain voltage of 50 mV was used, and the result is normalized to the circumference of the nanowire.](image)

The transfer characteristics of this sample are shown in Fig. 4.7. The strain is expected to increase the hole mobility in the GaSb nanowires, whether compressive or tensile. This would result in an increased current, which has not happened in
this case. When annealing the sample, the current was largely increased, which is
to be expected since the sample was idling for months before use which causes a
buildup of absorbed molecules etc., which annealing helps resolve.

After film deposition, the current is significantly reduced. Comparing the current
after deposition with the annealed state, the current is reduced by 39% at -10
V, by 95% at 0 V and by 98% at 10 V. This does not necessarily mean that the
wires are not strained or the hole mobility changed, but other consequences may
be in effect. Si$_3$N$_4$ films are typically positively charged, and this charge is likely
affecting the wire. The result is that the threshold voltage is reduced from the
extra charge that is present in the film.

What is evident from Fig. 4.7 is that the on/off-ratio is far lower after deposition.
The on/off-ratio after annealing was 3.2, and after deposition 96.0, a 29 times
increase. The transconductance peaks at roughly the same value in the three
cases however, as seen in Fig. 4.8 below, obtained using eq. 2.1.

![Figure 4.8: Transconductance of sample 1 in the three cases of untreated,
annealed, and with a film deposited.](image)

### 4.3.2 Incremental film thickness

For the second sample, a Si$_3$N$_4$ film with lower stress was employed to avoid de-
lamination. The film was also deposited in three stages to examine the effects of
increased strain. In Table 4.1, the sample is denoted ‘Sample 2’, with thicknesses
for each deposition of 9.1, 25.1 and 42.5 nm, resulting in a total thickness of 9.1,
34.2 and 76.6 nm, and a film stress of -2.19, -1.32 and -0.70 GPa respectively. Fig,
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4.9 shows the Raman spectrum obtained for this sample.

![Raman spectrum](image)

**Figure 4.9:** Raman shift measured on three untreated reference wires (red) and three wires on sample 2 with 76.7 nm Si$_3$N$_4$. The peak position prior to and after deposition are indicated by vertical lines.

Unfortunately, due to inaccessibility of the Raman measurement setup while producing this sample, measurements only exist with the final film thickness and not the intermediate stages. As for sample 1 in Fig. 4.6 there is a clear change in peak position, although smaller in this case than for sample 1. All three peaks are here found at 227.83 cm$^{-1}$, a shift of 2.70±1.25 cm$^{-1}$ as compared to the uncoated reference nanowires, corresponding to a strain of 0.32±0.15%. Compared to sample 1, this sample has a thicker film but lower stress, which led to the lower strain obtained.

The transfer characteristics for this sample are plotted in both logarithmic and linear scales, see Fig. 4.10. Besides measurements prior to deposition and after each deposition stage, there is also a result from a measurement conducted 2 months after the final deposition in order to study the effects of sample aging.
Chapter 4. Results and discussion

Similar to what was found for sample 1, the device turns off much better after a film being added, with the on/off-ratio increasing from 36.0 after annealing to 1950 with 76.6 nm film, a 54 times increase. In the region 0-7 V in the logarithmic plot, there is actually a clear current increase with film thickness, and at 6 V the 76.7 nm measurement has a 3.35 times higher current than the 9.1 nm measurement. This could be a result of an increased strain, or it could simply mean that the threshold voltage has shifted a bit more. It could also just be a measurement error, it is very hard to tell the origin of this shift in current.

There is a 10% increase in current at -10 V for the 76.7 nm measurement compared to 9.1 nm. However, the current is lower as compared to the measurement with the 34.2 nm film, which has the highest current at -10 V. At +10 V, the measurement at 34.2 nm actually had the lowest current, and as such it has the highest on/off-ratio of the three measurements, 2430 which is a 67 times increase from the annealed state. It is possible that the increased strain when going from 9.1 to 34.2 nm film outweighs the additional charge from the film, since the transconductance is slightly higher with 34.2 nm compared to 9.1 nm film. However, the added strain when going from 34.2 nm to 76.7 nm is minor and overcome by effects from having a thicker film. It is once again very difficult to tell what is happening. The transconductance for this sample is shown in Fig. 4.11.
When the wires had aged two months, the off-current was actually even lower, with very little change to the on-current, with an on/off-ratio of 5710. This could be explained by the charge in the film changing with time, reducing the off-current but having a very minor effect to the on-current. A more thorough analysis that could explain this is given in subsection 4.3.4.

The film is deposited on top of the wires and will directly affect them. But the film will also form on top of the contacts, and could influence them as well. To investigate this, the resistances of the wire and contacts were measured using the four probe method explained in section 2.2 and eq. 2.2. To calculate the mobility, the contact resistance also has to be taken into account and extracted to obtain the voltage drop over the wire.

Unfortunately, the resistance measurements showed very odd behavior. The size of the contact resistance would be on the same scale as the nanowire resistance, but would often become negative. This is obviously not physically feasible, and despite multiple people looking into the measurement settings, and two different probe stations being used, no realistic results could be obtained. The best explanation that can be given for this behavior is failing contacts. As seen in Fig. 3.1, the contacts had a wave-like shape, and one contact was for one functioning wire even found to be broken with a tiny gap, as if the current was flowing through the substrate instead. However, this is unlikely since there is a 100 nm SiO$_2$ layer between the substrate and contacts. Another possibility is that the gap was small enough for tunneling to occur for that particular wire, but still it remains a question why the resistance measurements behaved as they did.
4.3.3 Al₂O₃ interlayer

In the third and final sample discussed here, an attempt was made to avoid surface effects between the wire and film by depositing a thin layer of the high-κ oxide Al₂O₃. Since the air-GaSb interface is very different as compared to the Si₃N₄-GaSb interface formed after film deposition, a thin Al₂O₃ layer was initially deposited on sample 3. This allowed me to obtain a measure of the effect of the stressed film with identical GaSb surface conditions before and after Si₃N₄ deposition. Ellipsometry showed an Al₂O₃ thickness of 3.2 nm. Two dummy samples were used together with sample 3 during PECVD, one with the same layer of Al₂O₃ as sample 3, and one without. The results of both are shown in Table 4.1, denoted as 'Sample 3'.

The stress applied to this sample was rather low, but it should still be able to provide a decent amount of strain to the wires. In Table 4.1 the thickness and refractive index of both wafers are very similar, 104.4 and 104.1 nm, and 1.95 and 1.95 respectively, which is to be expected. However, there is a significant difference in the stress, with the sample without the ALD film having a much higher stress. This could mean that the Al₂O₃ is blocking stress from reaching the wires since Young’s modulus of Al₂O₃ is up to 410 GPa [29] compared to the 63 GPa of GaSb, as seen in Table 2.1. It could also just be a measurement error from the profilometry, as previously discussed. The results from the Raman measurements on this sample are shown in Fig. 4.12 below.

![Figure 4.12: Raman shift measured on three untreated reference wires (red) and three wires on sample 3 with 104 nm Si₃N₄. The peak position prior to and after deposition are indicated by vertical lines.](image-url)
As for previous samples, there is a clear change in the peak position after deposition of the film. The peak position is at 226.69 cm$^{-1}$ i.e. a shift of 2.84±1.25 corresponding to a strain of 0.46±0.15%. This is the same strain as in sample 1, which is not unlikely since despite sample 3 having a much lower stress, it has a higher film thickness. It is also possible that the Al$_2$O$_3$ film makes the wires more prone to strain. It is unknown what happens at the wires as the Si$_3$N$_4$ is deposited by PECVD. As the wires are lying freely on the surface, perhaps they can move slightly as the film is deposited in order to relax, which could reduce strain. With the Al$_2$O$_3$ film present, the position of the wires should be more fixed.

The transfer characteristics of this sample are shown in Fig. 4.13 and the transconductance in Fig. 4.14. The presence of the Al$_2$O$_3$ film appears to increase the off-current for a lower on/off-ratio, reduced from 15.0 to 5.21. With the application of the Si$_3$N$_4$ film, the same results as in previous samples is obtained, despite the Al$_2$O$_3$ layer. The on/off-ratio is now 139, a 9 times increase over the uncoated sample, and 27 times increase compared to after deposition of the Al$_2$O$_3$ layer. It appears that the dominant effect on the changed characteristics with the application of an Si$_3$N$_4$ film is the presence of positive charges in the film, since these charges will affect the wires through the Al$_2$O$_3$ while other surface effects between the wires and Si$_3$N$_4$ are of less importance.

![Figure 4.13: Transfer characteristics for sample 3 in a) logarithmic scale and b) linear scale. Data is obtained after annealing, after deposition of Al$_2$O$_3$ and after deposition of Si$_3$N$_4$.](image)
4.3.4 Summary

When comparing the results from each of the three samples, it is clear that they have some things in common. After deposition of Si$_3$N$_4$, the current is always reduced, and most significant at +10 V gate voltage, the off-current. Part of this can be explained by a change in threshold voltage due to the vicinity of positive charges in the Si$_3$N$_4$ film, but something else must be happening to cause the very significant reduction in off-current.

In [30] it is shown that in their 200 nm wires, the gate voltage only affect a very thin part at the bottom of the wires. The samples used here have roughly the same substrate thickness as in [30], so it can be assumed that this also happens to the wires used in this work. The wires used here are around 50 nm in diameter, but the volume affected by the gate voltage should still be very small.

What this means is that while the gate voltage is set to +10 V, where the off-current is obtained, the majority of the wire is not affected by this voltage and will not be turned off, see Fig. 4.15 for an illustration. In the untreated samples, the bottom part of the wire (blue) could be almost completely turned off by the gate voltage, but this would not matter much since current can still flow freely in the rest of the wire (red). In wires with a film deposited, the positive charge in the film will deplete a large part of the wire resulting in a conducting channel only existing in the thin bottom part of the wire. The entire wire would then have a large reduction in current at -10 V, and not only the bottom part, which could explain the significantly lower off-current in devices with a film.
When the device is on, the wire is affected by the gate voltage in the bottom region, which is where most of the current will flow. Although the current in the top region will be reduced by the positively charged film, this current is not as significant anymore as the majority will flow through the bottom area. As a result, the on-current is not reduced as much as the off-current.

The wires used are grown in the (111) direction, and it is known that the direction of the wires will influence the change in mobility with strain[19]. It is possible that other crystal directions would have different results compared to the (111) used here. This is something that would need to be simulated.
Chapter 5

Conclusions and outlook

There was no obvious enhancement observed due to strain. The effects of a positively charged film and possible changes to contact resistance made it difficult to determine if the strain of up 0.46±0.15% had any effect on the transport through the wires. The vicinity of a positive charge in the Si$_3$N$_4$ layer significantly reduced the off-current which improved the on/off ratio by up to 67 times, from 36.0 to 2430 for a sample with a 76.7 nm Si$_3$N$_4$ film with 0.7 GPa stress, resulting in a nanowire strain of 0.32±0.15%.

In order to better understand the physics of this effect and how much impact it has, simulations would need to be done. Simulations could also show how well strain improves current in the (111) direction the wires are grown in, as the current improvement is dependent on this direction.

The results of process induced strain is established for planar geometry[20][21], but it is unclear what method would be best for inducing strain in nanowires. Perhaps a planar geometry would be better to pursue with this straining method, and other methods like core-shell nanowire structures might be better at straining nanowires. It is however possible that using uniaxial strain along the wire channel rather than biaxial strain would show better results. Either way, the significantly improved on/off-ratio obtained in this project could help reduce power consumption, and might be something to strive for.
Appendix A

Popular abstract

"If cars had developed as fast as computer processors they would go at 760 000 km/h, drive 100 km on only 2.4 ml gas, and cost 3 cents" claims Paul Ottelini, former CEO of Intel which is the world leading developer and manufacturer of processors.

A processor is the unit in your phone or computer that perform all the instruction or calculations that programs require. Processors today consist of billions of transistors, which is the most important building block in most electronic components. It is an amazing accomplishment that’s been done in the development of transistors over the past 50 years that has led to the performance of our technology today.

A transistor behaves as a switch, that can be either on or off more than a billion times per second. By combining transistors that are turned on or off, the processor can perform complicated tasks fast.

Transistors have since long been made out of silicon, which is a material with good electrical properties, but it has mainly been used due to its ample availability on earth, since it is extracted from sand, which also makes silicon very cheap. The development of transistors has mostly been done by reducing their size which makes them faster, but they are now so small that this is no longer possible. Therefore, much research is taking place around other materials that could replace silicon, or finding other methods that can enhance transistors further. One such method that has been used on the market for some years now is straining the silicon in transistors. It has been found that by straining a material so that its atoms are closer together or further apart can considerably improve its electrical properties.
In this work, strain has been used on nanowires of gallium antimonide. A nanowire is a wire-shaped object so small that it would require a million adjacent wires to be spotted with a naked eye. Gallium antimonide is one of the materials that could replace silicon, although it is much more expensive. The nanowires that were used were lying on an open surface, with a thin layer of silicon nitride deposited on top. This layer pulls together everything beneath it. Imagine if you stretch a band-aid before putting it on a wound, it would try to pull itself back to its normal state, and also pull on your skin beneath it. In a similar way the nanowires are strained by the silicon nitride layer.

The results obtained in this project were of mixed nature. Optical measurements showed that the film could be used to strain the wires, but no big enhancement was found with increased strain, which could mean that other straining methods are probably better. A positive result was that the vicinity of the silicon nitride layer made the current through the transistors easier to turn off. A transistor is normally never completely turned off, there is always a small leakage of current. It was shown in this project that this leakage current was reduced up to 100 times when the wires were in contact with the silicon nitride.
Bibliography


