Quantum Dot Low Temperature Measurement and Analysis

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Abbreviations

BG  -  Back Gate
EBL -  Electron Beam Lithography
SDB -  Source Drain Bias
SEM -  Scanning Electron Microscope
SET -  Single Electron Transistor
PBG -  Potential Barrier Gate
PG  -  Plunger Gate
Acknowledgements

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Abstract

In this bachelor project, the electron transport within quantum dot transistor devices, whose barriers are electrostatically induced, was measured and analysed. The properties of devices with this particular architecture are not yet fully understood. We successfully synthesised several 150x50x50 nm of these devices, where the potential barrier gates are defined next to the nanowire to form the quantum dot island. These devices were trialled in a low temperature environment by the use of liquid helium and a dip rig in order to study the electron transport through the quantum dot of each device at a temperature of about 4.2 K.

These electrostatically induced dots were able to show the Coulomb diamonds produced only within the range of $n \rightarrow n + 4$ number of electrons. The lever arm $\alpha_G$, $\Delta E$ between energy levels $E_n$, the self capacitance $C_{\Sigma}$ and the energy $E_{ADD}$ required to add another electron per diamond of each device were also determined. In general, each device showed the artificial atomic shell structure shown directly by the even-odd electron coupling principle determining the energy required to add additional electrons to the island.

Due to time constraints, only two devices out of a total of 11 successfully synthesised were used in measurements. Measurements on the first device were used to explore the quantum dot behaviour induced by the potential barriers. The results from the second device showed that a dot could be induced without the barriers, prompting attempts to prove exactly how the second dot had been induced. It was found that the 350 nm distance between source and drain was sufficient to induce quantum dot behaviour.

1 Introduction

Attempting the synthesis of ever smaller electronic components requires the full understanding of the electron transport mechanisms whilst in dimensions that will show quantum confinement. This effect occurs in electronic devices whose dimensions are of the order of the wavelength of an electron. Such a confinement causes a drastic alteration in the electron transport mechanism, a change which is currently being researched within the field of solid state and is the focus of this study.

In particular, this thesis focuses on the study of an effect known as the Coulomb blockade, which reduces the current across the quantum dot to zero when the source drain bias
does not align to any of the confined energy levels $E_n$ inside the dot. This can only occur at sufficiently low temperatures however, and as such is unlikely to ever be used to reduce transistor size in consumer devices. But in a lab environment, smaller transistors can instead be limited by the Coulomb blockade, without having to use materials with a high dielectric constant to limit leakage.

The aim is therefore to synthesise electrostatically gated quantum dot transistor devices to study the electron transport, specifically within the Coulomb blockade regime, in a low temperature setting.

2 Theory

There are three main underlying principles of electron transport that must be understood to appreciate the content of this study.

2.1 Quantum Dots

The fundamental aspects of a quantum dot can be explained by the principles of quantum confinement, where the dimensions of a device are of the order of electron wavelengths. The quantum dot confines electrons in all three spatial dimensions, unlike the quantum well that confines electrons in one, and the quantum wire that confines electrons in two. Figure 1 illustrates what these three components look like in 3D space.\[1\]

![Figure 1: Illustrations of the three types of components that cause confinement in one, two or three dimensions.\[1\]](image)

The quantum dot is commonly thought of as a representation of an "artificial atom"[2] since the energy spectrum has bound, and discrete, electronic states akin to a spectrum that would be found in atoms or molecules.
2.2 Single Electron Transistors

Single electron transistors (SET’s) are nanoscale devices that utilise electron tunnelling mechanisms to control, and amplify, the flow of electrons across a tunnel junction under certain, very specific, conditions. They are characterised by a triple terminal design, consisting of a source, a drain and a gate. Between these terminals is a so called island. There are multiple ways to make a SET; the one used in this study connects source and drain contacts onto either end of a nanowire, defining two potential barriers to separate source and drain from the island. This can qualify the island as a quantum dot if it has dimensions small enough. The tunnel junctions can be defined either physically, or electrostatically, by either growing physical barriers, e.g. indium phosphide on top of indium arsenide or by applying a voltage to two potential barrier gates (PBG’s) pointed at, and in close proximity to, the nanowire. Figure 2 shows the circuit diagram of such a device.

![Circuit diagram of a conventional single electron transistor.](image)

Figure 2: Circuit diagram of a conventional single electron transistor. The capacitance $C_{Σ}$ is the total resultant capacitance from the labelled capacitors.

2.3 Coulomb Blockade

When studying electron transport in low-dimensional semiconductors, a recurring property of these devices is that the current through them is dependent on the principle of resonant tunnelling. In a standard SET whose island is a quantum dot with bound states $E_n$, when either source or drain energy (or both) equals that of a bound state $E_n$, then electrons can tunnel from either source or drain onto the island and through the
device.

If measuring current while altering the source-drain bias (SDB) and gate voltage, there will be regions where there is no resonance, and thus no current. This is the Coulomb blockade, and it produces so called Coulomb diamond, explained further in Figure 3.

**Figure 3:** An illustration containing the different resonant tunnelling conditions. The source (S) and drain (D) energies, dependent on the source-drain bias ($V_{SDB}$), and the island bound states, dependent on the applied gate bias $V_G$, are shown. The directions of electron tunnelling across the potential barriers at the boundary conditions of a Coulomb diamond are also labelled by green arrows. There is no current inside the diamond, as is shown by the top-right diagram. The energy difference between nearest island levels, or the width of the diamond, is $\Delta E$. Figure 4 shows a complete set of Coulomb diamonds that this diagram was based upon.

As is shown by the figure, the middle region of the diamond is the Coulomb blockade regime since electrons are unable to tunnel onto the island, and thus cannot produce a current. Furthermore, since increasing $V_G$ will drive down the Fermi level proportionally, if $V_{SDB} = 0$ then $\Delta E$ can be determined by the $\Delta V_G$ between resonances, giving that $e\Delta V_G = \Delta E$ between energy levels $E_n$ and $E_{n+1}$.

If a low source drain bias (SDB) is picked, and gate voltages are swept across a low
voltage range, the conductance of the device should oscillate with even intervals until the Coulomb blockade region disappears at a greater gate voltage. This happens because the Fermi level is eventually pushed below the source, meaning that electrons can always tunnel into the conductance band. These recurring peaks are known as Coulomb oscillations and, as stated before, occur when an energy level aligns with the source or drain energy (which is known as a resonance), increasing the tunnelling probability drastically. However, these prominent oscillations are not often seen in quantum dots whose PBG’s are defined electrostatically.

2.3.1 Lever Arm and Gate Capacitance

The lever arm \( \alpha_G \) is usually defined as a ratio of capacitances in the capacitance matrix.

\[
\alpha_{ij}^G = \frac{C_{ij}}{C_{\Sigma}} \Rightarrow \alpha_G = \left( \sum_{j=1}^{N} \frac{C_{ij}}{C_{\Sigma}} \right)
\]

Here, \( i \) gives the island index and \( j \) gives the component index of any capacitors incident to the island. Since the device used in this study only has one island, the index \( i \) is always zero, whereas the source, plunger and drain components have indexes 1, 2 and 3 respectively. \( C_{0j} \) is therefore the capacitance component between the island and component \( j \). Finally, \( C_{\Sigma} \) is the self capacitance of island. If devices with more islands, or more capacitor components, were to be tested, then there would be more indexes \( i \) and \( j \). Knowing this, it is otherwise simpler to determine the lever arm as a ratio of voltages between the source drain bias and the plunger gate (PG). Figure 4 shows the diamond dimensions whose ratio gives the lever arm \( \alpha_G \). From the figure, it can be stated that for each Coulomb diamond, the total width and the height from zero voltage determines the lever arm as is clearly evidenced by the following relation.\[5\]

\[
\Delta V_{SDB} = \Delta N_{+1} + \frac{e^2}{C_{\Sigma}} \quad \Delta V_{PG} = \frac{1}{\alpha_G} \left( \Delta N_{+1} + \frac{e^2}{C_{\Sigma}} \right) \\
\Rightarrow \alpha_G = \frac{\Delta V_{SDB}}{\Delta V_{PG}}
\]

This property permits the gate capacitance \( C_G \) to be determined as follows.

\[
C_G = \alpha_G C_{\Sigma}
\]
Figure 4: A graphic showing the distance-height ($V_G, V_{SDB}$) relations between diamonds. The small arrows indicate the spin orientations of the total number of electrons $N$ on the island, noted down at the bottom of each diamond. The diamonds not centered at $V_{SDB} = 0$ are first, and second excited state electrons. The $\Delta E$ values are as detailed in Figure 3, given as $e\Delta V_G$. The current inside the centered diamonds is zero.

In the particular set-up used, the charge $Q_i$ on the island is given by a sum of the charges on each capacitor.\[5\][6]

$$Q_i = \sum_{j=1}^{3} C_{ij} V_j = C_{01} V_1 + C_{02} V_2 + C_{03} V_3$$ (4)

Where it can alternatively be written that $C_{01} = C_S$, $C_{02} = C_G$, $C_{03} = C_D$ (It should be noted that $C_G$ describes any active gate, whether plunger or back gates). Furthermore, the gate capacitance can directly be determined by the measurement of odd (smaller) Coulomb diamond base heights ($H_{odd}$), giving the final capacitance as follows.

$$C_\Sigma = C_S + C_D + C_G = \frac{e^2}{E_C} = \frac{e}{H_{odd}}$$ (5)

Where $E_C$ is known as the charging energy, labelled and defined in Figure 4, representing the smallest energy required to add an electron to the island.

It should also be noted that the theoretical capacitance of any parallel plate capacitor structures in a material can be calculated through the means of a simple equation.

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$ (6)
Where $\varepsilon_0$ is the permittivity of free space, $\varepsilon_r$ is the material dielectric constant, $A$ is the cross sectional area, and $d$ the separation between components to the island within which the confinement is occurring. However, if one of the capacitor plates can be modelled as a cylinder on a plane, then instead another relation must be used.

$$C = \frac{\pi \varepsilon_0 \varepsilon_r}{ln \left(\frac{2d}{a} - 1\right)}L$$  \hspace{1cm} (7)

Where $a$ is the radius of the cylinder, and $L$ is the length of the region acting as a capacitor. Note that if the capacitor surfaces do not have contact then the $\varepsilon_r$ of the medium separating them is used. Since helium is used, it is worth noting that $\varepsilon_{He} = 1.0000665 \approx 1$, it can be ignored in those cases. These equations are important, since they will be used to make a theoretical estimate of the plunger and back gate capacitance values, since they represent the respective parallel and plane cylinder situations.

### 2.4 The Artificial Atom

As already stated, a quantum dot can be considered an artificial atom. This is clearly evident from Figure 4 which shows that the energy required to add another electron to the island is determined by the number of electrons already present. After determining $C_\Sigma$, the energy required to add an additional electron to $N$ already present on the island can be given by the following.\[4\]

$$E_{ADD}(N) = \frac{e^2}{C_\Sigma} + \Delta E(N) = E_C + \Delta E(N) = E_C + (\alpha H - E_C)$$  \hspace{1cm} (8)

Where $H$ is the height of the Coulomb diamond used in the calculation. It is important to note that $\Delta E(N)$ can both be calculated by using the lever arm and the height of the diamond, but it can also simply be the $e\Delta V_G$, since they are interchangeable. Otherwise, if it is assumed that there are already $N$ electrons on the island, the energy required to add an additional electron $E_{ADD}$ can be found.\[5\] Since $\alpha_G H_{Odd} \approx E_C$, then $E_{ADD}$ for odd diamonds should always equal $E_C$. This is related to the electron shell structure of a normal atom, where it takes less energy to fill an electron shell that is unoccupied. As such, the electrons that fill the levels $E_n$ will do so in an equivalent way as it would fill the shells of an atom. Thus, the energy difference between successive Coulomb diamonds should be in line with the general electronic configuration $1s^22s^22p^6$ etc.\[8\]
2.5 Limitations of Electrostatically Induced Potential Barriers

Unlike physically grown potential barriers, the electrostatically induced ones cannot be modelled as uniform square wells. Therefore, the biggest limitation is that they cannot be assumed to be uniform, with their potential looking more like a gaussian. This means that the bound energy levels $E_n$ are not, in fact, evenly distributed as they would be in a square well. Because of this, resonances will be reached at different gate voltages for the negative and positive SDB’s, meaning the diamonds will appear tilted, unlike in Figure 4. Fortunately, $\Delta E$ at $V_{SDB} = 0$ will still remain uniform, as in the square well case, but there will be much fewer energy levels $E_n$ because of this. It is possible however to produce symmetric diamonds if the two potential barrier potentials are made asymmetric and altered until the desired result is reached.
3 Method

The quantum dot device design used in this study can be seen in Figure 5. These devices are synthesised on a chip containing several so-called flower samples according to the method detailed in Appendix A. It is vital to inspect the devices with a scanning electron microscope (SEM) to check their quality. Any devices that have severed gates or overlapping components should be excluded. Only candidates whose source, drain, and gate are well defined should should be considered for experimentation. The chip is then cut into smaller pieces containing only 2-3 flower samples, ideally separating an approximately equal number of usable devices between them. This was done to prepare multiple device candidates in parallel for measurements.

There are two main ways in which the voltage of the devices can be altered, sweeping and stepping. Combining the two will construct a current matrix where rows of one voltage variable is swept, and columns of another is stepped. So if $V_A$ is swept across a range of $a_1 \leq V_A \leq a_n$ and $B$ is stepped across the range $b_1 \leq V_B \leq b_m$, the difference is that the full range of $V_A$ is measured over for each step of $V_B$. Thus, each measurement

\[ \text{Figure 5: An illustration of the quantum dot device design, drawn to scale} \]
should be considered as a matrix of the following form:

\[ I(V_A, V_B) = \begin{bmatrix}
I(a_1, b_1) & I(a_2, b_1) & I(a_3, b_1) & \ldots & I(a_n, b_1) \\
I(a_1, b_2) & I(a_2, b_2) & I(a_3, b_2) & \ldots & I(a_n, b_2) \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
I(a_1, b_m) & I(a_2, b_m) & I(a_3, b_m) & \ldots & I(a_n, b_m)
\end{bmatrix}, \quad (9) \]

which is a current intensity map, where Coulomb diamonds would be seen as near-zeroes when plotted.

### 3.1 Device Preparation

To test a device, all of its components must be wire-bonded onto a chip dock, containing corresponding contacts that can be connected to power supplies. After bonding, room temperature measurements are performed in a vacuum chamber, testing all the contacts to ensure they’re functioning before moving to low temperature measurements. Should a device fail here, another can simply be bonded. While it is possible to vary \( V_G \) and \( V_{SDB} \) and measure current in room temperature conditions, Coulomb blockade behaviour would not be visible without a low temperature. Furthermore, these measurements would be very likely to destroy the device.

Figure 6 shows an example of the "Dip Rig" set-up used in this study. The chip

![Figure 6: Illustration of a low temperature Dip Rig set-up. The set-up difference for Device 1 and Device 2 is the Amplifier type. Relevant grounds are also labelled.](image-url)
is mounted onto a sample holder on the dip rig that is then lowered into the liquid helium container. To ensure that the dip rig connector and dock contacts are working, a multimeter is touched at each connector contact pair and, if the resistance is low, then it means they are working properly. This is important to assert before testing, since otherwise the device will not work properly. When testing the device, all connectors that have corresponding wire bonded contacts on the dock are un-grounded. It is important to note is that the back gate has been bonded twice to ensure contact, and thus the second bond must be un-grounded since it is connected to the device but will not be connected to a power supply.

### 3.2 Coulomb Blockade Region Identification

The region of interest is where the current shows clear peaks in the midst of a zero current region. This usually occurs when sweeping the plunger gate at a low $V_{SDB}$, or sometimes when sweeping the back gate, either of which alter the Fermi level within the dot. Figure 7 shows an example of a back gate sweep across a range of voltages at a set $V_{SDB}$. From

![Figure 7](image)

**Figure 7:** An example of a back gate sweep, measuring current, with $V_{SDB} = 0.1$ mV. The region marked by the dotted rectangle that has current oscillations that return to zero between peaks is the ideal measurement range. The region to the right of this is where the Coulomb blockade region stops, and current flows regardless.
the figure, it is clearly evident that Coulomb blockades occur between all of the peaks that return to near-zero current at $V_{BG} < 0.8$ V. As such, the ideal region to study only the discrete Coulomb oscillations should be $0.3 \leq V_{BG} \leq 0.9$ V. When studying Coulomb oscillations at different PBG voltages, this estimation should be repeated as to identify this region.

3.3 Quantum Dot Bias Variations

For device 1 (a5R) only asymmetric barrier gate bias was performed. The aim was to bias the barrier gates asymmetrically until symmetric Coulomb diamonds were produced, something that is characteristic of symmetric tunnel couplings, which was unlike what was trialled. Most of the measurements that were made in the end used $V_{PBG1} = -5.5$ V and $V_{PBG2} = -5.3$ V whilst sweeping the SDB from $-0.01$ V $< V_{SDB} < 0.01$ V and stepping the plunger gate within the Coulomb blockade regime identified. These biases were varied between measurements, but this combination produced the best Coulomb diamonds.

For device 2 (a8L), all of the EBL printed gates were left unused and only the SDB and BG was used. SDB was swept in the same range as in device 1, and the BG was stepped within the identified Coulomb blockade regime. This was done to see if the unused PBG’s still influence the device in meaningful way. It was hypothesised that the printed gates could be shielding the nanowire from the back gate potential. If that is the case, then the dot would be induced in the same region as device 1, which had active gates, and thus these two devices should theoretically have similar capacitance values.

4 Results

4.1 Device Turnout

For the first electrostatically gated quantum dot design, a total of 11 devices were identified as potentially functioning. One device had the plunger overlap the nanowire, two devices had broken barrier gates and two had misaligned electron beam lithography (EBL) prints. The two devices used go by the names of a5R and a8L respectively, and can be seen in Figure 8. Device 1, the first one investigated, immediately showed Coulomb diamonds, and as such was used for analysis. Device 2 is the third device trialled, since the device
Figure 8: SEM images showing the final bonding result device 1 (Left) and device 2 (Right). Both were synthesised from the same lithographic design, but the PBG’s on device 2 ended up closer to the nanowire than on device 1.

used prior did not function. The measurement equipment used for each device can be reviewed in Figure 6.

4.2 Device 1

4.2.1 Theoretical Capacitances

Using a graphics program, the scale bar in each of the devices in Figure 8 was measured to find the conversion from pixels to nanometres. Therefore, measuring the number of pixels in each of the components allows for the determination of the component dimensions. The nanowire thickness was determined to be 28.8 nm and the distance $d_{PG}$ from the nanowire to the plunger gate was determined to be 50.8 nm thus giving better values for theoretical estimation. Unfortunately, the thickness of the gates cannot be determined accurately, and thus the previous EBL estimate is assumed to be true as given in Figure 5. Equation 6 can be used to determine the capacitance of the source to island, and the drain to island capacitors. To determine the plunger gate capacitance, Equation 7 should be used, since it assumed that the cylinder is on a plane, considering that the curved cylinder side is facing that gate. The following equation shows the theoretical green self
and gate capacitance determinations of device 1

\[ C_\Sigma = 2 \times \varepsilon_0 \varepsilon_r \frac{A_{NW}}{d_{PBG}} + \frac{\pi \varepsilon_0}{\ln \left( \frac{2d_{PG}}{R_{NW}} - 1 \right)} L_{PG} = 2 \times 17.477 \text{ aF} + 1.200 \text{ aF} = 36.154 \text{ aF} \]

(10)

where \( A_{NW} \) is the cross-sectional area of the nanowire, \( L_{PG} \) is the thickness of the PG, and \( \varepsilon_r = 15.15 \) for the InAs nanowire (for \( C_S \) and \( C_D \) in the first term).

### 4.2.2 Experimental Results

The intensity map containing the best results, with the clearest Coulomb diamonds was imported into MATLAB. The diamonds were difficult to make out initially; therefore value ranges were separated from one another by identifying regions considered to be conducting and making them sharper, and attempting to reduce the values for the inside of the diamonds to zero in order to make the Coulomb blockade region, and consequently the diamonds clearer. The final result of this can be seen in Figure 9. Since the intensity

![Image](image.png)

**Figure 9:** The boundaries four Coulomb diamonds, labelled as 1-4, have been determined and drawn out. The intensity in this graph does not represent the true dI/dV values.

map values have been filtered, all intensity map graphs in the results section have false colour. The raw data, with accurate colour bars, of the following graphs can be found in Appendix B.

When defining the diamond borders, linear equations were used to plot the border lines, relying upon that the diamonds should share the same gradient. MATLAB was
then used to automatically determine the intersections of these lines to automate the capacitance calculations, reducing manual work. The topmost diamond in Figure 9 was mostly extrapolated to. The middle two diamonds were the most uniform and best determined, and would most likely be more representative of the device properties. Table 1 shows a few of the calculated properties of this particular device.

**Table 1:** Determined lever arm, energy level difference ($E_{add}$) and capacitance values for device 1, where the plunger gate is used. Standard deviations for mean values have also been calculated.

<table>
<thead>
<tr>
<th>Diamond</th>
<th>$\alpha_G$</th>
<th>$E_{ADD}$ [meV]</th>
<th>$C_S$ [aF]</th>
<th>$C_{PG}$ [aF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>n (odd)</td>
<td>0.04270</td>
<td>3.8959</td>
<td>41.125</td>
<td>1.7512</td>
</tr>
<tr>
<td>n + 1 (even)</td>
<td>0.04281</td>
<td>5.5495</td>
<td>N/A</td>
<td>1.7462</td>
</tr>
<tr>
<td>n + 2 (odd)</td>
<td>0.04269</td>
<td>3.9379</td>
<td>40.686</td>
<td>1.7509</td>
</tr>
<tr>
<td>n + 3 (even)</td>
<td>0.04280</td>
<td>6.3624</td>
<td>N/A</td>
<td>1.7467</td>
</tr>
<tr>
<td>Mean</td>
<td>0.04275±0.00007</td>
<td>N/A</td>
<td>40.905±0.311</td>
<td>1.7487±0.0027</td>
</tr>
</tbody>
</table>

### 4.3 Device 2

When tested at room temperature, the device appeared to function properly, but when submerged into the liquid helium and tested in a low temperature environment, it was initially thought to be faulty. However, it appeared that the device was already in a state of Coulomb blockade due to a lack of biasing on the back gate. It was discovered that dot behaviour could be induced without any PBG’s whilst only applying a positive voltage to the back gate.

#### 4.3.1 Theoretical Capacitances

Unlike device 1, which used only the plunger gate, device 2 used the back gate to alter the levels inside the dot. This however means that determining $C_S$ and $C_D$ is impossible, since $d$ for both cases will be unknown. Instead, only $C_{BG}$ can be calculated. As before, the nanowire dimensions are measured with pixel measurements from Figure 8, giving $R_{NW} = 27.15$ nm. The length of the nanowire is assumed to be as per the EBL design at $L_{NW} = 350$ nm. It is known since prior that $d_{BG} = 100$ nm, which is through $\varepsilon_{SiO} = 3.9$ instead. Thus, using Equation 7 $C_{BG}$ can be determined.

$$C_{BG} = \frac{\pi \varepsilon_0 \varepsilon_{SiO}}{ln\left(\frac{2d_{BG}}{R_{NW}} - 1\right)}L_{NW} = 20.512 \text{ aF} \quad (11)$$
4.3.2 Small Back Gate Voltage Range Results

The range \(0.3 \text{ V} \leq V_G \leq 0.8 \text{ V}\) range was tested, with Figure 10 showing the initial result.

![Figure 10](image)

**Figure 10:** Edited intensity map showing the Coulomb diamonds found from device 2. The intensity in this graph does not represent the true \(dI/dV\) values.

The results seemed to end at \(V_G = 0.5\), but if a log scale was applied, then further diamonds could be found, as seen in give Figure 11.

![Figure 11](image)

**Figure 11:** A log scale of Figure 10, with an edited colour intensity scale. The dotted white and cyan lines differentiate between the two diamond gradient lines. The intensity in this graph does not represent the true \(dI/dV\) values.

From this figure, even if it might not be completely clear, there is an evident occurrence
of a gradient shift in the Coulomb diamonds between \( n + 2 \) and \( n + 1 \) whereby the lower diamonds attribute steeper sides. There also appears to have occurred something altering the electrical state of the device, leading to the horizontal defect clearly visible inside the \( n + 1 \) diamond separating the yellow and blue regions.

The properties of the device were determined using the same method as for Device 1. The results are listed in Table 2. Here, \( n \) should be treated as an anomaly since it deviates too strongly from the rest. Without it, standard deviation becomes near zero.

### 4.3.3 Larger Back Gate Voltage Range Results

Upon attempting a measurement of a larger range, the device appeared to have begun deteriorating. Figure 12 shows a measurement taken in the range of \( 0.3 \) \( V < V_G < 1.3 \) \( V \).

![Figure 12](image)

**Figure 12:** A graph containing a larger range of measurements for device 2. The intensity in this graph does not represent the true \( \text{dI/dV} \) values.

<table>
<thead>
<tr>
<th>Diamond</th>
<th>( \alpha_G )</th>
<th>( E_{ADD} ) [meV]</th>
<th>( C_\Sigma ) [aF]</th>
<th>( C_{BG} ) [aF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( n ) (odd)</td>
<td>0.11111</td>
<td>7.3333</td>
<td>21.848</td>
<td>3.1122</td>
</tr>
<tr>
<td>( n + 1 ) (even)</td>
<td>0.08846</td>
<td>6.3694</td>
<td>N/A</td>
<td>2.4779</td>
</tr>
<tr>
<td>( n + 2 ) (odd)</td>
<td>0.07362</td>
<td>5.1532</td>
<td>31.091</td>
<td>2.0620</td>
</tr>
<tr>
<td>( n + 3 ) (even)</td>
<td>0.07354</td>
<td>7.2072</td>
<td>N/A</td>
<td>2.0599</td>
</tr>
<tr>
<td>( n + 4 ) (odd)</td>
<td>0.07362</td>
<td>5.1532</td>
<td>31.091</td>
<td>2.0620</td>
</tr>
</tbody>
</table>

Table 2: Determined \( \alpha_G, \Delta E(E_{Add}) \) and capacitance values. Standard deviations for mean terms are also calculated.
It is worth noting that, in the figure, the Coulomb diamonds are no longer uniformly defined and appear to not follow the expected odd-even structure.

4.4 Device Overview

Using Equation 8, the energy required to add an additional electron can be determined for all trialled devices. Figure 13 and 14 shows exactly this.

**Figure 13:** Calculated $E_{ADD}$ values for Device 1 as compared to $E_C$, which is the minimum energy required.

**Figure 14:** Calculated $E_{ADD}$ values for the small (left) and large (right) voltage ranges trialled for Device 2 as compared to $E_C$, which is the minimum energy required.
5 Discussion

The synthesis of working quantum dot devices was achieved, and low temperature measurements of the Coulomb blockade region of these devices were carried out. Some theoretical capacitance estimation was also performed, finding the right order of capacitances, but with varying success for the two devices, as will be discussed further. However, there is much room for improvement and a fair few factors that have yet to be confirmed.

5.1 Validity of Results

5.1.1 Device 1

The $\Delta E$ and $C_\Sigma$ values were well within acceptable boundaries. Generally, in quantum dot devices of this size, the expected $\Delta E$ should be around 5 meV and $C_\Sigma$ should have a value in the order of 10’s of atto farads.[4] Finally, it is worth noting that odd-even diamond distribution is upheld in this the results from this device. However, the Coulomb diamonds visible in Figure 9 were quite difficult to discern, even after applying several intensity map modification to attempt to exaggerate the diamond border features. From just this, it is quite clear that there is some degree of error present in these results. Furthermore, the fact that the amplifier caused great over-saturation in the less negative $V_G$ regions, also caused further problems since the excited electron states could not be used to better identify the diamond borders.

Unfortunately, only one set of results could be produced from this device before it deteriorated to produce worse results, exhibiting great amount of leakage. This means that repeat measurements were impossible to achieve, and as such the measured properties cannot be assumed to be reliable. But since the mean capacitance value only has an approximate error of $\delta C_\Sigma = \pm 0.2185 \text{ aF}$, it could be considered accurate to two significant figures.

The capacitance $C_\Sigma$ was calculated about 4.751 aF lower than what was experimentally determined, but there could be several reasons for this. Firstly, the gate capacitance $C_G$ is near two thirds of the value that was theoretically determined (third term in the theoretical calculation). This is most probably due to an incorrect estimate of the capacitor area incident to the nanowire from the gate. As for the much larger capacitance, the potential barrier gates could have been made thinner than 20 nm, which would have
drastically increased the capacitance. More likely is that the effective area of influence of the electrostatically induced barrier is much smaller than the gates, causing this increase in capacitance. Furthermore, since about 100 nm of metal (15 nm titanium, and 85 nm gold) is deposited for each of the source, drain, potential barrier gates and plunger gate, it may well have increased the theoretical area $A$ that could be considered as the capacitor surface. On the other hand, it is much more likely that the theoretical calculation simply has the wrong dimensions for the area $A$ that defines the capacitor separated by distance $d$. But an 11% difference between theoretical and experimental in these conditions is really good.

5.1.2 Device 2

Coulomb oscillations produced from the second device could be considered incomplete. There appears to occur a shift in the measurement sampling set before and after $V_G = 0.526 V$, as is clearly evidenced in Figure 2 where there is a clear horizontal line that separates the high and lower intensity regions. No real conclusions can be drawn to suggest what caused this change, since it appears to change the diamond gradient as well. The only suggestions that can be put forth is that there occurred a charge reorganisation at the InAs-Oxide interface.

The focus of the measurements done on device 2 was to verify by which mechanism the quantum dot was being induced by. As stated prior, it was hypothesised that the potential barrier gates could have been shielding the back gate potential. Figure 15 shows the result of an attempt to offset the shielding, by introducing a $V_{PBG} = 1.5 V$ onto the PBG’s to try and remove the postulated shielding effect.

In theory, if it were so that the PBG’s were shielding the back gate potential, then this dot would still have produced a Coulomb blockade regime, but upon introducing a positive potential would reduce the size of the Coulomb oscillations, effectively “compressing” the height of the Coulomb diamonds. Interestingly, as is evident from the figure, the intensity map appears to suggest that the Coulomb diamonds were still present and, instead of having reduced height, had reduced width. Therefore, it is clear that making the PBG’s more positive did not have the intended effect on the Coulomb diamonds. Unfortunately, the lower region of this graph also shows were the device itself became damaged and begun to show excessive leakage, thus rendering any further experimentation impossible.
Figure 15: Depiction of the attempt to verify if the physical PBG’s were shielding the back gate potential, measuring current intensity across $I(V_{PBG}, V_{BG})$

The vast difference in the theoretical gate capacitance versus the experimentally determined gate capacitance is hard to explain. There may be several explanations, but none can be verified. An idea is that there was a dot formed in some defect within the nanowire itself, that allowed for a very small quantum dot to be induced. In fact, if assuming that the experimental results are correct, the estimated size of this dot is $L = 37$ nm. Alternatively, the Coulomb blockade regime could have been within bound states compressed in the narrowest part of the potential defining the quantum dot.

5.2 Potential Improvements

One of the most important improvements that could have been done for this study is repeat readings, and further testing on additional devices. Unfortunately, reliable and representative repeat readings were not possible since the devices trialled begun to experience leakage very early on. Therefore, trialling all 11 devices would have been preferable, or even trialling a new set of synthesised devices. The most important thing would have been to have enough time with device 2 to attempt to define exactly where the dot was being induced.

Only one device architecture was tested during the course of this study, and it would have been helpful to perform measurements on another device with a different architecture,
e.g. with the potential to properly symmetrically bias the gates to produce symmetric Coulomb diamonds. This would have improved accuracy and reduced interpretative errors when attempting to define the Coulomb barriers. In addition, comparisons between the nature of grown physical barriers and electrostatically gates ones could have also been explored further with additional device architectures.

6 Conclusion

Synthesis produced several electrostatically gated quantum dot devices that, upon inspection of their SEM images, appeared to have been successfully synthesised with no defects. From this outcome, two devices were tested to show the characteristic Coulomb blockade behaviour. These Coulomb diamonds could be used to accurately determine the lever arm $\alpha_G$, the energy level difference $\Delta E$ and both the self and gate capacitances $C_S, C_G$. Most importantly, these values are all within their respective orders of magnitude in value.

The hypothesis that the back gate potential could possibly be shielded by the PBG’s in order to define the quantum dot in the same region was disproved by the self capacitance difference of about 10 aF between device 1 and device 2, and by the fact that the Coulomb diamonds did not get a reduced height from the trial in Figure 15. If the shielding induced a dot between the PBG’s, the capacitance would be about the same. The percentage error was always less than 2 %, when measuring the self and gate capacitances, and thus the results could be considered reliable for both devices.

7 Outlook

The final results of this research shows promise for the development of smaller nanoscale devices to be used in a low temperature environment. More specifically, it shows the potential for the use of electrostatically gated devices instead of the more conventional physically gated devices. The increased simplicity of the architecture, limited only to EBL followed by metal deposition for source, drain, gate and potential barrier gates, usually produces a higher yield of functional devices since the margin of error is greater. This is in comparison to other methods, like epitaxial growth or aerotaxy, that instead grow the physical gates on the nanowire itself.
Since research into electrostatically gated devices is only very recent, most of the research is focused on simply studying the electron transport, specifically within the Coulomb blockade regime. As a result, attempts have been made to produce nanoscale versions of already prominent devices, like charge coupled devices (CCD) and complementary metal oxide semiconductors (CMOS). A recent study proved that this electrostatic gating can be used to produce these more complex devices that utilise the Coulomb blockade regime to operate.\[9\]

In summary, future research within this field should focus on further studying the potential that various different architectures of electrostatically gated devices have, and findings ways to more reliably reproduce high quality, low failure rate, samples. An important advancement would be to find a way to reliably automate the nanowire deposition, identification and EBL mapping procedures, since these are the most time consuming and human error prone segments of the synthesis process. Even writing software to automatically identify the Coulomb diamond dimensions and calculating the capacitance values would be beneficial.
References


Appendix A - Device Synthesis

A chip containing nine so called flower specimens, each with twelve symmetrically arranged contacts, were used in the fabrication of several quantum dot devices. The flower specimens can be seen in Figure 16, which contains an overview of its structure. The chip layout can also be seen in Figure 17, which also includes which flower specimens were unusable after this synthesis process.

Figure 16: A diagram showing an overview of the flower specimens, in addition to a close up of the gridded centre-point, where each of the contacts end. The red square denotes the zoom-in region between the left and right diagrams.

Figure 17: A simple graphic showing the flower specimen names, positions, and which ended up unused
Nanowire Deposition

A chip containing previously grown Indium Arsenide (InAs) nanowires was utilised in the transfer across onto the flower specimens. The transfer procedure is very straightforward.

1. A small triangle of clean-room paper is cut off, and the tip is dipped gently into the nanowire chip. This will pick up several nanowires onto the paper triangle.

2. The triangle is then gently tapped onto the centre of each of the nine flower specimens, depositing nanowires roughly across all specimens.

3. An optical microscope is utilised in dark field mode to ensure that nanowires were deposited into each specimen grid.

Ideally, each grid contains at least one nanowire deposited away and not contacting any other nanowires.

Device Design

The chip is observed in a Scanning Electron Microscope (SEM), where an overview picture of each specimen grid is taken, device candidate nanowires are selected, and a close up picture of each such nanowire is taken. Since there are twelve contacts in each specimen, it is possible to produce two devices with either five or six components.

For the first chip, the aim was to produce two devices per specimen, each containing a source, a drain, two barrier gates and a plunger gate, as can be seen in Figure 18. Since these contacts must be deposited using Electron Beam Lithography (EBL), a program must be used to plot the location of each nanowire, and show exact locations of gate and source components.

A program written by Claes Thelander, a professor at Lund University, is first used to match the SEM images to a pre-designed grid of the same dimensions which can be used directly with the EBL to print the devices.

1. The program asks for four grid dots to be selected in an \(X \times X\) square pattern, and will rotationally correct for, and assign the given scale scale (2.5 \(\mu m\) between each grid marker in this case). This only needs to be done once, since the SEM takes all images at the same rotation.
2. The co-ordinates of one of the selected grid markers is given, and then two points on a straight portion of the candidate nanowire are selected, whereby the program determines exactly where in the grid the nanowire is, and marks it.

3. A file containing the digitally reproduced grid, with a nanowire vector assigned to a specific co-ordinate is then exported.

4. RAITH, a design program, can import the specimen grid with the nanowire vector and superimpose the device design from Figure 18 over the nanowire vector.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{device_diagram}
\caption{Figures showing the device schematic (left) and circuit diagram (right)}
\end{figure}

5. Each component (Source, Drain and Gates) is then connected to a contact using a built in line tool in RAITH.

6. The designs are then exported as EBL maps that are compatible with the Lithograph.
Electron Beam Lithography of Source, Drain and Gates

Before performing the EBL, there are several preparatory steps

1. The chip is spin coated with a positive PMMA resist at 5000 RPM for one minute.

2. It is baked on an open hotplate at 180 °C for 3 minutes.

3. The EBL maps are read into the software that controls the lithograph and the EBL chamber is allowed to reach vacuum.

4. The sample is loaded onto the EBL disk which moves it into the machine. This step requires the chip to be clamped down, which most often needs to destroy one flower specimens. In this case, a4 was used for this purpose as it had no usable nanowire samples.

5. The internal SEM is used to focus and rotationally align the lithograph.

6. Corner alignment features are identified, these are used to rotationally correct the chip, and the SEM is used to burn a hole in the region between the fields.

Focusing is done by a systematic process, using the burn mark as a reference point. The machine will attempt to align itself to the mark, after which a manual correction is made. This is repeated until the machine can align itself without manual readjustment. A Faraday cup is used to determine the beam current, found to be 27.76 pA, after which the working distance, found to be 6.167775 mm, was determined. Therefore, a dose of 480 pA·cm² was required, whereby the region exposed per EBL point is 10 nm wide.

Since each field has four corner alignment features labelled in the EBL map, before performing the EBL, the SEM is used to align the machine to at least three of these features, which will allow the lithograph to accurately print the designs. Note that, while this process is repeated for each field, since the entire chip must be completed in two writes, another burn mark must be focused upon after completion of fields a1,a2,a3,a5 and a6 to allow a7,a8,a9 to also be processed with this method.
Metal Deposition and Lift-off

The metal evaporator is prepared by placing titanium and gold into separate tungsten boats. Sulphur passivation is then performed on the chip for 2 minutes in Ammonium polysulphide ($\text{NH}_4\text{S}_x$) diluted to 0.5% in water, first left to reach an equilibrium temperature 40°C. Immediately afterwards, the chip is dried in $\text{N}_2$, attached with carbon tape to the sample plate and is inserted into the metal evaporator. Next, a turbo pump is activated and 2 hours are allotted to allow for vacuum to be reached.

After vacuum is reached, 15 nm of titanium followed by 85 nm of gold are evaporated onto the sample. Titanium is evaporated first since it provides good adhesion to the InAs surface, gold is deposited since it is a very good conductor. The thickness of the layers does not need to be exact, but the gold layer needs to be thick enough to ensure that the deposition around the nanowire is continuous, to provide the best possible conductivity to it. The chip is placed in acetone overnight, the lift-off is performed, and the devices are observed carefully in an SEM while noting down which fields hold successful samples.
Appendix B - Raw Intensity Maps

Device 1

Figure 19: Raw dI/dV measurement data from Device 1 across $-0.01 \text{ V} \leq V_{SDB} \leq 0.01 \text{ V}$ with step size $0.0001 \text{ V}$ and $-1.5 \text{ V} \leq V_G \leq -0.75 \text{ V}$ with step size $0.002 \text{ V}$. Complementary to Figure 9 in the main text.

Device 2

Figure 20: Raw dI/dV measurement data from Device 2 across $-0.01 \text{ V} \leq V_{SDB} \leq 0.01 \text{ V}$ with step size $0.0001 \text{ V}$ and $0.3 \text{ V} \leq V_{BG} \leq -0.8 \text{ V}$ with step size $0.002 \text{ V}$. Complementary to Figure 11 in the main text.
Figure 21: Log scale of raw dI/dV measurement data from Device 2 across $-0.01 \, \text{V} \leq V_{SDB} \leq 0.01 \, \text{V}$ with step size 0.0001 V and $0.3 \, \text{V} \leq V_{BG} \leq -0.8 \, \text{V}$ with step size 0.002 V. Complementary to Figure 11 in the main text.

Figure 22: Log scale of raw dI/dV measurement data from Device 2 across $-0.01 \, \text{V} \leq V_{SDB} \leq 0.01 \, \text{V}$ with step size 0.0001 V and $0.3 \, \text{V} \leq V_{BG} \leq -1.3 \, \text{V}$ with step size 0.002 V. Complementary to Figure 12 in the main text.