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InAs nanowire metal-oxide-semiconductor capacitors

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We present a capacitance-voltage study for arrays of vertical InAs nanowires. Metal-oxide-semiconductor (MOS) capacitors are obtained by insulating the nanowires with a conformal 10 nm HfO_2 layer and using a top Cr/Au metallization as one of the capacitor's electrodes. The described fabrication and characterization technique enables a systematic investigation of the carrier density in the nanowires as well as of the quality of the MOS interface. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2949080]

The development of wrap-gate nanowire (NW) field effect transistors (FETs) is opening promising perspectives for future high-performance electronic devices.[1,2] NWs allow the integration of semiconductor materials with reduced lattice-matching constraints[3,4] and offer the intriguing possibility of growing III-V structures on Si substrates, thus introducing high-mobility and optically active elements on a Si platform.[5] However, many of the key parameters of the NWs such as doping level and carrier distribution are still difficult to determine in a direct and conclusive way. For conventional FETs it is possible to take advantage of capacitance-voltage (*CV*) characterizations to determine, in a precise way, carrier concentration and interface properties of planar metal-oxide-semiconductor (MOS) stacks. Similar measurements have been largely unavailable for semiconductor NWs because of the extremely small capacitance of these nanostructures (down to attofarad). Recent experimental studies showed that such a small capacitance can be detected using bridge measurements together with appropriate screening.[6] Here we demonstrate *CV* measurements of small arrays of vertical NWs, where the NW capacitance can be easily separated from the parasitic capacitance between the gate connection and the conducting substrate. Our vertical fabrication protocol is scalable and thus enables parallel processing, which is crucial for a systematic investigation of the device properties.

The device structure is presented in Fig. 1. NW arrays [Fig. 1(a)] were obtained by self-assembled growth in a chemical beam epitaxy system. NW formation is guided by gold nanoparticles that are deposited on a doped InAs (111)*B* substrate.[7] A number of arrays were defined in parallel with various nanoparticle sizes to study radius dependence. For the present investigation 5 different groups of 15 nominally identical NW arrays were fabricated with average radii r_{NW} of 23.0, 25.0, 26.5, 28.5 and 30.0 nm, respectively. Panel (b) shows a typical radius distribution in a single 11×11 array with a standard deviation of about 4.0 nm. The device structure is sketched in panels (c) and (d). NWs were first insulated by a conformal HfO_2 coating (purple) by atomic layer deposition (125 cycles at 250° C, corresponding to $d_{ox}\approx10$ nm); the top electrode encapsulating the NWs was then fabricated by sputtering a Cr/Au bilayer (nominal 20/25 nm). A polymeric film of S1813 from Shipley with a thickness of about 1 μm (green) was used as a lifting layer in order to increase the ratio C_{NW}/C_0 between the NW capacitance C_{NW} and stray capacitance C_0 in our devices. Single devices were finally defined by UV lithography and metal etching of 30×45 μm^2 gate pads.

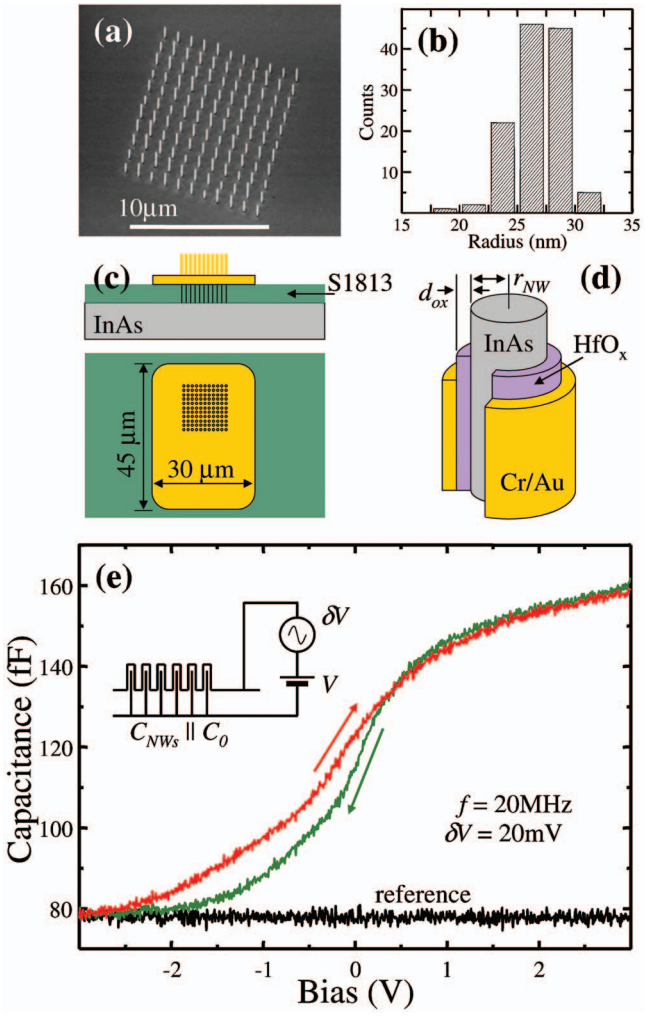

FIG. 1. (Color) (a) Scanning electron micrograph of an 11×11 InAs nanowire array (tilt angle of 52°). (b) Typical radius distribution in the array. [(c) and (d)] Details of the device structure. (e) Representative $C(V)$ scan from −3 to +3 V (red) and return (green) compared with a bare pad scan (black).

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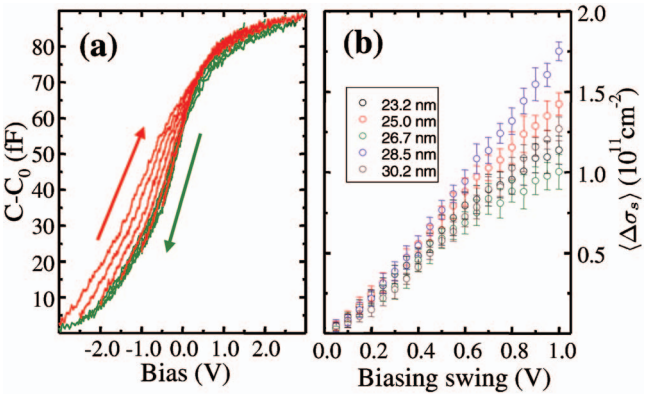

FIG. 2. (Color) (a) Evolution of the hysteresis cycle for increasing gate swings from $[-0.5,+0.5]$ up to $[-3.0,+3.0]$ V. (b) Charge loop integrals $\langle\Delta\sigma_s\rangle$ for different device geometries as a function of the biasing swing around 0 V.

The NW capacitance was measured at room temperature in a Cascade probe station system equipped with an Agilent 4294A impedance analyzer. The complex impedance $Z=|Z|e^{i\theta}$ was measured using a small ac modulation $\delta V=20$ mV on top of a dc bias V in the range $[-3\ \mathrm{V},+3\ \mathrm{V}]$. A simplified scheme of the biasing configuration is shown in the inset to Fig. 1(e). The measured Z was found to be mostly capacitive ($\theta\approx-90°$) and was interpreted in terms of a series RC model with $Z=R-i/\omega C$. Such a simple model is appropriate in our case and experimental $Z(\omega,V)$ data for $V\gtrsim+1$ V yield a frequency-independent and well-defined $C(V)$. The frequency evolution of $Z(\omega,V)$ in the depletion regime for $V<0$ is less trivial as expected due to the increasing NW resistance, to the activation of slow trap states at the interfaces, and to effects of inversion in the InAs semiconductor. In particular, the increasing importance of RC constants close to the pinch-off is a peculiarity of our cylindrical geometry and sets a qualitative difference with respect to conventional planar MOS capacitors. The plot in Fig. 1(e) shows typical $C(V)$ sweeps obtained on devices from the group $r_{\mathrm{NW}}=26.5$ nm at a frequency $f=20$ MHz: we mark the sweep going from negative to positive as $C_{\uparrow}(V)$ (red) and $C_{\downarrow}(V)$ for the opposite sweep direction (green). The capacitance saturates at negative voltages to $C_0\approx70-80$ fF, grows sharply across $V\approx0$ V, and flattens again for $V>1$ V in the accumulation regime. Differently from conventional MOS capacitors, here we expect the NW to become insulating in the depletion limit and C to approach *zero* instead of a finite depletion capacitance. Indeed, here the observed saturation $C\to C_0$ corresponds to the NW depletion, as proved by comparison with four bare pads of the same geometry (black curve). The presence of C_0 is not linked to the NWs and it is rather due to both the parallel capacitance between the pad and the substrate as well as the one between the probe tips and the substrate.

Hysteresis effects are analyzed in Fig. 2. In the first panel, the shift between the capacitances measured in the two opposite sweep directions is barely visible on small (less than 1 V) sweep ranges while it increases for larger V swings. $C_{\downarrow}(V)$ curves do not depend strongly on the dc sweep swing while $C_{\uparrow}(V)$ curves tends to move toward higher C values (or lower V values, for a given C) when the sweep is extended from ±0.5 up to ±3.0 V. The shift between $C_{\uparrow}$ and $C_{\downarrow}$ does not depend strongly on the sweep speed (about 150 mV/s in our case) and time-dependent measurements indicate that capacitances tend to relax from $C_{\uparrow}(V)$ toward $C_{\downarrow}(V)$ on a timescale $\tau\approx30$ min. We conclude that $C_{\downarrow}(V)$ results from an equilibrium distribution of charges at the capacitor's interfaces while a long-lived out-of-equilibrium distribution is present along $C_{\uparrow}(V)$. This effect can be evaluated quantitatively in a simple way if one assumes that trapped charges are located exactly at the NW surface: in that case the addition of a surface charge density $\Delta\sigma_s$ will shift an ideal $C(V)$ curve as

$$C_{\mathrm{meas}}(V)=C(V+S_{\mathrm{NW}}\times\Delta\sigma_s/C_{\mathrm{ox}}),\tag{1}$$

where $S_{\mathrm{NW}}=2\pi r_{\mathrm{NW}}L_{\mathrm{NW}}$ and L_{NW} are the surface and length of the gated NW, respectively, while C_{ox} is the oxide capacity $2\pi\varepsilon L_{\mathrm{NW}}/\log(1+d_{\mathrm{ox}}/r_{\mathrm{NW}})$. The value of $\Delta\sigma_s$ depends on the biasing history of the device; thus we obtain the different hysteresis cycles for different sweep swings. Figure 2(b) shows the average surface charge,

$$\langle\Delta\sigma_s\rangle=\frac{C_{\mathrm{ox}}}{S_{\mathrm{NW}}}\frac{1}{\Delta C}\oint CdV,\tag{2}$$

where ΔC is the capacitance swing of the cycle and we used an average $L_{\mathrm{NW}}=680$ nm (from scanning electron imaging of the devices), $\varepsilon=15\varepsilon_0$,[8,9] and $C_{\mathrm{ox}}=1.78$ fF. The plot reports the loop integrals for the various device groups we studied: for V swings below ≈0.5 V we obtain $\langle\Delta\sigma_s\rangle<1.0\times10^{11}$ cm^{-2}, which seems very promising for device applications of NW as wrap-gate transistors.[10] Note however, that the hysteresis in the surface charge becomes much larger if the bias sweep extends further into the depletion region.

To further analyze the data, we performed detailed calculations for the capacitance on the basis of a Poisson–Schrödinger code similar to Refs. 11 and 12. Figure 3(a) shows the unit length capacitance for three different doping

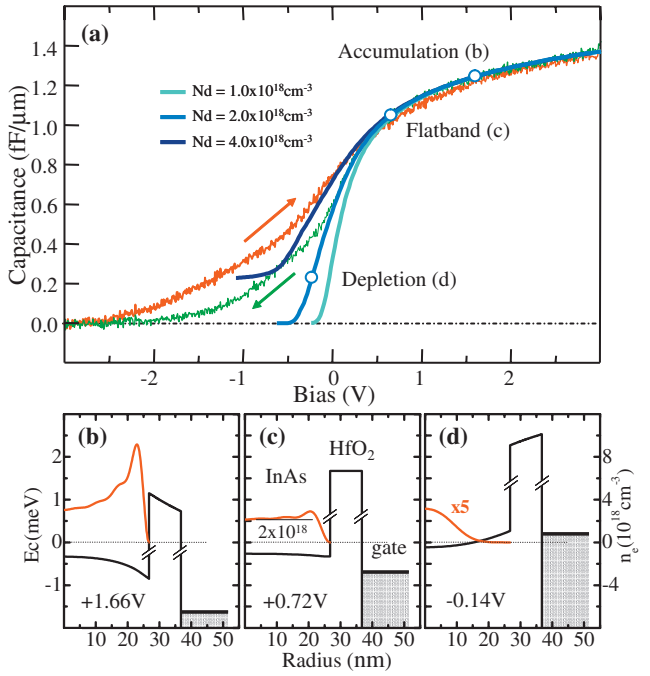

FIG. 3. (Color) (a) Theoretical fit of the dataset $C_{\downarrow}(V)$ of Fig. 1(e) using three different carrier densities. The band bending (black) and electron density (red) at the three different points along the blue line at doping $N_d=2\times10^{18}$ cm^{-3} are reported in the lower panels for accumulation (b), flatband (c), and depletion (d) conditions.

densities N_d of the wire, which are treated as a homogeneous positive background charge. The experimental data shown correspond to the assumption that 90 out of 121 wires are actually properly connected in the device: this scaling is required in order to match the geometry-set capacitance in accumulation and is not unreasonable given the present device parameters. The best fit is obtained using a doping of 2.0×10^{18} cm^{-3}: the curve at 1.0×10^{18} cm^{-3} rolls down too quickly with the voltage V. Differently at $N_d=4.0\times10^{18}$ cm^{-3} the valence bands cross the Fermi level at the interface before the conduction band is completely depleted (0.54 eV was used as the wurtzite InAs gap[13]) and screening effects due to inversion are expected to show up, inconsistently with observations. It is interesting to note that all the fit curves in Fig. 3(a) fall nearly 50% short of the classical $C_{ox}=2.61$ fF (for a 1.0 μm length, $r_{NW}=26.5$ nm, and $d_{ox}=10$ nm) even in the accumulation regime at $V\approx+3.0$ V. This is an effect of quantum capacitance that is due to the narrow radius of the NW with respect to the screening length. Lower panels indicate the corresponding conduction band diagram $E_c(r)$ in the capacitor in the accumulation (b), flatband (c), and depletion (d) regimes: the corresponding positions along the $C(V)$ fit are indicated in the top panel. We obtained the best agreement assuming the gate bias V to be 0.39 V larger than the calculated electrostatic potential at the gate. This shift can be attributed to the difference between the work function of Cr (4.5 eV) and the electron affinity of InAs (4.9 eV for zincblende lattice) as well as negative fixed charges with areal density $\approx8\times10^{12}$ cm^{-2} trapped in oxide. As the electron affinity of the nanowire is uncertain due to the uncommon wurtzite structure exhibiting a larger band gap,[13] this estimate for the density of fixed charges is probably too large. It is crucial to note here that we assumed that only electrons in the conduction band are able to contribute to the $C(V)$ at our frequency. We interpret the discrepancy between fit and experiments for $V<0$ V as due to the effect of screening of slow trap states in the InAs gap,[14] which indeed start becoming important at $V\approx0$ V in our simulations. Consistently with this interpretation, we observed experimentally that such discrepancies become larger as the frequency is decreased and a clear $C(V)$ step develops, similarly to what has been reported in previous studies on planar structures.[15]

In conclusion we have demonstrated a technique for capacitance-voltage characterizations of arrays of vertical InAs NWs. Our analysis allows evaluating the role of surface states as well as yields an estimate of the doping in the NW, thanks to a detailed comparison with Poisson–Schrödinger simulations. Preliminary results indicate promising device parameters in view of the application of wrap-gate NWs as high-performance transistors.

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[1] T. Bryllert, L.-E. Wernersson, T. Löwgren, and L. Samuelson, Nanotechnology **17**, S227 (2006).
[2] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, Nature (London) **441**, 489 (2006).
[3] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, and L. Samuelson, Nano Lett. **2**, 87 (2002).
[4] M. W. Larsson, J. B. Wagner, M. Wallin, P. Håkansson, L. E. Fröberg, L. Samuelson, and L. R. Wallenberg, Nanotechnology **18**, 015504 (2007).
[5] T. Mårtensson, J. B. Wagner, E. Hilner, A. Mikkelsen, C. Thelander, J. Stangl, B. J. Ohlsson, A. Gustafsson, E. Lundgren, L. Samuelson, and W. Seifert, Adv. Mater. (Weinheim, Ger.) **19**, 1801 (2007).
[6] R. Tu, L. Zhang, Y. Nishi, and H. Dai, Nano Lett. **7**, 1561 (2007).
[7] L. E. Jensen, M. T. Björk, S. Jeppesen, A. I. Persson, B. J. Ohlsson, and L. Samuelson, Nano Lett. **4**, 1961 (2004).
[8] D. Wheeler, A. Seabaugh, L. Fröberg, C. Thelander, and L.-E. Wernersson, Semiconductor Device Research Symposium, 2007 International, Washington, DC, 12–14 December 2007 (unpublished), pp. 1–2.
[9] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskelä, Chem. Vap. Deposition **8**, 199 (2002).
[10] C. Rehnstedt, T. Mårtensson, C. Thelander, L. Samuelson, and L.-E. Wernersson, Proceedings of the Device Research Conference, Notre Dame, 2007 (unpublished), pp. 135–136.
[11] E. Gnani, A. Marchi, S. Reggiani, M. Rudan, and G. Baccarani, Solid-State Electron. **50**, 709 (2006).
[12] L. Wang, D. Wang, and P. M. Aspeck, Solid-State Electron. **50**, 1732 (2006).
[13] J. Trägård, A. I. Persson, J. B. Wagner, D. Hessman, and L. Samuelsson, J. Appl. Phys. **101**, 123701 (2007).
[14] S. A. Dayeh, C. Soci, P. K. L. Yu, and E. T. Yu, D. Wang, Appl. Phys. Lett. **90**, 162112 (2007).
[15] P. Masson, J.-L. Autran, M. Houssa, X. Garros, and C. Leroux, Appl. Phys. Lett. **81**, 3392 (2002).