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A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit Switched Tuning

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***Abstract*— A 24 GHz 130-nm CMOS quadrature voltage controlled oscillator using 4-bit switched frequency tuning is presented. It consists of two differential oscillators coupled to oscillate in quadrature through transistors and mutual inductance between the source nodes. The frequency tuning is accomplished by 4 bits controlling an array of MOS varactors in each resonance tank, combined with a small continuously tuned varactor. The oscillator measures a frequency tuning range of 4.3%, and a worst case phase noise over the tuning range of -111.6 dBc/Hz at 1 MHz offset, with a 1.35 V supply and a power consumption of 24 mW.**

I. Introduction

Quadrature local oscillator signals are extensively used in modern wireless transceivers, which often use direct conversion or low-IF architectures. A commonly used technique to generate such quadrature signals is to use two coupled differential LC oscillators. This paper presents measurement results of such a quadrature oscillator operating at 24 GHz. The frequency tuning is realized using switched coarse tuning combined with continuous fine tuning [1]. In each resonance tank there is a small continuously tuned varactor, as well as an array of MOS varactors controlled by 4 digital bits. This is a modification of an oscillator previously reported by the authors [2], which was based on the original QVCO topology proposed by Rofougaran [3].

II. Circuit Design

The oscillator schematic is shown in Fig. 1. The QVCO previously reported by the authors [2] had a significant phase noise variation over the tuning range. The resonator was therefore modified to use 4 digital coarse tuning bits and a reduced size continuously tuned varactor. The ratio of the width of the coupling transistor to the width of the switch transistors was kept at 1/3.

As in the previous QVCO the phase noise is minimized by using a FET current source and applying filtering [4] at the source nodes of the two LC-oscillators. A current source is used because the best phase noise performance is achieved when the amplitude in the resonance tank is on the limit of being current limited. This requires a noiseless and high impedance current source to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state, i.e. when one transistor is off and the other one is in the triode region. Thus, a differential source inductor is used to resonate the parasitics of the source nodes at $2f_0$. The source inductor then approximates a high impedance current source at $2f_0$. Also, a capacitor in parallell with the current source shunts the high frequency noise at $2f_0$ from the current source to ground.

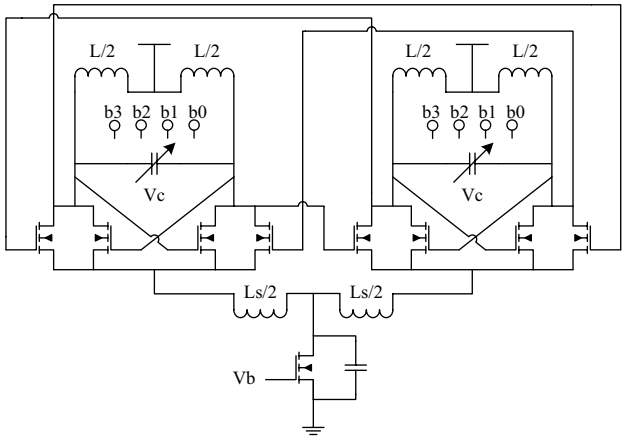

Fig. 1. QVCO Schematic

Simultaneously achieving a large frequency tuning range and a low phase noise is a major challenge in oscillator design. In oscillators using continuous frequency tuning, a large tuning range is obtained using a large varactor with a high maximum to minimum capacitance ratio. Noise and spuriouses on the varactor control voltage can then translate into significant phase noise and sidebands. The filtering technique described above prevents tail current noise at $2f_0$ from creating phase noise, but low frequency tail current noise will still cause amplitude noise. As shown in [5], the nonlinearities of the varactor convert harmless amplitude noise into phase noise. The larger the varactor the larger the problem. Furthermore, the Q of the varactor is due to series resistance inversely proportional to frequency. At high frequencies and wide tuning ranges, the varactor will therefore limit the total Q of the tank.

The varactors in this circuit are implemented using nMOS transistors operating in inversion-mode. By accepting a smaller maximum to minimum capacitance ra-

TABLE I
RELATIVE TANK CAPACITANCE

b3	b2	b1	b0	Vc
4x	2x	1x	1x	2x

TABLE II
SIMULATED INDUCTOR DATA

Inductor	Inductance (pH)	Q	fs (GHz)
L @ f_0	200	33	115
Ls @ $2f_0$	190	37	140

tio, the minimum channel length could be used, maximizing the Q of the varactor and thereby the whole resonator. For layout reasons the relative capacitance of the different bits and the continuous part was chosen according to Table I. Ignoring the parasitics, there will then be nine different states that can be used. The different states are set by applying either 0 V or 1.5 V on the digital control bits. The continuously tuned varactor has size 2x to ensure overlap between the different states.

Differential single turn inductors are used in this circuit. The capacitively coupled substrate losses are blocked by using patterned ground shields in metal 1 beneath the inductors. The in-house inductor optimization tool, Indentro [6], was used to find the inductor geometries. The simulated inductor data is shown in Table II. The source inductor has the same size as in the previous QVCO, [2], but the tank inductors were made slightly larger to lower the oscillation frequency.

The oscillator is connected to open drain buffers implemented on the same chip. The buffers are used to enable measurements and are designed to drive 50 Ω loads.

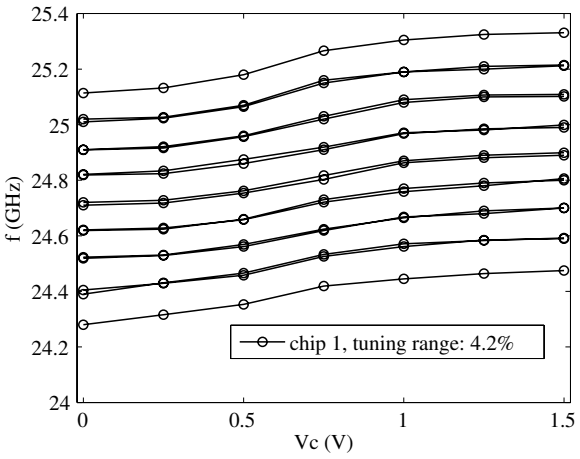

Fig. 2. Frequency vs. control voltage for chip 1

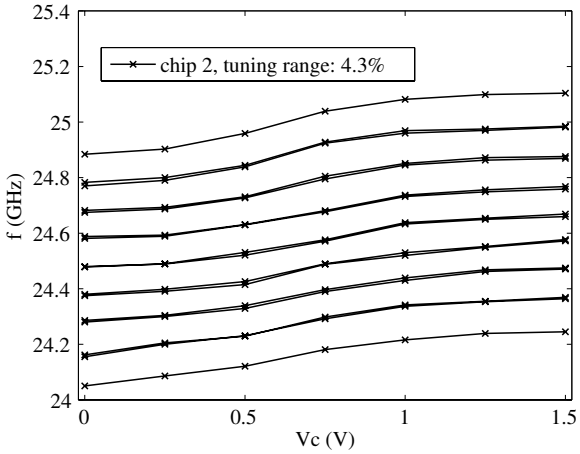

Fig. 3. Frequency vs. control voltage for chip 2

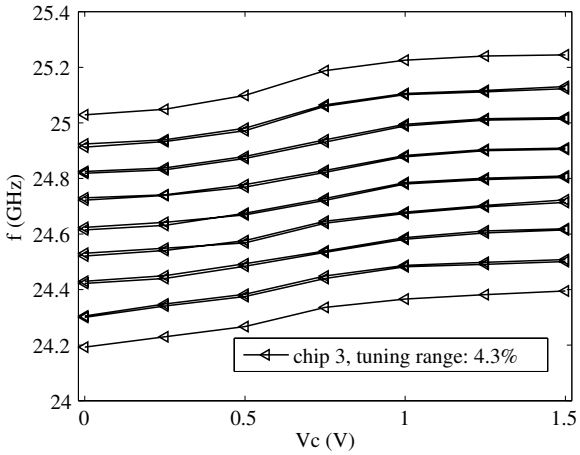

Fig. 4. Frequency vs. control voltage for chip 3

III. LAYOUT

The die photo of the oscillator is shown in Fig. 10, where the padframe area measures 985μm x 843μm. The pads on the top side are the four digital control bits and the varactor control voltage, Vc. The pads on the bottom side are used for supply and bias voltages. The outputs of the buffers are located on the left and right sides of the padframe. There are four coupling signal lines between the two differential oscillators. The length of these lines were kept as equal as possible to minimize phase errors. For the same reason the entire layout was designed as symmetric as possible.

IV. EXPERIMENTAL RESULTS

Three different samples of the oscillator have been measured. The measurements were performed with a probestation using on-wafer probing with signal-ground-signal (SGS) probes for the RF output and DC probes for biasing. The best performance of the quadrature oscillator was found at 1.35 V supply and 18 mA current. This gives a

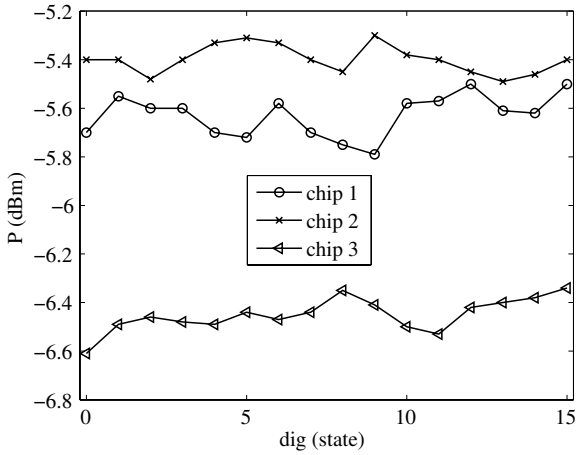

Fig. 5. Output power vs. dig (state) for Vc=0.75 V

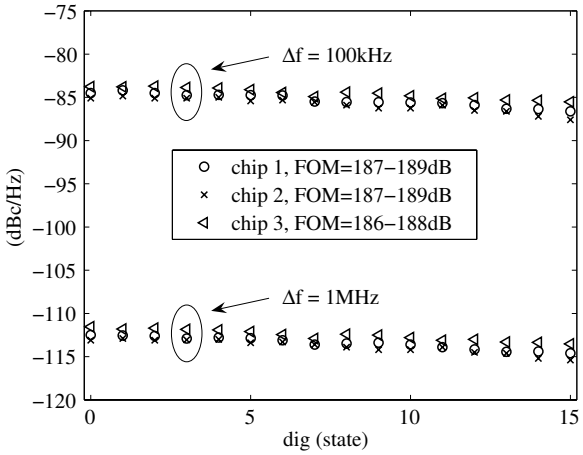

Fig. 7. Phase noise vs. dig (state) for Vc=0.75 V

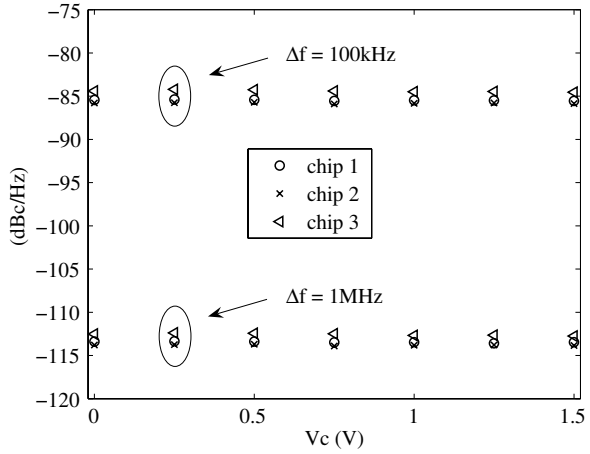

Fig. 6. Phase noise vs. control voltage for state 8 (1000)

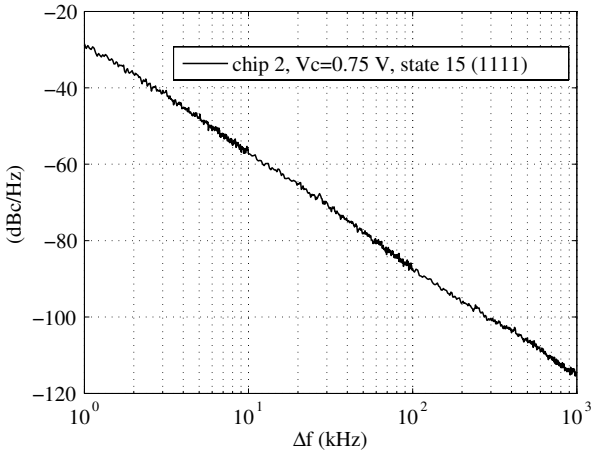

Fig. 8. Phase Noise, state 15 (1111) & Vc=0.75 V, for chip 2

power consumption of 24 mW for the quadrature oscillator core. The open-drain buffers were biased to a drain voltage of 1 V and a drain current of 9.4 mA per buffer. The following results were measured at this bias point.

A spectrum analyzer was used to measure the frequency tuning range and the buffer output power. The tuning characteristic for the three different samples can be seen in Fig. 2 - 4. As can be seen in the figures the tuning range is 4.3% and overlap between the different states guarantees continuous frequency coverage. The output power from the buffer for the three chips is shown in Fig. 5.

The phase noise of the three chips was measured using a Europtest PN9000 phase noise measurement system together with an external downconversion mixer. The previous QVCO had the worst phase noise in the middle of the tuning range. This is why the phase noise was measured for the mid state (b3b2b1b0=1000) versus the varactor control voltage, Fig. 6. As can be seen in the figure, the phase noise is almost flat over the varactor control voltage range, which corresponds to about 200 MHz in frequency tuning. The phase noise was also measured for the different states while keeping the varactor control voltage at Vc=0.75 V, Fig. 7. There is a phase noise variation of about 3 dB over the different states. Also shown in the legend of Fig. 7 is the phase noise figure of merit, FOM, which is between 186 dB and 189 dB for the measured samples, calculated at 1 MHz offset frequency using

$$FOM = 10\,log_{10}\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{10^{\frac{L(\Delta f)}{10}} P}\right) \qquad (1)$$

,where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L(\Delta f)$ the phase noise at Δf. The phase noise is also plotted versus offset frequency, Δf, for state 15 (1111) and Vc=0.75 V for chip 2, Fig. 8. A performance comparison of some previously reported QVCOs and this work is shown in Table III. Some references in the table report only the best case value of the phase noise, but it is the worst case value over the tuning range that should be used for comparison. To take also the tuning

TABLE III
PERFORMANCE OF SOME PREVIOUSLY REPORTED QVCOS AND THIS WORK

Ref.	Process	Frequency (GHz)	PN @ 1 MHz (dBc/Hz)	Core P_{DC} (mW)	FOM (dB)	FOM_T (dB)
This work	0.13μm CMOS	24.19-25.25	-111.6*	24	186	178
[7]	0.18μm CMOS	10.18-11.37	-118.7	11.8	188	189
[8]	0.13μm CMOS	44.8-45.8	-98.9	40	176	163
[2]	0.13μm CMOS	25.7-26.5	-96*	24	171	161
[9]	0.4μm SiGe	24.8-28.9	-84.2	129	152	156
[10]	0.25μm SiGe	30.6-32.6	-97	140	166	162

*worst case phase noise over the tuning range

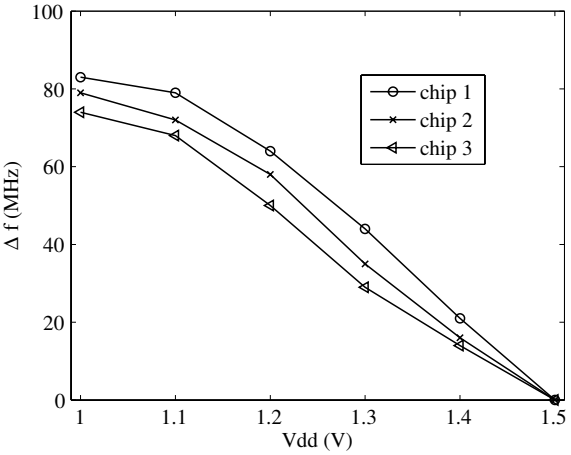

Fig. 9. Oscillator frequency pushing, state 8 (1000) & Vc=0.75 V

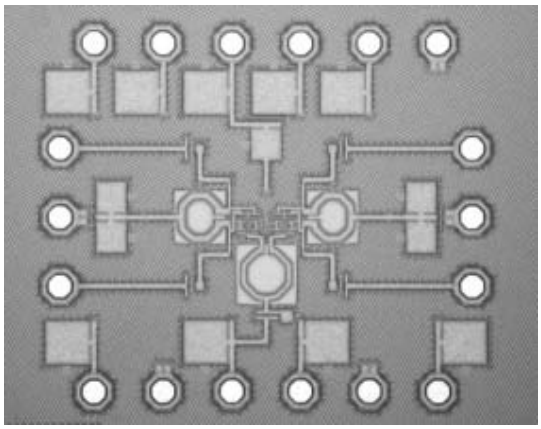

Fig. 10. Die photograph of the QVCO (985μm x 843μm).

range into account expression (1) can be modified [11]

$$FOM_T = 10log_{10}\left(\left(\frac{f_0 \cdot tuning\,(\%)}{10 \cdot \Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P}\right) \quad (2)$$

,which is also shown in Table III for comparison.

The oscillator pushing is shown in Fig. 9. As can be seen in the figure, there is approximately an 80 MHz frequency change for a supply voltage change from 1.5 V to 1 V.

V. CONCLUSION

A 24 GHz P-QVCO using 4-bit switched tuning has been implemented in a 130-nm CMOS process. The oscillator measures a frequency tuning range of 4.3%. A good phase noise performance is measured over the entire tuning range, at worst -111.6 dBc/Hz at 1 MHz offset, with a core power consumption of 24 mW. This gives a phase noise figure of merit, FOM, of 186 dB.

VI. ACKNOWLEDGMENT

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