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A 20-GHz 130-nm CMOS Front-End using Baluns on Glass Carrier

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***Abstract*—A 20-GHz 130-nm CMOS front-end using baluns on glass carrier is presented. The front-end consists of a CMOS die featuring a differential two-stage LNA, a passive double balanced mixer, and output buffers, which is flip-chipped on a glass carrier where baluns are realized for the RF and LO signals. The front-end measures a conversion gain of 11 dB, a noise figure of 7 dB, a 60 dB LO to RF isolation, an ICP_{1dB} of -16 dBm, an IIP3 of -5.2 dBm, and an IIP2 of +34.5 dBm. The power consumption, excluding output buffers, is 38 mW. Furthermore, the RF input is well protected as it can withstand a simulated 3 kV HBM ESD event.**

I. Introduction

The evolution of high data rate wireless communication systems has increased the demand for more bandwidth, which can be fulfilled by employing more and wider bands at higher frequencies for communications. The scaling of CMOS has now made it a viable technology for high frequency cost sensitive consumer applications. Publications have demonstrated high performance CMOS receiver front-ends at 60 GHz [1], and 24 GHz [2].

Differential receiver topologies are known to have higher linearity and a higher degree of stability compared to single-ended topologies, at the expense of higher power consumption. These properties were reported already 1965 [3]. A disadvantage of differential topologies is that the antenna signal typically is single-ended, and that a balun then is needed to convert it to differential form. To achieve good noise performance the balun must have low losses, which makes it difficult to realize on chip.

This paper presents measurement results of a front-end using a differential topology for increased linearity, and capacitive cross-coupling for increased LO to RF isolation. The CMOS die is flip-chipped on a glass carrier, where low loss baluns are realized for the RF and LO input signals.

II. Circuit Design

The block schematic of the front-end is shown in Fig. 1. It consists of a differential two-stage LNA, a passive double balanced mixer, and open drain output buffers. The baluns on the glass carrier, to generate the differential RF and LO input signals, are also shown in the figure.

The first stage of the LNA is an inductively degenerated common-source stage with a cascode device as shown in Fig. 2. This topology provides good input matching, a low noise figure, and high reverse isolation. To further increase the differential isolation, a capacitive cross-coupling technique is used. Capacitors C1 and C2 form voltage dividers used to feed part of the output signal to the gate of the opposite cascode devices. By setting the voltage division ratio correctly, the currents due to the drain-source conductance of the cascode devices can be cancelled for differential signals. Techniques like this will become more important when the MOS transistors are scaled to shorter channel lengths, since the drain-source conductance then increases. Spiral shunt inductors, Lsh, are used at the input to resonate with the capacitances of the pad and the flip-chip bump. The shunt inductors also provide good ESD protection to the input transistor gates. The gate inductance, Lg, is realized by two wires close to each other, and a small loop, which can be seen in the die photograph, Fig. 11. Differential inductors are used to provide inductive degeneration, Ls, and to resonate the output, La. The ouput of the first stage is loaded by the input impedance of the second stage of the LNA.

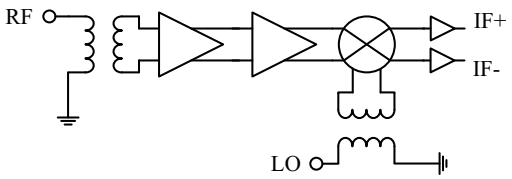

Fig. 1. Front-end block schematic

The second stage of the LNA is a differential common-source stage with cascode devices and capacitive cross-coupling, as shown in Fig. 3. The output is resonated by a differential inductor, Lb, and is also loaded by the input impedance of the mixer.

Having a two-stage LNA provides sufficiant gain for a passive mixer to be used. In this circuit, a double-balanced passive mixer is used. To enable measurements, open-drain buffers designed to drive $50\ \Omega$ loads are connected to the ouputs of the mixer. The mixer and open-drain buffers are shown in Fig. 4. The RF signal is AC-coupled to the mixer, pre-

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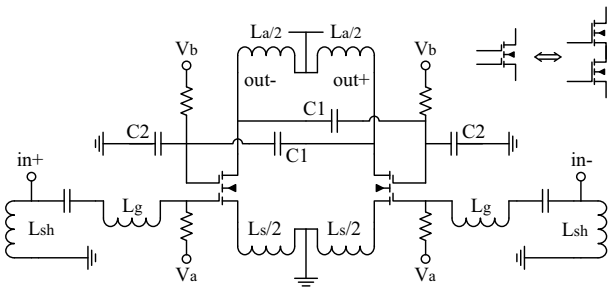

Fig. 2. First stage of the LNA

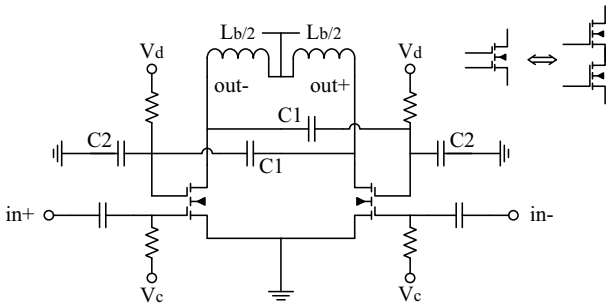

Fig. 3. Second stage of the LNA

venting DC-current, and setting the DC-voltage to zero through 40 kΩ resistors. In this way fast NMOS mixer devices can be used.

This circuit uses differential single turn and two turn spiral inductors. Their geometries were found by using FastHenry in combination with the in-house inductor optimization tool, Indentro [4]. Patterned ground shields in metal 1 are used beneath the inductors to block capacitively coupled substrate losses. The simulated inductance, quality factor, and self resonance frequency of the inductors are shown in Table I.

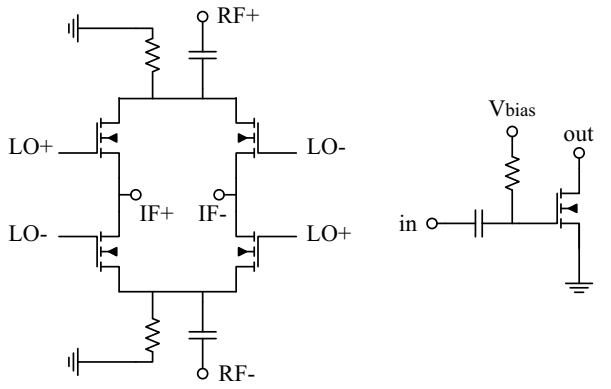

Fig. 4. Passive mixer and output buffer

TABLE I
INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
Lg	1	170	15	140
Lsh	2	220	18	56
Ls	1	230	27	126
La	1	180	29	130
Lb	1	240	32	97

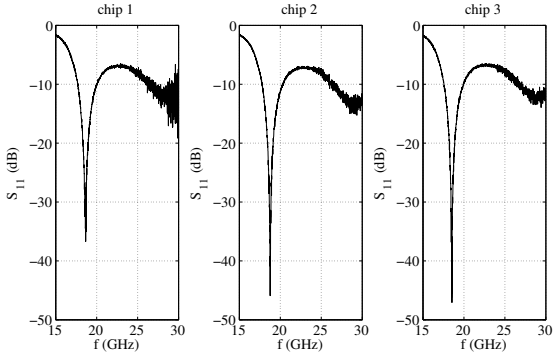

Fig. 5. Measured input matching of the three chips

III. LAYOUT

To minimize parasitic capacitance between the common-source and cascode transistors of the LNA, and thereby the noise contribution of the cascode device, a double-gate transistor layout was used [5]. The reduced capacitance also has a positive effect on the gain. The joint layout is indicated by the double gate transistor symbols used in Fig. 2 and 3.

The chip layout was designed as symmetrical as possible to minimize amplitude and phase errors. The die photo is shown in Fig. 11, where the padframe area measures

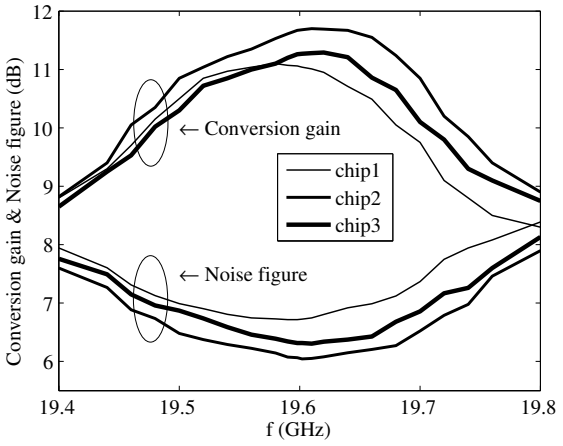

Fig. 6. Measured conversion gain & noise figure with LO = 19.6 GHz

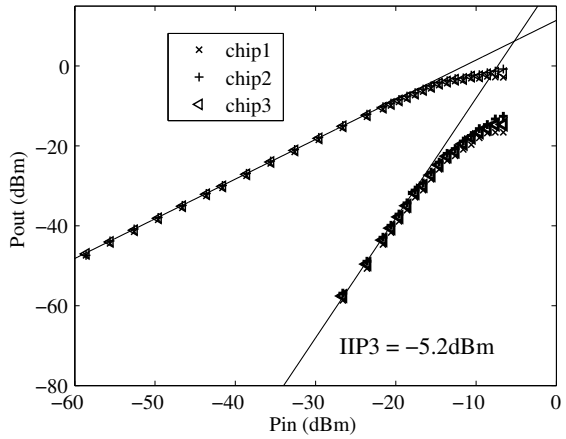

Fig. 7. Measured third order nonlinearity

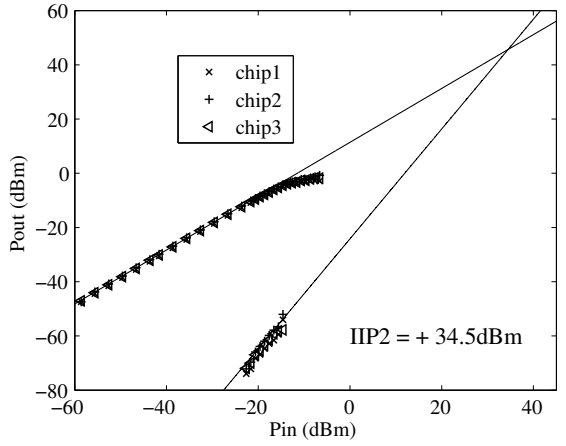

Fig. 8. Measured second order nonlinearity

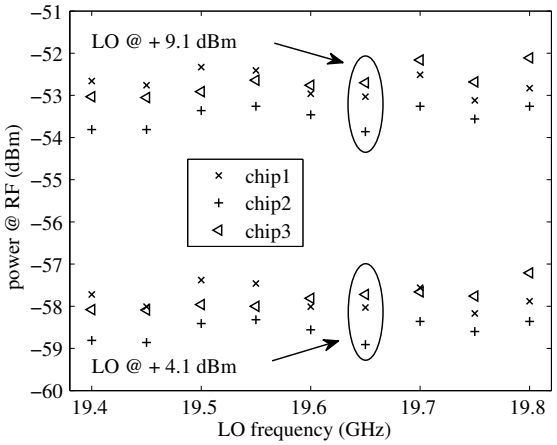

Fig. 9. Measured LO-RF isolation

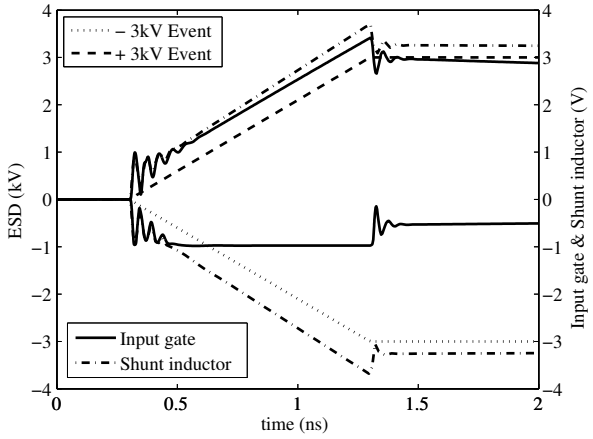

Fig. 10. Simulated HBM ESD events

1435μm x 985μm. The die was flip-chipped on a glass carrier, which is shown in Fig. 12. The chip can seen in the middle of the figure and the baluns for the RF and LO inputs can be seen on the left and right sides of the chip. The padframe area of the carrier measures 5620μm x 4960μm. The carrier was then glued to a PCB, and DC connections (supply, bias and ground) and IF outputs were wire-bonded from the carrier to the PCB.

IV. Results

Three samples of the front-end have been measured. Instruments used were Rhode & Schwarz spectrum analyzer (FSU50), Agilent network analyzer (E8361A) and signal generators (E8257D).

The measurements were performed with a probestation using Cascade Microtech ground-signal-ground (GSG) probes for the RF and LO input signals on the carrier. The IF outputs were connected to a Minicircuits balun, T2-1T (0.07 to 200 MHz), through bias-T:s. The best performance of the front-end was found at 1.35 V supply and 28 mA current for the LNA. The power consumption is then 38 mW, excluding the buffers. The open-drain buffers were biased to a drain voltage of 1.35 V and a drain current of 8.4 mA each, which gives a total power consumption of 60 mW. The following results were measured at this bias point.

The measured input matching for the three chips is shown in Fig. 5. The matching is good just below 20 GHz, where also the highest gain is observed. A second resonance that could not be seen in simulations was observed for all chips. This is probably due to improper modeling of the transition from chip to carrier.

The conversion gain and noise figure have also been measured, Fig. 6, where the LO frequency and amplitude was kept at 19.6 GHz and 9.1 dBm, respectively. At about 19.6 GHz, close to zero-IF, the conversion gain is above 11 dB and the noise figure below 7 dB.

The linearity was measured using two tone tests, one for

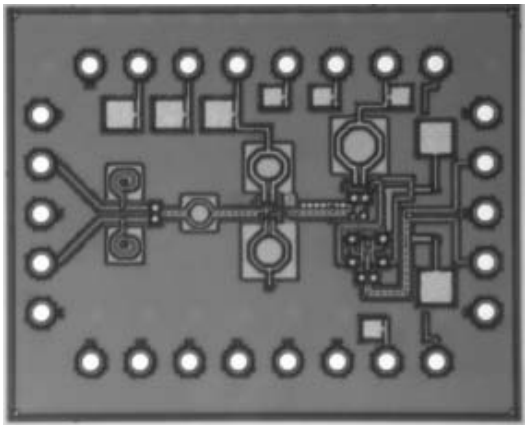

Fig. 11. Die photograph (1435μm x 985μm)

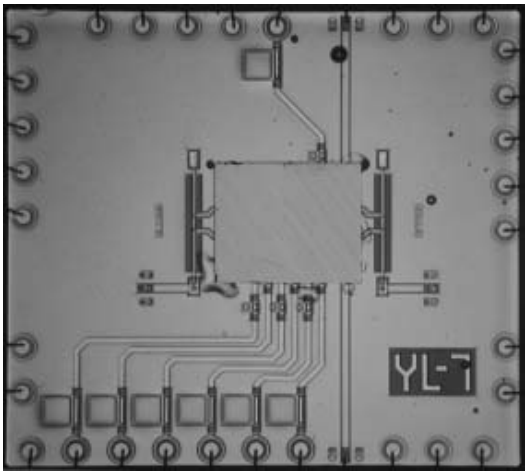

Fig. 12. Photograph of the die mounted on carrier (5620μm x 4960μm)

third order and one for second order intermodulation.

The two tones and the LO frequency were chosen such that the intermodulation product occured at an IF of 3 MHz. When measuring the second order nonlinearity a fifth order low-pass filter with a cut off frequency of 5 MHz was used to prevent intermodulation of the first order IF output tones (placed at 20 MHz and 23 MHz) in the spectrum analyzer. The input-referred 1 dB compression point, ICP_{1dB}, and third-order intermodulation, IIP3, are shown in Fig. 7. The ICP_{1dB} and IIP3 measures -16 dBm and -5.2 dBm, respectively. The second-order intermodulation measures +34.5 dBm and is shown in Fig. 8.

The LO to RF isolation has been measured at two different LO amplitudes, Fig. 9. As can be seen in the figure the isolation is at least 60 dB.

The ESD protection at the RF input has been simulated using the human body model (HBM), [6] [7]. A capacitor of 100 pF is first charged and then discharged through a 1500 Ω resistor to the test circuit. In Fig. 10 the voltages at the shunt inductor and input gate of the LNA are plotted for two simulated ESD events, +3 kV and -3 kV, with a rise time of 1 ns. As can be seen in the figure, the input gate of the LNA is well protected. For the negative event the gate is also protected by a diode used to prevent antenna errors during the chip fabrication, hence the lower voltage at the gate in Fig. 10.

V. Conclusion

A 20-GHz front-end in 130-nm CMOS using baluns on glass carrier has been presented. It achieves a conversion gain of 11 dB and a NF of 7 dB. The balanced topology enables a measured third-order input referred intercept point, IIP3, of -5.2 dBm, a second-order input referred intercept, IIP2, of +34.5 dBm, and an input-referred 1 dB compression point, ICP_{1dB}, of -16 dBm. The front-end uses a differential cross-coupling to increase the LO to RF isolation and measures an isolation of 60 dB. The RF input is well protected by a shunt inductor, and according to simulations it can withstand a 3 kV HBM ESD event.

VI. Acknowledgment

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