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A 15 GHz and a 20 GHz Low Noise Amplifier in 90 nm RF-CMOS

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***Abstract* — The design and measured performance of two low-noise amplifiers at 15 GHz and 20 GHz realized in a 90 nm RF–CMOS process are presented in this work. The 15 GHz LNA achieves a power gain of 12.9 dB, a noise figure of 2.0 dB and an input referred third-order intercept point (IIP3) of –2.3 dBm. The 20 GHz GHz LNA has a power gain of 8.6 dB, a noise figure of 3.0 dB and an IIP3 of 5.6 dBm. Compared to previously reported designs, these two LNAs show lower noise figure at lower power consumption.**

***Index Terms* — Low-noise amplifier, 90 nm, LNA, noise figure, RF–CMOS.**

I. Introduction

The very rapid evolution of wireless communication and the growing demand for higher bandwidth motivates RF circuits to move towards higher frequencies. Key circuits for an RF front-end are low noise amplifiers, (LNAs), mixers and oscillators and in this article the capability of RF–CMOS for LNAs operating at microwave frequencies is demonstrated.

Although several RF–CMOS LNAs in the 20 GHz region have been published, none of them has, to the authors' knowledge, reached a 3.0 dB noise figure. However, for many applications, like microwave radio links, an LNA noise figure of 3 dB, or even lower, is required. In this paper the design and measurements of a 15 GHz, 2.0 dB noise figure, and a 20 GHz, 3.0 dB noise figure, LNA in 90 nm RF-CMOS are presented. Moreover, it is shown that excellent noise and linearity performance can be achieved even as the supply voltage is scaled down to the 1V level.

II. Technology Overview

The LNAs have been fabricated in the IMEC 90 nm RF–CMOS process on a p-type 20 Ω·cm Si substrate with three layers of metals in a Cu damascene process. High quality MIM capacitors are available in this process. The NMOS transistors can reach an f_T of 150 GHz and an f_{max} of 200 GHz. The physics-based compact model MOS Model 11 with RF extensions has been used in simulations. Inductors were realized using thin-film wafer level packaging (WLP) techniques with two layers of BCB and thick electroplated Cu deposited on top of the passivation [1]. The inductors used in the designs have Q-values above 25 at 20 GHz, which together with the high performance transistors make design of very high performance circuits at microwave frequencies possible.

III. LNA Design Methodology

The LNA circuits are realized as cascode amplifiers, Fig. 1, with inductive source degeneration, a topology often used when designing LNAs at lower frequencies. The low input impedance of the common gate stage loading the common source stage results in low voltage gain for the common source stage and thus a reduced Miller effect. This becomes of particular importance as the frequency of operation is pushed up to 20 GHz since it results in higher gain and better stability. The extra transistor will, however, result in added noise and reduced voltage headroom, making design for low voltage operation a challenge.

To be able to measure the design in a 50 Ω test environment, a capacitive impedance divider consisting of MIM capacitors C1 and C2 is implemented at the output.

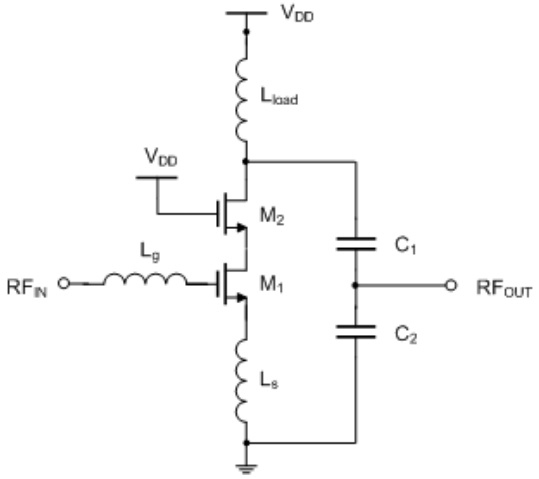

Fig. 1 . Schematic of LNA

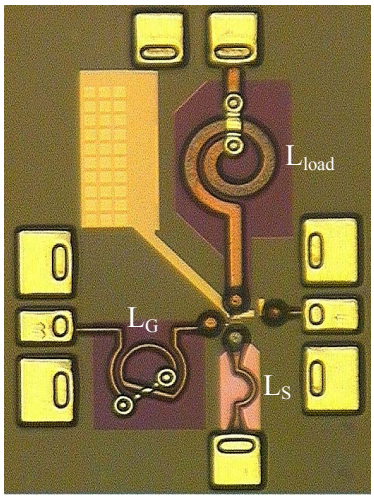

Fig. 2 . Photo of 15 GHz LNA

A. 15 GHz LNA

The 15 GHz LNA chip area is 680x1000μm^2 including bondpads, Fig. 2. As seen on the photo most of the chip area is occupied by the on-chip inductors and the decoupling capacitor in the upper left corner.

The gate width/gate length of M1 and M2 are both chosen to 80 μm/90 nm, as this was the best compromise between power consumption noise figure, and linearity. The transistors were laid out with 40 fingers, and with the gate fingers contacted at both ends. The inductors used are: 0.12 nH for L_s, 0.6 nH for L_g and 0.6 nH for L_{load}. As the values of the inductors are small, great care has been taken to include effects of interconnects on circuit performance in simulations. The value of the capacitances in the output impedance matching network is C_1=C_2=115 fF. To avoid stressing the gate oxide, the gate-drain and gate-source voltage of the transistors should not exceed 1.2 V. Simulations show that these requirements are fulfilled for supply voltages up to 2.0 V for this circuit.

B. 20 GHz LNA

The 20 GHz LNA area is 750x750μm^2 including bondpads, Fig. 3. The inductors used are: 0.12 nH for L_s, 0.6 nH for L_g and 0.2 nH for L_{load}. The value of the capacitances in the output impedance matching network are here C_1=C_2=250 fF.

IV. Experimental Results

Both circuits have been measured on-wafer.

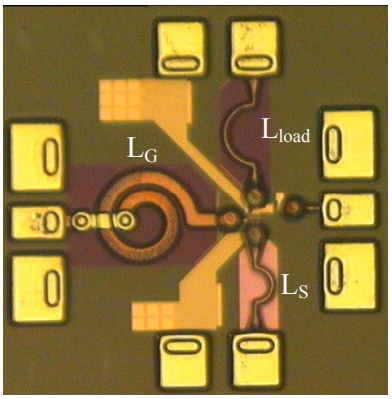

Fig. 3 . Photo of 20 GHz LNA

A. 15 GHz LNA

The performance of the 15 GHz cascode LNA has been measured at different bias points and the results are summarized in Table I. The 2.0 dB noise figure reported for V_{DD}=1.6 V and I_{DD}=12 mA is the lowest noise figure reported for a CMOS LNA at this frequency. The measured IIP3 is around -2 dBm, and is for the 15 GHz LNA quite independent on bias conditions. The noise figure and the power gain for V_{DD}=1.6 V and I_{DD}=12 mA are plotted vs. frequency in Fig. 4.

Table I. Summary of measured results for the 15 GHz LNA.

	Unit	Results for different bias conditions, fc=14.5GHz			
V_{DD}	V	1.0	1.2	1.4	1.6
I_{DD}	mA	5	8	8	12
P	mW	5	9.6	11.2	19.2
S21	dB	10.7	11.9	12.3	12.9
NF	dB	2.5	2.3	2.1	2.0
IIP3	dBm	-2.2	-2.3	-2.3	-2.3

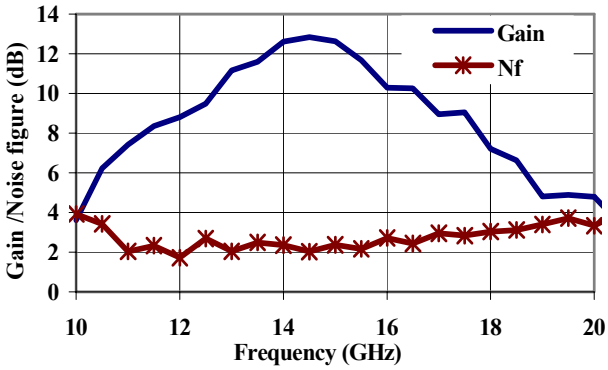

Fig. 4 . Gain and noise figure for the 15 GHz LNA at V_{DD}=1.6V and I_{DD}=12 mA

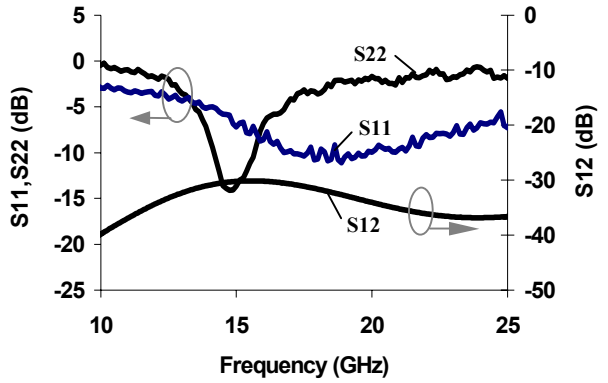

Fig. 5 . Measured S11, S22 and S12 for the 15 GHz LNA

Table II. Noise contributors 15 GHz LNA, V_{DD}=1.4 V, I_{DD}= 10 mA.

Noise source	Noise contribution
Drain current noise M1	29 %
Drain current noise M2	24 %
Substrate losses M1	9.3 %
Resistive losses in L_g	8.5 %
Substrate losses M2	8.3 %
Gate resistance M1	5.9 %

S11, S22 and S12 are shown in Fig. 5. The best input and output match does not occur at the same frequency due to a modeling problem. There is thus room for further improvements. In Table II the 6 largest sources of noise, obtained from SpectreRF simulations, are shown. The drain current noise of the two transistors is clearly the dominating noise source. The noise contribution from the input matching inductor L_g is compared to the transistor related noise quite low, partly due to the excellent Q-values achievable in this process and partly due to its small inductance value. The connection of the gates at both ends and the 40 finger structure helps to keep the gate resistance low and reduces its influence on noise to a small level.

B. 20 GHz LNA

The measured performance of the 20 GHz LNA is summarized in Table III. The 3.0 dB noise figure achieved when the LNA is biased at V_{DD}=1.6 V and I_{DD}=12 mA is the lowest noise figure reported for a CMOS LNA at this frequency. The noise figure and the power gain for V_{DD}=1.4 V and I_{DD}=10 mA are plotted vs. frequency in Fig. 6. For the 20 GHz LNA the IIP3 improves strongly with increasing V_{DD} and I_{DD}. S11, S22, and S12 are presented in Fig. 7 .

Table III. Summary of measured results for the 20.0 GHz LNA.

Parameter	Unit	Results for different bias conditions, fc= 20 GHz.			
V_{DD}	V	1.0	1.2	1.4	1.6
I_{DD}	mA	5	8	10	12
P	mW	5	9.6	14	19.2
S21	dB	6.9	8.1	8.4	8.6
NF	dB	3.6	3.2	3.1	3.0
IIP3	dBm	2.6	3.5	4.8	5.6

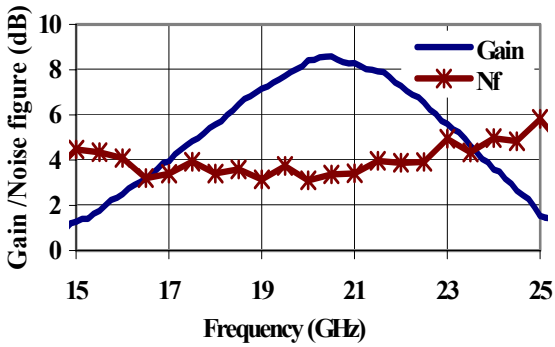

Fig. 6 . Gain and noise figure for the 20 GHz LNA at V_{DD}=1.4V and I_{DD}=10 mA

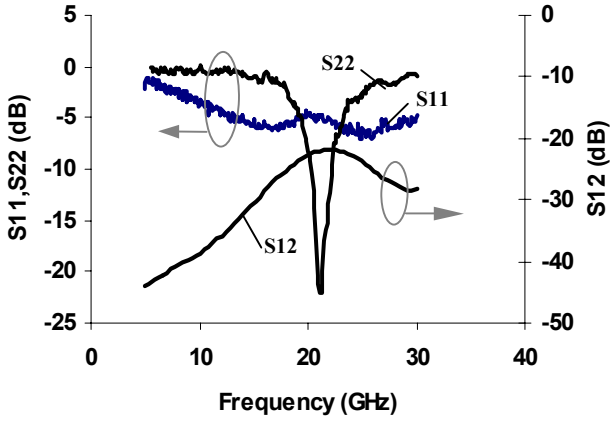

Fig. 7 . Measured S11, S22 and S12 for the 20 GHz LNA

V. Summary and Comparison with State-Of-The Art

In Table IV, the performance of the LNAs presented in this report is compared to previously published data. The 20 GHz single ended cascode LNA outperforms the published 20 GHz CMOS LNAs in terms of noise figure, linearity and low power consumption. The 15 GHz LNA has an excellent noise figure and also a high power gain taking the low power consumption into account.

Table IV. Summary of state-of-the art 15 GHz+ LNAs.

Ref.	Technology (μm)	F_C (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	P_{DC} (mW)	FOM
This work	0.09 CMOS	14.5	12.3	2.1	-2.3	1.4	11.2	20.8
This work	0.09 CMOS	14.5	10.7	2.5	-2.2	1.0	5	26.4
This work	0.09 CMOS	20	8.4	3.1	4.8	1.4	14	28.7
This work	0.09 CMOS	20	6.9	3.6	2.6	1.0	5	27.6
[2]	0.09 CMOS	20	6.4	5.8	7	1.5	10	11.3
[3]	0.09 SOI CMOS	35	11.9	3.6	- *	2.4	41	-
[4]	0.18 CMOS	24	12.86	5.6	2.04	1.8	54	5.2
[4]	0.18 CMOS	25.7	8.9	6.93	2.8	1.8	54	1.8
[5]	0.18 CMOS	22	15	6	-	1.5	24	-
[6]	0.10 SOI CMOS	23.8	10	7.3	-7.8	1.5	79	0.03
[7]	0.18 CMOS	24	13.1	3.9	-0.54	1.0	14	27.2

*Only output 1 dB compression point presented (+4dBm).

A figure-of-merit defined as [8]

$$FOM = \frac{Gain[abs] \cdot IIP3[mW] \cdot f_c[GHz] \cdot}{(NF-1)[abs] \cdot P_{DC}[mW]} \quad (1)$$

is calculated for the different designs and presented in Table IV. The performance of the 15 GHz and the 20 GHz LNAs are here truly seen to be state-of-the-art.

The two amplifiers behave quite differently when it comes to linearity. The IIP3 of the 15 GHz LNA stays more or less constant when the supply voltage and bias current is increased, while the IIP3 of the 20 GHz LNA improves considerably when the supply voltage and current is increased. This indicates that two different sources dominate the nonlinear behavior in the two designs. In the 15 GHz LNA the dominating nonlinearity is most likely the nonlinear output conductance, while it for the 20 GHz LNA is expected to be the nonlinear g_m.

VI. Conclusion

In this article it is shown that RF–CMOS has become a possible alternative for LNA design also at microwave frequencies. Further on the results demonstrates that it is possible to design high performance LNAs based on cascode topology at microwave frequencies even for supply voltages down to 1 V. The 2.0 dB noise figure achieved for the 15 GHz LNA and the 3.0 dB noise figure of the 20 GHz LNA are certainly state-of-the-art performance. Compared to previously reported designs, these two LNAs show lower noise figures at lower power consumptions. The excellent performance is a result of the high performance of the 90 nm RF-CMOS process and the high Q-values of the inductors achieved employing the WLP technology.

Acknowledgement

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References

[1] G. J. Carchon, W. De Raedt; E. Beyne, "Wafer-level packaging technology for high-Q on-chip inductors and transmission lines", *IEEE Transactions on Microwave Theory and Techniques*, Volume 52, Issue 4, April 2004, pp. 1244 – 1251.

[2] M. A. Masud, H. Zirath, M. Ferndahl and H.–O. Vickes, "90 nm CMOS MMIC amplifier," *IEEE RFIC Symposium*, 2004, pp. 201-204.

[3] F. Ellinger, "26-42 SOI CMOS Low Noise Amplifier," IEEE Journal of Solid State Circuits, vol. 39, no.3, March 2004, pp. 522-528.

[4] K.–W. Yu and M. F. Chang, "CMOS K-Band LNAs design counting both interconnect transmission lines and RF pad parasitics", *IEEE RFIC Symposium*, pp 101-104, 2004.

[5] X. Guan and A. Hajimiri, "A 24-GHz CMOS Front-End," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, February 2004, pp. 368-373.

[6] B. A. Floyd et al., "A 23.8-GHz SOI CMOS tuned amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 50, September 2002, pp. 2193-2195.

[7] S.–C. Shin et al., "A 24-GHz 3.9-dB NF low-noise amplifier using 0.18 μm CMOS technology", *IEEE Microwave and Wireless Components Letter*, vol. 15, no. 7, July 2005, pp. 448-450.

[8] R. Brederlow et al., "A mixed signal design roadmap", *IEEE Design & Test of Computers*, Vol. 18, No. 6, November-December 2001 pp. 34–36.