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Low-Frequency Noise in Vertical InAs Nanowire FETs

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***Abstract*— This paper presents DC characteristics and low-frequency noise (LFN) measurements on single vertical InAs nanowire MOSFETs with 35 nm gate length and HfO_2 high-κ dielectric. The average normalized transconductance for three devices is 0.16 S/mm with a subthreshold slope of 130 mV/decade. At 10 Hz the normalized noise power S_I/I_d^2 measures $7.3x10^{-7}$ Hz^{-1}. Moreover, the material dependent Hooge's parameter at room-temperature is estimated to $4.2x10^{-3}$.**

***Index Terms*— FET, flicker noise, InAs, nanowire (NW).**

I. Introduction

TO increase the drive currents in scaled MOSFETs, alternatives to the Si technology are considered. A vertical MOSFET based on InAs nanowires (NWs) is one example of a promising extension, or add-on, to the Si CMOS platform. InAs has a high electron mobility, a high saturation velocity, and low contact resistance [1]. The nanowire geometry also offers electrostatic advantages using a wrap-around gate, providing better control of the channel potential. Good DC performance of vertical InAs NW transistors based on arrays of nanowires with 50 nm gate length has been demonstrated [2], with g_m = 0.5 S/mm and a subthreshold slope of 90 mV/decade. We have recently also investigated the radio frequency (RF) performance of similar InAs nanowire FETs [3]. Here we present data of the DC and *1/f* characteristic for FETs based on individual vertical InAs NWs. Up to now, several papers of FETs based on individual lateral NWs have been published [4][5], but only a few in the vertical geometry.

In recent years, much effort has been put into characterization of low-frequency noise (LFN) of MOSFETs as the noise spectral density tends to increase linearly with the scaling factor [6], making it a major concern for analog and RF applications. Ultra-scaled devices not only suffer from high noise levels, but also large disparity between devices processed in parallel [6][7]. In MOS structures, flicker noise, also known as *1/f*-noise, has been shown to dominate the noise at low frequencies. Flicker noise stems from trapping and detrapping events related to the channel, the oxide and the interface. This paper presents, to the best of our knowledge, the first 1/f noise characterization of a III-V MOSFET including high-κ integration in a non-planar geometry. It is demonstrated that similar noise performance can be achieved as in advanced Si device architectures. Compared to previous LFN studies of InAs NW FETs [8], our study incorporate wires with high-κ dielectric. The study also differs as the wires have shorter gate length and include characterization of the subthreshold regime.

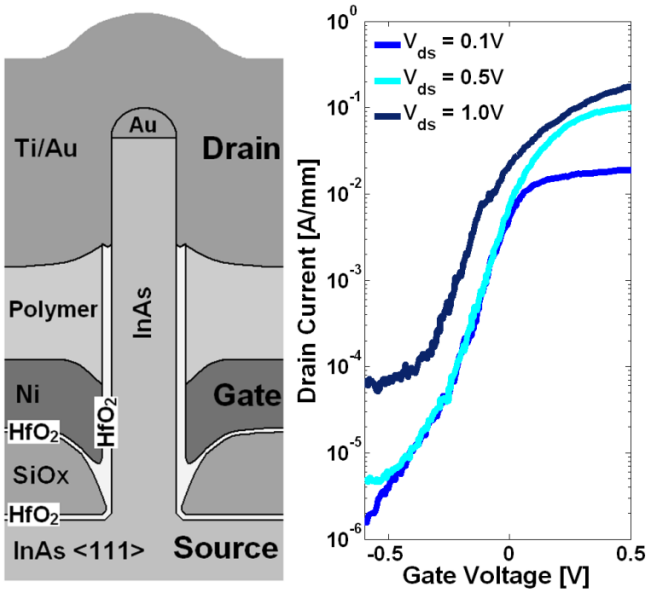

Fig. 1. (a) Schematic cross-section of a NW FET. (b) Device transfer characteristics of an individual NW FET (40 nm diameter, 35 nm gate length) at V_{ds} = 0.1 V, 0.5 V, and 1.0 V.

II. Device Fabrication

The NW FETs are fabricated from epitaxially grown InAs nanowires with a diameter of 40 nm, grown on an <111>-B InAs substrate [2, 9]. The wires are Sn-doped with a molar fraction of $3.49x10^{-8}$. The source to gate spacer layer consists of evaporated SiO_x. During evaporation, the sample is rotated and the wires are slightly tilted to the material source to avoid shadowing of the base. The buildup of small quantitys of porous SiO_x on the side facets of the wires is removed in a following wet-etch step, leaving the profile shown in the

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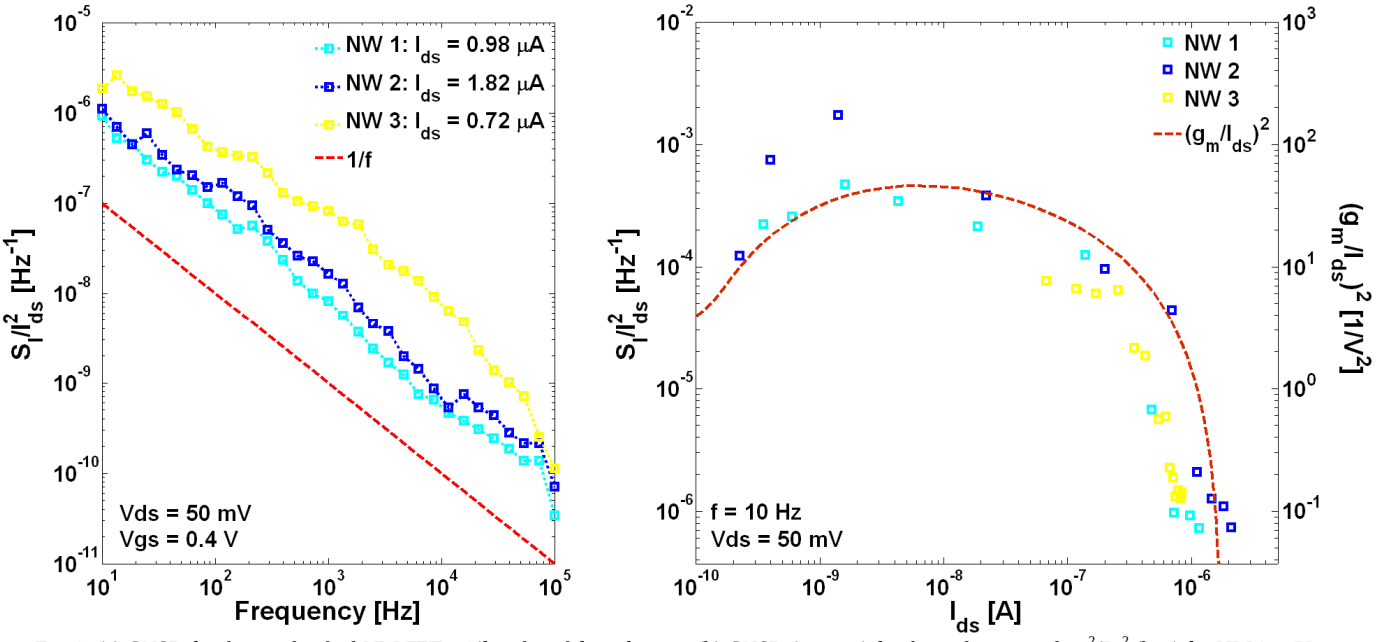

Fig. 2. (a) CNSD for three individual NW FETs. *1/f* is plotted for reference. (b) CNSD (squares) for three devices and g_m^2/I_{ds}^2 (line) for NW 2 at V_{ds} = 50 mV, plotted versus the drain current for f = 10 Hz.

schematic cross-section of the device in Figure 1a. A dielectric film (HfO_2) is deposited both before and after the SiO_x, utilizing atomic layer deposition, for total a thickness of 7 nm. The Ni gate is evaporated in a similar fashion as the SiO_2 and the gate length is set by the thickness of the evaporated film. When spin-coating the sample to fabricate the gate to drain separation layer, the film gets thicker around the wires. The final thickness of the polymer is set by a following dry-etch procedure with a typical variation in the range of 100-200 nm, making the structure more or less asymmetrical. We here present data for a gate length of 35 nm.

III. Measurements

DC characteristics for one device is shown in Figure 1b. The maximum on-current at V_{ds} = 0.5 V reaches 0.1 A/mm (where the width is set as the NW circumference) for V_g = 0.5 V. For three different individual NW FETs, values for the threshold voltage, V_T, was determined to be between -0.1 and 0.0 V for V_{ds} = 0.5 V. At the same bias, the subthreshold slope, averaged over two decades, are 149, 119, and 121 mV/decade. The maximum transconductance for each wire was 157, 257, and 67 mS/mm, respectively.

The LFN measurement setup consisted of a Stanford SR830 lock-in amplifier measuring the noise current spectrum from the source terminal of the NW FET. To increase the sensitivity, the source current was pre-amplified through a Stanford SR570 low noise amplifier (LNA). The measurements were performed in the range of 10 Hz to 100 kHz at room temperature. The drain-source voltage was set to 50 mV in the presented data, but we also conducted measurements with various V_{ds}, however without observing any significant differences.

IV. Results and Discussion

As compared to previously published data [2, 9], we note a larger subthreshold slope in these devices, 120 mV/decade as compared to 80 mV/decade. This can mainly be attributed to insufficient scaling of the wire diameter for this gate length, but also a high D_{it}. The threshold shift seen at high bias voltage is caused by a combination of impact ionization and band to band tunneling due to the narrow bandwidth of InAs, and band bending related to the comparably wide wire diameter [10]. While there is room for optimization of the structure, this study is one of the first on the properties of high-κ on non-planar III/V structures [11].

LFN was measured for single NW FETs and the normalized current noise spectral density (CNSD), S_I/I_{ds}^2, for three different FETs is shown in Figure 2a at V_{gs} = 0.4 V. We note a $1/f^{\gamma}$ dependence with the frequency exponent γ being equal to 1.05, 0.99, and 1.03 for NW 1, NW 2, and NW 3, respectively. The exponent being close to unity indicates an even distribution of slow and fast traps [12]. The *1/f* behavior was unchanged for V_{gs} smaller than 0.4 V, even in the subthreshold region (V_{gs} = -0.2V), with γ kept close to unity. This indicates that several traps are involved in the noise process. We also note that the noise level uniformity is fairly good with a variation, averaged over frequency, within a factor of 5. Other studies on advanced structures with comparable gate length, though including more measured devices, show up to five orders of magnitude in variation [7]. As a reference, we also measured the LFN for devices with varying number of nanowires (7-19), where we observed the CNSD level to decrease slightly as the number of wires was increased.

In Figure 2b, CNSD for NW 1 and 2 is plotted versus the drain current at a constant frequency of 10 Hz. It can be seen that the CNSD has strong dependence on the square of the normalized transconductance, g_m^2/I_{ds}^2, which is in line with the

number fluctuation theory, pointing towards domination of trapping/detrapping events at the InAs/HfO_2 interface [12]. The CNSD reaches down to $7.3x10^{-7}$ Hz^{-1} at a drain current of 1.2 µA. As a comparison, a study of LFN in Si NWs, with a 55 nm gate length and SiO_2 gate oxide, show a normalized CNSD at 10 Hz (above threshold and at roughly 6 µA) in the order of $1x10^{-7}$ Hz^{-1} [7]. A more recent study of similar Si NWs show values of about $5x10^{-10}$ Hz^{-1} for L_g = 350 nm at 10 Hz and 1 µA [13]. From a LFN temperature study of lateral InAs NWs with SiO_2 gate oxide (back-gated) and 2 µm gate length, we extrapolated the minimum normalized CNSD at 10 Hz (data taken at 250 K), to be about $1x10^{-7}$ Hz^{-1} [8]. Another study of an AlSb/InAs HEMT show, for L_g = 100 nm, by us extrapolated value at 10 Hz, a minimum of $3x10^{-10}$ Hz^{-1} [14]. While our device is not matching the planar heterostrucutre FET in noise level, our InAs NW MOSFETs have similar noise level as advanced Si transistors with comparable gate length or long-gated InAs NW FETs. For optimized and integrated devices, each transistor will likely consist of several parallel wires to ensure sufficient drive current, and a similar noise-behavior in a lateral and a vertical geometry may be expected.

Neither number nor mobility fluctuations perfectly describe the noise over the entire bias range [12]. Mobility fluctuations or correlated mobility-number fluctuations may however be considered at high gate overdrive voltages. Using the measured data above threshold, Hooge's prarameter, α_H, can be determined. Hooge's parameter depends on material and crystal quality and is a good measure to evaluate the properties of advanced structures and exotic materials [*6*]. The parameter is found from Eq. (1)-(3).

$$S_I/I_{ds}^{\ 2} = \alpha_H/(N * f^{\gamma}) \quad (1)$$

$$N = |V_{gs} - V_T| * C_g L_g / e \quad (2)$$

$$C_g = 2\pi\varepsilon_r\varepsilon_0/\ln((r + t_{ox})/r) \quad (3)$$

Here, N is the total number of charge carriers in the channel, C_g is the gate capacitance per unit length, L_g is the gate length, e is the electronic charge, r is the NW radius, t_{ox} is the gate oxide thickness, ε_0 is the permittivity of vacuum, and ε_r is the relative permittivity of HfO_2. Using (1)-(3), the average for device 1 and 2 in Figure 2b, (for V_{gs} = 0.2 and 0.4 V at 10 Hz) the Hooge's parameter is determined to $4.2x10^{-3}$. This can be compared with the minimum obtained room temperature value for the study of a lateral InAs NW FET device [8], corresponding to $8.4x10^{-3}$. This indicates that the addition of a high-κ oxide on an InAs surface does not seriously degrade the LFN performance

V. Conclusion

We report DC characteristics and low frequency noise of vertical InAs NW MOSFETs with HfO2 high-κ oxide based on individual nanowires. It can be determined that the *1/f*-noise at low current levels is caused by number fluctuations due to trapping and detrapping events at the gate oxide interface. The exponent of the *1/f*-curve being close to unity suggests an even distribution between slow and fast traps. There is also a relatively small deviation between samples. Comparing our values to other studies of advanced structures and/or materials, the noise level presented is in the same order. Evaluating the Hooge's parameter, which accounts for the quality in the channel material and gate length, we deduce a value of $4.2x10^{-3}$.

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