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Electrical Characterization of Integrated InAs Nano-Structures

Astromskas, Gvidas

2010

Link to publication

Citation for published version (APA):
Astromskas, G. (2010). *Electrical Characterization of Integrated InAs Nano-Structures*. [Doctoral Thesis (compilation), Solid State Physics]. Lund University (Media-Tryck).

Total number of authors:
1

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PO Box 117
221 00 Lund
+46 46-222 00 00

Thesis for the Degree of Doctor of Philosophy in Engineering

Electrical characterization of Integrated InAs nano-structures

Gvidas Astromskas

Lunds universitet
Lunds Tekniska Högskola

Division of Solid State Physics
LTH

2010

Organization
LUND UNIVERSITY

Deparment of Solid State Physics
Division of Solid State Physics
Box 118
S-221 00 Lund
Sweden

Document name
DOCTORAL DISSERTATION

Date of issue November 4, 2010

Sponsoring organization

Author(s)
Gvidas Astromskas

Title and subtitle

Electrical characterization of Integrated InAs nano-structures

Abstract

This thesis analyzes the electrical properties of InAs nano-structures, that are integrated into different materials and geometries. The thesis describes integration related issues of InAs, the epitaxial synthesis of the InAs nano-structures and summarizes experimental techniques for analysis of electrical properties of the integrated structures. InAs thin films, nanowires and membranes are investigated to determine their electrical quality.

The thin films (> 300 nm thick) are integrated onto GaAs substrates using overgrowth over the tungsten patterns. Such integration method allows varying the area of the surface pinning region within the material to measure the extent of this region in InAs. A carrier saturation is observed when the tungsten density is increased which allows determining the effective length of the surface pinning region to be under 400 nm.

InAs nanowire capacitors are investigated to measure their doping density and doping profile. The capacitance of the nanowire capacitors exhibits non parabolic band behavior and a full depletion, in contrast to conventional MOS capacitors. The threshold voltage of the fully depleted nanowires is extracted to determine doping density and dopant distribution profile within a nanowire. It is shown that dopants incorporate preferentially at the nanowire surface and the surface doping concentration is higher than in the nanowire bulk. Also, capacitance transients are analyzed to show the presence of traps in the oxide.

InAs metamorphic films are integrated onto GaSb buffer layer to evaluate the relation between the quality of the buffer layer and the InAs. It is observed, that metamorphic InAs membranes (23 nm thick) are highly resistive, while thicker membranes (90 nm thick) can be measured by Hall Effect measurements. The mobility of 90 nm membranes is found be 2700 cm2/Vs, which indicates a loss of the metamorphic lattice. It is shown that the resistivity of thin membranes is highly sensitive to surface treatment.

Key words: InAs, Fermi level pinning, GaSb, overgrowth, Hall mobility, nanowire capacitance, DLTS, threshold voltage, epitaxial growth

Classification system and/or index termes (if any):

Supplementary bibliographical information:

Language
English

ISSN and key title:

ISBN
978-91-7473-062-3

Recipient's notes

Number of pages

Price

Security classification

Distribution by (name and address)

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Thesis for the Degree of Doctor of Philosophy in Engineering

Electrical characterization of integrated InAs nano-structures

Gvidas Astromskas

Lunds universitet
Lunds Tekniska Högskola

Division of Solid State Physics
LTH, Lund University
Sweden
2010

Faculty Opponent: Professor Carl-Mikael Zetterling

Academic dissertation which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Tuesday, the 14th of December 2010, at 10.15 in lecture hall B, at the Department of Physics, Sölvegatan 14A, Lund.

Electrical characterization of integrated InAs nano-structures

Division of Solid State Physics
Faculty of Engineering
Lund University
PO Box 118
SE-221 00 Lund
Sweden

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List of Publications

This thesis is based on the following peer-reviewed publications and submitted manuscripts, which are appended at the end of this thesis. The author′s contribution is described below each article.

Paper I: **Electrical characterization of thin InAs films grown on patterned W/GaAs substrates**
Gvidas Astromskas, L. Reine Wallenberg, and Lars-Erik Wernersson
Journal of Vacuum Science and Technology B **27** (2009) 2222

I made the W patterned samples, performed epitaxial overgrowth, etched the mesa structure to form Hall devices, measured the Hall effect and wrote the article

Paper II: **InAs nanowire metal-oxide-semiconductor capacitors**
Stefano Roddaro, Kristian Nilsson, Gvidas Astromskas, Lars Samuelson, Lars-Erik Wernersson, Olov Karlström, Andreas Wacker
Applied Physics Letters **92** (2008) 253509

I arranged a capacitance measurement setup to detect signal from nanowire capacitors and actively participated in discussion.

Paper III: **Doping Incorporation in InAs Nanowires characterized by Capacitance Measurements**
Gvidas Astromskas, Kristian Storm , Olov Karlström , Philippe Caroff , Magnus T. Borgstrom , Lars-Erik Wernersson
Journal of Applied Physics **108** (2010) 054306

I arranged a low temperature CV setup, performed CV measurements in a wide temperature range, analyzed the data and wrote the article.

Paper IV: **Temperature and frequency characterization of InAs Nanowire and HfO2 interface using Capacitance Voltage method**
Gvidas Astromskas, Kristian Storm, Philippe Caroff, Magnus Borgström, Erik Lind, Lars-Erik Wernersson
Microelectronic Engineering accepted for publication

I measured the nanowire CV characteristics at a wide frequency range, analyzed the data and I wrote the article.

Paper V: **Transient studies in InAs/HfO2 Nanowire Capacitors**
Gvidas Astromskas, Kristian Storm, Lars-Erik Wernersson
submitted to Applied Physics Letters

I measured the capacitance transients of nanowire capacitors, performed deep level transient spectroscopy measurements, analyzed the data and wrote the draft of the article.

Paper VI: **Analyzing the capacitance-voltage measurements of vertical wrapped-gated nanowires**
Olov Karlström, Andreas Wacker, Kristian Nilsson, Gvidas Astromskas, Stefano Roddaro, Lars Samuelson, Lars-Erik Wernersson
Nanotechnology **19** (2008) 435201

I arranged the setup for nanowire capacitance measurements and participated actively in the discussion.

Paper VII: **MOVPE-grown InAs/GaSb layers and membranes on GaAs**
Gvidas Astromskas, B. Mattias Borg, and Lars-Erik Wernersson
manuscript, to be submitted

I performed AFM and Hall measurements of samples, analyzed the electrical data and wrote the article.

Related publications not included in this thesis

1. ***20 GHz wavelet generator using a gated tunnel diode*** M. Egard, M. Arlelid, E. Lind, G. Astromskas, L.-E. Wernersson,
   IEEE Microwave and Wireless Components Letters **19** (2009) 386.

2. ***Applications of SU-8 in the development of a Single Ion Hit Facility*** N. Arteaga-Marrero, G. Astromskas, M.G. Olsson, M. Elfman, P. Kristiansson, E.J.C. Nilsson, C. Nilsson, J. Pallon
   Nuclear Instruments and Methods in Physics Research B **267** (2009) 2117.

3. ***Temperature dependence of GaSb overgrowth of tungsten on GaSb (001) substrates using MOVPE*** G. Astromskas, M. Jeppsson, P. Caroff, L.-E. Wernersson
   IEEE 20th International Conference On Indium Phosphide And Related Materials (2008) 354

4. ***Heterogeneous integration of InAs on W/GaAs by MOVPE*** G. Astromskas, L. Wernersson
   Journal of Physics: Conference Series, **100** (2008) 042043

Abbreviations

AlSb	Aluminum Antimonide
AsH_3	Arsine
CV	Capacitance Voltage
CVD	Chemical Vapor Deposition
DLTS	Deep Level Transient Spectroscopy
GaAs	Gallium Arsenide
GaSb	Gallium Antimonide
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
InSb	Indium Antimonide
MIS	Metal Insulator Semiconductor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
MOVPE	Metal Organic Vapor Phase Epitaxy
NID	Not Intentionally Doped
HEMT	High Electron Mobility Transistor
TBAs	Tertiary Butyl Arsine
TEGa	Triethyl Gallium
TEM	Transmission Electron Microscope
TMGa	Trimethyl Gallium
TMI	Trimethyl Indium
TMSb	Trimethyl Antimony

Acknowledgments

I would like to express my sincere gratitude to my supervisor Lars-Erik Wernersson, who gave me the opportunity to carry out this work under his guidance. Also, I would like to thank Erik Lind for his continuous support through almost every day of my research. This thesis has come to light only with the help and contribution from my research colleagues. I especially want to thank Mattias Borg for his suggestion to print the process travelers. This made the difference between trying and experimenting. Phillipe Caroff is a key person for to discuss about epitaxy, research, physics, human relations and other important elements of a PhD student's life. Also, Mikael Edgard must be acknowledged, as his hard work makes splendid high speed devices. I am also in debt to the department of Solid State Physics for providing me with an excellent work place, an outstanding laboratory equipment and a friendly environment to spend the working days. I want to mention Ivan, Mariusz, Lena, Mona and Sören for providing the help when I needed it.

I want to thank my family for their dedication, especially Eimantas for being the driving force to pursue the studies.

Also, my life in Lund would be impossible without ever helping friends. I am very grateful to spend time with Alexander, Audrius, Henrik, Justas, Oleg, Nataliya, Natalia, Ramūnas, Sveta, Valeria and Vaida.

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1

Introduction

We live in a world, made of many different materials. They have particular mechanical, optical, electrical and thermal properties, which we can exploit, modify, suppress or enhance to suit our purpose. A type of materials, called semiconductors allow controlling their electrical, optical, magnetic and thermal properties only with the effect of electrical power, not larger then the provided by an AA battery. This makes them very convenient for building electronic components, that later are much used in our everyday items, like computers, phones, washing machines, cars and other electrical appliances. And all this is thanks to our understanding of electrical properties of semiconductors.

This thesis is focused on the investigation of the electrical properties of a semiconductor material, called Indium Arsenide (InAs). InAs has a narrow band gap of $0.354eV$ and a high mobility of 18000 cm^2/Vs at room temperature [1]. The mobility is eighteen times larger than the mobility of Silicon, of which the vast majority of electronic components are made.

The mobility quantifies how well the electrons respond to the applied electric potential. The higher value indicates that the control of the electron current is easier in InAs based devices as compared to Silicon. This is the basic reason why high sensitivity and high frequency performance is expected from InAs devices.

InAs is currently used for making very sensitive magnetic field sensors [2]. But it can have other applications, for example the terrestrial thermal imaging and high speed electronic devices [3]. Actually, a 640 GHz operation of low power InAs channel HEMT is already reported [4].

In order to make InAs based electronic devices, we have to consider their size. Large devices do not mean better performance, as small structures take less space, are cheaper, consume less power and can even operate faster (for example, smaller devices have lower parasitic capacitances and resistances). Of course, small size means less volume, therefore less current and less power. Low power is actually desirable, because devices consume less energy and produce less heat, therefore being more efficient. The current loss can be compensated by combining more nano devices together, or making the devices more sensitive. The high mobility electrons can respond well even to weaker electric fields, therefore higher sensitivity is expected from nano-sized InAs structures. Also, the narrow band gap of InAs allows electron control with less power. This is why InAs is an interesting material at small dimensions.

Of course, sensitive devices produce weak signals; which then have to be amplified

to the levels, used by other electronic components. This requires integrating nano-sized structures with larger devices, that are more powerful. Therefore the integration is a way to get the best of two worlds: to combine a conventional technology with its advanced measurement and processing techniques with sensitive nano devices. However, when nanostructures are integrated onto desired substrates, it is no longer certain that they can keep their high sensitivity, as integration can reduce mobility. Lower quality means lower mobility therefore it is important to identify the sources, that cause quality loss during integration. For epitaxial nano-structures, like InAs, the typical quality loss is related to the defect formation during epitaxial growth. The bulk structures also suffer from defect formation, but there it is understood how defects affect the quality. Nano structures are more sensitive to defects, but it is not clear how much the defects affect their properties. On the other hand, nano-structures can be used as a tool to identify the most important defects and to better understand their formation.

The drawback of nano-structures is their large surface to volume ratio. The surface is expected to affect the properties of nano structures, including the mobility. In the InAs case, the surface is known to exhibit a surface phenomena, called Fermi level pinning [5]. At the surface the Fermi level is fixed over the conduction band minimum (E_C) as opposed to the more common case where the Fermi level is under the conduction band and forms a Schottky contact instead. The pinning creates a conductive surface layer, which has to be evaluated in nano-sized InAs structures.

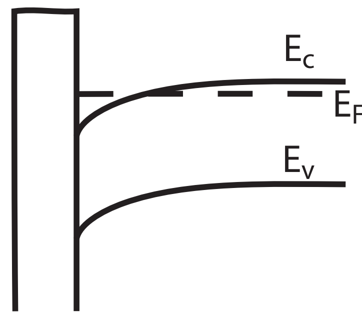

Figure 1.1: Band diagram illustrating the Fermi level pinning at the InAs surface

The pinning is illustrated in Figure 1.1. Such band configuration increases the sheet electron concentration at the InAs surface to as high as ($4 \cdot 10^{12}$ cm^{-2}) [6] allowing creating ohmic contacts to InAs with almost any metal. However, the surface mobility is estimated to be 2400 cm^2/Vs [7] and is much lower than in the bulk. The low mobility is attributed to scattering by the surface states, that create the pinning effect [8]. Therefore the low mobility indicates that there can be an upper limit to the scaling of InAs when the surface scattering starts to dominate in nano sized InAs structures. The effect might be detrimental to device performance, although currently it is considered to be advantageous

as it allows easily making good ohmic contacts to InAs structures [9]. Also, typical electrical characterization methods are developed for the bulk materials, where surface has negligible influence. Therefore they need to be reevaluated to include the surface effects.

The text of this thesis is organized as follows:

Chapter 2 describes in more detail the integration methods for InAs nano-structures.

Chapter 3 provides information about epitaxial growth, which is the method of choice for creating and integrating InAs structures.

Chapter 4 describes the techniques for measuring the electrical characteristics of nano-sized InAs structures.

Chapter 5 provides a background to the articles II-IV that deal with CV measurements. The key results are presented and the doping level determination method in nanowires is explained.

Chapter 6 provides a background for paper I, where overgrown InAs is investigated to determine the surface influence onto mobility. The overgrowth process is briefly explained, together with the method of testing the surface layer mobility.

Chapter 7 introduces the InAs grown on buffer layers to determine how defects influence the quality of InAs.

2

Integration of InAs

High quality InAs is easily grown in conventional epitaxy reactors, especially when grown on InAs substrates. The growth on native substrate is virtually defect free, ensuring high mobility. However, the InAs substrate is highly conductive, which acts as unwanted leakage path, making the substrate unsuitable for electronic components. To remove the substrate leakage, InAs has to integrated onto a wide gap material, as they have lower intrinsic carrier concentration. A suitable candidate is AlSb, which has a band gap of 1.58 eV, more than four times larger than that of the InAs. It also has a lattice constant of 6.13Å, therefore this substrate is nearly lattice matched to the 6.058Å InAs lattice. However poor substrate quality and strong reactivity to atmospheric oxygen makes it currently unavailable for device applications [10]. GaSb is also nearly lattice matched to InAs, but exhibits a narrow band gap of 0.72 eV, leading to high substrate conductance as well. Therefore InAs has to be integrated to lattice mismatched GaAs or InP substrates but at the cost of dislocation generation.

In order to integrate the material onto the lattice mismatched substrate, a few integration methods are available. The first option is growing a thick buffer layer, so that the generated dislocations can form loops and stop propagating [11]. The schematic of the integration using a buffer layer is shown in Figure 2.1a. The substrate is first covered with thick (typically $> 1\mu m$ thick) layer of the buffer material and then finished by a thin layer on top. Commonly used buffer materials to integrate InAs are: InAs itself, GaSb, AlSb, InPSb or InGaAs. The advantage of the buffer layer technology is that it makes planar layers and therefore it is compatible with standard processing and measurement techniques.

2.1 Integration options

A typical buffer layer is characterized by the curve shown in Figure 2.1b, where the dislocation density decreases with increasing buffer thickness. Dislocations form at the substrate/buffer interface and then propagate through the buffer layer to the top layer. However, as dislocations propagate through the layer, they are likely to form dislocation loops, that stop their propagation [12]. Particularly useful are (100) substrates, where threading dislocations tend to propagate at 60° angle, making it easier to form a loop. In some cases, it is even possible to achieve 90° threading dislocations, that slide parallel

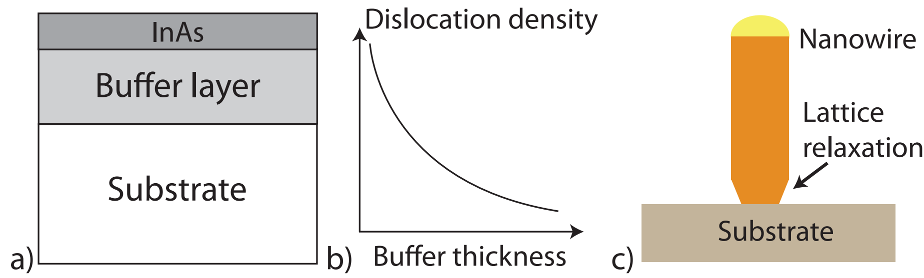

Figure 2.1: a) Schematic of the integration using buffer layer b) Schematic of the dislocation density vs. the buffer layer thickness. c) Schematic of the mismatch relaxation by nanowire diameter expansion

to the buffer/surface [13]. However, as a consequence of propagation, even thick buffer layers will not be defect free. The dislocation propagation can also be reduced by using step graded buffers, where the interface between heterostructures with different lattice constants tend to change the dislocation propagation direction [14]. To stop the propagation, the overgrown layers can be used, where the mask blocks the dislocation propagation path [15].

Another option for integrating nano-sized InAs structures is a nanowire growth. InAs nanowires already are grown on GaAs [16], InP [17] and Si [18] substrates. The small diameter of the nanowire allows lateral relaxation of the lattice mismatch, as shown in Figure 2.1c. The relaxation prevents the formation of threading dislocations [19], although stacking faults and twin boundaries can still be present under non optimized growth conditions [20]. It is important to mention that a typical InAs nanowire contains both wurtzite and zinc blende crystal structures [21], while the bulk InAs is found only as zinc-blende. The different crystal structure leads to formation of stacking faults and twin, which affect the quality of the nanowires. Also, the wurtzite crystal structure has a band gap of 0.54 eV instead of the 0.354 eV band gap of zinc blende InAs.

The vertical geometry of nanowires also opens a few new design possibilities. For example a better channel control can be achieved when the wrap around gate are used [22]. This can even allow the use of a higher mobility channel present in the undoped nanowires, without sacrificing the device current by the lack of doping [23].

2.2 Mobility of integrated InAs

It is interesting to compare which integration method gives better quality material. Also, whether the dislocation scattering is stronger than the surface scattering.

Typical studies that investigate the influence of dislocation density on the quality of integrated InAs, vary the thickness of the buffer layers and then measure the mobility.

When thick buffers layers are used ($> 4\ \mu m$), even a 60 nm thin InAs layer have the bulk mobility, if the surface states are suppressed by a GaSb cap [24]. However the epitaxial growth of thick layers is more expensive than the bulk growth, therefore thinner layers are desired, though they contain more dislocations. Also, the surface to volume ratio becomes larger, thus the pinning starts affecting the measurements. Also, only few measurements of the surface mobility are done [25].

In one of the measurements, two thin (20 nm) InAs membranes with different dislocation densities are measured [26]. The thin layers ensures a strong influence of surface to the mobility. As determined on low dislocation density membrane, mobility of the thin membrane exceeds 7000 cm^2/Vs [26,27], while for membrane with higher dislocation density the mobility lowers to 3000 cm^2/Vs. This shows that the dominant electron scatterer in the buffer layer based integration process remains the dislocation density. Therefore a desired outcome of the integration process is the reduction of dislocation density in InAs thin films.

It is interesting to compare this value with nanowire integrated InAs structures. Mobility of nanowires cannot be obtained by conventional Hall measurements, instead the field mobility is extracted from nanowire transistor measurements using a MIS model. The values obtained by this method reach 11 500 cm^2/Vs at a room temperature [28] for InAs nanowire with an InP shell, which suppresses the surface pining. However, the nanowire mobility is diameter dependent and decreases to 2000 cm^2/Vs for a 20 nm InAs nanowire [29]. This value can be increased to 5200 cm^2/Vs if the defect density is reduced [30]. These results indicate that the nanowire growth has to be optimized to reduce the stacking fault density. Also a careful surface control is required to obtain good quality devices.

The Hall and field mobilities are not equivalent, as the Hall mobility represents the bulk carrier scattering, while the field mobility is also affected by the surface scattering. The relation between the two is expressed as $\mu_{Hall} = r_h \cdot \mu_{field}$, where r_H is called a Hall scattering factor. The value of r_H in InAs varies between 1 and 1.3 [31, 32]. If the r_H factor is unaccounted (as is often done), then the field mobility can underestimate the Hall mobility for up to 30%.

3

Epitaxial growth

This thesis analyzes InAs nano-structures that are integrated epitaxially by three different methods: buffer layer, overgrowth and nanowire growth. Therefore this chapter presents the basics of epitaxial growth and explains the properties of each integration method. The epitaxial growth was performed using a Metal Organic Vapor Phase Epitaxy reactor, which is an industry standard growth technology. Therefore, the last section provides a short introduction to MOVPE growth and reactor related growth parameters.

3.1 Basics of epitaxy

Epitaxy is a process to create high quality crystalline structures of various materials. The term epitaxy comes from the Greek roots epi, meaning "above", and taxis, meaning "in ordered manner", so it can be translated "to arrange upon". During the epitaxial growth, the atoms order themselves onto the existing surface to create a new mono crystalline layer. The ordering occurs by diffusion, therefore the layer growth is slow. A typical growth rate 1 $\mu m/h$, which corresponds to 2.4 mm/day. On the other hand, the slow growth makes it easy to control the size of nano-structures.

Three factors are required for epitaxial growth:

1. a substrate,

2. a source material,

3. the ability to control the growth process.

The substrate is a flat piece of a single-crystal with the periodic order of atoms, which acts as a very precise template for the atoms. The source material forms strong intra molecular bonds (for example, covalent bonds) to the substrate atoms, causing the growing layer to follow the order of the substrate atoms and make a new crystalline layer. To achieve this and control the process, a growth reactor is used, where the supply of source material, the substrate temperature and the reactor pressure are controlled.

3.2 Heteroepitaxial growth

Heteroepitaxy is a type of epitaxial growth where the substrate and the grown layer are of different compounds, for example growth of InAs on GaAs. In order to achieve high quality heteroepitaxial growth, three major factors have to be considered:

1. lattice constant mismatch,
2. crystallographic orientation of the substrate,
3. interface type.

The lattice mismatch is the most common cause for defect formation in the heteroepitaxial structures. In order to maintain epitaxial relation, the growing layer aligns according to the lattice of the substrate. However, this creates an electrostatic force, as atoms are away from their equilibrium bond positions for the lattice mismatched layer. This force leads to the buildup of the strain energy in the growing layer. While the strain energy is under the energy threshold for the dislocation formation, the growing layer has the same parallel lattice constant as the substrate and is called metamorphic. If too much strain is present, the atoms cannot follow the order of the substrate and instead redistribute themselves to minimize the total energy, forming a dislocation. This process is a type of plastic relaxation and is the main mechanism for defect formation during heteroepitaxial growth. As the growth proceeds, the new layer follows the order of the deformed layer, therefore the dislocation propagates throughout the growing structure.

The maximum thickness for a stable metamorphic layer is called the critical thickness. The critical thickness for the InAs grown on GaSb is found to be of up to 3000 Å [33]. The mismatch between the lattices of InAs and GaSb is 0.65%, which should correspond to the critical thickness of 200 Å [34], according to the Matthews-Blakeslee model [35]. A better fit to experimental data is obtained if other dislocation generation models are used, for example People-Beans [36] which account for the screw dislocations [37].

The lattice mismatch also can be relaxed by the change of the growth mode. When misfits are larger than 2%, in most cases the epitaxial growth mode changes from layer by layer mode to 3D growth. Under the 3D growth mode, the islands are created, which have much greater capability of reducing strain compared to dislocations [38]. By continuing the growth, islands increase in size forming a layer by coalescence. But due to random sizes and positions, the atomic ordering is distorted, leading to defect formation during island coalescence. This is the main drawback of the 3D growth mode.

The different compounds can have different crystal phases therefore their crystallographic orientations can be different. For example, InAs nanowires have a wurtzite structure, but are grown on zinc blende InAs substrates. This distorts the epitaxial information and can lead to the formation of stacking faults and twin planes [39]. Also some strain is likely to be present. Heteroepitaxial growth allows choosing the interface type at the transition between one material to another, for example between InAs and GaSb. In this example, there are two possible interface combinations: GaAs like and InSb like, with InSb interface being superior [40].

3.3 Epitaxial overgrowth

Epitaxial growth normally occurs over the whole substrate and ensures a good uniformity of the growing layer. However, it is sometimes desirable to reduce the growth area by a mask and perform a selective area epitaxy. The conditions for selective epitaxy are chosen such, that source material nucleates only on the unmasked parts of the substrate, and no nucleation occurs on the polycrystalline mask. This is achieved when the critical-nuclei radius on the mask is larger than on the substrate. Epitaxial overgrowth is a special case of selective area epitaxy, when the growing layer completely covers the mask. But the layer does not nucleate or grow on the mask, instead it extends from the substrate by a lateral growth.

The overgrowth can be separated into two steps: lateral growth over the mask and layer planarization, illustrated in Figure 3.1. Over the mask, the crystal grows both laterally and vertically at the same time, forming facets at the crystal edge. The facet will be outward if the lateral growth rate exceeds the vertical growth rate or inward if the vertical growth rate is higher than the lateral growth rate. If inward facets meet, a void is formed, while outward facets tend to coalesce void free. Also, the facets have to conform to the Wulff theory of the stable crystal shapes [41], therefore multiple facets are present over the mask. If facets of different orientation meet then a grain boundary is formed. As the facet orientation is determined by the thermodynamic equilibrium, the growth parameters, like temperature and/or partial pressure, can be tuned to obtain desired facets shapes.

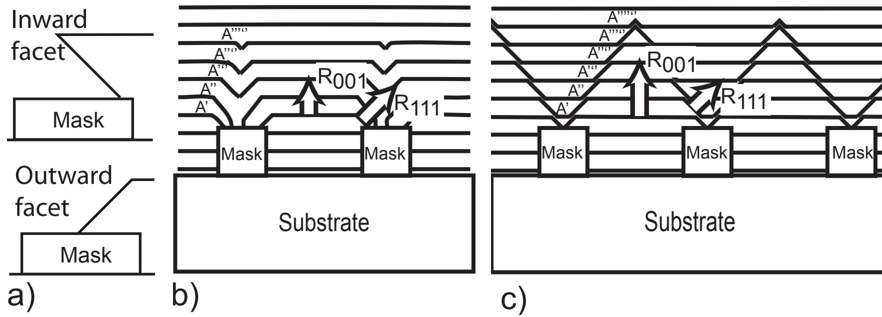

Figure 3.1: a) Schematic of the facet types: inward and outward. Schematic of epitaxial planarization process when: a) the lateral growth rate is higher than the vertical one $((R_{111} > R_{001}))$, b) the lateral growth is lower than the vertical one $((R_{111} < R_{001}))$

As illustrated in Figure 3.1b and c the planarization occurs when the lateral growth fronts (A') meet from both sides of the mask. There are two ways for planarization:

1. $R_{111} > R_{001}$ - the lateral growth rate is higher compared to the vertical one as shown in Figure 3.1b. In this case the growth front A' moves closer to the opposing

growth front with increasing layer thickness. When it reaches the opposing growth front, the surface becomes planar.

2. $R_{111} < R_{001}$ - when the lateral growth rate is lower than the vertical one, the layer planarization is also possible [42] as shown in Figure 3.1c. Here the growth front A' is moving away from the opposing growth front. The planarization occurs when the growth front A meets another growth front, created on the other mask. To achieve full planarization by this method, the mask pattern has to be periodic.

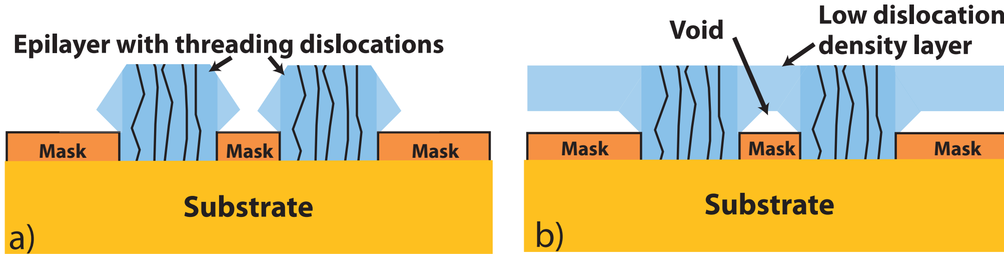

Figure 3.2: Schematic of the heteroepitaxial overgrowth process for dislocation reduction: a) before overgrowth and b) after overgrowth.

The epitaxial overgrowth is used to reduce the dislocation density in heteroepitaxial growth. As defects can not penetrate the mask, the overgrown areas result in better crystal quality, as shown in Figure 3.2. The lattice mismatch generates a large amount of dislocations to relieve strain, but the laterally growing edge follows the epitaxial order of the relaxed layer. This method is successfully used for reducing threading dislocation density in GaN. Although, grain boundaries and voids can still be present [43].

3.4 Nanowire growth

Typical nanowires are vertically standing high aspect ratio semiconductor structures. In order to grow a nanowire, the epitaxial process is tuned to enhance locally the vertical growth rate. To achieve this, a typical nanowire is grown on a native {111} substrate where the lateral growth rate is suppressed by lowering the growth temperature to $(450 - 470\ ^oC)$. To enhance the vertical growth rate a Au particle is placed on the substrate. During the growth, the particle becomes supersaturated with group III element, for example In, leading to a locally increased source material concentration. The group V element, for example As, is not soluble in the Au particle, and therefore is supplied to incorporation site by the surface diffusion. This forms a triple phase boundary at the incorporation site [44], where In and As combines to form an InAs layer under the particle. As a result the Au particle is lifted upwards during the growth, thus creating a typical nanowire as shown in Figure 3.3. As the growth continues, the nanowire develops

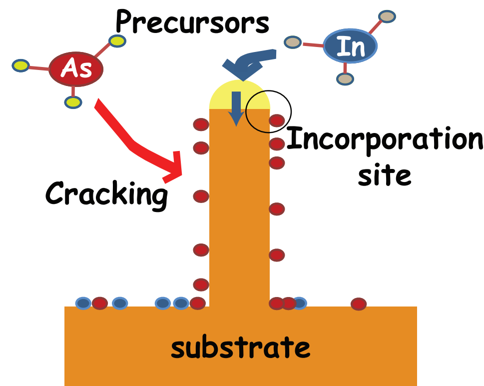

Figure 3.3: Schematics of InAs nanowire growth.

side facets, that are normally oriented along the {110} directions. In the simplest case, these side facets consist of {111} micro-facets [45], which have a slow growth rate. This suppresses the lateral growth on the nanowire walls to obtain tapering free nanowires. By raising the growth temperature it is possible to enhance the lateral growth rate and make for example, core/shell nanowires [46].

3.5 Epitaxial growth in MOVPE

Metal Organic Vapor Phase Epitaxy (MOVPE) is a type of Chemical Vapour Deposition (CVD) epitaxial reactor that uses metal organic source materials. The CVD technology uses gas molecules in the fluid flow regime, where molecules can interact with each other. The interaction can result in forming undesired compounds, thus deteriorating the growth quality. This is avoided by carefully choosing source materials (also called precursors) that are chemically stable at ambient conditions and only react at elevated temperatures. The probability of parasitic reactions is also lowered by diluting the growth precursors with carrier gases such as H_2 or N_2. The carrier gas also creates a laminar gas flow in the CVD reactor to improve the growth uniformity and to further reduce the mixing of gases. Suitable precursors for CVD growth are metal-organic molecules, that mostly come in the form of $(CH_3)_xR$, where R is the metal ion There are two major advantages with these precursors [47]:

1. growth reactions will normally form only gaseous compounds, like methane, which are easy to pump out from the reactor,
2. a wide variety of metals can be combined into Metal-Organic molecules.

Examples of the metal-organic sources are Trimethyl-Indium (TMI), Trimethyl-Antimony (TMSb) and Trimethyl-Gallium (TMGa), while Arsenic (As) can be supplied in the metal-

organic form as Tertiarybutyl-Arsine(TBAs) or as a hydride (AsH_3) [48]. These sources are routinely used for growing InAs or GaSb.

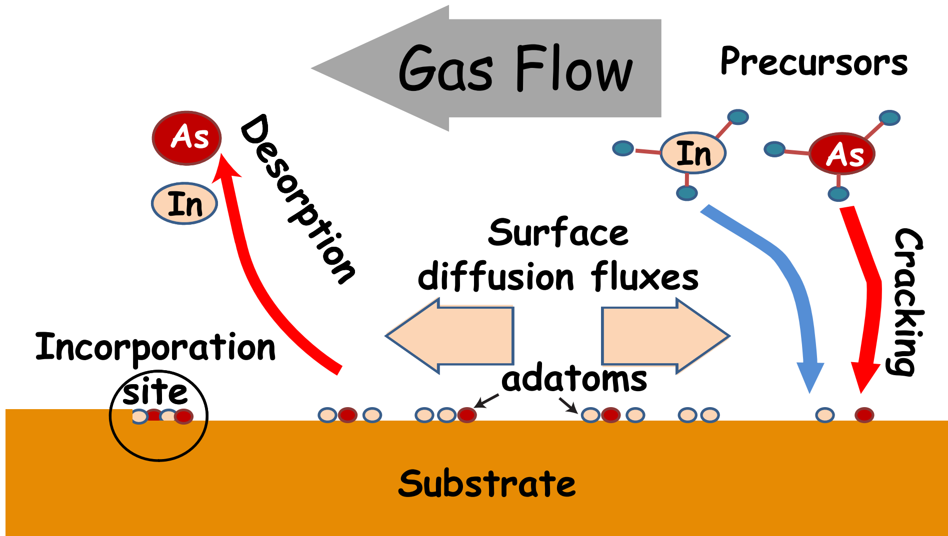

Figure 3.4: The schematic of the growth process inside the MOVPE reactor.

The MOVPE growth process is schematically shown in Figure 3.4. The carrier gas flow transports precursor molecules to the substrate in a gas mixture. When the precursors reach the substrate, the methyl bonds crack due to the high temperature of the substrate (typical ranges are from 400 to 800 °C) releasing the metal atom. It is important to mention, that the cracking efficiency is normally greatly enhanced if the precursor molecule is in direct contact with the substrate [49]. Therefore the substrate acts not only as a template, but also as a catalyst for cracking. After the cracking is complete (for example, TMI has to release three methyl groups in sequence), the gaseous (organic) parts of the molecule is pumped away. The metal atom now becomes an adatom, which means that it is physisorbed to the surface. The adatom diffuses on the substrate until finding a suitable incorporation site, like a monolayer step or any other non-uniformity on the substrate.

As group III elements are likely to clump together and form metallic particles, it is important to have excess group V elements near the incorporation site. Therefore a V/III ratio is normally much higher than one to ensure the excess. Also, cracking efficiencies vary between different precursors, so the ratio is adjusted to account for that. The excess adatoms can desorb from the substrate by overcoming the physisorption energy barrier and return to the gas phase. The desorption sets the upper limit of the growth temperature, while the lower limit is set by the need to have high diffusion rate and high cracking efficiency.

4

Electrical measurement techniques for thin films

In this thesis, two of the common methods for evaluating the electrical properties of semiconductor materials are used. These techniques are Hall measurements and Capacitance-Voltage characterization. Hall effect measurement is a standard technique to evaluate mobility, carrier type and carrier concentration, while Capacitance measurements reveal information about carrier density, their spatial distribution and oxide properties. This technique is also easily extended to evaluate interface trap densities. However, InAs nanostructures present a few difficulties for these standard characterization techniques. The capacitance of the nanowire structures exhibit non parabolic band effects and full depletion, while Hall measurements in thin films have to account for the surface pinning layer as well leakages from other layers, present in the integrated structures.

The first section presents what changes in the Capacitance Voltage characteristics when InAs nanowires are measured compared to the standard MOS structures. Second section describes the multilayer Hall mobility.

4.1 Nanowire Capacitance Voltage characteristics

A typical structure for performing CV measurements is a Metal Oxide Semiconductor (MOS) capacitor, as shown in Figure 4.1a. The oxide and the metal layer are deposited on the prepared semiconductor sample to form a capacitor. The oxide is chosen to have a large dielectric constant and a large band gap ($> 3\ eV$) in order to act as a good insulator. When a bias U is applied, the capacitance of the MIS structure depends on the voltage because the depletion layer varies inside the semiconductor. The depletion layer is a virtually carrier free region, therefore extending the oxide. As the width of the depletion layer increases, the measured capacitance decreases, creating a CV profile, shown in Figure 4.2a as a dashed line.

The nanowire MIS capacitor can be constructed by joining two MIS capacitors at their backsides, as shown in Figure 4.1b. This increases the oxide/semiconductor area, therefore allowing a higher capacitive coupling to the channel. However, the CV profile of a planar capacitor and the nanowire capacitor differ.

First, a near zero depletion capacitance can be measured in nanowires, as is shown in

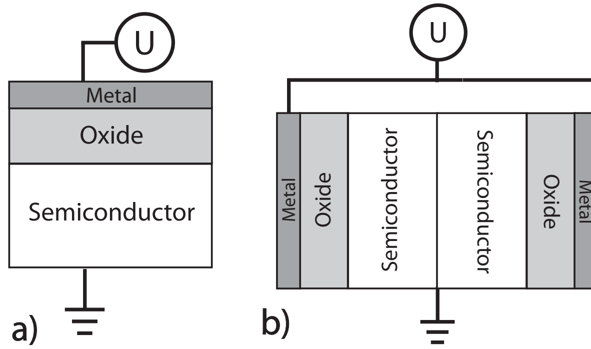

Figure 4.1: Schematics of a) Metal-Insulator-Semiconductor (MIS) and b) a nanowire MIS capacitor structures.

Figure 4.2a. This is not observed for the planar MOS capacitors, as a hole inversion limits the extent of the depletion layer, leading to a non zero $C_{depletion}$. But the nanowire can be thinner than the maximum depletion width, therefore no hole inversion is created in the radial direction. For example, for the InAs the maximum depletion layer width exceeds 20 nm at a 10^{18} cm^{-3} doping level. Therefore the full depletion is expected for all small diameter nanowires. If a higher bias is applied, the Fermi level will cross the intrinsic carrier energy level, creating the inversion layer, as shown in Figure 4.2b. However, the position of this layer will be at the bottom of the nanowire stem. The area occupied by the inversion layer remains small due to the small diameter of the nanowire, therefore the near zero capacitance will be observed.

A second difference in the CV profile is related to the specific material property of InAs. InAs exhibits non-parabolic band structure [50], which leads to low density of states. Therefore electrons fill higher states in the conduction band, and noticeably raise the Fermi level. This subsequently increases the potential difference between the metal and the semiconductor, thus lowering the capacitance. Therefore the accumulation capacitance of InAs nanowire as well as other InAs structures is lower than the geometrical limit [51]. As electrons fill higher states at higher positive bias, the separation between the Fermi level and the conduction band (ΔE in Figure 4.2c) increases and an increasing accumulation capacitance is measured instead of saturation.

The full depletion condition has an advantage for analyzing the nanowire CV characteristics, as under this situation there are no electrons to affect the potential distribution in the nanowire. In a depleted nanowire, the voltage will drop only over the uncompensated charges, that in most cases are donors, which then will be proportional to their number. This allows defining a threshold voltage at a point when the capacitance becomes zero. The threshold voltage can then be compared, for example, for nanowires with different doping levels. Such analysis is more convenient as a standard model requires calculating electron distribution using non-parabolic bands and solving the Poisson equation for that

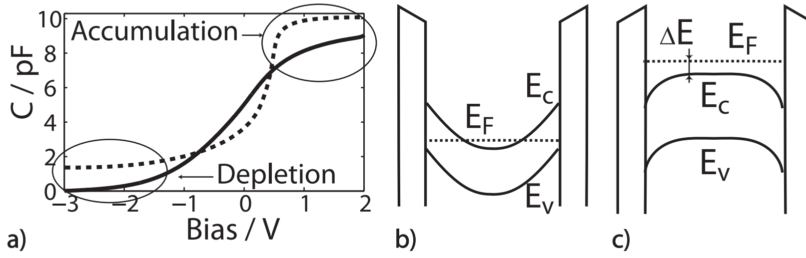

Figure 4.2: a) A typical CV curve of the n-type InAs nanowire MIS capacitor (solid line) and planar MOS capacitor (dashed line). InAs nanowire band structure at b) depletion c) accumulation. Here, U is an applied bias, E_F, E_C and E_V are a Fermi level, a conduction band and a valence band, respectively. ΔE is the separation between the conduction band and the Fermi level.

distribution in the radial geometry just to get the doping level.

The threshold voltage method can also be expanded to evaluate the surface trap density. The basic idea is that charges at the surface and charges inside the nanowire scale at different rates for different nanowire diameters. The bulk area increases as πr^2, while the surface scales only as $2\pi r$, with r being the nanowire radius, analysis of threshold voltage diameter dependence can reveal dopant distribution profile. Apparently, this also means that the nanowire threshold voltage is diameter dependent, while in the planar MOS case no size dependence is expected.

4.2 Multilayer Hall mobility

The Hall effect is used as a basic semiconductor film characterization technique to obtain the carrier concentration and the carrier mobility. The Hall effect is measured when the carrier current is deflected by the Lorentz force due to the magnetic field ($\vec{F} = q(\vec{E} + \vec{v} \times \vec{B})$). The deflection creates a carrier density gradient in the film, which results in a potential difference perpendicular both to the current flow and the magnetic field directions. The potential difference is then measured as the Hall voltage (V_H), which is inversely proportional to the electron density. Depending on the carrier type, the sign of V_H changes, being positive for holes, and negative for electrons. Once the carrier concentration has been determined, the mobility is obtained from a conductance relationship: $\sigma = en\mu$.

However, the current in InAs films can have more than one path: bulk conduction, surface layer conduction [52–54] and defect conduction [55,56]. Therefore the conductivity becomes a sum expressed as $\sigma = \sum_i en_i\mu_i$ and the Hall effect also has to be expanded to include multiple conductances. In general, the Hall effect is also magnetic field dependent [57]:

$$V_H = \frac{R_H I B}{h};\ R_H = \frac{1}{en} \tag{4.1}$$

V_H: Hall voltage
I: carrier current
B: magnetic induction
h: sample thickness
R_H: Hall constant
n: carrier density
e: electron charge

$$R_H(B) = \sum_i \frac{\sigma_{xy}/B}{\sigma_{xx}^2 + \sigma_{xy}^2} \tag{4.2}$$

$$\sigma_{xx} = \sum_i \frac{e n_i \mu_i}{1 + (\mu_i B)^2} \tag{4.3}$$

$$\sigma_{xy} = \sum_i \frac{e n_i \mu_i^2 B}{1 + (\mu_i B)^2} \tag{4.4}$$

R_H: Hall coefficient
σ_{xx}: longitudinal conductance tensor
σ_{xy}: transverse conductance tensor
e: electron charge
n_i: carrier concentration of i_{th} carrier species
μ_i: mobility of i_{th} carrier species

At small magnetic fields, when $\mu_i B \ll 1$, R_H becomes B field independent, leading to the classical Hall effect. However, when multiple conduction paths exist, the Hall coefficient remains magnetic field dependent. To separate each contribution we can analyze this dependence, as the influence from high mobility carriers is quenched due to the $(1 + (\mu B)^2)$ denominator and a step like behavior is obtained [58]. At strong magnetic field, the Hall constant is dominated by the lower mobility carriers. With the use of the magnetic field dependent longitudinal and transverse conductances, the contributions of each current path can be extracted from wide range magnetic field sweeps data [59]. However, the procedure requires considerable effort to obtain good measurements and to correctly extract the results. Therefore it is useful to have an approximation for the multiple conduction relation, valid at low magnetic fields [60]:

$$R_H = R_{Hb} \frac{d_b}{(d_b + d_l)} \left(\frac{\sigma_b}{\sigma_t}\right)^2 + R_{Hl} \frac{d_l}{(d_b + d_l)} \left(\frac{\sigma_l}{\sigma_t}\right)^2 \tag{4.5}$$

$$\sigma_t = \sigma_b + \sigma_l \tag{4.6}$$

R_{Hb}: Hall coefficient of buffer layer
R_{Hl}: Hall coefficient of thin film
d_b: thickness of the buffer layer
d_l: thickness of the thin film
σ_b: conductivity of the buffer layer
σ_l: conductivity of the thin film
σ_t: conductivity of the integrated structure

In this case the approximation is expressed for the structure consisting of two layers - the buffer and a thin film. Here, the total Hall coefficient of the sample is a sum of the respective Hall coefficients of each species, multiplied by their respective contributions to conductance. This formula is suitable to design experiments as it allows estimating whether a classical Hall effect measurement is sufficient, or a more detailed analysis will be required. However, one has to be careful in applying this expression to evaluate the mobility of separate species. If a high mobility carrier is present, then the $(1 + \mu_i^2 B^2)$ denominator makes the high mobility contribution to R_H non-linear, thus making the linear addition in the approximation inaccurate. In such a case a full two conducting layer R_H expression has to be considered [61]:

$$R_H = \frac{(d_b + d_l)\left[(R_{Hb}\sigma_b d_b + R_{Hl}\sigma_l d_l) + R_{Hb}R_{Hl}\sigma_b^2\sigma_l^2(R_{Hl}d_l + R_{Hb}d_l)B^2\right]}{(\sigma_b d_b + \sigma_l d_l)^2 + \sigma_b^2\sigma_l^2(R_{Hl}d_l + R_{Hb}d_l)B^2} \tag{4.7}$$

It is also important to note, that the mobility of a particular carrier type itself can be affected by more than a single type of scattering. The most common ones are polar optical phonon and impurity scatterings [62,63]. In this case, the mobility is expressed as: $\frac{1}{\mu_i} = \frac{1}{\mu_{imp}} + \frac{1}{\mu_{pol}}$, where μ_{imp} and μ_{pol} are impurity and polar phonon scattering limited mobilities. Fortunately, these scattering types are temperature sensitive therefore their effect is observed only in temperature dependent Hall measurements [64, 65].

5

Nanowire CV characterization

High quality InAs nanowires are routinely grown and used for building functioning Metal Insulator Semiconductor Field Effect Transistors (MISFET) [17, 66–68]. These devices already show performance of $f_{max} = 7\ GHz$, and are even integrated to Si substrates. However, little is known about the properties of the oxide and the oxide/semiconductor interface in nanowires. Basic properties like the magnitude of capacitance, the doping level and the trap density so far has not been determined for nanowires with gate structure.

A challenge is that the small size of the nanowire devices leads to small capacitances, which in turn are hard to measure. The capacitance can be as low as a few femto Farads [69, 70], which is below the detection limit of typical measurement equipments. Gated single nanowires have been measured using low noise equipment up to 20 kHz frequencies [29], but the frequency region is not suitable for investigating narrow gap InAs capacitors [71]. This requires building nanowire capacitor structures measurable by conventional equipment.

5.1 Undoped nanowire CV characteristics

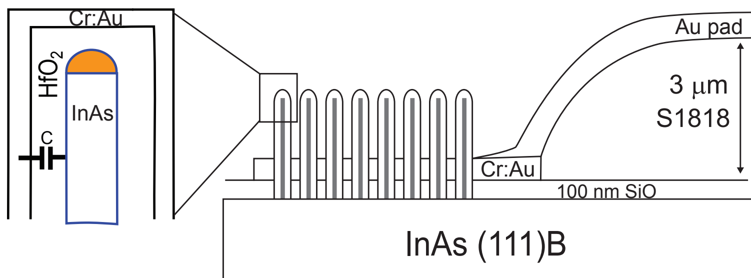

Figure 5.1: Schematic of the nanowire capacitor

A simplest solution to increase the nanowire capacitance to a measurable $0.5 - 10\ pF$

level, is connecting an array of identical nanowires in parallel as shown in Figure 5.1 There still remains a parasitic capacitance from the pad, that is used to connect probes to the capacitor array. To reduce it, the gate pad is raised from the substrate, reducing the pad capacitance to 300 fF.

The measured CV characteristics of such InAs nanowire capacitor are shown in Figure 5.2a. For the not intentionally doped nanowires, the depletion capacitance reaches zero at all temperatures up to room temperature. It also contains a temperature activated stretch-out region, which is attributed to the interface traps [72]. The accumulation capacitance does not saturate as expected due to the non parabolic band structure of InAs. The accumulation capacitance is temperature sensitive, but this cannot be attributed to the intrinsic carrier generation, as the doping level in NID InAs nanowires is $8 \cdot 10^{17}\ cm^{-3}$, which is much larger than the $5 \cdot 10^{15}\ cm^{-3}$ carrier density for intrinsic InAs [1]. Also, as nanowire InAs is a wurtzite instead of a zinc blende, the larger band gap should lower the intrinsic carrier concentration even more. The temperature variation of the accumulation capacitance is therefore attributed to traps present in the HfO_2.

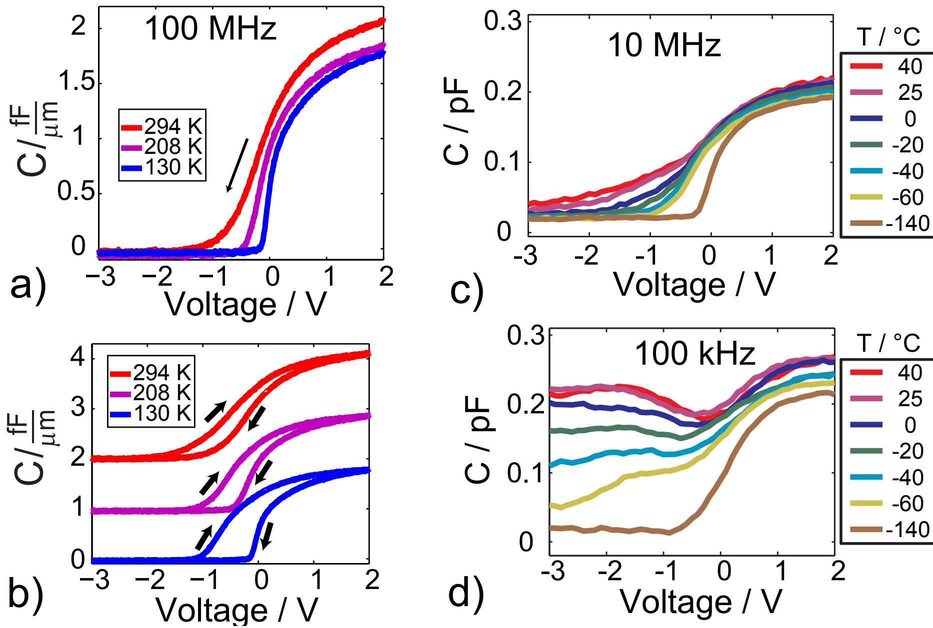

Figure 5.2: CV characteristics of undoped nanowire capacitor: a) CV curves, measured in DOWN sweep direction at different temperatures at 100 MHz. b) Nanowire CV hysteresis at different temperatures. The hysteresis loops are offset vertically for easier comparison c) CV characteristics at 10 MHz and d) 100 kHz

InAs nanowire CV profiles have a considerable hysteresis at all temperatures, as shown

in Figure 5.2b. The UP sweep curve (the voltage is ramped from -2 V to +2 V) is observed to be temperature independent, while the DOWN sweep curve (the voltage is ramped from +2 V to -2 V) stretches with increasing temperature. As only the semiconductor is expected to be temperature sensitive, the DOWN sweep is therefore related to the response from the oxide/semiconductor interface. The UP sweep is then attributed to the charge movement inside the HfO_2 oxide.

CV measurements at different frequencies are shown in Figure 5.2 c and d. It is clear, that both temperature and frequency increases the stretch-out. The increase in the depletion capacitance can be related to the hole inversion layer. However, a full depletion is expected before the increase of capacitance when only the inversion layer is present. The measurements at 100 kHz show that the capacitance decreases little during voltage sweep, indicating that the trap response is stronger than the minority carrier response at this frequency. At higher frequencies the nanowire becomes fully depleted showing that the hole inversion layer is negligible.

5.2 Nanowire doping level

The CV characterization is a standard technique to extract the doping density, as the capacitance is proportional to the electron density in the semiconductor. A typical method is to determine the threshold voltage from $1/C^2$ plot vs Voltage and calculate the doping concentration (N_D) using a standard MOS model. However, the radial geometry of the nanowires and the non parabolic bands makes it complicated to determine the exact capacitance behavior with applied voltage. Instead, the use of fully depleted nanowires offers a simpler solution.

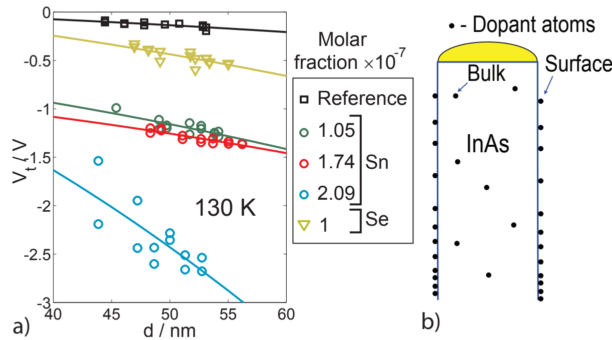

Figure 5.3: a) V_T-d_{nw} plot for Sn and Se doped nanowire capacitors b) Schematic of dopant distribution in InAs nanowire

In the fully depleted nanowire, the threshold voltage (V_T) is proportional to the uncompensated charge density only. V_T is extracted by making a linear fit to the CV profile and plotted vs a nanowire diameter (d), as shown in Figure 5.3a. It is apparent that V_T

is diameter dependent, as the nanowire area increases with πr^2, which means that the number of charges per area increase at the same rate. Therefore the increase in the slope means that more charges are present in the nanowire, implying a higher doping level.

It is also clear, that not only the slope of the $V_T - d$ curves increases, but also different doping levels cause a large shift of the threshold voltage. However, the shift of threshold voltage with higher dopant flow can not be related to the doping level as this is accounted by the slope of the curve. Therefore the shift has to be related to the dopant distribution profile. In analogy with standard MOS theory, the shift is attributed to the surface charge. This means, that doped nanowires contain charges not only inside it, but on the nanowire side facets as well. Interestingly, there are more charges on the surface than in the bulk of the nanowire. This is why there is a clear separation between different $V_T - d$ curves, as otherwise they should extend from the same origin. The important result is that dopants tend to preferentially incorporate at the nanowire surface, as shown in Figure 5.3b. A similar dopant distribution is observed in Ge nanowires, where the effect is enhanced by a lateral growth [73].

5.3 Nanowire capacitance transients

The capacitance hysteresis means that there is a time component, which is attributed to the electron release by a Schottky-Read-Hall process. To measure capacitance transients, first, a bias pulse is applied to push the capacitor into the accumulation. During this pulse, the traps are filled with electrons. Second, the bias is lowered in order to create a depletion layer. As the Fermi level is lowered to the band gap, the electrons, located in traps above the Fermi level are emitted, causing a change in the depletion layer width and therefore a capacitance transient. The rate of the transient is proportional to the difference in energy between the trap position and the conduction band. The rate therefore contains information about the energy of the trap.

The rate of capacitance transients can be measured using Deep Level Transient Spectroscopy (DLTS). This measurement technique sets the rate window, within which the transients can be detected and determines the temperature of the detected transient. By measuring transients at different rate windows, the temperature spectrum of the transient rate is obtained. As the rate is exponential to the trap energy level, the spectra is analyzed using Arrhenius plots to obtain the trap energy.

The DLTS measurements reveal a bias dependent trap energy, which exceeds the band gap of the InAs. Such behavior is unexpected, as the trap energy is determined by the separation between the level of the trap and the conduction band. As more negative bias is applied the Fermi level can be lowered to scan states deeper within the band gap, but as it approaches the valence band, the deep level traps can now emit their electrons directly to the valence band. However such situation is outside the bounds of the standard model. Still, the standard model can be applied to analyze data while Fermi level is above the mid gap. It is observed that traps with activation energy levels of 0.25 eV are present in $InAs/HfO_2$ interface

6

Characterization of Overgrown InAs

For nano-sized InAs structures, the pinning effect can be the dominant conduction mechanism. Therefore it is important to quantify the extent of the pinning within the material and evaluate how it affects the mobility of the structure. Overgrown metal patterns increase considerably the surface area within the semiconductor material, thus affecting the semiconductor properties. For example the conductance can be tuned by several orders of magnitude in GaAs [74] due to the carrier depletion around the overgrown metal pattern. Similarly the increased surface area within InAs should enhance the Fermi level pinning. Therefore overgrown metal patterns are integrated within the thin InAs layers. A well overgrown structure can increase the surface area in InAs in a controlled fashion, without affecting the crystalline structure or the defect density, thus allowing measuring the surface contribution to the thin film properties. As tungsten is thermally stable in InAs [75], and there is little expected W diffusion during low temperature growth [76], tungsten is chosen as a mask for the overgrowth. This chapter presents the tungsten overgrowth by the InAs on a GaAs substrate.

6.1 Overgrowth

In order to enhance surface to volume ratio, a thin InAs film is required. Therefore InAs has to be grown on semi-insulating substrate to avoid the substrate conduction, present in narrow gap substrates. A GaAs substrate is chosen as it allows easy transition to the InAs growth. However, GaAs is strongly lattice mismatched to InAs, therefore the growth is heteroepitaxial. Also the growth mode changes to 3D island growth, which can hamper the planarization. To overcome these difficulties, the growth parameters are investigated to obtain a successful overgrowth.

The overgrowth is done in a layer by layer growth mode, therefore the 3D growth mode has to be changed. This is best done by reducing the growth temperature to 500 ^oC as it reduces the Stranski-Krastanow island size distribution and increases their density. To obtain a layer, the islands have to coalesce, which is achieved at a low V/III ratio due to enhancement of the growth of the underlying wetting layer [77]. Of course, threading dislocations are created in the process, due to the nature of mismatched growth.

After the layer by layer growth mode is achieved, W patterns can be incorporated. W is placed directly on the GaAs substrate, as this does not hinder a successful overgrowth.

The overgrown InAs film is void free as shown in Figure 6.1a, but coalescence dislocations form over the W pattern during planarization. It is clear that their density is proportional to the number of W lines, and maximum two dislocations are generated over one tungsten line. The origin of the coalescence dislocation is attributed to different film relaxation on the left and right side of the tungsten film, thus epitaxial information no longer matches when the two growth fronts meet.

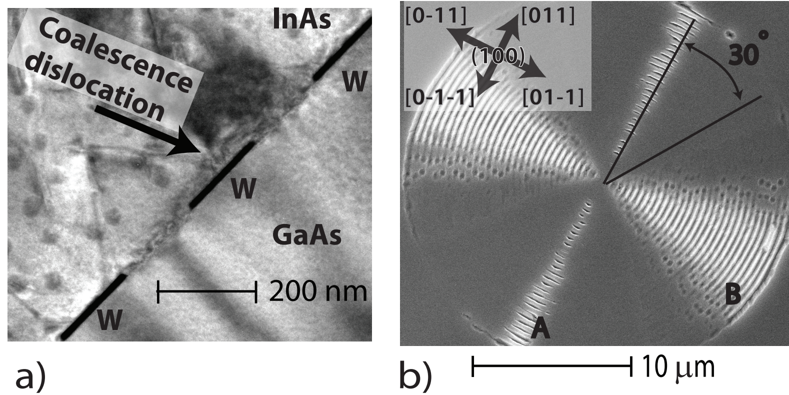

Figure 6.1: W patterns overgrown by InAs on GaAs substrate. a) TEM image of the overgrown W pattern, b) SEM image of overgrown concentric circles of tungsten.

As shown in Figure 6.1b, the tungsten lines are placed in concentric circles, which are overgrown by InAs. The overgrowth is preferential in a particular direction, determined to be 30° off the [011], while in others directions, a formation of {111} ridges is observed, as a {111} surface has the slowest growth rate.

To understand the origin of the preferential overgrowth direction, we have to analyze ridges A and B, that form along the [011] and [011] directions, respectively, marked in Figure 6.1b. Both of these ridges have {111} side facets, as shown in Figure 6.2a, but the side facets of A ridge are In terminated, while for the B ridge, they are As terminated. As In terminated surface has higher growth rate than the As terminated surface, therefore the A ridge is more overgrown and is shorter compared to the B ridge, as seen in Figure 6.1b.

The presence of W lines disturbs the thermodynamic equilibrium shape of the ridge, forcing the crystal to orient itself along the tungsten pattern. The new crystal shape along the tungsten line is composed of both A and B ridges, creating a vicinal surface, as shown in Figure 6.2b. As only A and B ridges are possible under low temperature growth conditions, the crystal edge forms kinks, composed only of A and B ridges. The preferential overgrowth direction is then along the highest kink density, as vicinal surfaces enhance the lateral growth rate. However due to asymmetry of the ridge length in InAs (Figure 6.2b), the number of kinks is largest not at the 45° angle, but at an angle closer

to the [011] direction. Therefore the preferential overgrowth direction in InAs is along the 30° off the [011] [78].

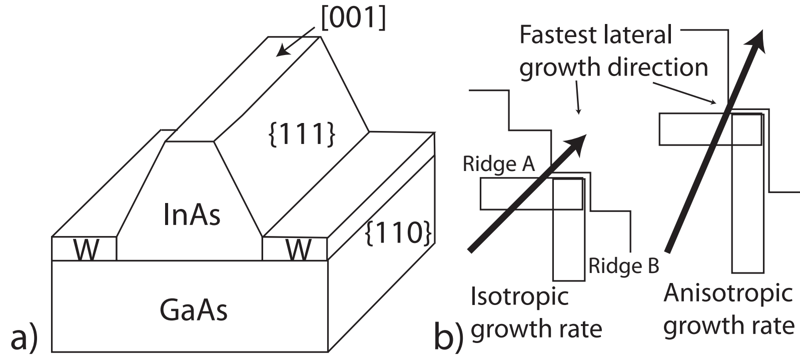

Figure 6.2: a) Schematic of the {111} ridge, formed between W lines. b) Schematic of the vicinal surface formation required for overgrowth

6.2 Electrical Characterization of overgrown InAs/W patterns

In order to evaluate the effect of the surface pinning in InAs, a simple device is used, shown in Figure 6.3a, where the overgrown W lines are placed parallel to each other and separated by a spacing d. By varying d, the density of the tungsten pattern is varied systematically, and thus the area of the surface pinning layer. It is therefore expected that at large d, the overgrown pattern has no effect on the material, while at lower d the overgrown surface area increases, affecting the electrical conduction of the device.

The measured overgrown devices have up to 5 times higher conductance, compared to the device without tungsten. This is much more, than the expected 15% increase due to the conductivity of the tungsten. Therefore the conductivity is related to the tungsten-semiconductor interface. Hall measurements reveal that the carrier concentration increases with increasing tungsten density and then saturates at $3.5 \cdot 10^{17}\ cm^{-3}$. The saturation indicates that there is an effective length (λ) of the surface pinning region, present around each tungsten line, as shown in Figure 6.3b and c. However, the mobility does not vary with the tungsten density and also is lower than the mobility of tungsten free device. First, this allows dismissing the influence of coalescence dislocations, as their density is higher when more tungsten is present. The mobility is therefore attributed to the surface pinning region, which is the dominant conduction path in the device. Even if the tungsten density is increased, the Hall signal is still dominated by the surface, therefore no mobility change is observed.

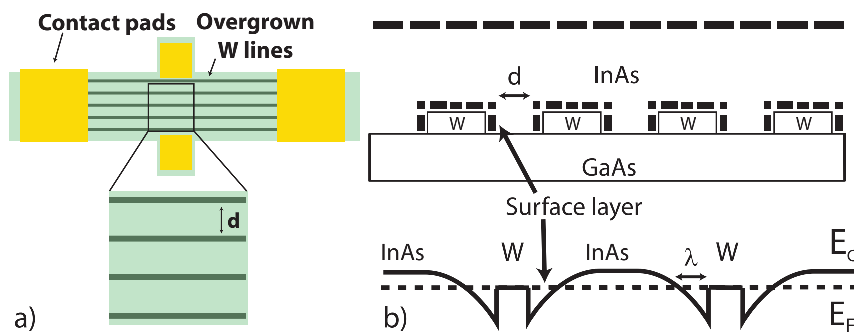

Figure 6.3: a) Schematic of overgrown device for Hall measurements. d is the distance between tungsten lines, while the line width is kept fixed. b) Schematic of the structure and the band diagram of the overgrown InAs.

7

InAs membranes on GaSb buffer layers

Thin InAs films with bulk mobility are obtained using buffer layers but at the expense of the buffer thickness, which exceeds $> 4\ \mu m$ [24]. However, such thick buffer makes it difficult to integrate InAs with other devices on the substrate due the large difference in height between the substrate and InAs layer. It is also very expensive and time consuming to grow thick layers in any epitaxial reactor. On the other hand, InAs is a high mobility semiconductor, and not all electronic applications require the highest possible mobility. Therefore it is interesting to learn whether InAs can be integrated using thin buffer layers and determine how much the mobility is lowered due to the lower structural quality of the buffer.

7.1 GaSb buffer growth

The GaSb is chosen as it has a lattice constant of 6.095 Å, which is only 0.6% lattice mismatched to InAs layer. This leads to a large critical thickness and more than a few monolayers of InAs can be grown directly on GaSb. As epitaxial growth conditions tend to be reactor dependent, a growth of GaSb has to be optimized before starting to investigate the quality of InAs. The growth optimization also establishes a baseline of quality for the buffer material. Typical parameters for optimization are growth temperature, V/III ratio and nucleation temperature. As GaSb is grown on GaAs, the growth mode is again 3D, therefore a low temperature nucleation is used to change the mode to layer by layer one. The low temperature nucleation increases the density of GaSb islands on GaAs surface to favor the transition.

The growth of GaSb is not trivial, as Sb tends to segregate and coat surfaces with an Sb monolayer. This means that during the growth, the Sb adatoms have to bind to Ga atoms without creating an excess. Ga atoms also cannot be oversupplied, as then they will start forming Ga droplets, deteriorating the growth. To avoid this, both the V/III ratio and the growth temperature are optimized. The optimum growth conditions are 450 ^oC for nucleation temperature, 3 for V/III ratio and 570 ^oC for buffer layer growth temperature.

7.2 InAs integration onto GaSb

In order to have a reference of a consistent quality, metamorphic InAs film is chosen, that have the same lattice constant as the GaSb layer. This means that defect density in both layers is expected to be the same as well. If thicker InAs layers are grown, then they relax their metamorphic lattice and generate additional defects in the process. A 23 nm film thickness was chosen as it is under the critical thickness according to a conservative Mathews-Blackeslee model [35]. A conservative critical thickness is used to ensure that the dislocations in GaSb do not enhance the relaxation of the InAs metamorphic layer.

To vary the quality of the buffer layer, the dislocation density is changed by varying the thickness of GaSb buffer layers. As InAs is metamorphic, the dislocation density depends directly on the defect density in the buffer layer, as shown in Figure 7.1a. Therefore a relation between the structural quality of the buffer layer and InAs layer can be evaluated. The quality of both layers is known to be proportional to each other, but in this way it can be quantified as well.

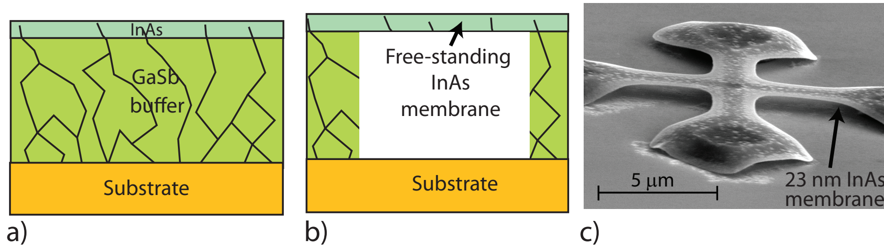

Figure 7.1: a) Schematic of a grown InAs/GaSb structure. b) Schematic of the free-standing InAs membrane. c) SEM image of a free-standing InAs membrane for Hall measurements.

To establish a relation between the quality of the buffer and the InAs, first the InAs layer is selectively etched away. The remaining GaSb layer is measured and mobility is shown to be proportional to the structural quality as expected. The second step is to remove the GaSb layer by selective etch, as shown in 7.1b and measure InAs membranes. This removes the large substrate conduction, but retains the metamorphic lattice of InAs. As shown in Figure 7.1c, the the edges of the InAs membrane are bent downwards, although the bending should be upwards, as InAs is tensile strained. The downward bend is attributed to the Van der Waals forces between the etching liquid and the InAs membrane. However, membrane bridges are flat and also do not bend in the middle, which indicates that the structure has not relaxed.

The electrical measurements on membranes reveal that thin InAs structures are highly resistive. High resistivity normally means low material quality. If thicker (90 nm thick) membranes are measured than resistivity is much lower and a mobility of 2000 cm^2/Vs is obtained. Therefore the high resistivity of the thin membranes should be related to the

membrane processing, but not a sign of a low quality. By passivating the surface of thin membranes with sulfur solution, the resistivity of membranes is lowered about 5 times. This decrease indicates that thin membranes are very sensitive to surface treatments. However, even passivated structures are still moderately resistive, indicating that the passivation is not sufficient. The possible approach is to investigate membranes with thicknesses of about 50 nm, as these are shown to be conductive [27]. Although it is not clear whether these layers will still be under the critical thickness to remain metamorphic after the membrane processing.

Therefore currently it is established that structural qualities of InAs and GaSb layers are directly proportional to each other. It is expected that the electrical quality will follow this relation as well, which is shown to be valid at least for the GaSb buffer layer.

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Electrical characterization of thin InAs films grown on patterned W/GaAs substrates

Gvidas Astromskas[a)]
Solid State Physics, Lund University, Box 118, S-22100 Lund, Sweden

L. Reine Wallenberg
Polymer and Materials Chemistry/nCHREM, Lund University, Box 118, S-22100 Lund, Sweden

Lars-Erik Wernersson
Solid State Physics, Lund University, Box 118, S-22100 Lund, Sweden

(Received 25 April 2008; accepted 10 August 2009; published 15 September 2009)

InAs has been grown on W–GaAs patterned substrates using metal organic vapor phase epitaxy. It is shown that the W pattern guides the nucleation of the InAs on the GaAs substrate and that the islands formed may be used to embed metal features in a hybrid InAs/GaAs structure. A lower resistance (factor of 2) was measured for the hybrid structures as compared to reference structures. The reduction in the resistance is attributed to an increased carrier concentration as observed from Hall measurements on devices with different tungsten densities. Cross-sectional transmission electron microscopy investigations reveal a void-free overgrowth above the metal despite the large mismatch of the InAs/GaAs system. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3222859]

I. INTRODUCTION

Materials with a narrow band gap are attractive for high-speed devices and long wavelength optical devices. For instance, high electron mobility transistors[1] and lasers operating above 2 μm (Ref. 2) have been fabricated in materials lattice matched to InAs or GaSb. Due to the lack of semi-insulating substrates, the layers are typically grown on GaAs or InP semi-insulating substrates using thick and complex buffer layers. In a typical process, the initial stage of the deposition results in a highly defective layer close to the interface, where the strain is released via dislocation formation. As the deposition continues, the number of defects is reduced and the material quality improves. Eventually, epitaxial layers suitable for device fabrication may be obtained.

In this article, we present an alternative technology in that we grow InAs on a patterned W–GaAs substrate. We show that the W pattern affects the growth of the InAs both in the nucleation stage and by subsequent lateral overgrowth over the metal and that the electrical properties of the layer are influenced by the presence of the W layer. These results are discussed in terms of surface carrier accumulation around the W pattern.

II. MATERIALS AND METHODS

The fabrication of the W–GaAs patterns for the overgrowth is based on a lift-off process using evaporated metal.[3] The patterns formed consist of lines (width of 90–100 nm and periods of 200–700 nm) and concentric rings (width of 100 nm and periods of 400 nm). Metal organic vapor phase epitaxy (MOVPE) was used to epitaxially overgrow the patterned substrates with InAs at a growth temperature of 500 °C and a V/III ratio of 14. Trimethylindium (TMI) and arsine (AsH_3) were used as sources for the InAs growth at a MOVPE reactor pressure of 100 mbars. The molar fractions of the TMI and AsH_3 were 2.75×10^{-5} and 3.74×10^{-4}, respectively, and the total flow was 6000 slm (standard liters per minute). After the growth, the samples were inspected using scanning electron microscopy (SEM) to evaluate the quality of the deposited material. Atomic force microscopy (AFM) measurements were performed to extract the thickness of the overgrown layer. At these growth conditions, no deposition occurred on the tungsten structures and thus larger W patterns were used as references when measuring the thickness of the InAs layer. After thickness determination, device mesas were processed. For the electrical characterization of the InAs/W/GaAs integrated structure, patterns with 70-μm-long tungsten wires oriented 30° off the $[0\bar{1}1]$ direction were used. These gratings had different periods, 200–700 nm, and different metal widths, 70–90 nm. Electron beam lithography (EBL) was used to align and expose mesa patterns on the sample, employing positive EBL resist polymethyl methacrylate. Mesa structures were formed by etching the developed sample down to the semi-insulating GaAs using $H_3PO_4:H_2O_2:H_2O$. The depth of the etching was controlled using profilometer scans, as the etching solution attacks both InAs and GaAs. EBL was finally used to align contacting pads with the etched mesas. Au:Ti layers (500:5 nm thick) were evaporated to make Ohmic contacts for the measurement structures. Reference devices (without tungsten lines) were fabricated on the same sample by exposing the mesa structure outside the W-patterned areas.

The overgrown patterns were analyzed using transmission electron microscopy (TEM) in order to evaluate the effect of the overgrown patterns on the layer quality. TEM lamellas (about 40 nm thick) were made using focused ion beam/SEM system FEI Nova NanoLab 600 and the inspection was performed with a JEOL 3000F.

a)Electronic mail: gvidas.astromskas@ftf.lth.se

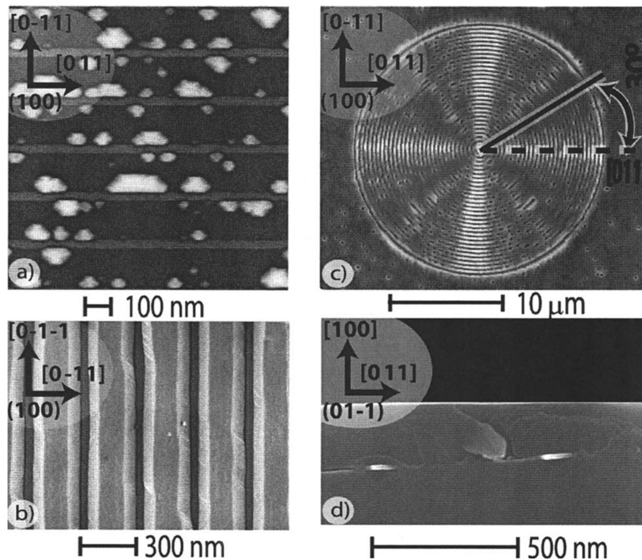

FIG. 1. (a) Formation of Stranski–Krastanow islands along tungsten lines at 600 °C (10 nm deposition). (b) Formation of mesa ridges in between lines at 500 °C (90 nm deposition). (c) Overgrown circle showing preferential overgrowth direction to be 30° of the [011] direction, corresponding to grating directed at 30° from the [0$\bar{1}$1] direction (290 nm deposition). (d) SEM image of cross section of the overgrown (290 nm deposition) tungsten pattern, with two tungsten lines shown as white contrast.

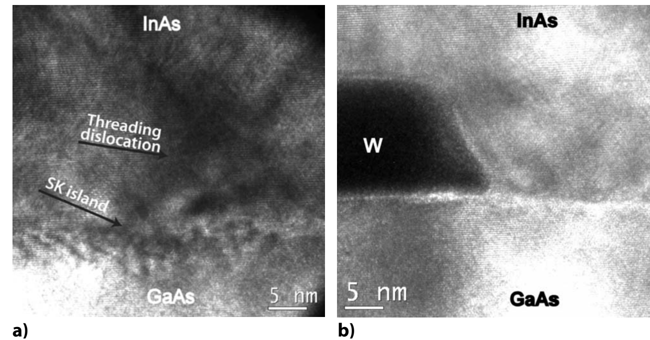

FIG. 2. TEM images of (a) interface between InAs and GaAs of the reference device. (b) Interface between InAs/W/GaAs of the overgrown structure. The arrows mark the SK island and the threading dislocation, originating from the island. The interface of the metal patterned device is smoother and leads to less stacking faults at the interface in between the metal pattern structure.

III. EPITAXIAL GROWTH

Successful homoepitaxial InAs overgrowth over W patterns has been reported when growing at a V/III ratio of 20 and at a growth temperature of 600 °C;[4] therefore we evaluated whether these growth conditions result in overgrowth when InAs is grown on GaAs. But due to the large lattice mismatch, InAs forms Stranski–Krastanow (SK) islands when deposited on a GaAs substrate (Fig. 1). Outside the patterned areas we observed nonuniform island sizes, ranging in diameter from less than 2 nm up to 20 nm for the used growth temperature of 600 °C. In contrast to the unpatterned areas on the same substrate, we found that inside the grating, Fig. 1(a), most islands nucleated along the tungsten lines, with only a very few SK islands forming in between the tungsten lines. Besides, the islands along the tungsten lines were substantially larger in size than the ones in the middle. This indicates that larger islands also had higher growth rate as more material was deposited, preventing surface planarization.[5] In order to reduce size nonuniformity and increase the SK island density, a lower deposition temperature of 500 °C was selected.[6,7] Here, the choice of temperature was crucial, as we found that the use of higher growth temperatures resulted in a rougher surface for the overgrown layer. At the new growth conditions we observed that the deposited InAs (about 70–90 nm thickness) resulted in a flat (001) top surface grown in between lines oriented along the [0$\bar{1}$1] direction, as shown in Fig. 1(b). This was confirmed by AFM inspection, which also revealed that the side planes extended down to the tungsten grating and had angles of either 45° or 54.6° toward the (001) surface, corresponding to {110} and {111}*A* planes, respectively. Such ridges were reported in the homoepitaxial InAs overgrowth at 600 °C.[4] Therefore, the identification of the same shape and direction of the limiting growth planes as in homoepitaxial overgrowth indicates that the strain did not considerably influence the growth of InAs on W-patterned GaAs at the growth temperature used.

The overgrowth of the W and the planarization above the grating were achieved with a thicker InAs layer of 290 nm. The circular patterns of tungsten revealed a strong directional dependence of the InAs growth, as shown in Fig. 1(c). Three clearly distinguishable growth modes in different directions can be identified in the developed patterns above the circles: complete overgrowth, mesa-type ridge formation along the [011] direction, and a mixed region of mesa ridges and partial overgrowth along the [0$\bar{1}$1] direction. Complete overgrowth of the tungsten occurred when the grating was aligned 30° off the [0$\bar{1}$1] direction. This direction corresponds to the fast growing facet of InAs.[4] The complete overgrowth was void-free as shown in Fig. 1(d).

IV. TEM RESULTS

High resolution cross-section TEM images in Fig. 2 compare the InAs quality between the reference (a) and the overgrown (b) devices. The location of the interface between InAs and GaAs is easily identified in both images, but the reference in (a) has a wider area of mottled contrast due to Moiré patterns of overlapping lattices with slight misorientation, indicating a much more uneven interface. The contrast in (a) also indicates the formation of a Stranski–Krastanow dot (arrow) with the base at the interface and 60° stacking fault pairs emerging from the top of the dot, which may form the origin of threading dislocations. In the W-patterned sample in (b), the interface was relatively smooth and abrupt and with a much lower density of lattice disturbances in the area in between the dark W patterns. Lattice planes are visible in both images even near the interface, but individual edge dislocations at the interface cannot be identified due to insufficient image quality of the comparably high sample thickness. However, the only threading dislocations, propa-

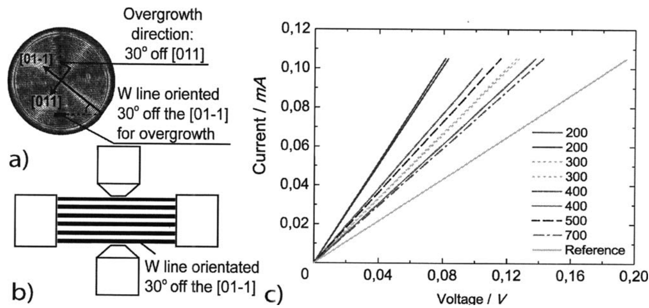

FIG. 3. *IV* characterizations of the overgrown devices. (a) Layout of the directions on the sample. (b) Schematic structure of the overgrown devices. (c) *IV* characteristics of overgrown devices and references. Numbers in the legend stand for the period of the 90-nm-wide tungsten lines.

gating along the {111} direction observed in the patterned device, were in most cases located at the middle of the tungsten mask. The origin of the dislocation at the center of the mask coincides with the coalescence region for the two InAs growth fronts meeting above the W structure.

The InAs lateral overgrowth starts after 15 nm of InAs deposition (height of W) and a better structural quality of the overgrown layer is achieved as compared to the reported heteroepitaxial overgrowth of InAs.[8] Our samples are grown under a low V/III ratio and a low growth temperature to favor the growth on high energy facets that form along the overgrowth direction. We observe that dislocations are more frequent at the unpatterned InAs/GaAs interface, whereas W patterns yield lower defect density in the overgrown layer. However, the overgrown layer is not defect-free, as 60° threading dislocations originating from the coalescing growth fronts create propagating dislocation lines with about one coalescence dislocation per wire. This is in contrast to the TEM results of GaAs overgrowth on W (Ref. 9) and may be attributed to the strain relaxation in the overgrown material.

V. ELECTRICAL CHARACTERIZATION

Electrical measurements were done to evaluate the resistance of the material and to determine the carrier concentration and the carrier mobility. Experiments were carried out on $70 \times 20\ \mu m^2$ devices (Hall bars) containing embedded gratings oriented 30° off the $[0\bar{1}1]$ direction ("Overgrown devices") and devices without any metal lines ("Reference"). Figure 3(a) illustrates the direction of overgrowth and how tungsten lines should be aligned in order to investigate the electrical properties of the overgrown layer and device schematic is shown in Fig. 3(b).

As shown in Fig. 3(c), the overgrown devices had a lower resistance as compared to the reference and, in total, the resistance was reduced to less than half for the hybrid (InAs/W) devices as compared to the references without any tungsten lines. The mesa geometry was used to deduce the conductivity of the devices from the measured data. Based on reported values for the resistivity for overgrown tungsten lines ($120\ \mu\Omega$ cm),[3] it was calculated that the contribution from the metal accounted only for about 15% (it varied with pattern density from 11% to 18%) of the total measured conductance in our devices. It may hence not be responsible for the observed reduction in the resistance as the metal density increased.

In order to analyze the origin of the low resistance in the overgrown structures, Hall measurements were performed on samples with an InAs thickness of 290 nm at room temperature and at 77 K. Figure 4 shows the deduced values for the carrier densities (a) and mobilities (b) of the fabricated devices. The main results are that the reference structure had a comparably low carrier concentration but a high mobility, while the mobility in the overgrown structures did not exceed 3000 cm^2/V s. However, all overgrown devices exhibited higher carrier density than the reference structure. The deduced Hall mobility value for the reference InAs layer (4850 cm^2/V s) corresponds well to the measured mobilities at room temperature for thin InAs layers grown on GaAs.[10] This value increased to 6300 cm^2/V s at 77 K, while the mobility for all the hybrid structures remained essentially constant. To remove the influence of the metal, the tungsten conductance was subtracted from the total conductance when calculating the electron mobility. Also, the Hall constant for our sample may be assumed to have contributions from two sources—the tungsten wires and the InAs layer. This can be evaluated using Petritz's approach:[11]

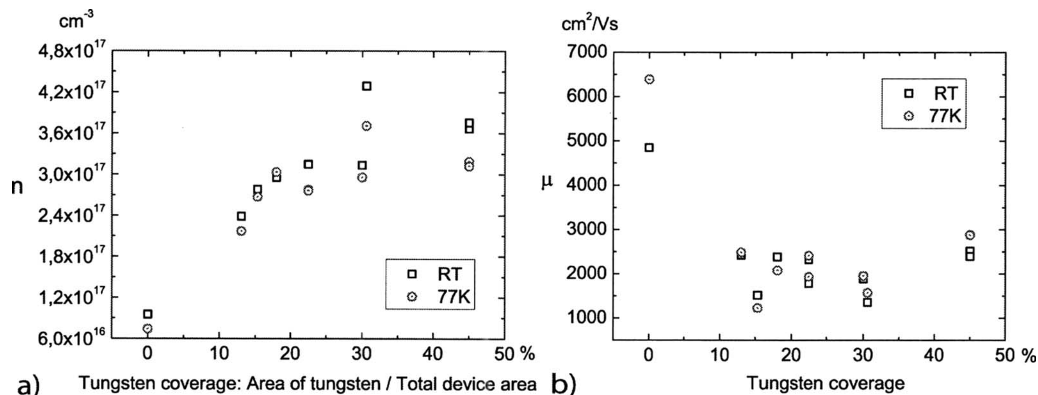

FIG. 4. Hall effect measurement results: (a) carrier density and (b) mobility as a function of the tungsten coverage.

$$R_H = R_{H_W} \frac{d_W}{d}\left(\frac{\sigma_W}{\sigma}\right)^2 + R_{H_{InAs}} \frac{d_{InAs}}{d}\left(\frac{\sigma_{InAs}}{\sigma}\right)^2.$$

Here, R_H is the Hall constant, d is the total layer thickness, and σ is the total conductivity of the hybrid structure. d_W, d_{InAs}, σ_W, and σ_{InAs} are the thicknesses and conductivities of the tungsten wires and the InAs film, respectively. According to the formula, the Hall coefficient for the tungsten was negligible compared to the InAs layer due to the large resistivity of tungsten ($\rho = 120\ \mu\Omega$ cm).

VI. DISCUSSION

Studies of strained InAs grown on GaAs and Si substrates[10–14] have shown that the deposited layer may be separated into three regions: the interface, the bulk, and the surface. The extent of the interface layer varies with different growth conditions and especially with various attempts to reduce the dislocation density where it can be reduced from 1 μm (Ref. 14) to 200–300 nm.[12] As we have been studying thin InAs layers in our overgrown devices (290 nm), they should consist of only the surface layer and the interface. Lack of any bulk layer, for instance, explains the low value for the mobility of the reference device.

Inserting the tungsten into the InAs layer affects primarily the dislocated interface layer, although a second surface layer may be expected to form around the tungsten lines. As shown in a study with metal-insulator-semiconductor capacitor measurements,[12] the mobility at the surface is heavily dependent upon the total charge in the accumulation region, explaining the reduction in mobility when tungsten is present. Figure 4(a) shows an increased carrier concentration with the addition of tungsten. The possible source for this increase is the accumulation of electrons around the tungsten due to the pinning of the Fermi level in the conduction band. Also, the Hall mobility of the overgrown samples was not decreasing with higher tungsten coverage while the carrier concentration demonstrated a weak increase with the higher W coverage. This relation suggests that the observed reduction in resistance may be attributable to a conducting layer around the W. This conclusion is further supported by other studies of dislocated InAs layers[11–13] that show temperature dependent mobility, which we did not observe in our measurements.

The electrical measurements may be explained considering a simple model where change in the surface from GaAs/InAs-like to W/InAs-like occurs when the tungsten coverage increases. Either interface can be characterized with a specific carrier density or the measured total carrier concentration will be proportional to the area occupied by each surface type. In this case, a linear increase would be expected as observed for a low W coverage [Fig. 4(a)]. The nonlinear dependence of measured carrier concentration can be explained if one assumes that surface regions around neighboring tungsten lines overlap, locally modifying the band bending. In this regime, the electron concentration has a weaker dependence on the coverage. From the TEM inspection we conclude that the dislocation density changes when tungsten is present; therefore one has to take into account a change in dislocation density as well. As most of the tungsten lines inspected in the TEM had a coalescence dislocation related to them, we assume that the number of these dislocations increases linearly for devices with more tungsten lines. One may thus expect that the carrier concentration should increase linearly when more coalescence dislocations are present. However, the carrier concentration, shown in Fig. 4(a), saturates at higher tungsten coverage. Also, the increasing dislocation density should reduce the carrier mobility, but we observed a rather constant trend in the measured Hall mobilities [Fig. 4(b)]. We hence describe a possible electrical transport mechanism for the overgrown hybrid InAs/W/GaAs devices as a combination of surface accumulations, appearing at the InAs surface and at the InAs/W interface, and dislocation scattering. Electrically, this results in the observed increased conductance for the overgrown devices as compared to the reference.

VII. SUMMARY

We studied the conditions for the epitaxial overgrowth of InAs on W–GaAs patterned substrates. It was demonstrated that the InAs preferentially nucleates along the metal patterns and that these nucleation sites form the basis for subsequent lateral overgrowth over the metal. A deposition temperature of 500 °C was preferred as it was sufficiently high to prevent polycrystalline deposition on the metal, while it still provided a high density of nucleation sites and reduced diffusion of In species on the growing surface. A complete, void-free overgrowth with a planarized top surface could be achieved after 290 nm of deposition for a metal grating oriented 30° off the $[0\bar{1}1]$ direction as confirmed with TEM inspection. Hybrid InAs–W–GaAs structures showed a lower resistivity when compared to InAs–GaAs reference devices. An increased carrier concentration in the overgrown structures compensated for the reduced mobility and resulted in a net increase in the conductivity of the overgrown structure.

ACKNOWLEDGMENTS

This work was supported by the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF), and the Knut and Alice Wallenberg Foundation (KAW).

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InAs nanowire metal-oxide-semiconductor capacitors

Stefano Roddaro,[1,a)] Kristian Nilsson,[1] Gvidas Astromskas,[1] Lars Samuelson,[1] Lars-Erik Wernersson,[1] Olov Karlström,[1,2] and Andreas Wacker[1,2]
[1]*The Nanometer Structure Consortium, Lund University, P.O. Box 118, 22100 Lund, Sweden*
[2]*Mathematical Physics, Lund University, P.O. Box 118, 22100 Lund, Sweden*

(Received 1 May 2008; accepted 2 June 2008; published online 27 June 2008)

We present a capacitance-voltage study for arrays of vertical InAs nanowires. Metal-oxide-semiconductor (MOS) capacitors are obtained by insulating the nanowires with a conformal 10 nm HfO_2 layer and using a top Cr/Au metallization as one of the capacitor's electrodes. The described fabrication and characterization technique enables a systematic investigation of the carrier density in the nanowires as well as of the quality of the MOS interface. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2949080]

The development of wrap-gate nanowire (NW) field effect transistors (FETs) is opening promising perspectives for future high-performance electronic devices.[1,2] NWs allow the integration of semiconductor materials with reduced lattice-matching constraints[3,4] and offer the intriguing possibility of growing III-V structures on Si substrates, thus introducing high-mobility and optically active elements on a Si platform.[5] However, many of the key parameters of the NWs such as doping level and carrier distribution are still difficult to determine in a direct and conclusive way. For conventional FETs it is possible to take advantage of capacitance-voltage (*CV*) characterizations to determine, in a precise way, carrier concentration and interface properties of planar metal-oxide-semiconductor (MOS) stacks. Similar measurements have been largely unavailable for semiconductor NWs because of the extremely small capacitance of these nanostructures (down to attofarad). Recent experimental studies showed that such a small capacitance can be detected using bridge measurements together with appropriate screening.[6] Here we demonstrate *CV* measurements of small arrays of vertical NWs, where the NW capacitance can be easily separated from the parasitic capacitance between the gate connection and the conducting substrate. Our vertical fabrication protocol is scalable and thus enables parallel processing, which is crucial for a systematic investigation of the device properties.

The device structure is presented in Fig. 1. NW arrays [Fig. 1(a)] were obtained by self-assembled growth in a chemical beam epitaxy system. NW formation is guided by gold nanoparticles that are deposited on a doped InAs (111)*B* substrate.[7] A number of arrays were defined in parallel with various nanoparticle sizes to study radius dependence. For the present investigation 5 different groups of 15 nominally identical NW arrays were fabricated with average radii r_{NW} of 23.0, 25.0, 26.5, 28.5 and 30.0 nm, respectively. Panel (b) shows a typical radius distribution in a single 11×11 array with a standard deviation of about 4.0 nm. The device structure is sketched in panels (c) and (d). NWs were first insulated by a conformal HfO_2 coating (purple) by atomic layer deposition (125 cycles at 250° C, corresponding to $d_{ox}\approx10$ nm); the top electrode encapsulating the NWs was then fabricated by sputtering a Cr/Au bilayer (nominal 20/25 nm). A polymeric film of S1813 from Shipley with a thickness of about 1 μm (green) was used as a lifting layer in order to increase the ratio C_{NW}/C_0 between the NW capacitance C_{NW} and stray capacitance C_0 in our devices. Single devices were finally defined by UV lithography and metal etching of 30×45 μm^2 gate pads.

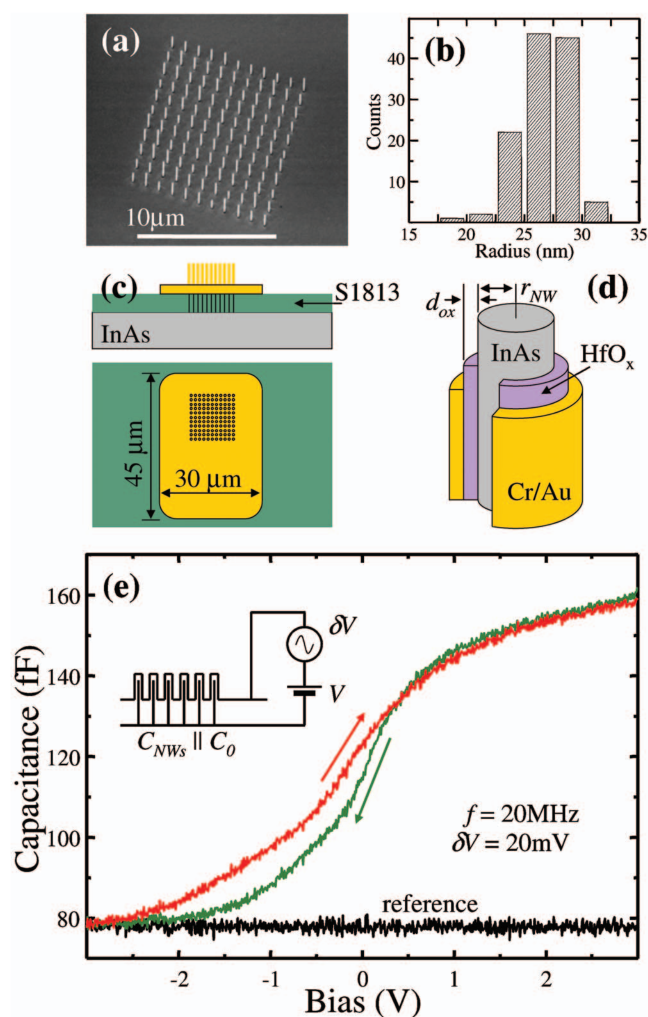

FIG. 1. (Color) (a) Scanning electron micrograph of an 11×11 InAs nanowire array (tilt angle of 52°). (b) Typical radius distribution in the array. [(c) and (d)] Details of the device structure. (e) Representative $C(V)$ scan from −3 to +3 V (red) and return (green) compared with a bare pad scan (black).

a)Present address: NEST Laboratory, P.za S.Silvestro 12, I-56124 Pisa, Italy. Electronic mail: roddaro@sns.it.

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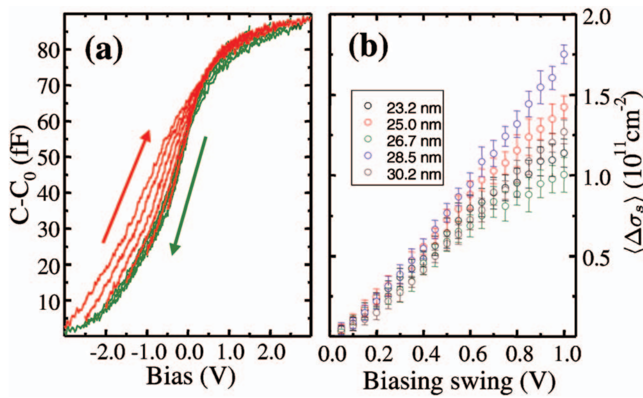

FIG. 2. (Color) (a) Evolution of the hysteresis cycle for increasing gate swings from $[-0.5,+0.5]$ up to $[-3.0,+3.0]$ V. (b) Charge loop integrals $\langle\Delta\sigma_s\rangle$ for different device geometries as a function of the biasing swing around 0 V.

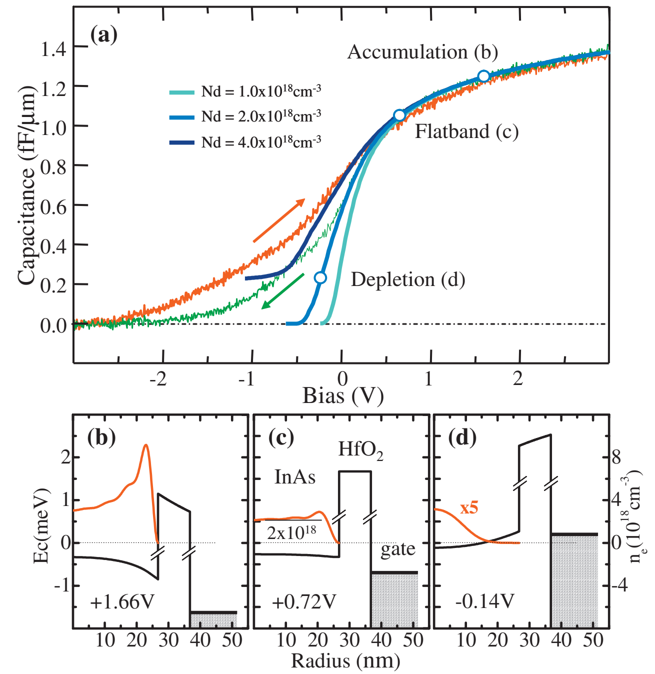

FIG. 3. (Color) (a) Theoretical fit of the dataset $C_{\downarrow}(V)$ of Fig. 1(e) using three different carrier densities. The band bending (black) and electron density (red) at the three different points along the blue line at doping $N_d=2\times10^{18}$ cm^{-3} are reported in the lower panels for accumulation (b), flatband (c), and depletion (d) conditions.

The NW capacitance was measured at room temperature in a Cascade probe station system equipped with an Agilent 4294A impedance analyzer. The complex impedance $Z=|Z|e^{i\theta}$ was measured using a small ac modulation $\delta V=20$ mV on top of a dc bias V in the range $[-3\text{ V},+3\text{ V}]$. A simplified scheme of the biasing configuration is shown in the inset to Fig. 1(e). The measured Z was found to be mostly capacitive ($\theta\approx-90°$) and was interpreted in terms of a series RC model with $Z=R-i/\omega C$. Such a simple model is appropriate in our case and experimental $Z(\omega,V)$ data for $V\gtrsim+1$ V yield a frequency-independent and well-defined $C(V)$. The frequency evolution of $Z(\omega,V)$ in the depletion regime for $V<0$ is less trivial as expected due to the increasing NW resistance, to the activation of slow trap states at the interfaces, and to effects of inversion in the InAs semiconductor. In particular, the increasing importance of RC constants close to the pinch-off is a peculiarity of our cylindrical geometry and sets a qualitative difference with respect to conventional planar MOS capacitors. The plot in Fig. 1(e) shows typical $C(V)$ sweeps obtained on devices from the group $r_{\rm NW}=26.5$ nm at a frequency $f=20$ MHz: we mark the sweep going from negative to positive as $C_{\uparrow}(V)$ (red) and $C_{\downarrow}(V)$ for the opposite sweep direction (green). The capacitance saturates at negative voltages to $C_0\approx70-80$ fF, grows sharply across $V\approx0$ V, and flattens again for $V>1$ V in the accumulation regime. Differently from conventional MOS capacitors, here we expect the NW to become insulating in the depletion limit and C to approach *zero* instead of a finite depletion capacitance. Indeed, here the observed saturation $C\rightarrow C_0$ corresponds to the NW depletion, as proved by comparison with four bare pads of the same geometry (black curve). The presence of C_0 is not linked to the NWs and it is rather due to both the parallel capacitance between the pad and the substrate as well as the one between the probe tips and the substrate.

Hysteresis effects are analyzed in Fig. 2. In the first panel, the shift between the capacitances measured in the two opposite sweep directions is barely visible on small (less than 1 V) sweep ranges while it increases for larger V swings. $C_{\downarrow}(V)$ curves do not depend strongly on the dc sweep swing while $C_{\uparrow}(V)$ curves tends to move toward higher C values (or lower V values, for a given C) when the sweep is extended from ±0.5 up to ±3.0 V. The shift between $C_{\uparrow}$ and $C_{\downarrow}$ does not depend strongly on the sweep speed (about 150 mV/s in our case) and time-dependent measurements indicate that capacitances tend to relax from $C_{\uparrow}(V)$ toward $C_{\downarrow}(V)$ on a timescale $\tau\approx30$ min. We conclude that $C_{\downarrow}(V)$ results from an equilibrium distribution of charges at the capacitor's interfaces while a long-lived out-of-equilibrium distribution is present along $C_{\uparrow}(V)$. This effect can be evaluated quantitatively in a simple way if one assumes that trapped charges are located exactly at the NW surface: in that case the addition of a surface charge density $\Delta\sigma_s$ will shift an ideal $C(V)$ curve as

$$C_{\rm meas}(V)=C(V+S_{\rm NW}\times\Delta\sigma_s/C_{\rm ox}),\qquad(1)$$

where $S_{\rm NW}=2\pi r_{\rm NW}L_{\rm NW}$ and $L_{\rm NW}$ are the surface and length of the gated NW, respectively, while $C_{\rm ox}$ is the oxide capacity $2\pi\varepsilon L_{\rm NW}/\log(1+d_{\rm ox}/r_{\rm NW})$. The value of $\Delta\sigma_s$ depends on the biasing history of the device; thus we obtain the different hysteresis cycles for different sweep swings. Figure 2(b) shows the average surface charge,

$$\langle\Delta\sigma_s\rangle=\frac{C_{\rm ox}}{S_{\rm NW}}\frac{1}{\Delta C}\oint C dV,\qquad(2)$$

where ΔC is the capacitance swing of the cycle and we used an average $L_{\rm NW}=680$ nm (from scanning electron imaging of the devices), $\varepsilon=15\varepsilon_0$,[8,9] and $C_{\rm ox}=1.78$ fF. The plot reports the loop integrals for the various device groups we studied: for V swings below ≈0.5 V we obtain $\langle\Delta\sigma_s\rangle<1.0\times10^{11}$ cm^{-2}, which seems very promising for device applications of NW as wrap-gate transistors.[10] Note however, that the hysteresis in the surface charge becomes much larger if the bias sweep extends further into the depletion region.

To further analyze the data, we performed detailed calculations for the capacitance on the basis of a Poisson–Schrödinger code similar to Refs. 11 and 12. Figure 3(a) shows the unit length capacitance for three different doping

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densities N_d of the wire, which are treated as a homogeneous positive background charge. The experimental data shown correspond to the assumption that 90 out of 121 wires are actually properly connected in the device: this scaling is required in order to match the geometry-set capacitance in accumulation and is not unreasonable given the present device parameters. The best fit is obtained using a doping of 2.0×10^{18} cm^{-3}: the curve at 1.0×10^{18} cm^{-3} rolls down too quickly with the voltage V. Differently at $N_d = 4.0 \times 10^{18}$ cm^{-3} the valence bands cross the Fermi level at the interface before the conduction band is completely depleted (0.54 eV was used as the wurtzite InAs gap[13]) and screening effects due to inversion are expected to show up, inconsistently with observations. It is interesting to note that all the fit curves in Fig. 3(a) fall nearly 50% short of the classical $C_{ox} = 2.61$ fF (for a 1.0 μm length, $r_{NW} = 26.5$ nm, and $d_{ox} = 10$ nm) even in the accumulation regime at $V \approx +3.0$ V. This is an effect of quantum capacitance that is due to the narrow radius of the NW with respect to the screening length. Lower panels indicate the corresponding conduction band diagram $E_c(r)$ in the capacitor in the accumulation (b), flatband (c), and depletion (d) regimes: the corresponding positions along the $C(V)$ fit are indicated in the top panel. We obtained the best agreement assuming the gate bias V to be 0.39 V larger than the calculated electrostatic potential at the gate. This shift can be attributed to the difference between the work function of Cr (4.5 eV) and the electron affinity of InAs (4.9 eV for zincblende lattice) as well as negative fixed charges with areal density $\approx 8 \times 10^{12}$ cm^{-2} trapped in oxide. As the electron affinity of the nanowire is uncertain due to the uncommon wurtzite structure exhibiting a larger band gap,[13] this estimate for the density of fixed charges is probably too large. It is crucial to note here that we assumed that only electrons in the conduction band are able to contribute to the $C(V)$ at our frequency. We interpret the discrepancy between fit and experiments for $V < 0$ V as due to the effect of screening of slow trap states in the InAs gap,[14] which indeed start becoming important at $V \approx 0$ V in our simulations. Consistently with this interpretation, we observed experimentally that such discrepancies become larger as the frequency is decreased and a clear $C(V)$ step develops, similarly to what has been reported in previous studies on planar structures.[15]

In conclusion we have demonstrated a technique for capacitance-voltage characterizations of arrays of vertical InAs NWs. Our analysis allows evaluating the role of surface states as well as yields an estimate of the doping in the NW, thanks to a detailed comparison with Poisson–Schrödinger simulations. Preliminary results indicate promising device parameters in view of the application of wrap-gate NWs as high-performance transistors.

This work was supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, the EU-project NODE 015783, the Knut and Alice Wallenberg Foundation, and the Italian Ministry of University and Research.

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Doping Incorporation in InAs nanowires characterized by capacitance measurements

Gvidas Astromskas,[1,a)] Kristian Storm,[1] Olov Karlström,[2] Philippe Caroff,[1] Magnus Borgström,[1] and Lars-Erik Wernersson[1]
[1]*Department of Solid State Physics and The Nanometer Structure Consortium, Lund University, Box 118, Lund SE-22100, Sweden*
[2]*Department of Mathematical Physics, Lund University, Box 118, Lund SE-22100, Sweden*

(Received 22 April 2010; accepted 6 July 2010; published online 1 September 2010)

Sn and Se doped InAs nanowires are characterized using a capacitance-voltage technique where the threshold voltages of nanowire capacitors with different diameter are determined and analyzed using an improved radial metal-insulator-semiconductor field-effect transistor model. This allows for a separation of doping in the core of the nanowire from the surface charge at the side facets of the nanowire. The data show that the doping level in the InAs nanowire can be controlled on the level between 2×10^{18} to 1×10^{19} cm^{-3}, while the surface charge density exceeds 5×10^{12} cm^{-2} and is shown to increase with higher dopant precursor molar fraction. © *2010 American Institute of Physics*. [doi:10.1063/1.3475356]

I. INTRODUCTION

The metal-oxide-semiconductor field-effect transistor (MOSFET) technology follows Moore's law for device scaling, where transistors with better performance are developed for each generation. The wrap-gate nanowire technology offers a possibility to extend the validity of Moore's law beyond that of traditional planar devices due to improved electrostatic control,[1,2] that can easily be combined with high-mobility III/V nanowire channels.[3,4] However, one major requirement for the transistor design is the ability to increase and control the carrier concentration, which is normally achieved by doping. Even though doped nanowires have been presented in the literature,[5,6] there is still a need to improve the control and understanding of the carrier concentration in nanowire systems.

Traditionally, the carrier concentration is determined by Hall measurements, but due to their one-dimensional geometry, this technique cannot be applied to the nanowires. Instead, the common approach is to study the transport in gated nanowires and deduce the carrier concentration from the threshold voltage. However, this method is based on the gate capacitance that often is calculated only. Additionally, it is known from atom probe tomography studies that donor atoms tend to preferentially incorporate at the surface of the nanowire.[7] This affects the capacitance of the structure and hence the determined carrier concentration. It is thus of great importance to measure experimentally and study the capacitance for individual[8,9] as well as arrays of nanowires.[10]

We present an experimental study of vertical InAs nanowire capacitors. We vary the diameter to evaluate the nanowire carrier concentration by employing a radial metal-insulator-semiconductor field-effect transistor (MISFET) model. By varying the dopant precursor molar fraction we demonstrate how the dopants are introduced into the core of the nanowire, but also show how additional charges are formed at the surface of the nanowire during the doping process. In order to account for the two doping incorporation paths, we add the surface charge density to the radial MISFET model. The new model is shown to be adequate to explain the measured threshold voltages of capacitance-voltage (CV) characteristics and also allows quantifying the nanowire carrier concentration and the surface charge at the side facets of the nanowire.

II. EXPERIMENTAL DETAILS

The nanowire capacitor fabrication starts by defining Au seed particles with a density of 1 particle/μm^2 using electron beam lithography. After Au liftoff, the samples are transferred to an Aixtron AIX 200/4 low-pressure metal organic vapor phase reactor equipped with trimethylindium, tetraethyltin (TESn), di-tertiarybutyl selenide (DTBSe), and AsH_3 precursors. InAs nanowires are grown at a temperature of 450 °C at a V/III-ratio of 68. The dopant precursor molar fractions were varied between 1×10^{-7} and 10×10^{-7}. It was observed that the nanowire length decreased linearly with increasing TESn molar fraction; from 1.4 μm for TESn free growth down to 0.9 μm for TESn molar fraction of 6.3×10^{-7} with 5 min growth time, therefore the growth time was adjusted to obtain about 1 μm (±5%) long nanowires. In order to account for the length variation due to different Au particle diameter,[11] the nanowire length in each array were determined from scanning electron microscope (SEM) inspection.

In order to make the capacitors, the nanowires were coated with a 10 nm-thick HfO_2 layer deposited by atomic layer deposition (250 °C) directly after the growth and followed by thermal evaporation of a 100 nm-thick SiO_x spacer layer. A nominally 50 nm-thick Cr and 100 nm-thick Au bilayer was deposited by sputtering, which resulted in roughly 1/3 of the thickness on the nanowire facets. The nanowire arrays were protected with a negative resist and the samples were wet etched to remove the unprotected Cr:Au

a)Electronic mail: gvidas.astromskas@ftf.lth.se.

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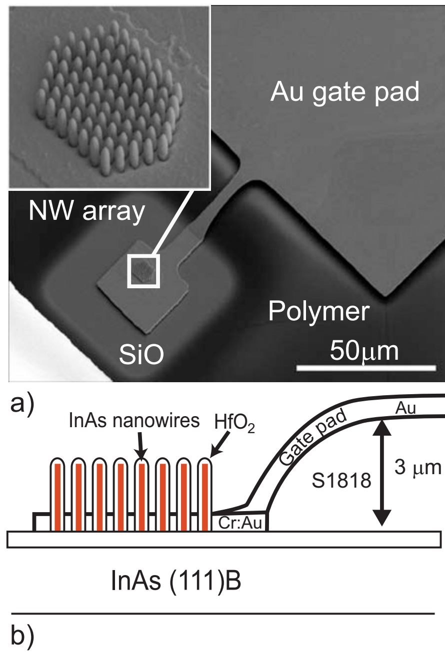

FIG. 1. (Color online) (a) SEM image of the finished capacitor. The inset shows a magnified image of the nanowire array. (b) Schematic of the nanowire capacitor structure. The frame capacitor is placed on top of S1818 surrounding the nanowire capacitors.

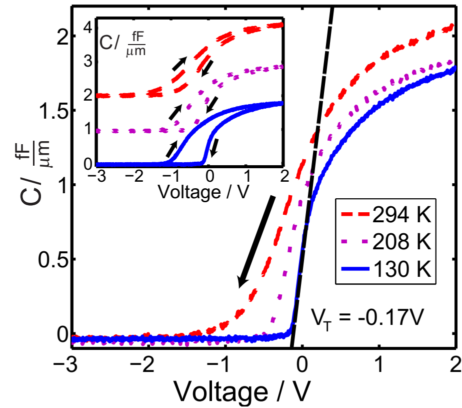

FIG. 2. (Color online) Measured CV characteristics of the nonintentionally doped InAs nanowire capacitor at different temperatures. The average nanowire diameter in this capacitor is 53 nm. The threshold voltage is linearly fitted on the down sweep of the CV curve. The inset compares the hysteresis obtained when voltage sweeping direction is changed, as marked by arrows (data are offset for clarity).

layer. The samples were spin-coated with a S1818 resist and the nanowire arrays were made accessible by means of optical lithography. The slope in the resist profile of S1818 allowed connecting the elevated gate pad to the nanowire capacitor array, as shown in Fig. 1. The device preparation was then finished by a 500 nm-thick sputtered Au gate pad defined by optical lithography and wet etching. The double step metal deposition process is used to reduce the parasitic capacitance of the gate pad. The fabricated samples contained capacitor arrays with varying nanowire diameter in the range of 44 to 54 nm with nominally 79 nanowires per array for Sn doped samples, while 2500 nanowires were defined in Se doped samples. The nanowire diameters were determined from SEM images taken after growth and the diameter spread within a single device was found to be less than 5%.

The fabricated capacitors were evaluated with an Agilent 4294A impedance analyzer in a Cascade probe station, equipped with a temperature control unit. The measurements were done with two probes of which one was placed on the nanowire gate pad and the other on a large (1–50 nF) frame capacitor in series with the nanowire capacitor. The complex impedance was measured at 100 MHz using a small AC modulation ($\Delta V = 20$ mV) on top of a dc bias V in the range from -3 to $+2$ V. The high measurement frequency was used to obtain a good signal to noise ratio and to suppress the influence of minority carriers as well as defect response at reverse bias. The capacitance was extracted from the measured impedance using a capacitance in series to resistance model, as less than 1 pA leakage currents were measured by DC. The typical capacitances were 700–1000 fF for Sn doped samples and 5–7 pF for the Se doped samples, while the parasitic plate capacitance was about 10% and 40% of the total capacitance for 2500 and 79 nanowire capacitors, respectively. The parasitic plate capacitance was subtracted from the data to simplify the data analysis.

A. Determination of threshold voltages

We start by analyzing the measured CV characteristics of the nominally undoped InAs nanowire capacitor array at different temperatures, shown in Fig. 2. It is apparent that the CV curves shift toward more negative biases and that the accumulation capacitance increases as the temperature is raised. As nonintentionally doped InAs nanowires have a large background carrier concentration due to carbon incorporation,[12] the shift cannot be related to thermal activation of carriers across the band gap. A similar observation is also reported in the InAs and InSb MOSFET structures[13] and may after a more detailed analysis be attributed to thermal activation at the interface or within the dielectrics.

The CV curves of nanowire capacitors have a measurable hysteresis, which is present at all temperatures as shown in the inset of Fig. 2. As noted, the down sweep varies with temperature, but the up sweep is observed to be almost temperature independent. We interpret the degree of hysteresis to depend on charge trapping in the dielectrics as well as at the $InAs/HfO_2$ interface. As we experimentally observed that the up sweep curve slowly relaxes to the down sweep CV profile over time (not shown), only the capacitance measured during the down sweep of voltage ($+2$ V$\rightarrow -3$ V) was used in this study.

The CV characteristics of nominally undoped and nanowires grown under TESn molar fraction are compared at 130 K in Fig. 3(a). Similar curves were also obtained for the Se doped capacitors. It is apparent, that the use of dopant precursors during the growth affects the shape and the magnitude of the nanowire CV characteristics. The larger the dopant precursor molar fraction, the less steep is the CV curve. Also, at higher doping levels, the dopant precursor molar fraction considerably raises the depletion capacitance, which saturates at a level above zero. The effect of the nanowire diameter on the shape of the CV curves is less pronounced,

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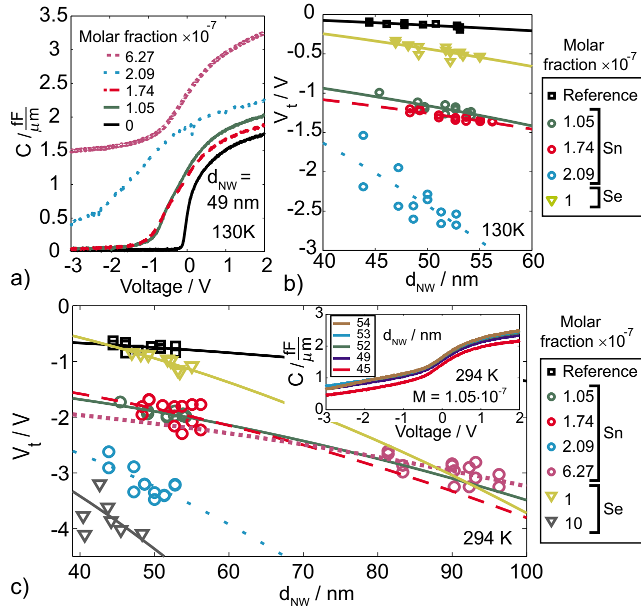

FIG. 3. (Color online) (a) Comparison of CV characteristics of different TESn molar fractions, (b) threshold voltage (V_T) vs nanowire diameter (d_{NW}) at 130 K, and (c) at room temperature. Solid curves show the best fit to the radial MISFET model. The inset in (c) compares CV characteristics of the sample grown with TESn precursor molar fraction of 1.05×10^{-7}.

only a minor increase is observed, as shown in the inset in Fig. 3(c). Also, the depletion capacitance for nanowires with different diameter remains essentially constant. Therefore, we conclude that different factors contribute to the CV profile when comparing capacitors with different dopant precursor molar fractions versus capacitors with different nanowire diameters.

In order to quantify the change of CV characteristics at different diameters or dopant precursor molar fractions, the threshold voltage (V_T) is determined for each CV curve by linearly extrapolating the CV profile around the inflection point to zero capacitance, as shown in Fig. 2. We plot V_T versus d_{NW} in Figs. 3(b) and 3(c) and observe that V_T decreases as the diameter is increased, as expected for a radial MISFET type device.[14] Interestingly, for doped samples using both TESn and DTBSe, the V_T data sets shift toward more negative biases and the magnitude of the shift depend on the dopant precursor molar fraction. This is consistent with the qualitative observations from the CV profiles. The threshold voltage is determined using linear extrapolation as measured CV characteristics do not follow the standard $1/C^2$ behavior used in planar geometries and explicit analytical models for nanowire CV relation are not yet available.

B. Modified radial MISFET model

It is observed in Fig. 2 that the depletion capacitance reaches zero under reverse bias, indicating that the nanowires are depleted. In this regime, the nanowire capacitor can be modeled as a simple radial MISFET device,[14] as shown in Fig. 4. The structure of the nanowire capacitor is composed of a semiconductor cylinder with radius R and constant carrier concentration (N_D) and is surrounded by a dielectric layer with thickness t_{ox}. We also add a surface charge density

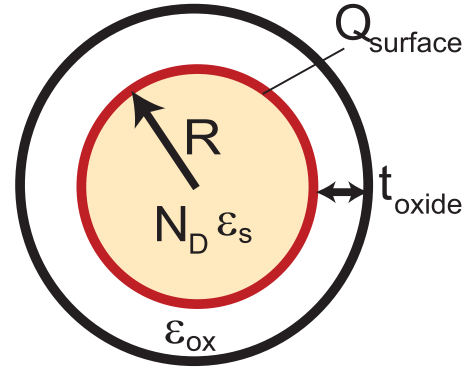

FIG. 4. (Color online) (a) Schematic of the nanowire cross-section with surface charge density (Q_s) at the nanowire/oxide interface.

(Q_s) at the perimeter between the InAs nanowire and the HfO_2 in order to include threshold voltage (V_T) shifts in the model. Using Gauss law we then obtain the relationship

$$V_T = V_{FB} - \frac{qN_DR^2}{4\varepsilon_0\varepsilon_s} - \frac{qN_DR^2}{4\varepsilon_0\varepsilon_{ox}}\ln\left(\frac{R+t_{ox}}{R}\right) - \frac{qQ_sR}{4\varepsilon_0\varepsilon_{ox}}\ln\left(\frac{R+t_{ox}}{R}\right). \quad (1)$$

Here, V_{FB} is the flat band voltage, ε_0 is the permittivity of vacuum, while ε_{ox} and ε_{InAs} are relative static dielectric constants of HfO_2 and InAs, respectively, with q being the elementary charge. The equation is valid under the full depletion approximation and for capacitors without inversion layer, which is the case for nanowires with zero depletion capacitance.

The formula can be simplified by making a first order Taylor expansion of the logarithm terms

$$V_T \approx V_{FB} - \frac{qQ_st_{ox}}{4\varepsilon_0\varepsilon_{ox}} - \frac{qN_Dt_{ox}}{4\varepsilon_0\varepsilon_{ox}}R - \frac{qN_D}{4\varepsilon_0\varepsilon_s}R^2 = V_0 + \frac{qN_D}{4\varepsilon_0}\left(\frac{t_{ox}R}{\varepsilon_{ox}} - \frac{R^2}{\varepsilon_s}\right). \quad (2)$$

It is straightforward to identify that qualitatively the slope and the nonlinearity in the V_T versus nanowire diameter (d_{NW}) dependence will correspond to N_D, while the offset (V_0) will be proportional to Q_s.

Fittings to Eq. (1) are included in Figs. 3(b) and 3(c) as solid lines. We note a good agreement between the measured data and the model at the low temperature (130 K) and for devices that have a low doping level, whereas we find a larger scattering in the data at higher temperatures and for devices that show a nonzero depletion capacitance. We attribute the capacitance minima to the trap and minority carrier responses, which become stronger with increasing temperature and higher doping levels. We note that the depletion capacitance of nanowires is affected by the stray capacitances present in the samples. When the nanowire capacitors are fully depleted, the measured depletion capacitance is corrected to zero, allowing more precise V_T evaluation. However, this correction cannot be applied when the nanowires no longer are fully depleted, but exhibit a capacitance minima, leading to an increased scattering in the data.

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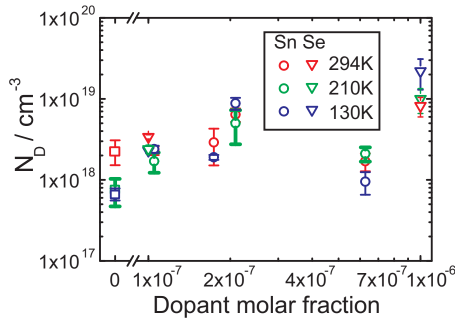

FIG. 5. (Color online) Nanowire doping concentration (N_D) vs the dopant precursor molar fraction. Errors are estimated as a 2σ deviation from the least square minima point. The nanowires grown with TESn precursor molar fraction of 6.27×10^{-7} have almost two times larger diameter than the size of the Au particle.

C. Nanowire doping

In order to determine the nanowire carrier concentration, we fit Eq. (1) to the V_T-d_{NW} plots using a least square method as shown in Fig. 3(b). A good fit is obtained for samples, exhibiting zero depletion capacitance, as discussed above. It is clear that not only the V_T is shifting with increasing precursor molar fraction, but also the slope of the fitted curves is increased as well. This indicates that higher dopant precursor molar fractions lead to higher doping levels in the nanowires. We also fit the room temperature data as shown in Fig. 3(c), where the same increase in the slope is observed. The only exception is the sample grown under the TESn precursor molar fraction of 6.27×10^{-7}. However, in this case, the large TESn precursor molar fraction also doubled the diameter of the nanowire.

Using the fitted data, we deduce the carrier concentration for all samples at three different temperatures as shown Fig. 5. The first observation is the increasing carrier concentration for higher dopant precursor molar fractions at all temperatures. Second, the carrier concentration shows little change with temperature, which is the case for semiconductors with shallow donor levels under a complete ionization. Therefore, we can conclude that Sn and Se are incorporated into InAs nanowire as donors, agreeing with results obtained using gated single nanowire structures.[15] The sample grown under TESn precursor molar fraction of 6.27×10^{-7} shows lower carrier concentration than samples grown under lower precursor flows, but this can be accounted by the doubled nanowire diameter, which effectively reduces the donor concentration.

D. Doping induced surface charges

We now analyze the shift in the nanowire CV characteristic in more detail and determine the surface charge density. We examine the offset voltage V_0, which is plotted in Fig. 6(a) as a function of dopant precursor molar fraction. Due to the increased scattering in V_T for not depleted nanowires, we focus our analysis to fully depleted nanowires. Here, we observe an increase in $|V_0|$ with higher precursor molar fraction. This indicates that the surface charge is related to the donor density where donors may incorporate at side facets of the nanowire.

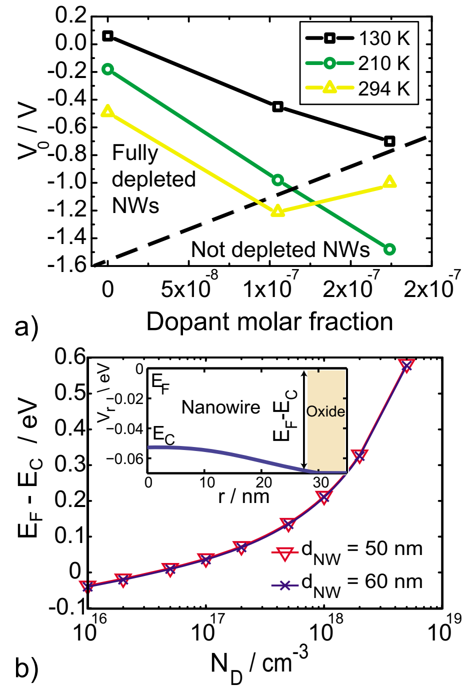

FIG. 6. (Color online) (a) Extracted offset voltage (V_0). The dashed line separates measured CV characteristics between fully and not depleted nanowires. Lines are to guide the eye. (b) The potential shift due to the state filling in the doped InAs nanowire. The inset shows a calculated nanowire band diagram for the doping density of 2×10^{17} cm^{-3}. A small band bending occurs due to the termination of the electron wave functions at the interface to the oxide, where an infinite quantum well is assumed.

We also have to take into account the strong shift in the Fermi level position as the doping level is increased in particular due to the low density of states of InAs.[16] We simulate the band diagram of the InAs nanowire using the method presented in Ref. 17, where the Fermi level position is adjusted to obtain zero net charge in the nanowire in order to simulate a flat band condition. We then deduce the difference between the Fermi level (E_F) and the conduction band edge (E_C) at the interface between InAs and HfO_2, as shown in Fig. 6(b). From the data, we note that the state filling cannot explain the observed V_0 increase by itself, because the maximum calculated E_F-E_C is less than 0.6 V, while the determined V_0 exceed 1 V. Although we do not include effects of Fermi level pinning at the interface or effects due to the nonparabolicity in the conduction band, this would only reduce the Fermi level shift. Hence our estimated Q_s values are regarded as a lower bound.

The dopant induced surface charge density is determined from the offset of the V_T-d_{NW} curve with respect to the reference sample and after subtracting the Fermi level shift due to the nanowire doping. This is calculated as: $qQ_{doping}t_{ox}/4\varepsilon_0\varepsilon_{ox}=V_0^{doped}-V_0^{ref}-[(E_F-E_C)^{doped}-(E_F-E_C)^{ref}]$ and is presented in Table I. It is clear that higher dopant precursor molar fractions cause higher surface charge densities. The temperature variation in Q_{doping} may be attributed to thermal activation of carriers from the dielectrics or the interface. The increasing surface charge density indicates that donors accumulate at the nanowire facets during the nanowire growth and that they are electrically active and contribute to the capacitive response of the nanowire. Similar doping pro-

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TABLE I. Dopant induced surface charge density (Q_{doping}).

Molar fraction/10^{-7}	T (K)	Q_{doping} (cm^{-2})
1.1 (TESn)	130	5.22×10^{12}
1.1 (TESn)	208	1.15×10^{13}
1.7 (TESn)	130	1.05×10^{13}
1.7 (TESn)	208	2.42×10^{13}

file occurs in Ge nanowires, where large nanowire tapering is clearly responsible for the donor incorporation at the surface.[5,7] The CV characteristics broaden with increasing doping level as shown in Fig. 3(a), consistent with increasing trap density at the nanowire surface. For conventional capacitors, the broadening is usually associated with an energy dependent trap distribution. However, to estimate the trap density from our narrow band gap CV profiles, a good nanowire CV model is required that accounts for the carrier distribution in the InAs nanowire capacitor including the low density of states, the reduced dimensionality in the nanowire, the minority carriers, energy dependent defect profiles, and different doping profiles.

The offset voltages, and the surface charge density, of the Se doped samples were also evaluated from the data in Fig. 3(c). Interestingly, the obtained value for the low doped sample is close to V_0^{ref} independent of temperature. This indicates that Se incorporates less effectively at the nanowire surface as compared to Sn. A careful analysis also indicates a change of sign for this sample, although within the experimental error.

III. CONCLUSIONS

We evaluated Sn and Se doped InAs nanowires using a CV technique and deduced the carrier concentration and the surface charge density using a modified radial MISFET model. We observe that nanowire carrier concentration increases with the dopant precursor molar fraction. We also observe a shift in the nanowire threshold voltage with higher dopant precursor molar fractions that we attribute to a surface charge density related to donor incorporation at the nanowire facets. We also observe that the surface charge density increases with higher dopant precursor molar fraction.

ACKNOWLEDGMENTS

This work was supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, VINNOVA, the EU-project NODE 015783 and the Knut and Alice Wallenberg Foundation. The authors would like to thank Karl-Magnus Persson for his help in sample processing and support provided by The Nanometer Structure Consortium at Lund Univeristy (nmC@LU).

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Microelectronic Engineering xxx (2010) xxx–xxx

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Temperature and frequency characterization of InAs nanowire and HfO_2 interface using capacitance–voltage method

Gvidas Astromskas *, Kristian Storm, Philippe Caroff, Magnus Borgström, Erik Lind, Lars-Erik Wernersson

Department of Solid State Physics, Lund University, Box 118 SE-22100, Sweden

ARTICLE INFO

Article history:
Available online xxxx

Keywords:
III/V
Nanowire doping
Capacitance–voltage
InAs
Vertical wrap gate

ABSTRACT

$InAs/HfO_2$ nanowire capacitors using capacitance–voltage (CV) measurements are investigated in the range of 10 kHz to 10 MHz. The capacitors are based on vertical nanowire arrays that are coated with an 8 nm-thick HfO_2 layer by atomic layer deposition. CV characteristics are measured at temperatures in the range between −140 and 40 °C and the CV characteristics for nanowires with different Sn and Se *n*-type doping levels are compared. The comparison of the data at various doping levels points towards large number of traps for highly doped samples, caused by the preferential dopant precursor incorporation at the nanowire surface. We also evaluate the frequency dispersion of the accumulation capacitance and determine values below 2% with weak temperature dependence, indicating the existence of border traps in these nanowire capacitors.

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1. Introduction

III-V MOSFETs are considered as a candidate to extend the transistor scaling roadmap. Among these, InAs vertical nanowire wrap-gate transistors including HfO_2 gate dielectrics have shown high transconductance (0.5 S/mm at $V_d = 0.5$ V), advantageous sub-threshold characteristics (<100 mV/dec) at 50 nm L_g as well as low $1/f$ noise characteristics [1,2]. The performance could be increased further by a better understanding of the oxide quality and the interface between the oxide and/or the nanowire or gate metal. However, the characterization of nanowire devices, including capacitors, is challenging due the small size and vertical device geometry. One common method is to break off the nanowires from the substrate, transfer them to another substrate and then apply standard planar device processing and characterization techniques to investigate single nanowires. Unfortunately, this approach allows characterization of only very few nanowires and also limits the measurements to low frequencies due to weak signals in single nanowire capacitors [3,4]. Therefore, we manufacture vertical nanowire capacitors containing more than 2000 nanowires per capacitor and evaluate the capacitance–voltage (CV) characteristics in a wide frequency range between 10 kHz and 10 MHz. The CV characteristics of nanowires with different doping levels are also compared, in order to study the effect of a hole inversion layer in the *n*-doped nanowires.

2. Sample fabrication

Nanowire capacitors are fabricated from InAs nanowires grown on InAs (1 1 1)B substrates. The fabrication starts by defining Au seed particles for nanowires with a density of ~1 particle/μm^2 using Electron Beam Lithography. A single layer of ZEP 520 A7 resist is exposed and developed, followed by thermal evaporation of a 15 nm-thick Au layer. After liftoff, the samples are transferred to an Aixtron AIX 200/4 low-pressure MOVPE reactor equipped with TMIn, TESn, DTBSe, and AsH_3 as precursors. InAs nanowires are grown at a temperature of 450 °C at a V/III-ratio of 68 (82 for DTBSe doped nanowires). A 5 min growth results in about 1 μm long InAs nanowires. The exact dimensions of the nanowires are measured using a scanning electron microscope. Directly after the growth, the nanowires are coated with a 8 nm-thick HfO_2 layer using atomic layer deposition (250 °C) to form the capacitor dielectric layer, which is then followed by thermal evaporation of a 100 nm-thick SiO_x spacer layer to decrease the gate to substrate parasitic capacitance, as shown in Fig. 1. A 50 nm Cr and 100 nm Au bilayer gate structure is deposited by sputtering, resulting in roughly 1/3 of the thickness on the nanowire side facets of the nanowire capacitor due to geometrical considerations. The nanowire arrays are protected with an optically exposed S1813 resist layer and the samples are wet etched to remove the unprotected Cr:Au layer. The samples are then spin-coated with a 3 μm thick S1818 resist and the nanowire arrays are made accessible by means of optical lithography. The slope in the resist profile of S1818 allows connecting the elevated gate pad to the nanowire capacitor array, as shown in Fig. 1. The device preparation is then finished by a 500 nm

* Corresponding author.
E-mail address: gvidas.astromskas@ftf.lth.se (G. Astromskas).

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doi:10.1016/j.mee.2010.08.010

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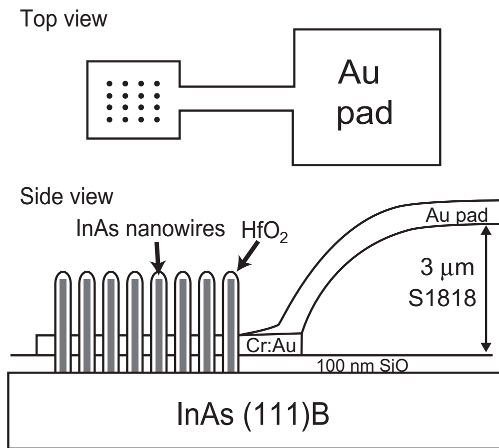

Fig. 1. Schematic of a vertical nanowire capacitor.

sputtered Au gate pad defined by optical lithography and wet etching. The fabricated samples contained capacitor arrays with nominally 79 (not intentionally doped (NID) and Sn doped nanowires) and 2500 (Se doped nanowires) nanowires per array. Also, capacitors without nanowires were fabricated in order to evaluate the level of the parasitic pad capacitance.

The fabricated capacitors were characterized with an Agilent 4294A impedance analyzer in a Cascade probe station, equipped with a temperature control unit. The measurements were performed with two probes of which one was placed on the nanowire gate pad and the other on a large (1–50 nF) frame capacitor in series with the nanowire capacitor. The complex impedance was measured in the range of 10 kHz to 10 MHz using a small AC modulation $\Delta V = 40$ mV on top of a DC bias V in the range from -3 to +2 V. The capacitance was extracted from the measured impedance using a capacitance in series to resistance model, as DC leakage currents less than 1 pA were measured. The typical capacitances were 0.7 and 5 pF for the Sn and Se doped nanowire capacitors, respectively while the parasitic plate capacitance was about 0.5 pF.

3. Results

The CV characteristics for the nominally undoped nanowire capacitor show a typical MOS capacitor behavior as shown in Fig. 2. Both accumulation and depletion regions are observed, although the accumulation capacitance does no saturate due to the low electron effective mass in InAs [5,6]. The low density of states also lowers the magnitude of the accumulation capacitance below the geometrical limit [7]. We note that the leakage current density for nanowire capacitors is below 1×10^{-5} A/cm^2, while the breakdown voltage is around 4 V. The measurement frequency affects the nanowire CV characteristics by modulating both the depletion and accumulation capacitances, especially at higher temperatures as shown in Fig. 2b. An increase in depletion capacitance at lower measurement frequencies and a non zero capacitance minima at room temperature are characteristic signs of defect response. The response is not observed at 130 K as nanowires are depleted of majority carriers.

In Fig. 3, we compare CV profiles for two samples with the same geometry, but with different doping levels (4×10^{18} and 1×10^{19} cm^{-3} for samples grown under DTBSe molar fractions of 1×10^{-7} and 10×10^{-7}, respectively). The lower doped sample in Fig. 3a shows the same shape in the CV curve as the reference sample in Fig. 2b, with a clear modulation of the capacitance with voltage. However, the heavily doped sample in Fig. 3b no longer fully depletes at negative biases, only an increase in depletion capacitance is observed. Also, the accumulation capacitance of the highly doped sample is lower as compared to the low doped sample. This indicates a high density of interface traps in the highly doped sample, limiting the ability to modulate the Fermi level at the interface. This agrees with our previous finding that high dopant flow results in a trap accumulation at the nanowire surface [8].

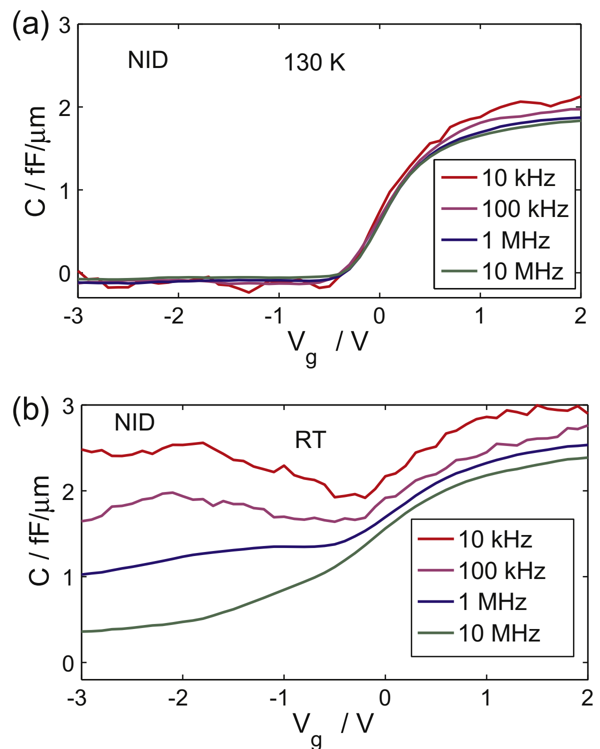

Fig. 2. CV characteristics of a nanowire capacitor at different frequencies measured at (a) 130 K (b) 294 K.

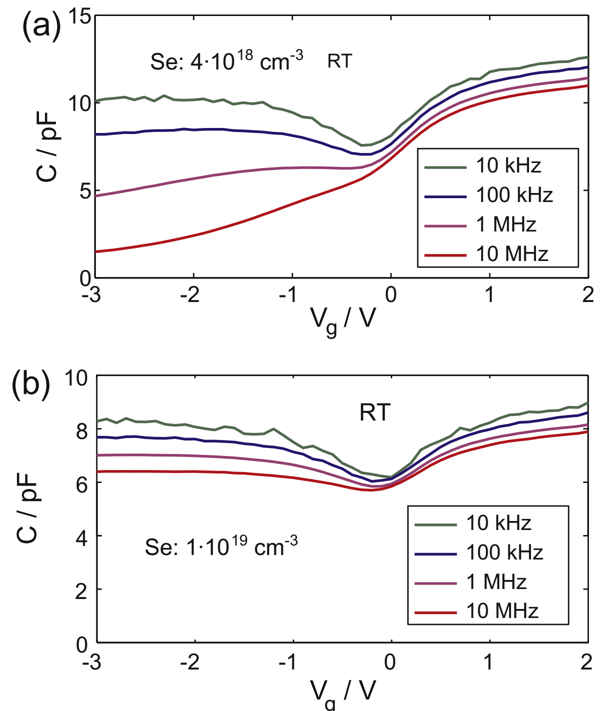

Fig. 3. Room temperature CV characteristics of samples grown under DTBSe molar fractions of (a) 1×10^{-7} (low doped) and (b) 10×10^{-7} (highly doped).

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We further analyzed the frequency dependence in the accumulation capacitance, as shown in Fig. 4a. As noted before, the accumulation capacitance increases with increasing temperature, but the slopes of the capacitance–frequency curves change little with temperature. We also observe the same effect for doped nanowires as shown in Fig. 4b (Se doped sample). As the capacitors in this sample contain more nanowires, the noise level is considerably reduced, revealing the weak variation in the slope with temperature.

The measured temperature dependence in the frequency dispersion per decade is shown in Fig. 5, where we compare samples with different doping levels (various dopant precursor types as well as different dopant molar fractions). The frequency dispersion of accumulation capacitance is defined as $(C_{10\,kHz} - C_{1\,MHz})/C_{1\,MHz}\cdot 100$ at +2 V. The obtained values vary between 2 and 7% for nanowire capacitors, which are comparable to frequency dispersions measured for planar reference samples with (1 1 1)B InAs/HfO_2/Au capacitors formed by the same HfO_2 deposition conditions. We observe no clear correlation between the frequency dispersion and the nanowire doping level, which could be expected as it is known that a large fraction of the dopants are incorporated at the nanowire surface [8–10]. Instead, we conclude that the quality of the HfO_2 layer determines the frequency dispersion in these nanowire capacitors. We further attribute the variation in frequency dispersion with temperature to the noise in the measured capacitance, which increases at lower frequencies as seen in Fig. 4a. Moreover, we compare the frequency dispersion versus nanowire diameter for the sample with DTBSe molar fraction of 10×10^{-7} in Fig. 5b and observe no significant correlation. Our data suggest a weak temperature variation in the accumulation capacitance that hints towards tunneling of carriers into border traps in the oxide [11,12]. Since a similar variation is present in reference and doped samples, it suggests that the variation in the accumulation capacitance is related to the HfO_2 layer, rather than the nanowire itself.

In summary, we have characterized the frequency dependent CV characteristics for InAs/HfO_2 nanowire capacitors. We show that nanowire capacitors with larger dopant concentration exhibit CV profiles which are characteristics for interfaces with large quantity of interface traps. The frequency dispersion of nanowire accumulation capacitance is measured to be as low as 2%. It exhibits a weak temperature dependence, indicating the presence of border traps inside the oxide layer.

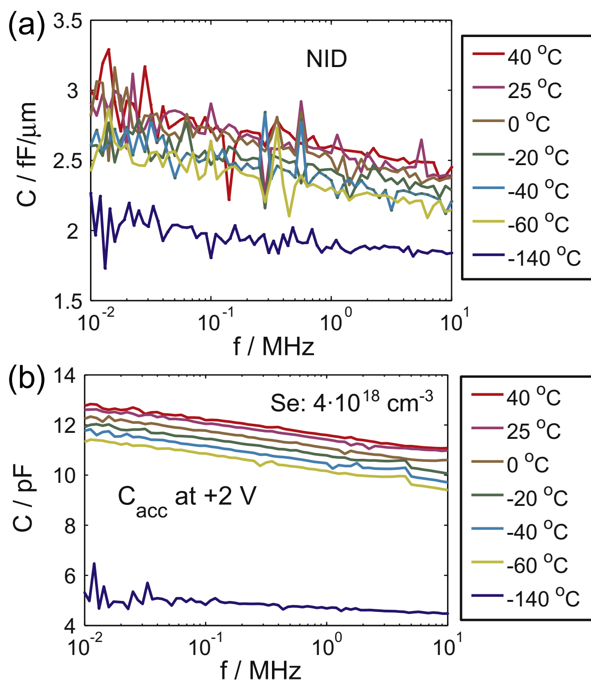

Fig. 4. Accumulation capacitance comparison versus frequency at different temperatures (a) NID sample. (b) Doped sample grown under DTBSe molar fraction of 10^{-7}.

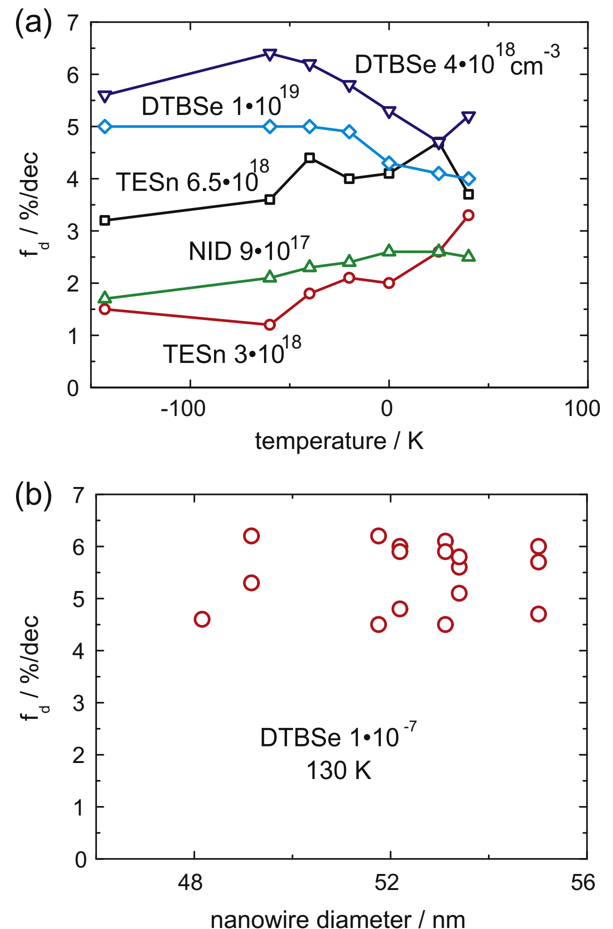

Fig. 5. Frequency dispersion per decade (f_d) versus (a) temperature (b) nanowire diameter. Samples grown under DTBSe molar fractions of 1×10^{-7} and 10×10^{-7} have *n*-type doping levels of 4×10^{18} and 1×10^{19} cm^{-3}, respectively. The TESn molar fractions of 1.7×10^{-7} and 2.1×10^{-7} correspond to *n*-type doping concentrations of 3×10^{18} and 6.5×10^{18} cm^{-3}, respectively.

Acknowledgement

This work was supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, VINNOVA, the EU-project NODE 015783 and the Knut and Alice Wallenberg Foundation. The authors would like to thank Karl-Magnus Persson for his help in sample processing.

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Transient studies on InAs/HfO_2 Nanowire Capacitors

Gvidas Astromskas[1], *Kristian Storm*[1],

Lars-Erik Wernersson[2]

[1]Solid State Physics/Nanometer Structure Consortium

[2] Electrical- and Information Technologies

Lund University,

Box 118 SE-22100, Sweden

Evaluation of single-shot transients and deep-level transient spectroscopy (DLTS) are used to investigate characteristic times and origin of transients and hysteresis in n-doped InAs nanowire/HfO_2 capacitors. Capacitance transients with characteristic time scale in the order of 100 µs are measured that are attributed to emission from electron traps. The trap energy is determined to be in the range from 0.12 eV to 0.17 eV. The capture cross-sections are determined to be about $1.7 \cdot 10^{-17}$ cm^{-2}. During filling, the measured capture time is below 100 ns with no sign of capture barrier. Under the reverse bias, that is when minority carriers may be collected at the interface, the transients show a reduced emission rate indicating a more complex carrier dynamics. These traps are believed to be located in the oxide film.

The introduction of high-k dielectric layers on III-V semiconductors offers great promise for the realization of high performance III-V MOSFETs. For instance, planar devices with a transconductance of 0.45 S/mm and a subthreshold slope of 280 mV/dec have been demonstrated [1] and nanowire devices with wrap-gates showing a normalized transconductance of 0.44 S/mm and a subthreshold slope of 100 mV/dec have been reported [2]. However, several aspects of the high-k integration are still critical and need further studies. These include the detailed understanding and control of the defect states in the oxide [3], the accurate determination of the interface state density [4] as well as the noise properties in III-V MOSFETs [5].

In this paper, we perform a detailed study of capacitance transients in InAs/HfO_2 nanowire-based capacitors. We use both real-time measurements, so called single-shot transients, and deep-level transient spectroscopy (DLTS) to measure and evaluate the dynamic behavior in the capacitors. The bias conditions under which detailed studies may be reliably performed are identified and the capture cross-section as well as the activation energy is determined. It is shown that these transients may be attributed to defects within the dielectric film rather than interface states.

The nanowire capacitor fabrication starts by defining Au seed particles with a density of 1 particle/μm^2 using Electron Beam Lithography on S-doped n-type (3×10^{18} cm^{-3}) (111)B InAs substrates. After Au liftoff, the samples are transferred to an Aixtron AIX 200/4 low-pressure metal organic vapor phase (MOVPE) reactor equipped with TMIn, TESn, DTBSe, and AsH_3 precursors. InAs nanowire growth is performed at 450°C using trimethylindium and arsine as primary precursors at a V/III-ratio of 68. While the full study included both Sn- and Se doped samples where the dopant precursor molar fractions were varied between 1×10^{-7} and 10×10^{-7} [6], the main focus in this article is related to Se-doped n-type capacitors doped with DTBSe (molar fraction of 1×10^{-7}). Similar capacitance transient characteristics are demonstrated by all doped as well as non-intentionally doped samples.

Nanowire capacitors are made by depositing a 10-nm-thick HfO_2 layer on the grown nanowires at 250°C by atomic layer deposition, followed by deposition of a 100-nm-thick thermally evaporated planar SiO_x-layer. A first Cr/Au gate layer of thickness 15 nm/50 nm is defined by sputtering. Due to

the geometry of the nanowires, about 1/3 the material is deposited on the vertical NW facets as compared to the horizontally oriented substrate. By optical lithography and wet etching in KI and HCl, the thin metal layer is removed outside a small area enclosing the NW array. In order to enlarge the contact area to access the capacitors by macroscopic probes or bonding, large bond pads are defined on top of a 3 μm-thick S1818 resist by sputtering 15 nm Cr and 500 nm Au followed by optical lithography and wet etching, as shown in Figure 1. This layer also reduces the parasitic pad-to-substrate capacitance. The fabricated capacitors were evaluated using a Semilab DLS-83D deep level spectrometer. The measurements are done with two probes of which one was placed on the nanowire gate pad and the other on a large (1-50 nF) frame capacitor in series with the nanowire capacitor.

The nanowire CV characteristics at 1 MHz are shown in Figure 1b, where measurements at different temperatures reveal a change in both CV profile and a degree of hysteresis. The depletion capacitance (defined at V_g< -0.5 to 0 V, depending on temperature) as well as the accumulation capacitance increase with temperature. However, the hysteresis of the CV sweep becomes smaller, diminishing above room temperature. In a previous study, we have measured the frequency dispersion of the CV characteristics in order to evaluate the interface state density [7]. However, an unambiguous determination of the contribution from the minority carriers and the interface states could not be made from the frequency dependence, as the common methods like the Terman and the high-low frequency methods are troublesome due to the influence of the state filling in the accumulation capacitance [4]. Nevertheless, the data in Figure 1b shows evidence of a strong response from minority carriers and/or interface states in the depletion regime. From CV measurements at 77K we know that these states respond at frequencies up to 10 MHz.

In order to evaluate the characteristic response time related to the hysteresis, we apply a pulse train to the gate electrode and evaluate the resulting capacitance transients. Figure 2a shows representative capacitance transients of the nanowire capacitor for various depletion voltages (V_{dep}), measured in a time window of about 300 μs. The filling pulse voltage is +2V in all cases. The first observation is that the capacitance increases after the positive gate pulse have been applied, indicating emission of

electrons as the main source for the transients in this time window. The amplitude of these transients are typically on the order of 10% ($\Delta C/C=0.12$) and we may thus assume that the surface potential essentially remains constant during the emission. Besides, there is a notable change in the characteristic time constant in the transients at the various bias conditions ranging from 88 μs to 102 μs. Measurements over longer time windows (not shown) indicate the presence of further transients with characteristic time constants between 10^{-3} and 10^{2} s.

A second observation is that the amplitude of the transient signal is the strongest at about V_{dep} = -0.9 V, while it diminishes both above and below this bias. This behavior is likely a combination of dynamic processes in the oxide combined with depletion of carriers in the nanowire. As the depletion region in the nanowire increases at large reverse biases, the hysteresis in the CV characteristics decreases, as is shown in Figure 1b, thus no transient signal is observed below -1.5 V.

Figure 2b shows DLTS spectra measured at two different bias conditions. The measured DLTS spectra show the expected frequency dependence. The rather broad peaks may be attributed to surface fluctuations, nevertheless DLTS analysis is still applicable [11]. Generally, a DLTS spectrum contains information about both capture and emission processes that are related via the detailed balance equation, therefore it is essential to study the capture initially. Figure 3a shows measurements of the amplitude of the DLTS signal as a function of the filling pulse time. The data shows a small increase in DLTS amplitude for all rate windows, indicating an almost saturated capture process. The fast capture (below 100 ns) and the weak temperature dependence demonstrate a vanishing capture barrier and that the potential remains constant during the capture process, in contrast to other complex systems like capture into point defects associated with dislocations [8] and embedded particles [9]. The DLTS analysis of interface states is more complicated than for bulk traps as the surface potential may change during the emission and that different fractions of the distribution of interface states may contribute at various temperatures and frequencies [10]. Besides, the transients may not be single exponential. These problems are usually circumvented by the use of small bias changes to allow response of only a limited part of the interface state distribution [11]. We therefore focus the analysis for the bias conditions of

V_g>0 V, where Fermi level is still above the midgap. A large 2 V filling pulse is used to ensure that an accumulation region is created at the oxide/nanowire interface, as the nanowire capacitance does not saturate at accumulation due to the non-parabolic conduction band in InAs [12].

At gate voltages above zero, the Fermi level is still in the upper part of the band gap, as can be seen in the CV curves presented in Figure 1b. The corresponding Arrhenius plots of the measured temperature dependence of the emission rates are shown in Figure 3b and we deduce values for the activation energies and capture cross-sections to be E_a=0.12 V and $\sigma_p=1.9\cdot10^{-17}$ cm^{-3} at V_{dep}=0.4 V and E_a=0.17 V and $\sigma_p=1.7\cdot10^{-17}$ cm^{-3} at V_{dep}=0.1 V using the standard expression for the emission time constant: $e_n = \sigma_p v_t N_c \exp\left(-E_a/kT\right)$. The low values of the capture cross-section are an indication that the traps are located in the oxide as compared to the oxide-semiconductor interface.

Figure 3b also shows the Arrhenius analysis of emission rates measured at reverse bias. Interestingly, the measured emission rate decreases as more negative bias is applied for all bias conditions studied. This is also true for the single-shot transients presented in Figure 2a, where the time constants agree well with the values measured by DLTS ($1/e_n$=398 μs from DLTS and $1/e_n$=367 μs from single-shot transients at V_{dep}=+0.1V, both measured at 167 K). A similar agreement is observed for reverse bias measurements, indicating that transients remain single exponential. The voltage dependence is surprising as normally the emission rate is increased with the electric field due to the Poole-Frenkel effect, although similar effects have been observed in studies of DX-centers in AlGaAs [13]. The slower emission results in an apparent increase in the activation energy and also an increase in capture cross-section. However, we argue that the values deduced are less reliable, as the CV curves in Figure 1b show substantial response from minority carriers/interface states at negative gate voltages. The narrow band gap of InAs implies a higher minority carrier density at the MOS interface and in particular at reverse bias these may influence the carrier dynamics in the system and a more advanced model may be needed to fully interpret the data. The fact that the activation energies deduced widely exceed the value

of the InAs band gap (E_g=0.54 eV for wurtzite InAs, found in nanowires [14]) is also an indication that the transients studied are related to dynamic processes in the HfO_2 dielectric film.

In summary, we have investigated the hysteresis and the transient behavior of InAs nanowire capacitors by measuring capacitance transients. Emission transients with a characteristic time scale of 100 μs are measured, indicating the presence of electron traps. The trap energy is determined using DLTS measurements and is found to be about at least 0.12 eV. The smallest capture cross-sections are determined to be $1.7\cdot10^{-17}$ cm^{-3}. Analysis of the data measured at negative voltages demonstrates a reduced emission rate and provides activations energies that exceed the band gap of InAs, which indicates that the traps are located within the oxide and that a more advanced model is required to fully interpret the data under those bias conditions.

ACKNOWLEDGEMENT

This work was supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, VINNOVA, the Knut and Alice Wallenberg Foundation and the Nanometer Structure Consortium at Lund University (nmC@LU). The authors would like to thank Magnus Borgström and Karl-Magnus Persson for their help in sample growth and processing.

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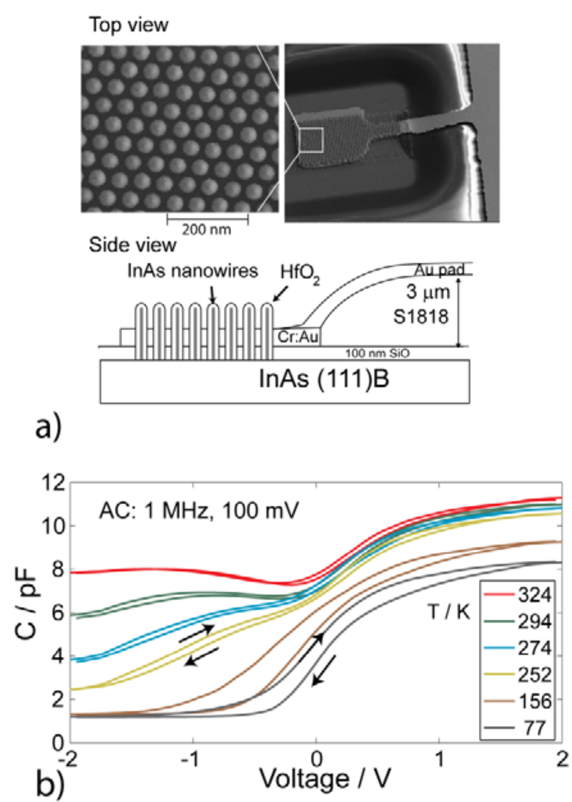


Figure 1. a) SEM image and schematic of the nanowire capacitor b) Nanowire CV hysteresis at different temperatures. Arrows mark the direction of the CV sweep.

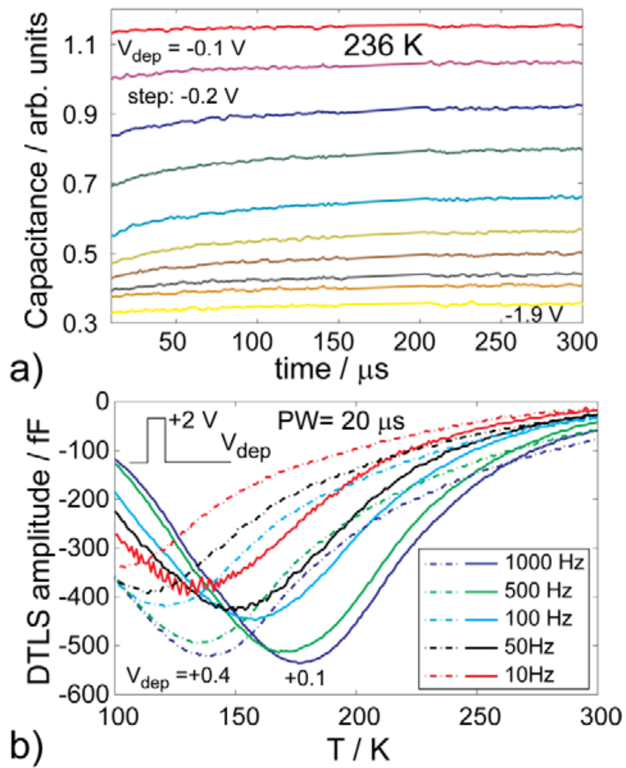
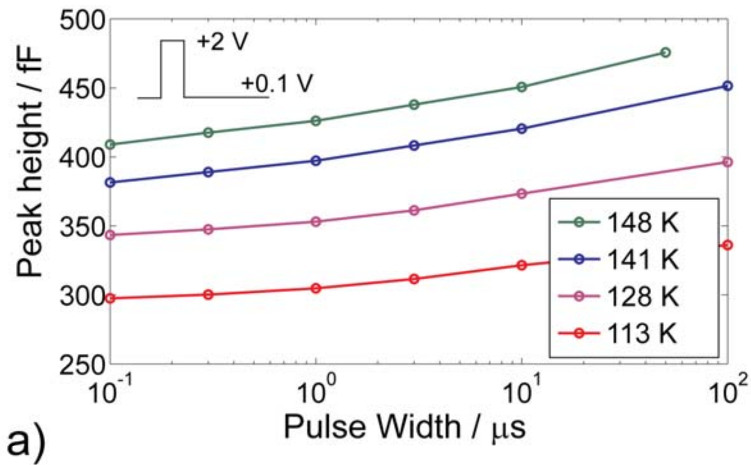


Figure 2. a) Capacitance transients and b) DLTS temperature spectra measured at different depletion voltages. The filling pulse width is 20 μs and the amplitude is +2 V.



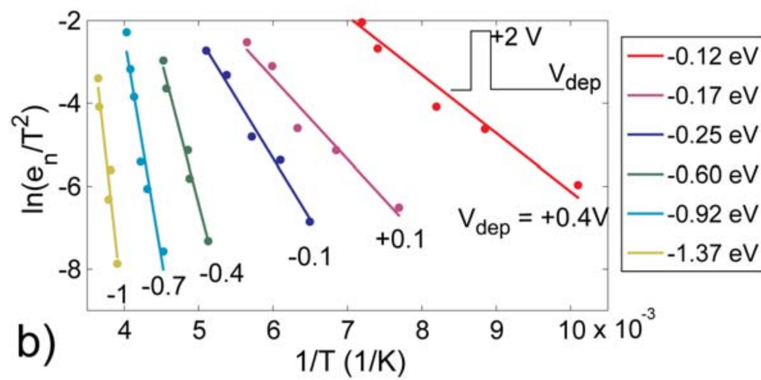


Figure 3. a) DLTS signal peak height vs the filling pulse width b) Arrhenius plot at different depletion biases, with indicated extracted energy levels.

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Analysing the capacitance–voltage measurements of vertical wrapped-gated nanowires

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Nanotechnology 19 (2008) 435201 (6pp) doi:10.1088/0957-4484/19/43/435201

Analysing the capacitance–voltage measurements of vertical wrapped-gated nanowires

O Karlström[1], A Wacker[1], K Nilsson[2], G Astromskas[2], S Roddaro[2], L Samuelson[2] and L-E Wernersson[2]

[1] Mathematical Physics, Lund University, Box 118, 22100 Lund, Sweden
[2] Solid State Physics, Lund University, Box 118, 22100 Lund, Sweden

E-mail: Andreas.Wacker@fysik.lu.se

Received 18 June 2008, in final form 20 August 2008
Published 22 September 2008
Online at stacks.iop.org/Nano/19/435201

Abstract
The capacitance of arrays of vertical wrapped-gate InAs nanowires is analysed. With the help of a Poisson–Schrödinger solver, information about the doping density can be obtained directly. Further features in the measured capacitance–voltage characteristics can be attributed to the presence of surface states as well as the coexistence of electrons and holes in the wire. For both scenarios, quantitative estimates are provided. It is furthermore shown that the difference between the actual capacitance and the geometrical limit is quite large, and depends strongly on the nanowire material.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Great efforts are currently being made to develop new schemes for the manufacturing of nanowire (NW) devices [1]. For example, recent progress in vertically processed semiconductor NWs with a cylindrically symmetric gate electrode, such as the wrapped insulator-gate field effect transistor [2], have shown great promise for application in future highly scaled electronic devices. Besides the possibility of incorporating wrapped gates for improved gate control, NWs offer other intriguing possibilities not easily accessible to planar designs, such as an inherent one-dimensionality as well as relaxed constraints in terms of combining highly lattice-mismatched materials along the NW channel due to radial relaxation of interface strain [3, 4].

In order to facilitate the development of high performance NW electronic devices, it is important to accurately characterize the doping profile and interface properties of the system as well as further fundamental material parameters. Si-based metal–oxide–semiconductor (MOS) stacks have long benefited from well developed capacitance–voltage (CV) measurement schemes for device characterization. However, similar methods have so far been largely unavailable for NW devices. Recently, CV characteristics of individual Ge NWs on SiO_2/Si substrates were measured [5]. Here we are focusing on vertical wrapped-gate NWs for which we have earlier demonstrated a scalable processing protocol for routine CV spectroscopy [6]. An overview of the device structure considered here is given in figure 1. The device consists of an 11×11 array of InAs NWs, covered with a 10 nm conformal HfO_2 dielectric layer and a top Cr/Au metallization as one of the capacitor electrodes. The capacitance is measured between this gate electrode and the core of the wire, which is connected via the substrate. Details of the fabrication protocol and measurement techniques can be found elsewhere [6]. In this paper we further develop the quantitative as well as qualitative understanding of these measurements, and also discuss various features of the CV characteristics in detail.

2. The model

The nanowires are modelled as cylinders in which the radius of the InAs will be referred to as R_{nw}, whereas R_{gate} is the radius of the InAs and HfO_2 together. Typical values are length $h = 680$ nm, and radial dimensions $R_{nw} = 27$ nm, $R_{gate} = 37$ nm.

We assume that the unintentional doping of the NWs is of n-type. By changing the applied gate voltage, V_{gate}, the charge within the NW, Q, can be affected. This defines the

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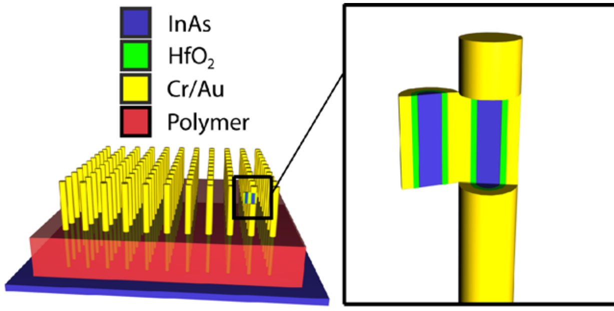

Figure 1. Illustration of the array of NWs. Each NW consists of an InAs core surrounded by a dielectric layer of HfO_2 and a Cr/Au gate. The lifting layer of polymer is inserted to reduce the capacitance between the gate and the substrate.

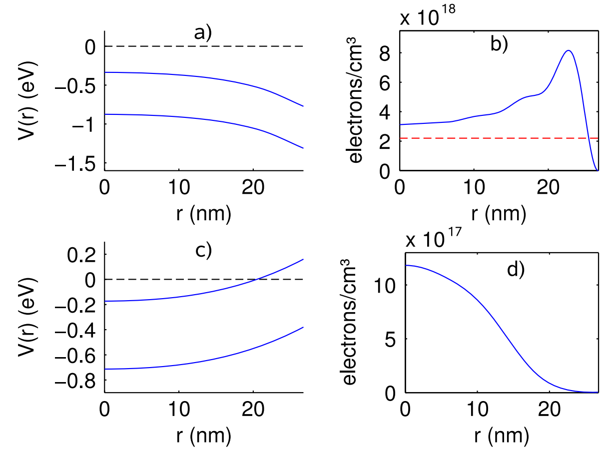

Figure 2. (a) Potential $V(r) = -e\phi(r)$ and valence band edge $V(r) - E_g$ for $\phi_0(R_{gate}) = 1.08$ V, corresponding to the operation point 1 of figure 3. The dashed line depicts E_F of the wire, which is set to zero as reference. (b) Corresponding electron distribution $n_e(r)$. (c) and (d) are the same plots for $\phi_0(R_{gate}) = -0.46$ V (operation point 2). Parameters: $N_D = 2.2 \times 10^{18}$ cm^{-3} (dashed line in (b)), $R_{nw} = 27$ nm.

capacitance:

$$C = \frac{dQ}{dV_{gate}}. \quad (1)$$

The total charge Q is the spatial integral over the charge distribution $\rho(r)$ containing three components $\rho = e(N_D - n_e + n_h)$ inside the InAs nanowire. Here, e is the positive elementary charge and N_D, n_e and n_h are the concentrations of ionized donors, electrons, and holes, respectively. The donors are assumed to be entirely ionized at room temperature, as considered throughout this paper. All concentrations are assumed to depend only on the radial distance r from the centre of the NW. This greatly facilitates the calculations as it reduces the problem to one dimension. Working with homogeneous doping profiles is motivated by averaging over arrays of long wires. However, microscopic fluctuations are neglected by this approach.

The effective density-of-state masses for electrons and holes in InAs are $m_e^* = 0.023m_e$ and $m_h^* = 0.41m_e$, respectively [7, 8]. Non-parabolicity effects are neglected, albeit they can cause some quantitative deviations for large positive biases. For the determination of hole concentrations, we use the bandgap $E_g = 0.54$ eV for InAs NWs with wurtzite structure [9]. The relative dielectric constant is $\varepsilon \approx 15$ both for the InAs NW and the HfO_2 insulator [8, 10, 11].

To calculate the capacitance, a Poisson–Schrödinger solver was implemented similar to the one demonstrated in [12, 13]. For a given charge distribution $\rho(r)$, the cylindrical geometry permits the use of Gauss's law to solve Poisson's equation for the electrostatic potential $\phi(r)$. Thus, we obtain the Hamiltonian

$$H = -\frac{\hbar^2}{2}\frac{1}{m_e^*}\nabla^2 - e\phi(r) \quad (2)$$

together with the boundary condition for the wavefunction $\Psi(R_{nw}) = 0$, assuming that the HfO_2 layer constitutes an infinite barrier. Due to the cylindrical symmetry of the problem, Bessel functions were used as a basis set for the diagonalization of equation (2), resulting in the wavefunctions $\Psi_{\nu j}(r, \varphi)$ and corresponding energies $E_{\nu j}$. Here ν and j are the angular and radial quantum numbers, respectively. The relatively long length of the wires compared to their radial dimensions justifies the use of a 1D density of states along the z-direction, $g(E_z)$. Using Fermi–Dirac statistics the electron concentration is then given by

$$n_e(r) = \sum_{\nu j} |\Psi_{\nu j}(r)|^2 \int_0^\infty \frac{g(E_z)\, dE_z}{\exp((E_z + E_{\nu j})/kT) + 1}. \quad (3)$$

Here the electrochemical potential E_F was set to zero in the wire, which is used as a reference point throughout this paper. Together with the similarly calculated hole concentration n_h, this provides a new charge distribution $\rho(r)$. By iterative solution of the Poisson–Schrödinger equation, a self-consistent solution is obtained.

In figure 2, calculated potentials and electron distributions are shown. Figures 2(a) and (b) correspond to a positive electrical potential at the gate electrode. The corresponding bending of the conduction band edge causes electrons to accumulate close to the semiconductor–oxide interface (accumulation mode). Figures 2(c) and (d) correspond to a negative electrical potential at the gate electrode. Here the electrons are depleted close to the surface of the wire (depletion mode).

In the simulation we assume that the insulating oxide layer is neutral of charge and use the corresponding electric potential $\phi_0(R_{gate})$ at the gate as a parameter. However, trapped charges are likely to occur both at the surface of the wire and within the oxide [14]. If an areal charge density σ is present at position R_{trap}, the potential for $r \geqslant R_{trap}$ is modified according to

$$\phi(r) = \phi_0(r) - \frac{\sigma R_{trap}}{\varepsilon\varepsilon_0} \ln\left(\frac{r}{R_{trap}}\right), \quad (4)$$

while $\phi(r)$ is not affected for $r < R_{trap}$. Experimentally, one measures the applied gate voltage V_{gate} which is related to the

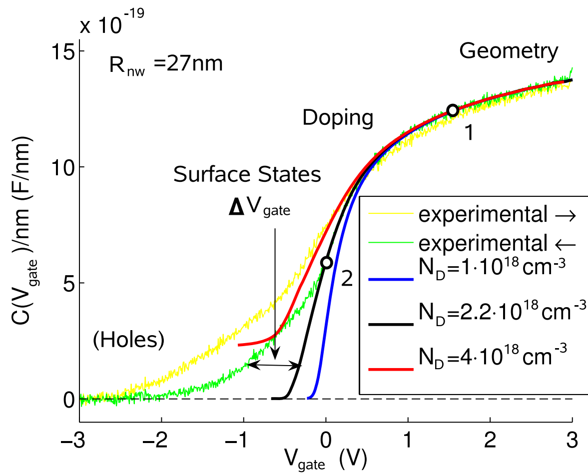

Figure 3. Experimentally measured capacitance and theoretical fits for a mean wire radius $R_{nw} = 27$ nm. The green curve shows the measured capacitance when sweeping from positive to negative bias, while the yellow curve is for the opposite sweep direction. The gate–substrate capacitance, which is independent of bias, has been subtracted.

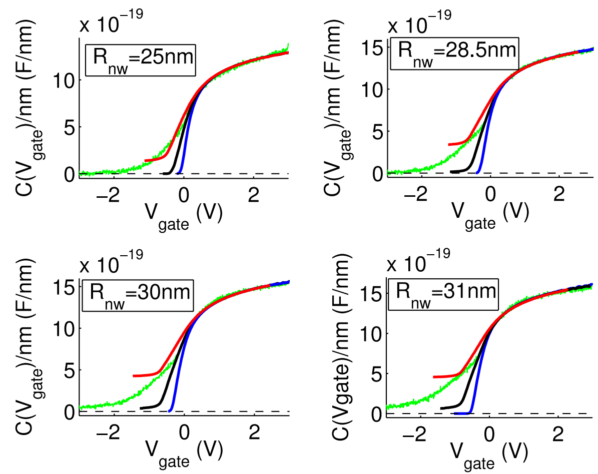

Figure 4. Experimentally measured down-sweep capacitance (green) and simulation results for different NW radii R_{nw}. The doping densities for the different simulations are identical to figure 3.

actual electric potential at the gate via

$$V_{gate} = \phi(R_{gate}) + \frac{W_{Cr} - \chi_{InAsNW}}{e}. \tag{5}$$

Here W_{Cr} is the work function of Cr and χ_{InAsNW} the electron affinity of the InAs in the nanowire. As long as the trapped charges are unchanged they provide a constant bias offset

$$V_{gate} = \phi_0(R_{gate}) + V_0 \tag{6}$$

between the measured bias and the parameter $\phi_0(R_{gate})$ used in the simulation. As both the magnitude of the trapped charges and the electron affinity of InAs in the wurtzite modification appearing in the nanowire are not *a priori* known, we use V_0 as a fit parameter in the subsequent data analysis.

3. Understanding the experimental data

In figure 3, the experimentally measured capacitance for the device with mean radius 27 nm is shown together with our calculations for different doping densities. The main trend is the increase of capacitance with bias. This can be attributed to the location of charges inside the NW. From Gauss's law it follows that the change in Q induced by a change in bias will be larger if $\rho(r)$ is affected at large values of r. As can be seen in figure 2(b) (corresponding to the operation point 1 in figure 3), the charges are mainly located close to the NW surface in the accumulation region. In contrast, they are close to the centre of the wire at operation point 2; see figure 2(d). This explains why the capacitance is higher at point 1 than at point 2.

The measurements reported here are performed by adding a small AC signal with a frequency of 20 MHz atop the DC gate bias. The impedance is found to be almost completely imaginary, showing a negligible influence of any series resistance to the accumulation capacitance. For positive bias the measured capacitance shows less than 10% frequency dispersion between 50 kHz and 100 MHz, demonstrating good properties of the MOS structure and that a reliable quantitative data analysis can be performed for $V_{gate} > 0$. In contrast, for $V_{gate} < 0$ the frequency dispersion is more pronounced, which we attribute to the presence of surface states; see section 3.3.

The calculations provide a capacitance per wire length, as given in figure 3. For the experimentally measured capacitance C, the gate–substrate capacitance, which is independent of bias, see [6], has been subtracted, and the result has been divided by an effective length L, which has been taken as a second fit parameter in addition to V_0. The data shown assume an effective length corresponding to an effective number of 90 wires with the nominal length of 680 nm. This has to be compared with a total of 121 wires in the fabricated array. The difference can be attributed to the lack of electrical connection of some wires and/or variations from the nominal length.

Each fabricated array showed a certain distribution of radii R_{nw} [6]. To accommodate for this, an ensemble of three different values of R_{nw} was used in the simulation for each device, while the oxide thickness of 10 nm was held constant. The calculated curves in figures 3 and 4 are the results from such ensembles with appropriate weights for each radius reflecting the measured radius distribution[3].

In figure 3 it is indicated that different factors, such as geometry, doping, surface states, and inversion (holes), affect the capacitance at different gate voltages. We will in turn explain the contribution from each factor. Measurements indicate that the down-sweep curve (green curve) is closer to equilibrium as time-dependent sweeps are more stable and the up-sweep (yellow curve) relaxes towards the down-sweep curve. Therefore, all fits of our stationary model are made to the down-sweep curve.

[3] We used $R_{nw} = 25$ nm: 0.5×25 nm $+ 0.3 \times 27.5$ nm $+ 0.2 \times 22$ nm. $R_{nw} = 27$ nm: 0.4×26 nm $+ 0.45 \times 28.5$ nm $+ 0.15 \times 24$ nm. $R_{nw} = 28.5$ nm: 0.4×27.5 nm $+ 0.45 \times 31$ nm $+ 0.15 \times 25$ nm. $R_{nw} = 30$ nm: 0.4×30 nm $+ 0.4 \times 32$ nm $+ 0.2 \times 27.5$ nm. $R_{nw} = 31$ nm: 0.35×30 nm $+ 0.5 \times 32.5$ nm $+ 0.15 \times 28$ nm.

Table 1. Effective number of wires and bias offset V_0 resulting in a best fit of the capacitance–bias characteristics for different arrays of NWs and different assumed doping densities.

		Offset V_0 (V)		
R_{nw} (nm)	No. of wires	$N_D = 10^{18}$ cm^{-3}	$N_D = 2.2 \times 10^{18}$ cm^{-3}	$N_D = 4 \times 10^{18}$ cm^{-3}
25	71	0.27	0.42	0.63
27	90	0.26	0.39	0.60
28.5	86	0.13	0.32	0.53
30	90	0.12	0.28	0.51
31	84	−0.05	0.14	0.38

3.1. Geometry

According to figure 3 the capacitance is independent of the donor concentration in the accumulation mode, but rather depends on the geometry of the wire. The reason is that during accumulation electrons are added close to the semiconductor–oxide interface; see figure 2(b). Thus different doping concentrations result in the same capacitance. The capacitance in this region can therefore not be used to determine the doping concentration. Fitting to the experimental data instead determines the effective length of the wires.

In figure 4, the capacitance (experimental down-sweep) for NWs with different radii R_{nw} are shown. All fabricated arrays have 121 NWs, and the effective number of wires used for fitting L is displayed in table 1. As a general trend, the capacitance increases with the radius R_{nw} as there is a larger surface area of the NWs. Note that the capacitance in the accumulation region is significantly lower than the geometrical capacitance $C/L = 2\pi\epsilon\epsilon_0/\ln(R_{gate}/R_{nw})$, which is 2.48×10^{-18} F nm^{-1} for $R_{nw} = 25$ nm and $R_{gate} = 35$ nm. This deviation is strongly dependent on the density of states for the nanowire wire material; see section 4.

3.2. Doping

As the bias is lowered, the electrons will be depleted in the NW. A large doping concentration provides a positive background charge with a strong attraction for the electrons, requiring a higher negative gate voltage to deplete all the electrons. Thus, the doping concentration strongly affects the slope of the capacitance curve around $V_{gate} = 0$ V. Comparison between fits and experimental data shows that $N_D = 4 \times 10^{18}$ cm^{-3} is too flat while $N_D = 1 \times 10^{18}$ cm^{-3} is too steep. The doping of $N_D = 2.2 \times 10^{18}$ cm^{-3} fits very well up to the 'kink' at point 2 of the experimental down-sweep curve in figure 3. This also holds for all devices shown in figure 4. As all devices were manufactured using the same method, this provides a consistent estimate of 2.2×10^{18} cm^{-3} for the doping density.

3.3. Surface states

The experimental curves exhibit a 'kink' at point 2 of figure 3, which is most clearly seen for the down-sweep curve. For biases below the kink the measured capacitance is significantly larger than the simulation result. In this section we attribute this to the emptying of surface states, situated at the semiconductor–oxide interface.

The surface states are assumed to be located in the forbidden gap [15], and are treated as donors [16]. As the states are located in the bandgap, they remain filled as long as E_F is in the conduction band. Theoretical evaluation of the potential at R_{nw}, for the doping of $N_D = 2.2 \times 10^{18}$ cm^{-3}, shows that E_F is 0.1–0.2 eV below the conduction band edge at the kink; see figure 2(c). This makes it feasible that the kink is an effect of such surface states. For gate voltages more negative than the one corresponding to the kink, surface states are emptied, which produces the discrepancy between simulations and experiment.

While conduction band electrons as majority carriers can almost adiabatically follow the AC signal at 20 MHz, the filling and emptying of surface states is a slower process. Therefore these states do not directly contribute to the capacitance under our measurement conditions. For lower AC frequencies, we observe an enhancement of the capacitance in the bias region below the kink which we attribute to the direct contribution of surface states. The situation is, however, intricate due to a strong variation of charging times, and its analysis is a matter of ongoing research. Thus we focus on the high-frequency data at 20 MHz here.

Even if the surface states do not directly contribute to the capacitance signal, they affect the capacitance–voltage characteristics indirectly by the presence of a bias-dependent surface charge. This positive charge screens effectively the gate bias from the NW, so that a more negative V_{gate} is needed to deplete the electrons from the wire. This can be quantified using equations (4) and (5). An additional (bias-dependent) surface charge density $\delta\sigma$ at R_{nm} gives an additional shift of the gate bias $V_{gate} = \phi_0(R_{gate}) + V_0 + \delta V$ with

$$\delta V = -\frac{\delta\sigma R_{nw}}{\varepsilon\varepsilon_0} \ln\left(\frac{R_{gate}}{R_{nw}}\right). \tag{7}$$

This explains the shift of the capacitance curve to lower bias while emptying the surface states. With δV being of the order of −1 V, positive surface charge densities of $\sim 10^{13}$ cm^{-2} are observed for gate biases far in the depletion region.

To summarize, if surface states are not included in the model, the simulations should be fitted to the part of the down-sweep curve right of the kink. The difference in V_{gate} between experiment and simulation below the kink allows for an estimate of the surface charge density.

3.4. Holes

As the electrochemical potential in the wire starts to approach the valence band, holes will appear. The creation and

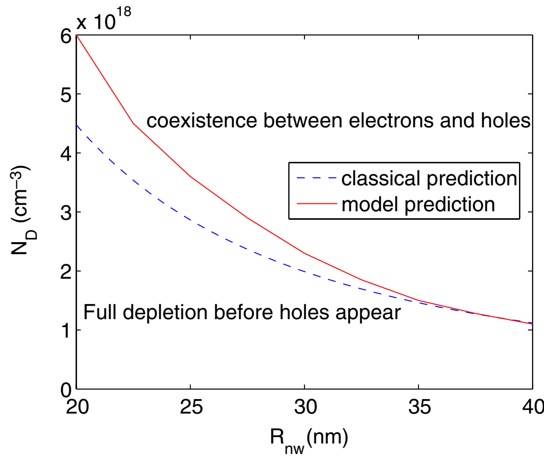

Figure 5. Doping density of InAs NWs required for the coexistence of holes and electrons.

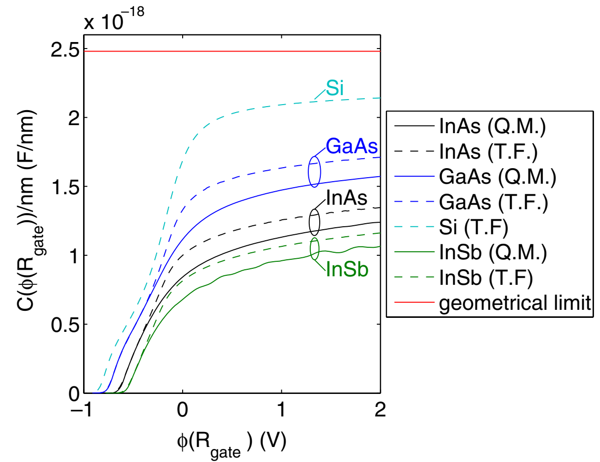

Figure 6. Comparison between theoretical capacitance and geometrical limit = 2.48×10^{-18} F nm^{-1}, for $R_{\rm nw} = 25$ nm, $R_{\rm gate} = 35$ nm, $N_{\rm D} = 2 \times 10^{18}$ cm^{-3}, plotted against the electrostatic potential at $R_{\rm gate}$.

annihilation of holes are slow processes. The holes, like the surface states, will therefore not directly contribute to the capacitance at high frequencies but instead screen the electrons. The high effective mass of the holes implies a large density of states, which results in a strong screening. If holes are created, practically no electrons will be removed any longer from the conduction band. The constant electron concentration causes the capacitance curve to flatten out at a finite value. This can be seen for the simulated doping $N_{\rm D} = 4 \times 10^{18}$ cm^{-3} in figure 3. The lower doping concentrations are too small for inversion to start before the last electrons have been removed, and the capacitance goes to zero in agreement with the experimental data.

From figure 4 we see that inversion also has an effect for the thicker wires for $N_{\rm D} = 2.2 \times 10^{18}$ cm^{-3}. This is in agreement with the measured capacitance, which seems to flatten out at a finite value for negative bias rather than dropping to zero as for the thinner wires.

In this context it is interesting to evaluate the doping required for the coexistence of holes and electrons. For zero temperature, this situation corresponds to the electrochemical potential entering the valence band at $r = R_{\rm nw}$ before it leaves the conduction band at $r = 0$. Thus, a certain doping concentration is required if the inversion should have any effect on the capacitance. This doping concentration can be classically estimated with the help of Gauss's law:

$$N_{\rm D}^{\rm coexist}(R_{\rm nw}) = \frac{4\varepsilon\varepsilon_0 E_{\rm g}}{e^2 R_{\rm nw}^2}. \tag{8}$$

The required doping as a function of $R_{\rm nw}$ can also be estimated with the Poisson–Schrödinger solver. The results are displayed in figure 5. Due to the confinement energy, the prediction of the simulation is higher than for the classical estimate. The difference is most significant for small $R_{\rm nw}$. For large values of $R_{\rm nw}$, the classical prediction is equal to, or even larger than, the model prediction. The reason is that the full bandgap is used in equation (8). In contrast, due to the thermal distribution, holes are already occupied slightly before the electrochemical potential enters the valence band. From figure 5, we conclude that at the estimated doping concentration $N_{\rm D} = 2.2 \times 10^{18}$ cm^{-3}, inversion will not affect the capacitance for $R_{\rm nw} \lesssim 30$ nm, in accordance with the findings of figure 4.

4. Comparison between different materials

We will now show that equating the capacitance of an NW with its geometrical limit can lead to large overestimates. In figure 6, the theoretically calculated capacitances of InAs, InSb, GaAs and Si NWs are plotted. The effective masses of these materials are 0.023, 0.0145, 0.063 and 0.33 [14], respectively. (For Si the density-of-state mass per conduction band valley was used and the valley degeneracy was explicitly taken into account.) They are all surrounded by HfO_2 and have the same geometry, $R_{\rm nw} = 25$ nm and $R_{\rm gate} = 35$ nm, i.e. they have the same geometrical limit. For comparison, the results from a Poisson–Thomas–Fermi solver have been plotted as well. In the Thomas–Fermi approximation, the electron concentration at each point is determined by the distance between the conduction band edge and $E_{\rm F}$. Multiplying the Fermi–Dirac distribution with the three-dimensional density of states and integrating over the conduction band yields the electron concentration as

$$n_{\rm e}(r) = \int_0^\infty \frac{\frac{1}{2\pi^2}\left(\frac{2m}{\hbar}\right)^{3/2} \cdot E^{1/2}\,{\rm d}E}{\exp((E - e\phi(r))/(kT)) + 1}, \tag{9}$$

where the conduction band edge is given by the electrostatic potential times the electron charge $-e\phi(r)$. Again we use $E_{\rm F} = 0$ as a reference.

Due to the complex band structure of Si, only the Poisson–Thomas–Fermi results have been calculated for this material. The main difference between the two solvers is that classically the electron concentration does not have to be zero at the semiconductor–oxide interface, resulting in a higher capacitance. It is evident that the two models give the same results for a repulsive gate voltage. In this case the electron concentration approaches zero at $R_{\rm nw}$ as the potential surpasses the electrochemical potential; see also [12].

There is a reason why the geometrical capacitance cannot be reached even classically. Let us compare with a metallic coaxial cable. In this case the geometrical limit is reached as all charge is added at the surface. This requires an infinite density of states, which cannot be found in a semiconductor, and thus the geometrical capacitance will not be reached. Materials with a high effective mass, such as Si, have a large density of states and will therefore come closer to the geometrical limit.

Frequently, it is assumed that the capacitance is constant for large positive gate voltages. Both experimental and theoretical results point out that this is not the case: the capacitance is slowly increasing with bias. As the gate becomes more attractive, electrons will be filled higher up in the conduction band. Since the 3D density of states goes as $E^{1/2}$, the density will increase as the bias is raised, resulting in a larger capacitance.

5. Conclusions

It has been shown how information about the doping and surface state concentrations can be obtained for semiconductor nanowires by comparing experimental and simulated capacitance data. The above procedure suggests how the contribution from these two factors can be separated. Analysis shows that the doping density $N_D = 2.2 \times 10^{18}$ cm^{-3} gives good agreement with the experimental data. The surface state charge at full depletion is estimated to be around 10^{13} e cm^{-2}. Finally, the actual capacitance can be significantly smaller than its geometrical limit even in accumulation mode. The difference is of particular importance for nanowires with low effective mass.

Acknowledgments

This work was supported by the Swedish Research Council, the Swedish Foundation for Strategic Research, the Knut and Alice Wallenberg Foundation, the EU-project NODE 015783, and the Italian Ministry of University and Research.

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MOVPE-grown InAs/GaSb layers and membranes on GaAs

Gvidas Astromskas[†], B. Mattias Borg[†], and Lars-Erik Wernersson[††]

[†]Solid State Physics

[††]Electrical and Information Technologies

Lund University, Box 118 SE-22100, Sweden

Abstract

Thin metamorphic InAs layers are fabricated on GaAs substrates using GaSb buffer layers grown by MOVPE. The quality of the GaSb buffer layers are optimized and epitaxial InAs layers are grown on GaSb layers of different thickness. A clear relationship between the structural quality of the GaSb and InAs layers is established and a high quality 23-nm-thick InAs layer is obtained (μ = 7200 cm^2/Vs at RT with a 004 reflection peak FWHM of 362") when grown on a 1.3-μm-thick optimized GaSb buffer layer. The best GaSb buffer layers are obtained for a nucleation temperature of 450 °C and a subsequent growth temperature of 570 °C with a V/III-ratio of 3, as confirmed by both the structural (HR-XRD, AFM) and electrical (Hall) measurements. Free-standing InAs membranes are finally fabricated and characterized to analyze the properties of the metamorphic InAs layers.

Keywords: A3. Metalorganic vapor deposition, A3. Metalorganic vapor phase epitaxy, A3. Organometallic vapor phase epitaxy, B1. Antimonides, B2. Semiconducting III-V materials, B2. Semiconducting ternary compounds, B2. Semiconducting indium compounds, B2. Semiconducting gallium compounds.

[†]both authors contributed equally to the article

PACS classification codes: 81.15.Gh, 61.05.cp, 68.55.ag

Introduction

The roadmap for the Si industry predicts a continued increase in the performance of the CMOS technology, although the ultimate scaling of devices leads to challenges of achieving high drive currents and low leakage current densities. Both aspects can be enhanced using high mobility III/V materials [1], currently used for very high-speed electrical and optical devices. InAs has a high electron mobility (30 000 cm^2/Vs) and high-performance InAs High Electron Mobility Transistors have been demonstrated [2]. Also, InAs and high-Indium-content InGaAs-based MOSFETs have been demonstrated [3,4]. These devices require integration of thin InAs layers onto insulating substrates. One option is to grow lattice-mismatched InAs/GaSb heterostructures on semi-insulating GaAs. The generation of misfit dislocation due to the very high lattice-mismatch (7%) can be controlled by carefully adjusting the growth conditions for the GaSb buffer layer [5,6,7], however, at the expense of several microns thick layers [8]. Thick buffer layers are not attractive for electronic device integration as leakage currents and aspect ratios greatly complicate device design and fabrication. Therefore, we investigate the vertical scaling of InAs/GaSb structures on GaAs (100) substrates.

The paper consists of two parts: first we optimize the GaSb growth using our MOVPE reactor and characterize the quality of the buffer layer. Secondly, we use the optimized GaSb buffers to deposit a thin metamorphic layer of InAs. We vary the thickness of the GaSb buffer layer while the metamorphic InAs layer is grown under the same conditions. The structural and electrical properties of the InAs layers are then evaluated and compared.

1. Experimental procedure

GaSb layers are grown using a horizontal reactor MOVPE system Aixtron 200/4. TMIn, AsH_3, TMSb, and TEGa are used as precursors with hydrogen as a carrier gas with a total flow of 13 l/min. Undoped epi-ready GaAs (001) substrates were either directly loaded into the reactor or first cleaned by etching in 37% HCl for 3 min and rinsed in deionized water for 1 min. No significant improvement was observed for the etched samples. The GaSb buffer layers were grown using a two-step process with first a nucleation step at low temperature followed by a buffer growth step at a higher temperature. To optimize the GaSb buffer layer, we varied the buffer growth temperature between 550 and 600 °C, the V/III-ratio between 1 and 5, and the nucleation temperature between 420 and 480 °C. It is verified by X-ray reflectometry (XRR) and AFM measurements that the nucleation step (4 min growth at V/III-ratio of 4) results in a rough 15-nm-thick layer.

In the optimization series all samples are grown for 35 min, resulting in a 1.3-μm-thick GaSb layer. The thickness of the GaSb buffer layer was controlled in-situ by reflectivity measurements.

23-nm-thick InAs films were grown on GaSb buffers layers of various thickness. In order to obtain high quality heterointerfaces, the growth temperature was lowered to 500 °C after the GaSb growth. An additional GaSb layer was grown for 1 min before switching to InAs, in order to obtain a controlled switching between GaSb and InAs. The InAs layer was grown for 34 s at a growth temperature of 500 °C and a V/III-ratio of 55, which is known to give high mobility InAs layers [9]. The chosen 23-nm thickness is below the critical thickness for the InAs/GaSb system and it is expected that the metamorphic InAs growth does not generate dislocations. The grown samples are characterized by high resolution X-ray diffraction (HR-XRD) measurements using a Bruker-AXS D8 system with a Cu K_α X-ray source. Rocking curves and 2θ-ω scans of the 004 reflection are performed, as well as reciprocal space maps of the 224 reflection to evaluate the composition and strain. The full width at half maximum (FWHM) of the 004 rocking curves, related to the mosaicity of the film, is used to compare the crystal quality. Also, carrier mobility and concentration in the grown layers are measured using Van-der-Pauw Hall technique on samples with Ti/Au ohmic contacts. The Hall measurements were performed at 0.19 T at both room temperature and 77 K.

2. GaSb buffer optimization

The growth of GaSb buffer layers has been investigated by a few groups, but the growth conditions for high quality GaSb buffers are varying, indicating that a reactor specific growth optimization is required [6,7,10,11]. Therefore, we first optimize the growth of comparably thick GaSb buffer layers (1.3 μm) with respect to nucleation temperature, growth temperature, and V/III-ratio. On these samples, as shown in Figure 1a, no InAs layers were grown, in order to investigate the structural quality of only the GaSb buffer layer using HR-XRD, AFM, and Hall measurements.

The highest hole mobility and the sharpest XRD peaks are obtained at a V/III-ratio between 2 and 3.5 as shown in Figure 1b. A V/III-ratio of less than 1 is detrimental for the GaSb growth, as confirmed by XRD and Hall measurements. Under these conditions, a lack of Sb causes the formation of Sb vacancies or even formation of Ga droplets. The hole mobility of the GaSb layer starts to decrease when the V/III-ratio exceeds 4, although the FWHM of the 004 peak remains narrow. A similar behavior is reported for GaSb grown from TMGa [7]. The FWHM of the XRD peak of the sample grown under a V/III-ratio of 3 is measured to be 291

arcsec, while the sample grown under the V/III-ratios of 4 and 5 show FWHM of 320 and 318 arcsec respectively.

The buffer layers grown at a temperature of 570 °C are found to be optimal as shown in Figure 1c. The quality increases with the growth temperature due to the increase in diffusion length for Sb, while the decrease at higher temperatures is related to an increasing Sb desorption from the substrate. A similar relation is obtained for thicker buffer layers [8].

Finally, we optimized the nucleation step temperature to be 450 °C as shown in Figure 1d because the nucleation can affect the subsequent buffer growth [7]. Although, the GaSb 004 peak FWHM varies little, the Hall mobility is strongly affected by the nucleation layer, particularly at the lowest nucleation temperature. We note that the GaSb buffer layer fully relaxes within the thickness of the nucleation layer, as no strain is measured in the GaSb buffer layers. The RMS values of the surface roughness are presented in table 1, which show a moderately low surface RMS for the optimized buffer layers. The correlation between the growth conditions and the surface morphology is weaker as compared to the XRD or Hall mobility measurements, which can be attributed to the presence of screw dislocations, shown in Figure 2a. These screw dislocations are observed in all samples and we observe no clear variation in their density. This indicates that effects originating from the screw dislocations do not contribute directly to the improvement in the layer quality under optimized growth conditions. Therefore the improvement in material quality is attributed to the reduction of the threading dislocation density.

Sample	V/III	T_G / °C	T_{nucl} / °C	GaSb RMS / nm
#2159	1	570	450	107
#2157	2	570	450	8.4
#2158	3.5	570	450	6.7
#2165	4	570	450	6.42
#2160	5	570	450	6.28
#2161	5	600	450	4.22
#2162	5	540	450	6.66
#2163	5	570	420	23.7
#2164	5	570	480	6.47

Table 1: RMS values of GaSb buffer layers

3. Structural evaluation of InAs/GaSb

In a second series of samples, thin layers of InAs were grown on top of the GaSb buffer layers. In order to correlate the quality of the InAs layer with the quality in the GaSb buffer layer, we varied the thickness of the GaSb buffer layer in the InAs/GaSb heterostructures and performed HR-XRD measurements of the structure. The thickness of the InAs layer was kept at 23 nm, which is below the critical thickness (36 nm) according to People and Bean [12]. XRD 2θ-ω scans of InAs/GaSb samples with varying GaSb buffer thickness are compared in Figure 3a. Here, it is observed that the InAs peaks exhibit clear Pendellösung fringes for the samples with a buffer thickness above 800 nm, indicating a high-quality interface between the GaSb and the InAs. Also, the peak position of the InAs shifts towards lower 2θ values for the thicker buffer layers, which can be caused by a combination of strain relaxation and a modification of the InAs composition due to a carry-over of Ga or Sb.

The FWHM of the GaSb 004 rocking curve decreases as the GaSb buffer thickness increases, as shown in Figure 3b. The crystal quality is improving rapidly as the buffer thickness is increased to 1 μm. A clear correlation between the rocking curve FWHM of the GaSb buffer and the InAs is observed and the FWHM of the InAs layer follows the GaSb data, although with a roughly 100” wider peak. The quality of the thin InAs film thus appears to be directly dependent on the quality of the underlying GaSb buffer. The increased FWHM of the InAs is attributed to the use of a thin InAs film (23 nm).

Reciprocal space maps of the 224+ reflection were obtained (not shown) in order to separate the influence of strain and composition. It was found that the InAs layer grown on a 310 nm GaSb buffer was 7% relaxed and had a Bragg peak that was significantly shifted from the position of pure InAs. For GaSb buffer thickness exceeding 800 nm, the InAs film was only 2% relaxed, and the InAs peak position was closer to the position of pure InAs. This indicates that the amount of Ga and Sb carried over into the InAs layer is related to the quality of the InAs and GaSb layers. Previously, Ga carryover in the InAs(Sb)/GaSb system has been reported by Lackner et al. [13], where it was found not to be an effect of the gas switching, but rather due to adsorbed Ga. The Ga carry-over is aggravated as the comparably high dislocation density present in the thin GaSb buffers could give additional absorption sites for Ga. It is also likely that there is a few percent of Sb carried over into the InAs layer, due to the well-known segregation effect of Sb [14]. Sb and Ga would move the InAs diffraction peak in opposite directions, and the composition of the resulting quaternary In(Ga)As(Sb) compound can thus not be fully evaluated by HR-XRD, but additional photoluminescence measurements are

required. It is clear, however, that InAs growth on thicker GaSb buffers gives not only a better crystal quality, but also less incorporation via carry-over effects.

We also scanned the InAs surface with AFM to evaluate the surface morphology. The RMS values for the InAs films grown on the optimized buffers were found to be lower than 7 nm, which is similar to values reported by others [15]. However no clear dependence of RMS roughness versus buffer thickness was obtained. Despite that the InAs growth mitigates the terraces, forming around the screw dislocations as shown in Figure 2b, the dislocation density can be still be evaluated. Interestingly, no significant change in screw dislocation density was observed for samples with different buffer layer thicknesses. Therefore, the improvement in the structural and electrical quality is not due to a reduction of the screw dislocation density, but has to be attributed to reduction in threading dislocation density.

4. Electrical evaluation of InAs/GaSb layers and membranes

To characterize the layers electrically we first removed the InAs layer and evaluated the properties of the GaSb buffer layer only. Secondly, we formed InAs membranes by selective etching of the underlying GaSb layer. The InAs layer was selectively etched away using a citric acid:H_2O_2 solution (1:1) and Van der Pauw-Hall measurements were performed on the GaSb buffer layer. The results are shown in Figure 3b, where the GaSb mobility increases with increasing buffer thickness, supporting the XRD results. The 1.3-µm-thick GaSb buffer exhibited a mobility of 620 cm^2/Vs and a hole concentration of $3.6 \cdot 10^{16}$ cm^{-3} at room temperature. At 77 K the mobility increased to 3000 cm^2/Vs and the carrier concentration was $9.2 \cdot 10^{15}$ cm^{-3}. These values are comparable to other reported results [6,8,10]. Due to the Sb carry-over it is likely that a thin layer of InAsSb remains after the selective InAs etch. To minimize its effect, measurements by profilometer is used to verify that at least 23 nm layer is etched away. Therefore any residual layer will have only minor influence on the measured values [16].

To separate the InAs film from the GaSb layer in a selective process, electron beam lithography combined with a wet etch with a low concentration NH_4:H_20 solution (1:4) is used for creating a free standing InAs membrane, as shown in Figure 4a. The InAs membrane is suspended on GaSb supports that provide stability and large areas for contacts. The under-etch procedure allows the variation of the width (W) of the GaSb mesa that remains under the InAs film, and the resistivity of the integrated InAs/GaSb structure can be evaluated to separate the contributions from InAs and GaSb. It is expected that the value for the integrated

structure should converge towards the InAs resistivity when the GaSb mesa is etched away. However, Figure 4b shows that resistivity is independent of the width of the under-etched mesa. This indicates that for the geometries used, the GaSb layer has a stronger contribution to current than InAs in this partially under-etched structure. It should be noted that the resistivities of samples with different GaSb thickness do not differ despite the varying crystal quality. This is attributed to the measured increase in carrier concentration for the thinner layers which comes at the expense of mobility, thus balancing the resistivity change.

It is interesting that for completely under-etched structures, the measured resistivity increases almost 50 times as compared to not fully under-etched structures. To verify our processing conditions, we used a thicker (90 nm) InAs film and when it is completely under-etched, the resistivity decreases below the value of GaSb, as expected. The mobility of this thicker InAs membranes formed from material grown on a 1.3-μm-thick buffer is measured to be around 2700 cm^2/Vs with an electron concentration of $1.2 \cdot 10^{17}$ cm^{-3}. As a reference, we also measured the Hall mobilities of InAs layers (23 and 90 nm) grown on 1.3-μm-thick buffers without removing the GaSb buffer layer. In this case, the mobility for the 23 nm InAs film exceeded 7200 cm^2/Vs, while for the 90 nm sample it was 1300 cm^2/Vs. The low mobility of the 90nm film is attributed to lattice relaxation, while the 23 nm film remains metamorphic. This is confirmed by XRD analysis, where a relaxed InAs peak was measured for the 90 nm sample. The large resistivity value of the metamorphic 23-nm-thick InAs membranes is therefore attributed to surface effects, occurring during the under-etch process. We tested to passivate the surface by a NH_4S_X-solution and observed on average five times lower resistivities after the treatment.

The GaSb mobility results clearly indicate that electrical quality of the buffer layer is directly related to the structural quality. The fact that we measured realistic mobility values for the not under-etched InAs layer on the 1.3-μm-thick buffer layer indicates that the electrical properties of thin InAs can be measured only when the quality of the buffer layer is sufficiently good. We hence conclude that the conductivity of the buffer has to be decreased to reliably evaluate the properties of InAs on thinner buffer layers. This can be achieved by isolating the GaSb buffer from the InAs by the introduction of a higher band gap material, like AlSb.

Summary

The growth conditions for thin GaSb buffer layers were optimized and the structural quality and electrical properties were evaluated. The optimal growth conditions for the GaSb buffer layer were found to be a

growth temperature of 570 °C and a V/III-ratio of 3, with a thin nucleation layer grown at 450 °C. We also showed that both the electrical and structural quality of the GaSb buffer quality increase with increasing thickness. Screw dislocations are observed for all samples, but their density does not appear to affect the layer quality.

We integrated an InAs layer onto the GaSb buffer layer and observed a direct relation between the quality of the GaSb buffer and the InAs layer. A significant improvement in the structural quality with increasing thickness was observed for GaSb thickness up to 1.3 μm. The mobility of the GaSb layer correlates directly with the XRD peak FWHM value, and a higher buffer layer quality results in better electrical properties. We also observe that the structural quality of the InAs is directly proportional to the GaSb quality. The FWHM value of the InAs layer is increased by 100" as compared to the GaSb layer, but the shift is attributed to surface effects of the thin InAs film. The electrical mobility of the thin InAs layer exceeds 7200 cm^2/Vs when grown on the 1.3-μm-thick buffer layer. For thinner buffer layers, the GaSb buffer conduction contributes to the Hall signal and reliable measurements could not be performed. We used the buffers to fabricate thin (23 nm) InAs membranes that show a comparably high resistance, which is attributed to surface effects originating from the GaSb etching.

Acknowledgements

This work was supported from the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF), Knut and Alice Wallenberg Foundation (KAW) and the Nanometer Structure Consortium at Lund University (nmC@LU).

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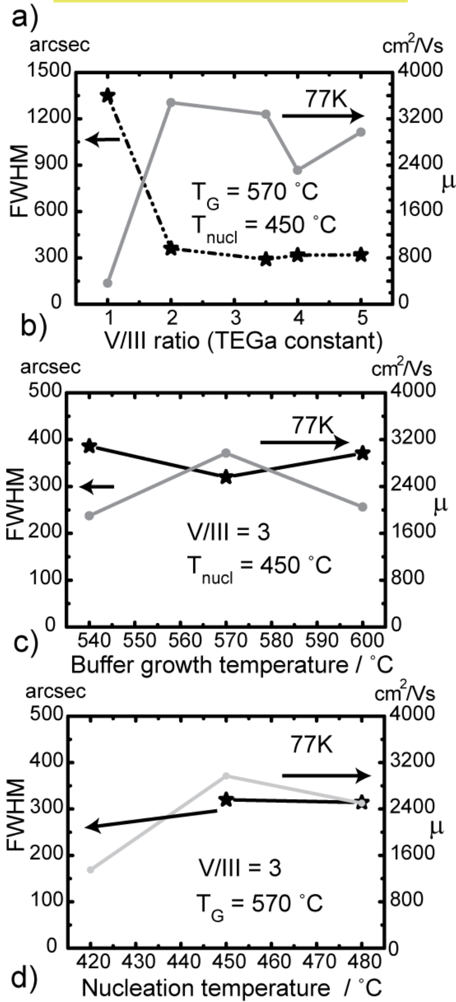


Figure 1. Structural and electrical quality of GaSb buffer layers as a function of a) V/III-ratio, b) temperature during buffer growth, and c) temperature during nucleation. The growth temperature (T_G), nucleation temperature (T_{nucl}) and V/III ratio were set to optimal values in each sample series.

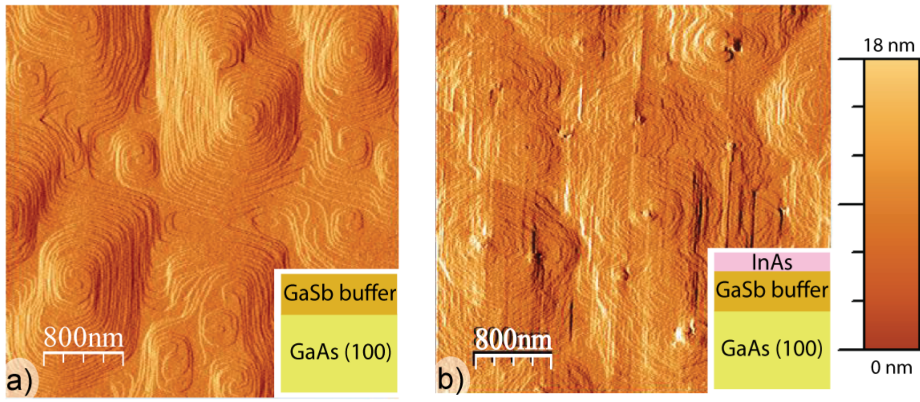


Figure 2. 4x4 μm^2 AFM images of a) 300 nm optimized GaSb buffer layer, b) InAs surface, grown on 1.3 μm GaSb buffer. The screw dislocations are clearly visible on the GaSb surface, while the InAs growth starts to mitigate them. The RMS values are 4.35 nm and 5.93 nm for a) and b) respectively.

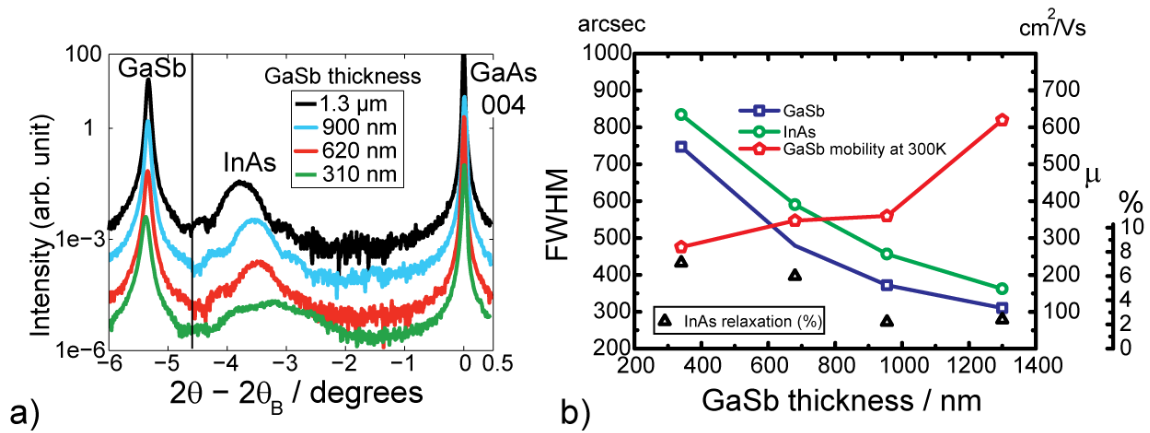
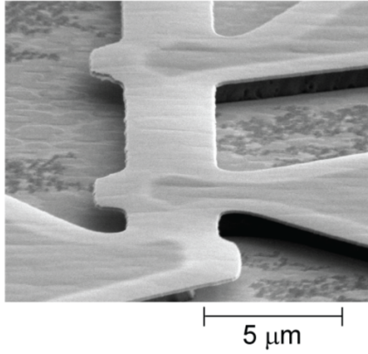


Figure 3. a) XRD scans of the InAs/GaSb structure for various GaSb thicknesses. The thickness of the InAs layer is 23 nm for all samples. Interference fringes are observed for the InAs peak at higher buffer thicknesses. The vertical line indicates the position of fully strained InAs. b) Structural and electrical properties of InAs/GaSb as a function of the GaSb layer thickness. The quality of the InAs layer is directly related to the GaSb buffer layer and the quality of the GaSb layer increases with the thickness.



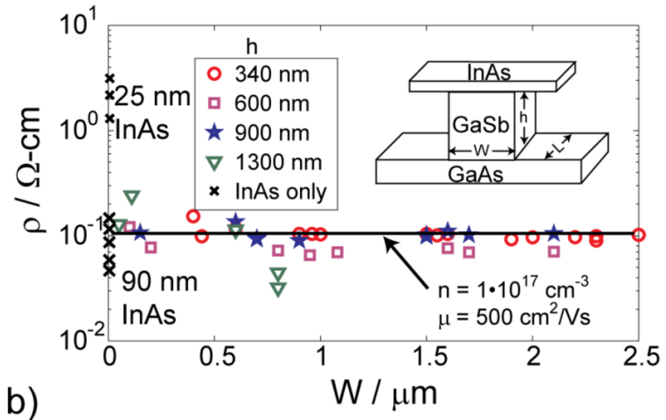


Figure 4. a) SEM image of under-etched InAs membrane, b) the resistivity of partially under-etched InAs membranes including parts of the GaSb buffer layer vs. the mesa width. The resistivity of InAs is about 50 times higher than the resistivity of GaSb. The resistivity of the partially etched GaSb corresponds to mobility of about 500 cm^2/Vs, as shown by a black line.