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Digital Implementation of a Wavelet-Based Event Detector for Cardiac Pacemakers

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Abstract—This paper presents a digital hardware implementation of a novel wavelet-based event detector suitable for the next generation of cardiac pacemakers. Significant power savings are achieved by introducing a second operation mode that shuts down 2/3 of the hardware for long time periods when the pacemaker patient is not exposed to noise, while not degrading performance. Due to a 0.13-μm CMOS technology and the low clock frequency of 1 kHz, leakage power becomes the dominating power source. By introducing sleep transistors in the power-supply rails, leakage power of the hardware being shut off is reduced by 97%. Power estimation on RTL-level shows that the overall power consumption is reduced by 67% with a dual operation mode. Under these conditions, the detector is expected to operate in the sub-μW region. Detection performance is evaluated by means of databases containing electrograms to which five types of exogenic and endogenic interferences are added. The results show that reliable detection is obtained at moderate and low signal to noise-ratios (SNRs). Average detection performance in terms of detected events and false alarms for 25-dB SNR is $P_D = 0.98$ and $P_{\mathrm{FA}} = 0.014$, respectively.

Index Terms—Cardiac pacemaker, event detector, gated supply, sleep transistors, wavelet filter.

I. INTRODUCTION

DEVICE longevity is a crucial design constraint in the evolving area of medical implants since replacement of implanted devices results in discomfort for the patient and high economical costs. Medical implants such as the cardiac pacemaker may last up to 20 years (projected longevity for one of the world's longest lasting pacemakers *Regency SC+, St-Jude Medical*). At the same time, reliable detection performance, closely related to longevity, is essential as the number of devices that may interfere with the pacemaker is ever increasing.

A variety of event detectors for electrocardiograms (ECGs) have been proposed during the last three decades [1]–[3]. However, most of them are unsuitable for pacemaker applications since they do not operate in real time. Traditionally, event detectors for pacemakers are composed of a band-pass filter followed by a programmable threshold level, implemented in analog circuitry [4]. The proposed implementation is optimized for digital circuitry, and the wavelet-based structure offers a
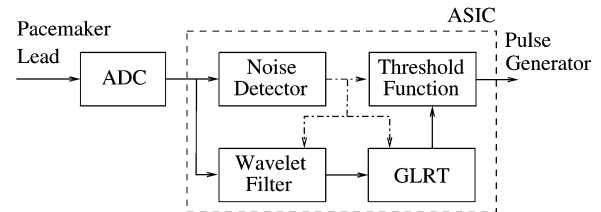
Fig. 1. Block diagram of the event detector and the target environment. Solid lines represent the dataflow while dashed-dotted lines the mode-select signals.

higher flexibility for different morphologies. Together with a low-power analog-to-digital converter (ADC) a single-chip solution becomes possible.

Digital hardware is feasible for today's pacemaker generation due to recent development in low-power ADCs, e.g., the ADC in [5] operates at 2.2 μW. Moreover, shrinking technologies and advances in low-power digital circuitry makes a digital solution a competitive alternative to analog solutions. In favor to analog circuitry [6], a digital implementation has the advantage of accommodating more advanced signal processing such as features for morphology classification, e.g., in implantable cardioverter defibrillators (ICDs), and data compression for postanalysis [7], [8]. Postanalysis provides better knowledge of diseases and improves pacemaker/ICD parameter tuning [9], [10].

The proposed event detector is based on a wavelet filterbank that decomposes the input signal into subbands, followed by hypothesis testing [11]–[15] see Fig. 1. The threshold function of the hypothesis test determines whether the incoming beat is considered as cardiac activity or as noise. A dual operation mode of the detector is proposed by which major parts of the hardware can be shut down when the pacemaker patient is at rest or in a low-noise environment. Reliable detection performance is sustained by a noise detector that operates in supervision mode and reactivates the sleeping hardware when necessary, see Fig. 1.

Dynamic power savings are achieved using a gated clock to shut off parts of the deactivated detector. However, as the event detector is targeted to operate at a low frequency of 1 kHz, leakage is the main contributor to the total power figure. Therefore, leakage reduction techniques are required to efficiently address power dissipation. In the present implementation, gate transistors are used to effectively turn off the supply voltage and, thereby, reduce the leakage power [16]–[19].

In Section II, the detector principles are presented as well as the databases used for evaluation. Section III describes the implementation and optimization in digital hardware. Moreover, a hardware realization for a dual operation mode is presented. The performance of the event detector is discussed in Section IV.
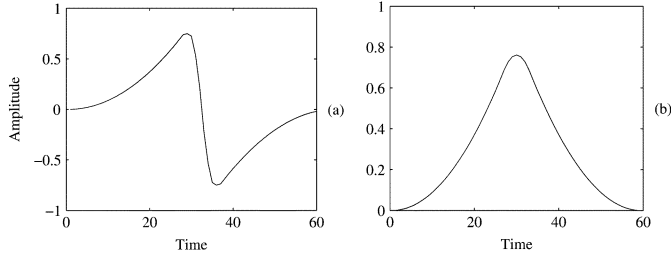
Fig. 2. Electrogram events with (a) typical biphasic and (b) monophasic signal.
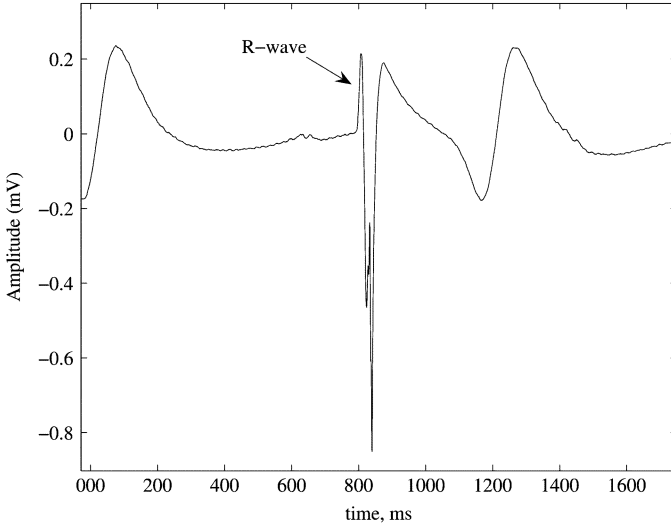

Fig. 3. Electrogram of a cardiac cycle. Ventricular depolarization is reflected by the R-wave.

Power optimization, an estimate for the core power consumption, and application-specific integrated circuit (ASIC) placement and routing are presented in Section V. Finally, conclusions are presented in Section VI.

II. Materials and Methods

The electrical activity at the pacemaker electrode tip is reflected by the intracardiac electrogram (EGM) [20]–[23]. The depolarization and repolarization waves are decomposed into two perpendicular waves: one that propagates horizontally and another that propagates transversally to the myocardial wall [24]. Thus, the morphologies of these two waves differ significantly. The horizontal wave is composed of a large positive charge that rapidly changes to a negative charge resulting in a *biphasic wave*, whereas the transversal wave results in a *monophasic wave*, see Fig. 2.

Ventricular depolarization usually represents the cardiac event in an EGM and is referred to as the "R-wave" in this study, see Fig. 3; its duration is normally between 60 and 100 ms [4], [20].

A. Wavelet Filterbank and GLRT

This section presents a brief theoretical background of the wavelet filterbank and GLRT needed to comprehend the hardware implementation. A more detailed description is to be found in [15] and [25].

The detector structure was developed with efficient digital hardware implementation in mind. The wavelet filterbank is a combination of a biphasic (antisymmetric) and a monophasic (symmetric) filter function that approximates biphasic and monophasic morphologies. The transfer function $h_{q,b}(n)$ of the biphasic wavelet filterbank is modeled as

$$
\begin{aligned}
h_{1,b}(n) &= g_b(n) \\
h_{2,b}(n) &= f(n) * g_b(2n) \\
h_{3,b}(n) &= f(n) * f(2n) * g_b(4n) \\
&\vdots \\
h_{q,b}(n) &= f(n) * \cdots * f(2^{q-2}n) * g_b(2^{q-1}n) \quad (1)
\end{aligned}
$$

where q is the scale factor. An analysis has shown that three scales, $q = 2, 3, 4$, are sufficient to cover the frequency spectrum of an R-wave [15]. The case $q = 1$ is not considered in the design, as no prior filtering is defined. The functions $g_b(n)$ and $f(n)$ in (1) are defined as

$$ g_b(n) = \begin{bmatrix} -1 & 1 \end{bmatrix} \quad (2) $$

and

$$ f(n) = \begin{bmatrix} 1 & 3 & 3 & 1 \end{bmatrix} \quad (3) $$

respectively. To achieve power-efficient hardware mapping, short filters with integer values are chosen, and, therefore, $g_b(n)$ in (2) is chosen as a first-order difference, and the impulse response $f(n)$ in (3) was chosen as a third-order binomial function [15]. The monophasic filterbank $g_m(n)$ is modeled by reusing $g_b(n)$ as

$$ g_m(n) = g_b(n) * g_b(n) = \begin{bmatrix} 1 & -2 & 1 \end{bmatrix} \quad (4) $$

such that the transfer function $h_{q,m}(n)$ of the monophasic filterbank is modeled as

$$ h_{q,m}(n) = f(n) * \cdots * f(2^{q-2}n) * g_m(2^{q-1}n). \quad (5) $$

The output of the wavelet filterbank is defined as

$$ \mathbf{y}(n) = \mathbf{x}^T(n)\mathbf{H} \quad (6) $$

where

$$ \mathbf{x}(n) = [x(n) \ldots x(n+N-1)]^T \quad (7) $$

is the input to the wavelet filterbank; $\mathbf{H}$ is defined as

$$ \mathbf{H} = [\tilde{\mathbf{H}}_b \quad \tilde{\mathbf{H}}_m] \quad (8) $$

and can be efficiently implemented by Mallat's algorithm [26]. The matrices $\tilde{\mathbf{H}}_m$ and $\tilde{\mathbf{H}}_b$ in (8) denote the reversals of $\mathbf{H}_m$ and $\mathbf{H}_b$, respectively, where the latter is defined as

$$ \mathbf{H}_b = [\mathbf{h}_{2,b} \quad \mathbf{h}_{3,b} \quad \mathbf{h}_{4,b}]. \quad (9) $$

The matrix $\tilde{\mathbf{H}}_m$ in (8) is computed according to (5). Finally, the decision signal $T(n)$ is computed by a generalized likelihood ratio test (GLRT) as

$$ T(n) = \mathbf{x}^T(n)\mathbf{H}(\mathbf{H}^T\mathbf{H})^{-1}\mathbf{H}^T\mathbf{x}(n) \quad (10) $$
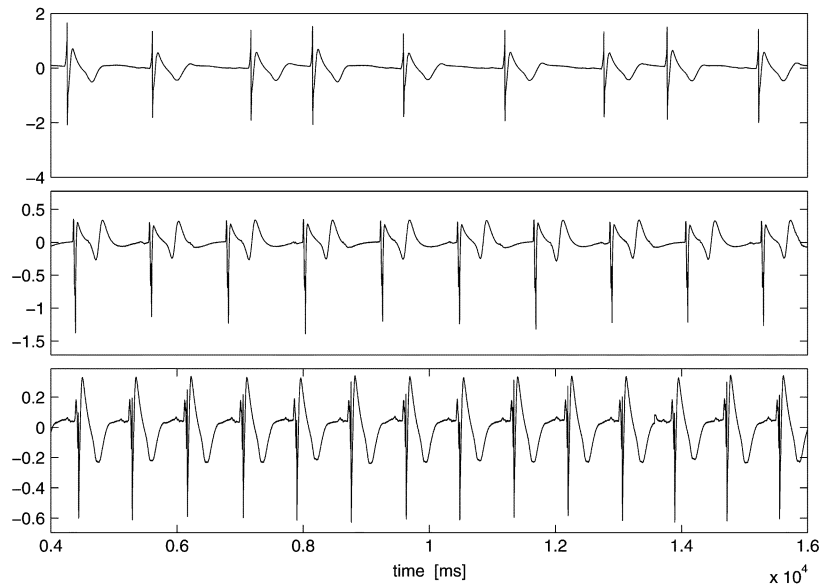
Fig. 4.   Examples of EGMs from different patients.

and compared to a threshold [11], [15]. Due to orthogonality of the mono- and biphasic functions, the matrix $(\mathbf{H}^T\mathbf{H})^{-1}$ in (10) is symmetric and sparse with half of the elements equal to zero. Thus, half of the multiplications with the elements of the matrix in (10) do not need to be implemented. The threshold level determines the presence of an R-wave and controls the pulse generator as

$$T(n) \geq \beta T_{\max} \qquad (11)$$

where β denotes a amplitude threshold fraction, and $T_{\max}$ the average value of the maximum amplitudes of the previously detected events. If the condition in (11) is met, an R-wave is detected.

B. EGM Database

The database contains EGMs from 50 patients, recorded from ventricular pacemaker electrodes, and is used to evaluate the performance of the detector. The EGMs were recorded either during initial implantation or pacemaker replacement, throughout hospitals in Germany (coordinated by Justus-Liebig Universität, Gießen, Germany). The recordings were obtained from patients suffering from AV block and sick sinus syndrome [4]. Most signals were recorded from a unipolar electrode, however, a few signals were recorded with a bipolar electrode. The sampling rate was 44.1 kHz with a resolution of 16 bits. For this particular study the signals were decimated to 1 kHz, since frequencies above 400–500 Hz were judged to be less significant to detection. In order to be compliant with the ADC in [5] a resolution of 8 bits is chosen. The recordings were annotated with respect to a time reference of each R-wave, required for performance evaluation of the detection algorithm. The annotation of an event was defined as the steepest transition phase in the cardiac cycle. Three EGM recordings from different patients are displayed in Fig. 4, and illustrates the inter-patient variability in morphology.
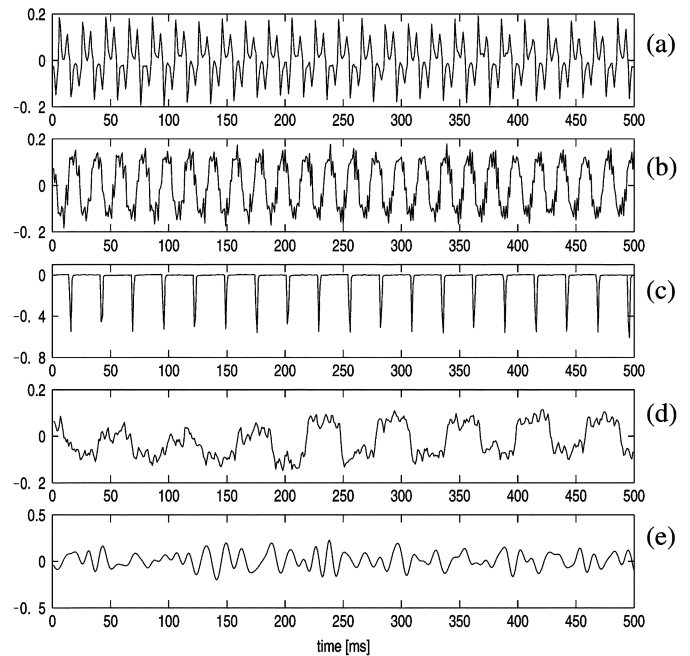
Fig. 5.   Exogenic interference recordings generated from (a) 500-W ac hand drill, (b) electric hand mixer, (c) EAS 1, and (d) EAS 2. Endogenic interference caused by (e) muscular activity.

C. Interference Database

The present event detector is tested with respect to sensitivity to exogenic and endogenic interferences, originating outside and inside the body, respectively [27]. The test is done in order to simulate situations when the pacemaker patient is subjected to electronic or magnetic noise. Exogenic interference is limited to sources in everyday life, e.g., caused by electronic household appliances or electronic article surveillance (EAS) systems. Endogenic interference is represented by muscular activity [28]. Fig. 5 presents examples of the different types of interference.
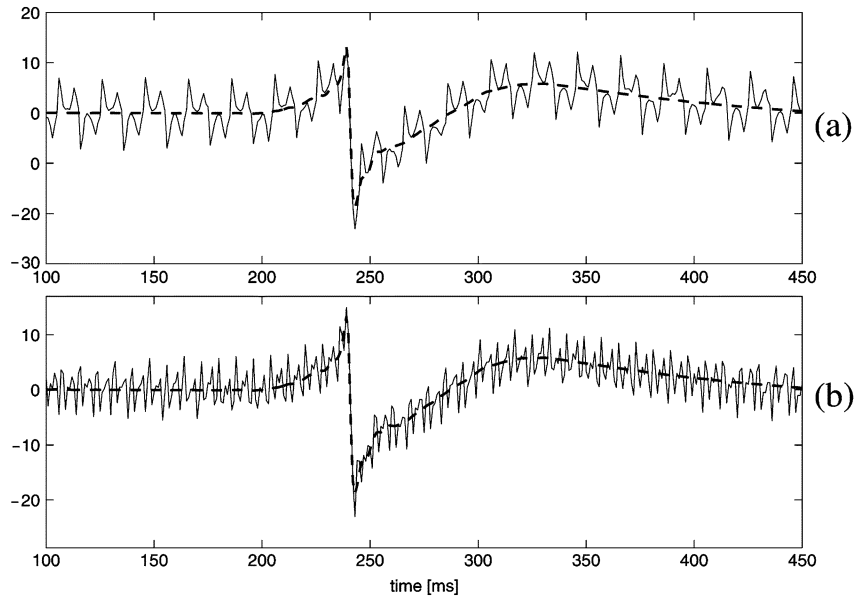
Fig. 6. Typical EGM interfered with 20-dB SNR from an (a) ac hand drill and (b) muscular activity.
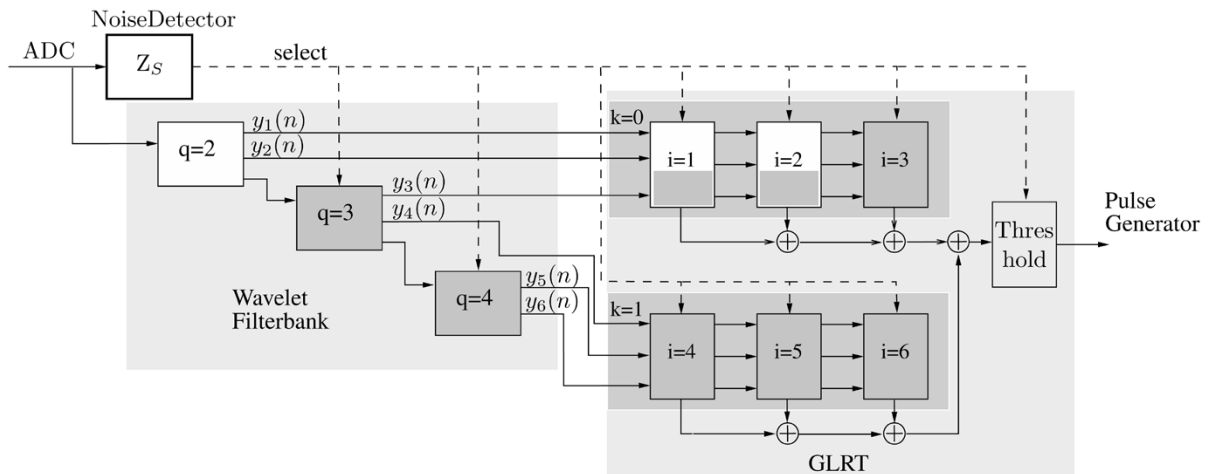
Fig. 7. Block diagram of the R-wave detector. The darker shaded blocks in the wavelet filterbank and GLRT are inactive in normal mode.

Household appliances represent a common source of interference, caused by electric and magnetic activity within the same frequency range as the R-wave. Furthermore, the magnetic field intensity is dependent on the signal transiency. In this study, recordings from an ac powered hand drill and an electric hand-mixer were used.

Electronic article surveillance systems have been identified as a common interference source [29]–[32]. Such systems use widely different transmission techniques which makes it difficult to generalize results to how such systems interfere with the pacemaker. In this study, two systems that operate within the R-wave frequency spectra have been tested. The EAS 1 system uses a 16.6-Hz triangular wave modulated with 5 or 7.5 kHz. The EAS 2 system transmits 3-ms long bursts of 58-kHz acoustomagnetic signals with a high amplitude at an interval of 27 ms. The pulse period of 30 ms (33 Hz) is considered to be the reason for possible interference with pacemakers.

Muscular activity is an endogenic interference source which spectrally overlaps with heart signals. In this study, signals recorded pressing the palms together have been considered. The effect of muscular noise on pacemaker performance was one of the first studies on pacemaker interference [28].

Fig. 6 shows the morphology of an EGM with interferences originating from a hand drill and muscular activity, respectively.

III. DIGITAL HARDWARE MAPPING AND OPTIMIZATION

This section describes how the wavelet filterbank and the GLRT are implemented in digital hardware. The proposed structure has been optimized with respect to wordlength and numerical strength reduction to reduce area and power consumption [33], [34].

A. Structure of the R-Wave Detector

The implemented wavelet filterbank consist of three branches, $q = 2, 3, 4$, that scale and filter the signal from
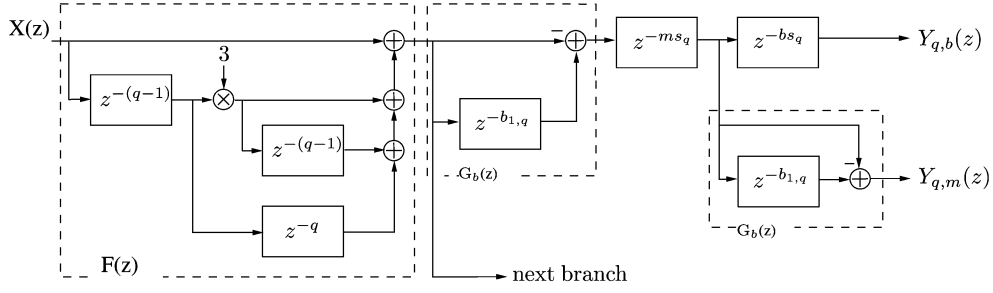
Fig. 8. Data flow diagram of the first wavelet filterbank branch using Mallat's algorithm [26]. The number of registers in $F(z)$ is minimized, and bi- and the monophasic filter output are represented as $Y_{q,b}(z)$ and $Y_{q,m}(z)$, respectively.
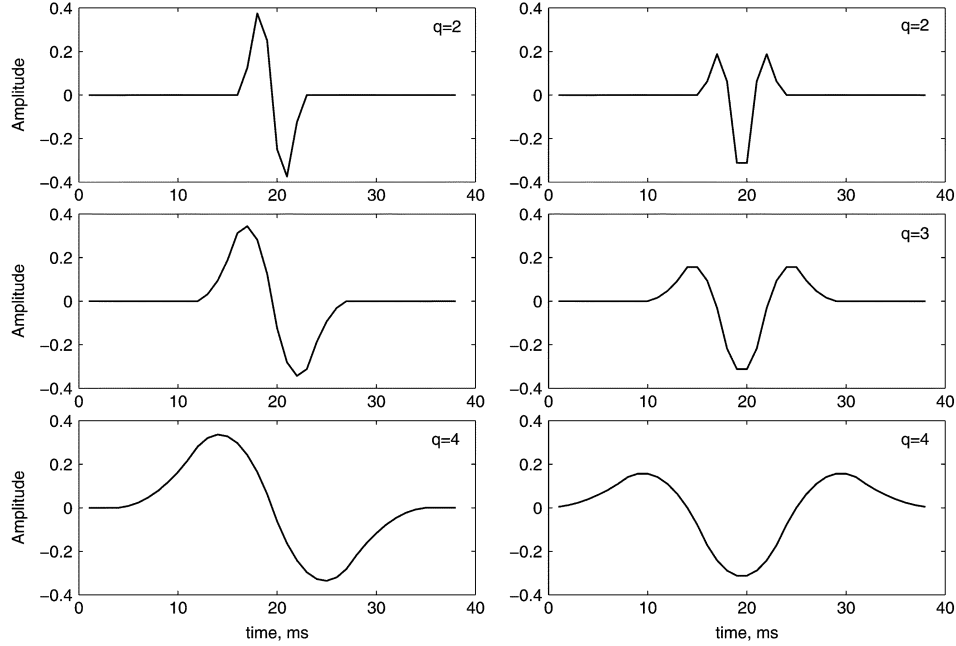
Fig. 9. Impulse responses of the wavelet filterbank. The biphasic impulse responses $y_{b,q}(n)$ for $q = 2, 3, 4$ are displayed in the left panel and the monophasic impulse responses $y_{m,k}(n)$ in the right panel.

the ADC, see Fig. 7. The first biphasic branch realizes a straightforward implementation of (2) and (3) as

$$F(z) = 1 + 3z^{-(q-1)} + 3z^{-(2q-2)} + z^{-(2q-1)}$$
$$G_b(z) = -1 + z^{-q}.$$

Reusing $G_b(z)$ according to (4) realizes the monophasic filterbank using a single branch for one scale factor, see Fig. 8, and the output of the filterbank realizes (6). However, in order to center the functions to the longest propagation delay, which is in the third branch, it is necessary to introduce additional delays

in $G_b(z)$, see Fig. 8. The delays for each branch are presented in Table I, and the impulse responses of the filterbank are presented in Fig. 9.

Since $\mathbf{x}^T(n)\mathbf{H} = \mathbf{H}^T\mathbf{x}(n)$, the remaining part of (10) to be implemented is the multiplication by (12), shown at the bottom of the page. A matrix which is symmetric and sparse with half of its elements equal to zero. The multiplication of $\mathbf{y}(n)$ with the first column of $(\mathbf{H}^T\mathbf{H})^{-1}$ and the first element of $\mathbf{H}^T\mathbf{x}(n)$ is carried out as depicted in Fig. 10, where $c_{3k+j,i}$ are elements of $(\mathbf{H}^T\mathbf{H})^{-1}$ and $y_{3k+j}(n)$ the output of the filterbank, with $k = 0, 1$ and $j = 1, 2, 3$.

$$(\mathbf{H}^T\mathbf{H})^{-1} = \begin{bmatrix} 4.25 & -2.81 & 0.71 & 0 & 0 & 0 \\ -2.81 & 4.47 & -1.75 & 0 & 0 & 0 \\ 0.71 & -1.75 & 1.49 & 0 & 0 & 0 \\ 0 & 0 & 0 & 4.84 & -2.31 & 0.6 \\ 0 & 0 & 0 & -2.31 & 4.29 & -1.49 \\ 0 & 0 & 0 & 0.6 & -1.49 & 1.77 \end{bmatrix} \tag{12}$$

TABLE I
DELAYS IN $G_b(z)$ AS ILLUSTRATED IN FIG. 8

q	$b_{1,q}$	ms_q	bs_q
2	2	15	1
3	4	10	2
4	8	0	4

TABLE II
COMPARISON OF WORST CASE SCENARIO AND IMPLEMENTED WORDLENGTH N_{wc} AND N_{Imp}, RESPECTIVELY, WHERE $N = 8$ IS THE WIDTH OF THE INPUT SIGNAL PROVIDED FROM THE ADC

	$y_1(n)$	$y_2(n)$	$y_3(n)$	$y_4(n)$	$y_5(n)$	$y_6(n)$
N_{wc}	$N+6$	$N+7$	$N+11$	$N+12$	$N+14$	$N+15$
N_{Imp}	$N+1$	$N+1$	$N+2$	$N+1$	$N+2$	$N+1$

B. Hardware Optimization

The aim of hardware optimization is the reduction of silicon area as well as the reduction of power dissipation.

1) Optimization of the Wavelet Filterbank: The internal wordlength of the wavelet filterbank and the output signal $\mathbf{y}(n)$ are bit-optimized in order to reduce complexity. In a theoretically worst case scenario mathematical operations in the filterbank leads to an extended dynamic range and therefore wordlength has to increase accordingly, in order to be sure to avoid overflow. However, this is a very pessimistic approach leading to large overhead due to excessive number of bits. In order to determine the maximum number of required bits for a more realistic scenario, all recordings in the EGM database have been analyzed using the filterbank. The internal wordlength at $F(z)$ and the output $Y_1(z), \ldots, Y_6(z)$ was traced in order to determine the number of bits required to represent the largest occurring number. This analysis has shown that overflow can be avoided if the dynamic range is increased by two bits compared to the input wordlength N. Thus, the wordlength, N_{wc}, for a worst case scenario could be reduced significantly from $N + 15$ to $N + 2$, see Table II, and the target implementation has a wordlength of ten bits at $y_1(n), \ldots, y_6(n)$. Saturation logic guarantees that the signal at $\mathbf{y}(n)$ is upwards limited to values representable by ten bits if overflow should occur. This optimization leads to significant reductions in the filterbank and results in narrower multipliers and adders in the following GLRT.

Furthermore, the fixed multipliers in each branch of the filterbank are implemented as shift-add instructions, carried out during one clock cycle, referred to as *numerical strength reduction* [33]. This optimization results in area and power reduction.

The straightforward block diagram of the filterbank in Fig. 8 has an excessive number of delays. Thus, the number of registers in $G_b(z)$ are minimized by reusing the registers needed to center the impulse responses in Fig. 9. This results in a reduction of approximately 300 (1-bit) registers.

2) Optimization of the GLRT: Substitution of the real values in $(\mathbf{H}^T\mathbf{H})^{-1}$ with their respective rounded integer values reduces the computational cost of the GLRT, see Table III. As multiplication is a more complex operation than addition, complexity reduction is achieved by trading multipliers against adders [33]. Therefore, all the multiplications with the elements of $(\mathbf{H}^T\mathbf{H})^{-1}$ are replaced with shift and add operations performing the same operation during one clock cycle. The only multiplication that remains in the GLRT is the one by $\mathbf{H}^T\mathbf{x}(n)$, which is the output of the wavelet filterbank and already computed in (6). The result of this operation is implemented by the rightmost multiplier in the schematic in Fig. 10.

TABLE III
SUMMARY OF STRENGTH REDUCTION AFTER OPTIMIZATION OF WAVELET FILTERBANK AND GLRT

	not optimized	optimized	savings %
MULT	26	6	-77
ADD	32	45	+41

Fig. 10. Data flow diagram of a block in the GLRT. The multipliers with shaded background are realized by shift-add operations.

This optimization achieves a reduction of 77% in multipliers while the number of adders is increased by 41%, see Table III. Thus, power and area is reduced in the filterbank hardware.

A typical decision signal using *Matlab* floating point and integer coefficients, respectively, is presented in Fig. 11. It is shown that the deviation of the GLRT output after numerical strength reduction is minor. Detection performance using the database, between optimized and original structure was compared, and remained unchanged.

C. Dual Operation Mode

The R-wave detector in [12] is designed to assure good detection performance when the EGM is corrupted with noise, see Fig. 13 shown later. However, during long periods the pacemaker patient is not exposed to noise, e.g., during sleep (rest), low physical activity, etc. Therefore, it is highly desirable to automatically shut off parts of the R-wave detector during such periods to save power. At the same time the R-wave detector must be able to operate with full noise suppression performance whenever necessary. Operation when the patient is not exposed to noise is referred to as normal mode as this is the case most of the time. Alert mode is when the entire filterbank and GLRT are active.

One approach is to shut off one or two branches in the wavelet filterbank during normal mode. Thus, it is also possible to shut off parts of the GLRT with respect to the inactivated branches in the filterbank. Section IV-C presents a performance analysis of how the branches are activated or deactivated in alert and normal mode, respectively. The parts of the R-wave detector being shut off in normal mode are triggered by a gated clock [35]. This clock tree is enabled by the noise detector. Another
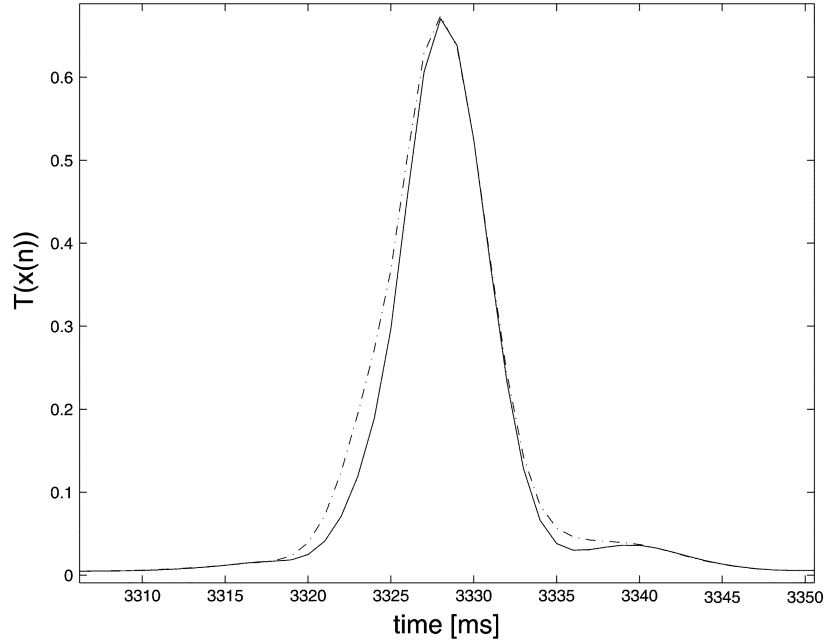
Fig. 11.   Decision signal $T(n)$ computed for floating-point values (solid line) and integer values (dashed line).

alternative to consider is a time-multiplexed architecture, however, this leads to a more complex control structure and a higher operating frequency.

In order to make the R-wave detector resilient to noise, a noise detector has been supplemented, see Fig. 7. The noise detector operates in supervision mode and guarantees full noise suppression performance by reactivating the hardware that has been shut off during normal mode. The power savings gained by deactivating parts of the R-wave detector must not be dissipated by the noise detector since the proposed modification would then lack significance. Therefore, it is necessary to design a low-complexity noise detector.

D. Noise Detector

In this study, noise quantification is based on a zero-crossing rate measurement $Z_S(n)$ [36]; the number of zero crossings is the number of times a sequence changes sign. The $Z_S(n)$ measurement on all the recordings in the database show that an typical upper bound for a patient ranges from 5 to 7 zero-crossings during 100 ms.

If the input signal has a dc component, a zero-crossing measurement cannot be carried out correctly. Therefore, any dc component of an EGM is filtered out before $Z_S(n)$ is estimated by a differencing filter as

$$d(n) = x(n) - x(n-1) \qquad (13)$$

which has a low complexity implemented in digital hardware. The zero crossing measure in the long term, i.e., from 0 to ∞, is defined as [36]

$$Z_D = \frac{1}{2} \sum_{n=0}^{\infty} |\text{sgn}\{d(n)\} - \text{sgn}\{d(n-1)\}| \qquad (14)$$

where

$$\text{sgn}\{d(n)\} = \begin{cases} +1, & d(n) \geq 0 \\ -1, & d(n) < 0. \end{cases} \qquad (15)$$

In order to define a short-term $Z_S(n)$, (14) can be used as

$$Z_S(n) = \frac{1}{2N} \sum_{m=n-N+1}^{n} |\text{sgn}\{d(m)\} - \text{sgn}\{d(m-1)\}| \qquad (16)$$

where N is the length of the short-term interval. Since most zero-crossings occur during an R-wave, the length of N needs to be longer than this interval, usually no longer than 100 ms [4]. However, to achieve a flexible implementation N is a programmable parameter in the target implementation.

E. Noise Detector Implementation

A zero crossing can be identified by comparing the signs of two successive samples computed in (13). Using digital hardware and two's complement representation the comparison can be carried out by analyzing the most-significant-bit (MSB) which indicates the sign of a number. A zero crossing has occurred if

$$\text{MSB}\{d(n)\} \oplus \text{MSB}\{d(n-1)\} = 1$$

where $\oplus$ is the XOR function. The number of zero-crossings, indicated by a low to high transition at the XOR gate, is accumulated for the time N, see Fig. 12. Noise is detected when $Z_S(n)$ exceeds an upper bound $\hat{Z}_S$, causing the R-wave detector to switch to alert mode. $\hat{Z}_S$ differs for every patient and needs to be programmed during pacemaker surgery or check-up. The Z_S-accumulator is reset after N samples are processed to start a new Z_S determination for the next input sequence. Thus, a counter that provides a reset signal after N samples is needed in addition to the schematic in Fig. 13. The Z_S-accumulator is implemented by a register and an adder. The simple noise detector

Fig. 12. Zero-crossing detector logic.

Fig. 13. (a) EGM recording distorted by an ac hand drill (20-dB SNR). (b) Output $T(n)$ of the GLRT.

structure results in very little area and power overhead when implemented in digital hardware. More sophisticated alternatives can be considered but would result in higher complexity.

IV. DETECTION PERFORMANCE

The performance of the implemented detector is analyzed by adding various interferences to the EGM recordings such that different signal-to-noise ratios (SNRs) are obtained. Detection performance is measured by computing the probability of missed detection P_D and false alarms P_{FA} as

$$P_D = \frac{N_T}{N_T + N_M} \quad \text{and} \quad P_{FA} = \frac{N_{FA}}{N_T + N_{FA}} \qquad (17)$$

where N_T is the number of true detections, N_M the number of missed detections, and N_{FA} the number of false alarms. A true detection is defined as an event that occurs within 50 ms of the annotation, whereas events outside this interval are declared as false alarms.

A. SNR Definition

The analyzed signal consists of the nonstationary EGM, $x(n)$, to which a noise signal, $v(n)$, has been added. The SNR of $y(n)$ is defined as

$$\text{SNR} = 20 \cdot \log \frac{V_x}{\sigma_V}, \qquad (18)$$

where V_x is the average peak-to-peak amplitude of all the R-waves in one EGM recording and σ_V the standard deviation of the noise to be added. The peak-to-peak amplitude V_x is calculated according to

$$V_x = \frac{1}{N_x} \sum_{i=1}^{N_x} \left| \max_{-50 \leq m \leq 20} \{ x(R_i + m) \} \right| \\ + \left| \min_{-50 \leq m \leq 20} \{ x(R_i + m) \} \right| \quad (19)$$

where $x(R_i)$ is a vector containing an R-wave positioned at R_i, and N_x is the number of R-wave templates. The standard deviation σ_V is calculated according to

$$\sigma_V = \sqrt{\frac{1}{N_v} \left(\sum_{i=1}^{N_v} v(i) - \bar{v} \right)^2} \qquad (20)$$

where $\bar{v}$ is the mean of the noise signal and N_v the number of discrete samples.

B. Detection Performance for Noisy EGMs

Although the pacemaker patient is mostly exposed to low-noise environment, the importance of handling heavily disturbed EGMs must nonetheless be addressed. The detection performance for the circumstance when the pacemaker patient is exposed to various interferences is analyzed in this section. The EGMs are disturbed with recordings of the interference database, see Sections II-B and C.

Shape and body constitution of humans vary considerably and, therefore, it is not possible to find one single estimate of how much noise can interfere with the pacemaker. However, a SNR of 20 dB corresponds to a very high interference level which should include the worst case situation in real life. Thus, noise levels are chosen which results in SNRs of 20 and 25 dB to assure that this situation can be handled by the detector. A typical EGM that is disturbed by interference and the corresponding decision signal $T(n)$ is shown in Fig. 13.

The threshold level β is varied from 0.3 to 0.5. A low value for β produces high rates of P_D, however, P_{FA} will also increase as more false events will exceed the threshold. Contrarily, a high β leads to a lower value for P_D and P_{FA}.

It can be observed that the detector is more sensitive to interference that originates from the EAS2 system and muscular activity than from other sources, see Fig. 14. This is the case for P_D and P_{FA} for both noise levels. Interference that originates from muscle contractions is the most difficult noise to suppress in all the tested EGMs [28]. The results show that the detector attains reliable detection performance at moderate to low SNRs. For 20-dB and 25-dB SNR the average performance for all noise sources is $P_D = 0.88$ and $P_{FA} = 0.13$ and $P_D = 0.98$ and $P_{FA} = 0.014$, respectively. Moreover, a threshold level that strikes a good balance between P_D and P_{FA} is $\beta = 0.4$.
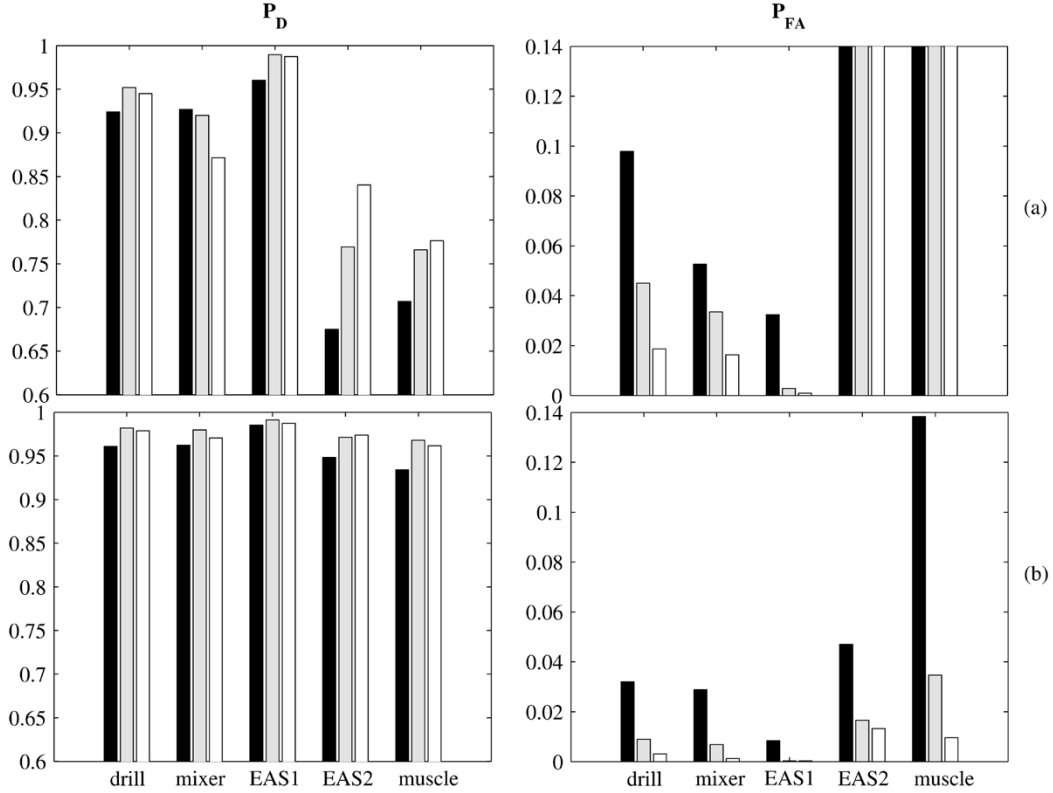
Fig. 14. Means of detection performance in terms of P_D and P_{FA}. The recordings from the EGM database are disturbed with interferences originating from a hand drill, mixer, EAS1, EAS2 and muscle contraction. The applied noise results in SNRs of (a) 20 and (b) 25 dB. The threshold level β is set to following values: 0.3 (black bars), 0.4 (grey bars), 0.5 (white bars).

TABLE IV
DETECTION PERFORMANCE FOR NOISELESS CASE. MODE COLUMN
INDICATES WHICH BRANCH IS OPERATES, $\beta = 0.4$

Mode	P_D	P_{FA}
001	0.973	0.021
010	0.997	0.001
011	0.972	0.020
100	0.997	0.001
101	0.994	0.021
110	0.997	0.001
111	0.997	< 0.001

C. Detection Performance for Normal Mode

The pacemaker is mostly operating in a low-noise environment and, therefore, a performance analysis is carried out where no additional noise is added to the EGM. The threshold level β is 0.4. The total number of 3200 events for all the recordings in the EGM database has been analyzed.

In order to find out which branches of the filterbank can be shut off without performance degradation for all recordings in the EGM database, the branches have been activated in different combinations, see Table IV. The mode of a single branch, active or inactive, is binary coded. If a branch is active it is coded as 1 in a 3 digit word, e.g., 110 indicates that branch one and two $(q = 2, 3)$ are active while three $(q = 4)$ is inactive. However, as the branches are connected in series it is not possible the entirely shut off the first branch if the second or third branches is active, see Fig. 7. For such cases, only the filtering part $G_b(z)$ of the preceding branches are shut off, see Fig. 8.

The average detection and false alarm rate P_D and P_{FA}, respectively, is presented in Table IV. In none of the simulated cases, the detection performance drops below 0.97 whereas the highest P_{FA} rate is less than 0.021, for a threshold level $\beta = 0.4$. The highest detection and lowest false alarm rates, P_D and P_{FA}, are obtained if all branches, i.e., 111, in the filterbank are operating, >0.99 and <0.001, respectively. However, the difference between 111 and 100 is negligible as only a minor difference for P_{FA} is measurable. Furthermore, it is possible to shut off block three to six in the GLRT, whereas block one and two operate partially, see Fig. 7. As the first branch has to operate partially in all the combinations it is of further advantage to inactivate filterbank two and three since the amount of hardware that can be shut off is higher compared to other combinations.

In the target implementation, not all presented modes will be implemented. Only two modes will be considered, 100 for the normal mode and 111 for the alert mode.

1) Noisy Signal in Normal Mode: The noise detector reactivates branch two and three if the EGM is corrupted by noise, and, thereby, sustains filtering performance. Nevertheless, it is of interest to analyze detection performance for the circumstance that noise is present but not indicated by the noise detector. To evaluate detection performance for such a circumstance, noise is added (25-dB SNR) to the recordings in the EGM database. The situation that no noise is detected is simulated by a forced normal operation mode, i.e., branch two and three are permanently off. Detection performance is analyzed by computing P_D and P_{FA} for $\beta = 0.4$ for all the recordings in the database, see Table V. It can be seen that performance degrades

mode	normal		alert	
Noise	P_D	P_{FA}	P_D	P_{FA}
-	0.997	0.001	0.997	< 0.001
drill	0.926	0.083	0.982	0.009
mixer	0.983	0.019	0.980	0.007
EAS1	0.975	0.024	0.991	0.003
EAS2	0.513	0.082	0.970	0.016
muscle	0.960	0.083	0.970	0.034

if the EGM is disturbed and the R-wave detector continues the normal mode operation. The P_D rate for EAS2 drops to ~ 0.52 which is unacceptable. Thus, it is necessary to switch to alert mode and to reactivate branch two and three to sustain reliable performance.

V. POWER CONSUMPTION

The power consumption of a digital ASIC is defined as

$$P = P_{\text{dyn}} + P_{\text{dp}} + P_{\text{leak}} \qquad (21)$$

where P_{dyn} is the switching power, P_{dp} the direct-path power, and P_{leak} the leakage power [37]. For a long time, dynamic power consumption has been the dominant source whereas leakage power has been ignored for most applications. However, with shrinking technology and decreasing threshold voltage V_t, P_{leak} represents a substantial or dominant share of the total power. Leakage power is consumed as long as the supply voltage is switched on, regardless of the switching activity. For the presented design leakage power is the main contributor due to the low clock frequency and correspondingly low switching activity.

A. Gated Supply Lines

The R-wave detector is operating at a low clock frequency of 1 kHz, implying that leakage power will have a large share of the total power consumption. To reduce the leakage current effectively three approaches can be applied: a multithreshold CMOS (MTCMOS) process, transistor stacking or the combination of transistor stacking and MTCMOS [38], [16], [39]. Using MTCMOS the design is implemented using high V_t devices for the noncritical and low-V_t devices for the critical path. Transistor stacking, on the other hand, cuts off one of the supply supply rails and thereby reduces the leakage power. This can be implemented by using a standard CMOS process without dual V_t. Combining the two techniques by using high-V_t transistors for transistor stacking will lead to a higher leakage reduction but requires extra process steps with corresponding costs [38].

The presented design has been implemented in a United Microelectronics Corporation (UMC) low-leakage process that provides high-V_t devices. Furthermore, transistor stacking is applied to achieve substantial leakage power reduction. An extra gate transistor is introduced in the leakage path and can either be placed between the power supply, V_{dd}, and the cells or between ground (GND) and the cells, see Fig. 15 [37]. The gate transistor is turned on and off in the alert and normal mode,

Fig. 15. Schematic of the gate-transistor circuit simulation; $L_P/W_P = 0.13/100, L_N/W_N = 0.13/33, L_{\text{Gate}}/W_{\text{gate}} = 0.13/33$.

respectively, and thus the cell supply voltage is gated which achieves significant leakage reduction. An extra sleep transistor reduces leakage current by orders of ten and the gate transistor can be shared among multiple cells which amortizes the area overhead of an extra transistor [37].

1) Transistor Sizing: The gate transistor must be large enough to sink the current flowing through the cells during alert mode. However, a too large transistor degrades the stacking effect and introduces an area overhead. The dimensions of a transistor that match the needs to gate a single cell can be determined analytically. Unfortunately, this is not the case if several cells with different properties are driven by one gate transistor, which is the case in the proposed design. Therefore, *Spice* level simulations are carried out to find out how leakage current is influenced by the chosen size of the gate transistor, see Fig. 15. The static resistance of a transistor can be computed as

$$R_{\{P,N\}} = \frac{L_G}{W k_p' |V_{\text{GS}} - V_t - V_{\text{DS}}|} \qquad (22)$$

where L_G is the channel length, W is the channel width, and k_p' the process transconductance, which for the provided cell library results in $R_{\{P,N\}} < 1\ \Omega$ for a 33 μm wide nMOS and a 69-μm wide pMOS transistor [37]. Thus, $R_{\{P,N\}}$ is negligible compared to the wire resistance for power routing.

B. Leakage Reduction Estimation

In order to find an estimate for leakage reduction, the schematic in Fig. 15 is used, since gate transistors cannot be included in a gate level power-simulation. The number of equivalent inverter cells with respect to the R-wave detector hardware that is shut off needs to be determined. Therefore, the number of cells to shut off in normal mode and their corresponding leakage power are identified. A brief overview of these cells is presented in Table VI. This overview represents 88% of the hardware being shut off in normal mode, and is considered to be sufficient to determine the sleeping hardware leakage in this simulation. In order to be consistent with the schematic in Fig. 15, the leakage power of the cells in Table VI is interpolated to the leakage power using only inverters, e.g., an AND2 cell has 20% higher leakage than an INV cell, thus 91 AND2 cells are approximated by 109 INV cells. Thus, an equivalent leakage power to the shut down part of the detector would result in ~ 4500 minimum sized inverter cells. To simplify simulation, the maximum dimension for a transistor,

TABLE VI
BRIEF SUMMARY OF CELLS THAT ARE SHUT OFF IN NORMAL MODE.
SUMMARY REPRESENTS APPROXIMATELY 88% OF IMPLEMENTED HARDWARE

	Number	I_{leak}	INV equivalent
D-latch	395	46	1211
NAND	365	11	277
NOR	329	11	241
FA	633	43	1815
XOR	61	11	45
AND2	91	18	109
INV	791	15	791
total	2665	-	4489

TABLE VII
LEAKAGE CURRENT REDUCTION (RED.) USING GATED V_{dd} AND GATED
GROUND. LOAD IS NUMBER OF CELLBLOCKS THAT ARE SUPPLIED BY
GATE-TRANSISTOR. $W_P = 100\,\mu$m, $W_N = 33\,\mu$m, $L_P = L_N = 0.12\,\mu$m,
$W_G = 33\,\mu$m, L : # INVERTERS IN FIG. 15

	PMOS			NMOS		
L	I_{gl1}[nA]	I_{l1}[nA]	Red.	I_{gl1}[nA]	I_{l1}[nA]	Red.
1	46.4		85 %	50.1		84 %
2	27.6	317	91 %	32	317	89 %
5	18.4		94 %	15		95 %
10	12.5		96 %	7.9		97 %

TABLE VIII
CORE POWER ESTIMATION AT GATE LEVEL USING A 0.13-μm
LOW-LEAKAGE LIBRARY. $F = 1$ kHz, $V_{dd} = 1.2$

	Alert [nW]	Normal [nW]	Reduction
dynamic	24.6	6.8	72 %
short-circuit	22.1	6.1	72 %
leakage	67.8	< 25	> 63 %
total	114	< 38	> 67 %

restricted by the simulation tool, is used, which is 625 times the minimum size. The number of maximum sized transistors is indicated by the load factor (L). With the equivalent number of inverters estimated in Table VI the load can be approximated by 7. The width of the gate transistor in Fig. 15 is set to 33 μm and loaded with an increasing number of balanced inverters with the transistor dimension of $L_P/W_P = 0.13/100$ and $L_N/W_N = 0.13/33$. The width of the pMOS transistor is thrice that of the nMOS width to balance the inverter cell. The leakage current I_l is estimated for having either nMOS/pMOS of the inverter gate in on or off mode, with equal likelihood. The average of these measurements is presented in Table VII, where I_{gl1} and I_{l1} is the gated leakage current and the non-gated leakage current, respectively. Simulation on *Spice* level results show that the leakage reduction rate increases with the number of inverters driven by the gate transistor. As presented in Table VII, gated-ground is more suitable if a large number of cells will be shut off, and the area overhead for a nMOS gate transistor is 52% smaller compared to the pMOS solution. Thus, gated ground is chosen for this silicon implementation. The expected leakage reduction is approximately 96% according to the simulation results presented in Table VII.

C. Gate Level Power Estimation

In order to confirm the expected power savings, the power dissipation of the two modes is estimated on gate level [40]. Since sleep transistors cannot be included in a gate level simulation, results of the leakage reduction estimation in Table VII are used. The power estimation in normal mode is carried out by removing the hardware that is shut off from the netlist, i.e., the hardware neither leaks nor switches. However, leakage is included in the estimate by adding a fraction, according to Table VII. Using gated ground and an estimated load of 7 results in a leakage reduction of approximately 96%. The power analysis confirms that leakage power is the dominant power source, using the provided technology and a clock frequency of 1 kHz, see Table VIII. Using solely a gated clock would not result in equal power savings since this only effects the dynamic power consumption and leakage current still exists as long as the cells are connected to the supplies. Thus, the power saving would only be 29% if no gated-supply is used. The presented estimates only serve for identification of the dissipation sources and to provide a relative measurement of the power savings. A
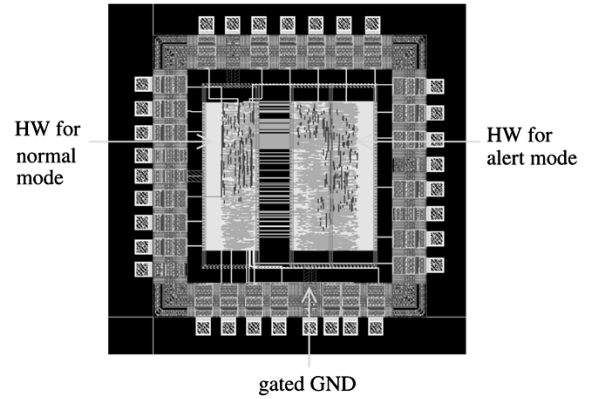

Fig. 16. Layout of the routed ASIC.

more accurate estimate will be available on the fabricated ASIC level. Due to a large time slack in the critical path it is possible to gain further power savings by lowering V_{dd}. Furthermore, as a scaled supply voltage increases the threshold voltage, a reduction in leakage is expected [41]–[43]. Such low supply voltage eliminates short-circuit power as V_{dd} is expected to be below $V_{tn} + V_{tp}$ [37].

However, such estimates cannot be obtained in the current gate-level simulation. The ASIC core is expected to operate in the 100 nW region in the target implementation.

D. Placement and Routing

The ASIC core consists of two regions with shared V_{dd} and two independently routed GND supplies. The sleep-transistors that gate GND supply are implemented between the GND core-ring and power-supply pad. The transistor gates are connected to the alert signal and thereby shut off the transistors in normal mode. The total chip area, inclusive pads, is 1 mm^2 with 7842 gates using a 0.13-μm UMC process, see Fig. 16. The ASIC has been sent for fabrication and further power analysis will be carried out in the future.

The design is pad-limited as various control signals are fed to the IOs for verification purpose. These control signals are not needed in the target implementation and therefore is it possible to reduce the chip size significantly. Moreover, the sleep transistors can be accommodated in the supply pads which results in further area reduction.

VI. CONCLUSION

The implementation of a wavelet-based R-wave detector in 0.13-μm low-leakage UMC technology has been presented in this paper. The design has been power optimized by applying strength reduction, as well as wordlength and register minimization. The inclusion of a noise detector facilitates a dual operation mode. Thus, 2/3 of the hardware can be shut down if the pacemaker patient is at rest or not exposed to interferences (normal mode). Reliable detection performance is sustained by reactivating the sleeping hardware whenever necessary.

Gate transistors in the GND supply lines are used to address the dominating leakage power and to effectively reduce the power consumption when operating in normal mode. Gate-level power estimation predicts 67% power savings if operating in normal mode; no performance degradation is measurable for such cases. The total chip area is 1 mm^2 and is expected to operate in the 100 nW range.

The ASIC has been fabricated in 0.13-μm UMC low-leakage technology and further performance measures as well as power analysis will be carried out.

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