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Al_2O_3/InAs metal-oxide-semiconductor capacitors on (100) and (111)B substrates

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The influence of InAs orientations and high-k oxide deposition conditions on the electrical and structural quality of Au/W/Al_2O_3/InAs metal-oxide-semiconductor capacitors was investigated using capacitance-voltage (C-V) and x-ray photoemission spectroscopy techniques. The results suggest that the interface traps around the conduction band edge are correlated to the As-oxide amount, while less to those of As-As bonds and In-oxides. The quality of the deposited Al oxide determines the border trap density, hence the capacitance frequency dispersion. The comparison of different processing conditions is discussed, favoring a 350 °C high-k oxide deposition on (111)B substrates followed by an annealing procedure at 400 °C. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3698094]

III-V semiconductors with high-k dielectrics are attracting increasing interest for high-speed and low power electronics. Besides the well studied GaAs, a growing attention has in recent years been paid to the other materials of the III-V family such as the binary InAs which exhibits superior transport properties.[1] The quality of the oxide layer and the semiconductor oxide interface is of crucial importance for the device performance[2] targeting good subthreshold characteristics, high transconductances, and the large drive-current. The presence of the native oxides is believed to generally degrade the electrical properties of the gate dielectrics.[3–7] Although much effort in recent years has been made to study the electrical properties[2,7] and the amount of different native oxides[8,9] using C-V and x-ray photoemission spectroscopy (XPS) measurements, further studies related to the influence of the InAs orientation and high-k deposition conditions on the metal-oxide-semiconductor (MOS) performance are required. In particular, studies on (111)B-oriented substrates are important as it has been identified that the In-oxides are less effectively reduced, which makes As-terminated surfaces attractive. Furthermore, they serve as an important reference for zincblende InAs nanowires[10,11] grown by the vapor-liquid-solid (VLS) method, where (111) microfacets are found to dominate the surface.

In this work, we combine electrical measurements with XPS characterization to study metal/Al_2O_3/InAs MOS capacitors with different InAs orientations and oxide deposition temperatures. The results indicate that the interface traps around the conduction band edge are correlated to the amount of AsO_x, and generally a lower amount of interfacial oxides leads to a lower interface trap density D_{it}. The effectiveness of the In-oxide reduction at various temperatures is also found to depend on the surface termination, but only very weakly on the deposition temperature. Meanwhile, an additional annealing at 400 °C in the forming gas is found to suppress the amount of interface traps. The results also show that the border traps[12,13] mainly reside inside the Al oxide and can be reduced by using lower deposition temperatures and higher annealing temperatures.

MOS capacitors were fabricated on InAs substrates with two different orientations (100) and (111)B with comparable n-type doping densities of $3.5 \times 10^{16}/cm^3$ and $7.5 \times 10^{16}/cm^3$, respectively. The InAs substrates were pre-treated with HCl:H_2O (1:1) for 60 s and rinsed in isopropanol for 15 s. 80 cycles of Al_2O_3 (24 cycles for XPS measurements) were grown using trimethylaluminum and water as precursors at deposition temperatures of 200 °C, 250 °C, and 350 °C in a Cambridge Nanotech Savannah-100 ALD chamber starting with a Al-pulse. W/Au contacts were fabricated by sputtering combined with optical lithography and followed by dry/wet etching of the metals. The electrical properties were measured at room and liquid nitrogen temperatures[7] using a Keithley 4200 parameter analyzer and a 4294 A impedance analyzer. The interface properties of reference samples with 24 cycles of Al_2O_3 were measured using XPS at beam-line I311 of the MAX-II synchrotron.[9]

Figures 1(a) and 1(b) show the measured, room temperature, multi-frequency C-V curves of the (111)B and (100) deposited at T = 350 °C. A stronger C-V modulation for the (111)B sample is clearly visible, indicating a lower amount of interface traps. Figures 1(c) and 1(d) show the 1 kHz curves of the (100) and (111)B samples with different deposition conditions. For both cases, a stronger C-V modulation is observed for increasing the deposition temperature. To quantify these trends, the D_{it} levels were extracted using a low frequency fitting method[14] from the 1 kHz data at room temperature and conductance measurements at T = 77 K. The extracted values are shown in Figure 2. For trap levels around the conduction band edge, the D_{it} levels are seen to decrease with increasing the deposition temperature, with a stronger reduction for the (111)B sample, especially for the T = 350 °C sample. The lowest D_{it} value is around 2×10^{12} $cm^{-2}eV^{-1}$ at E_t - E_c = 0.2 eV. Close to the valence band edge (−0.3 eV), the D_{it} levels remain fairly high, around

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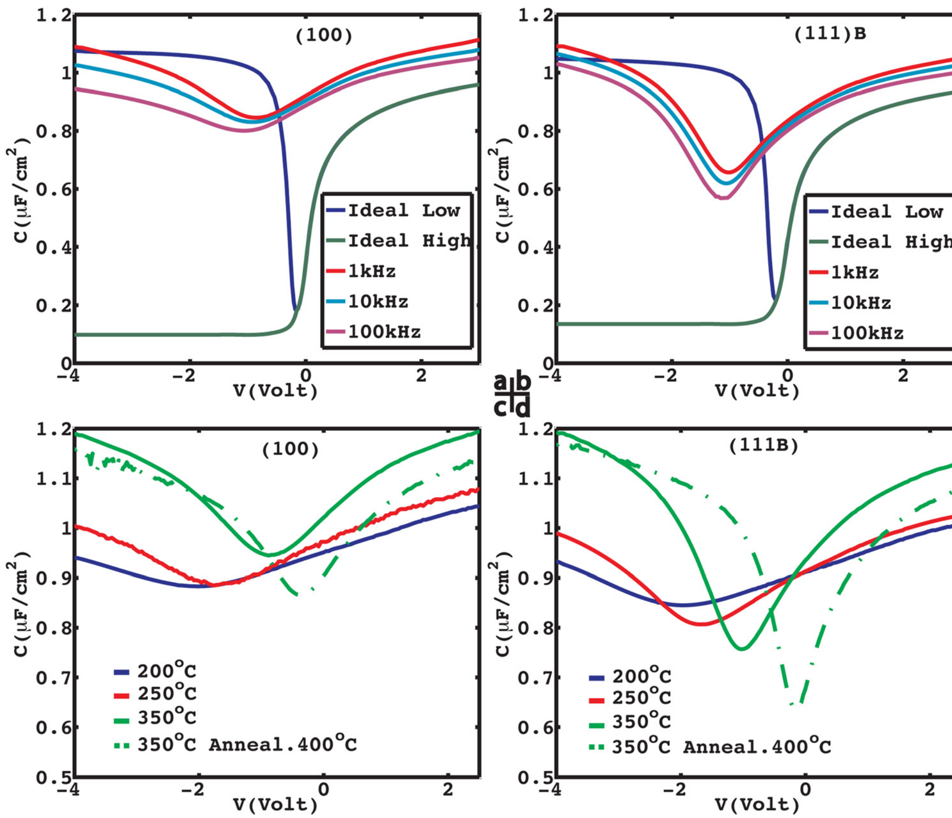

FIG. 1. Comparison of measured and simulated device C-V characteristics of (a) (100) and (b) (111)B samples with the deposition temperature being 350 °C. The effective oxide thickness used in the simulation is 6.45 nm for (100) and 6.62 nm for (111)B, respectively. [(c)–(d)] Comparison of the deposition temperature and annealing influence on the 1 kHz C-V characteristics of (100) and (111)B samples.

$2-3\times10^{13}$ independent of deposition temperatures. D_{it}-levels extracted by the Terman method[15] and conductance method[16] at T = 77 K show similar results. The G_p/ω measurement yields a magnitude lower D_{it} (at E_t - E_c = 30 meV), around $1-1.5\times10^{12}$ cm^{-2} eV^{-1} for the (100) samples, and $0.5-1\times10^{12}$ cm^{-2} eV^{-1} for the (111)B samples. This large discrepancy between the results obtained from two electrical methods can in part be explained by the omission of potential fluctuations[16] in the conductance method used, and that the defect densities extracted from the C-V curves are a mixture of interface and border traps.

In order to reveal the cause for the different D_{it} values, we used XPS to characterize the interface. Figure 3(a) shows different components of the fitted As 3d spectra (In 3d spectra not shown), from which the native oxide thickness is extracted (d). The In-oxide is found to dominate the native oxide layer in agreement with a previous study,[8] which may explain the preference for the As-terminated (111)B-surface for the MOS capacitors. The amount of In-oxides after ALD deposition is essentially independent of the ALD temperature, but lower for the (111)B sample. The As-oxides decrease with increasing the temperature for both (100) and (111)B, to levels below the detection limit ($\sim2\times10^{13}$ cm^{-2}) at T = 350 °C. Interestingly, the amount of As-oxides after ALD depositing is lower for the As-rich (111)B surface, as compared with (100) substrates. There are also substantial amount of As-As bonds (>10^{13} cm^{-2}), with a slightly lower level for (100) at T = 200 °C and with similar levels for both (100) and (111)B at T = 350 °C, a trend that is inconsistent with the C-V data. The high and constant D_{it} at the valence band edge could be related to In-oxides or to As-As bonds or As dangling bonds as suggested in Refs. 5 and 6, since the amount of As-As as well as InO_x seems to be fairly independent of the temperature. Our data thus seem to indicate that the D_{it} around E_c is mainly correlated to the amount of AsO_x that is decreasing for both orientations and with lower values for (111)B. Unlike GaAs MOS systems[3,4] where Ga-dangling bond and As-As dimer induced states are generally present near the conduction band edge and the midgap, the narrower InAs band gap may move those states far into the conduction band.[5,6] The rise of D_{it} after 0.2 eV hence could be correlated with those defect amounts. Besides, Ga_2O_3 induced states are also found near the valence band edge for GaAs, which is similar to the InAs case.

From the XPS data, we also looked for energy shifts between the (100) and (111)B samples to quantify the

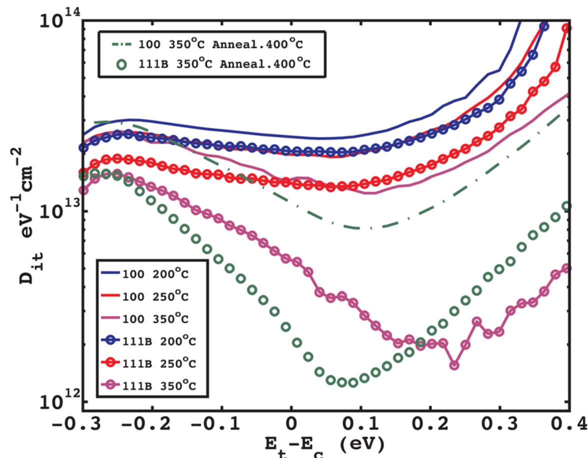

FIG. 2. D_{it} vs. E_t - E_c extracted using the low frequency fitting method (see Ref. 14) as a function of InAs orientation and oxide deposition temperature. The x-axis denotes the position of the trap level E_t in the band gap with respected to the conduction band edge E_c.

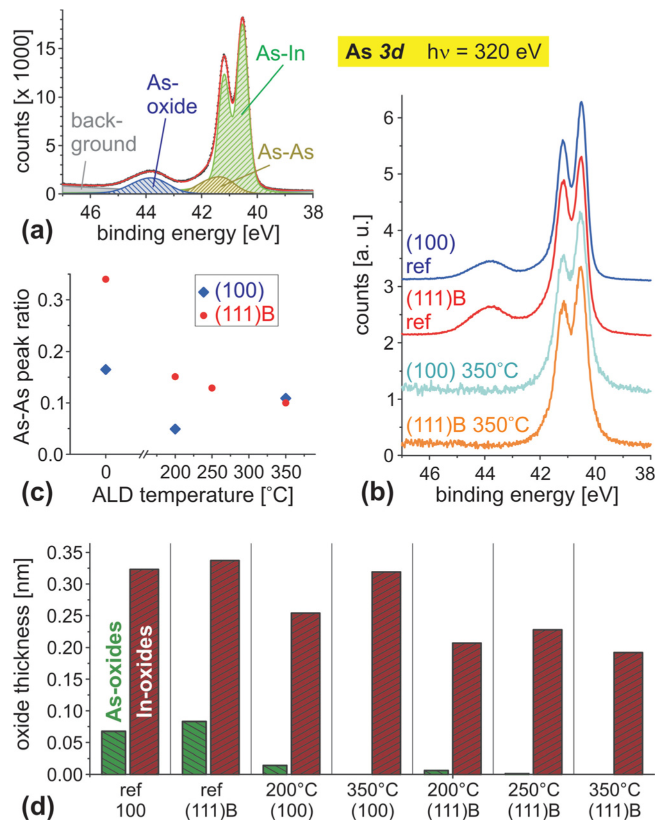

FIG. 3. XPS results from (a-c) the As 3d core-level with a photon energy of 320 eV. (a) Fitted spectrum with different components as indicated. (b) Comparison of spectra from reference samples with a native oxide layer and samples with Al_2O_3 deposited at 350 °C, for (100) and (111)B. The spectra are background-subtracted and normalized for the better clarity. (c) Relative intensity of the spectral component related to As-As bonds, as compared to the bulk InAs component, for different ALD temperatures. The value at 0 °C refers to the corresponding reference sample. From the measured XPS intensities of the oxide components in As 3 d and corresponding In 3 d spectra, the absolute thickness and the stoichiometry of the oxide film can be calculated (see Ref. 8). This is shown in (d) for the native surface oxide of reference samples and the interface oxide between InAs samples and Al_2O_3 films with different ALD temperatures.

flat-band shift. For deposition at low temperatures, the shift is found to be negligible, but as the temperature increases, the magnitude of the shift increases and a value of 90 meV is measured for the 350 °C deposition. This compares well with the data obtained from the low-f D_{it} fitting, where the (111)B sample has a ~70 meV larger surface potential as compared with the (100), for the T = 350 °C case.

The amount of border traps is studied by measuring the frequency dispersion of the accumulation capacitance as shown in Figure 4. No clear orientation dependence is found, which is consistent with the expectation that the border traps are located mainly inside the Al_2O_3 film. The measured dispersion for both orientations generally increases with the deposition temperature, differing from the trends of both the As- and In-oxides shown in Figure 3. This supports the assumption that the effect is caused by defects deeper in the oxide rather than at the interface. In addition, the frequency dispersion is found to be suppressed by decreasing the measurement temperature,[13] possibly due to a reduction in the thermally assisted tunneling to higher lying trap states.[12]

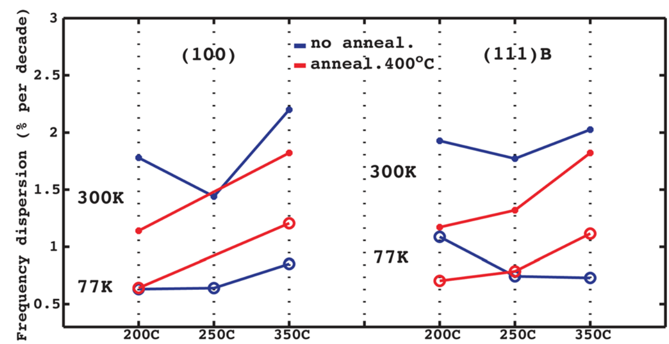

FIG. 4. Accumulation capacitance frequency dispersion at ($V_{fb}+2.3$) Volt as a function of different deposition conditions. The frequencies chosen range from 1 kHz to 100 kHz.

In conclusion, we have studied the influence of the InAs orientation and high-k oxide deposition conditions on the MOS electrical performance. We find that the (111)B samples generally show lower D_{it} than the (100) samples and that the interface defect properties are improved upon annealing at 400 °C. The XPS studies further indicate a reduction of AsO_x with increasing the ALD deposition temperature, whereas InO_x and As-As are relatively unaffected. In addition, the quality of the Al oxide layer dominates the border trap amount.

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[1]*Silicon (Si), Electro Mobility; Gallium Arsenide (GaAs), Electron Mobility; Indium Arsenide (InAs), Carrier Mobilities*, Landolt-Brnstein, New Series, Group III, edited by O. Madelung, U. Rssler, and M. Schulz (Springer, New York, 2002).
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