Embedded DfT Instrumentation: Design, Access, Retargeting and Case Studies

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Embedded DfT Instrumentation: Design, Access, Retargeting and Case Studies

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Abstract:
As semiconductor technologies enables highly advanced an complex integrated circuits (ICs), there is an increasing need to have more embedded design-for-test (DfT) instruments for test, debug, diagnosis, configuration, monitoring, etc. As these instruments are to be used not only at chip-level but also at board-level and system-level, a key challenge is how to access these instruments from chip terminals in a low-cost, non-intrusive, standardized, flexible and scalable manner. The well-adopted IEEE 1149.1 (Joint Test Action Group (JTAG)) standard offers low-cost, non- intrusive and standardized access but lacks flexibility and scalability, which is addressed by the on-going IEEE P1687 (Internal JTAG (IJTAG)) standardization initiative. We will discuss the need of embedded instrumentation, the shortcomings of IEEE 1149.1, the features and challenges of IEEE P1687, as well as cases studies on the usage of IEEE P1687.

Index Terms: IEEE P1687, IJTAG, IEEE 1149.1, embedded instruments

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Introduction:

Due to the constant increase in complexity and a decrease in feature sizes of integrated circuit (IC) designs, there is need of on-chip (embedded) instruments for test, debug, diagnosis, configuration, and monitoring. These is obviously a need of an access method for these instruments. It is desirable that the access method has *low-cost* in terms of added silicon, is *non-intrusive* such that it does not impact the regular functionality, and is *standardized* to ease integration of instruments from various vendors and to ease access of instruments in the final IC. It is also desirable that the access method is *flexible* such that instruments can be accessed in an arbitrary manner and *scalable* such that a high number of instruments can be added without a too high overhead penalty.

The IEEE Standard 1149.1 (a.k.a. JTAG (Joint Test Action Group)) [1], originally intended for board test, has proved to be useful in ad hoc access to on-chip infrastructure [2]. However, there is a lack of flexibility and scalability.

The IEEE P1687 standard proposal [2], [3], [4], [5], [6] aims to address the need of standardization, by describing a flexible data transport infrastructure (called *network*) to interface JTAG to the chip internal instruments. P1687 has therefore received the informal name of Internal JTAG (IJTAG). When ratified, IEEE P1687 will specify methods for access and control of embedded instruments [3]. An instrument refers to any device that could be included in the JTAG scan- path. Examples of instruments include embedded sensors, internal scan-chains and IEEE standard 1500 wrapped cores. P1687 is characterized by a hardware component called Segment Insertion Bit (SIB). The use of SIBs makes it possible to create a multitude of different networks for the same set of instruments, and to have the benefit of flexibility in scheduling the

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access to those instruments. To setup the scan-path, P1687 proposes to transport SIB control data together with instrument data on a single wire (the JTAG scan- path), and this will affect overall access time (OAT).
The work on IEEE P1687 is on-going and not yet ratified, and only a few studies have considered it [4], [7], [8], [9], [10]. We will discuss and compare JTAG and IJTAG from a hardware perspective, and elaborate on challenges related to the introduced flexibility and scalability.

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