Test Planning for Core-based 3D Stacked ICs under Power Constraints

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***Abstract*—Test planning for core-based 3D stacked ICs under power constraint is different from test planning for non-stacked ICs as the same test schedule cannot be applied both at wafer sort and package test. In this paper, we assume a test flow where each chip is tested individually at wafer sort and jointly at package test. We define cost functions and test planning optimization algorithms for non-stacked ICs, 3D SICs with two chips and 3D SICs with an arbitrary number of chips. We motivate the problem by demostrating the trade-off between test time and hardware, within a power constraint, while arriving at the minimal cost.**

***Index Terms*—Test Scheduling, Power Constraint, 3D stacked IC, JTAG.**

I. Introduction

3D stacked ICs (3D SICs) are emerging and have attracted a fair amount of research [1]–[6]. As the cost of test, which is highly related to test time and the additional design-for-test (DfT) hardware, accounts for a considerable part of the total manufacturing cost, it is important to develop a test plan minimizing the overall test cost. The testing of non-stacked ICs is well-defined; each IC is tested twice during the manufacturing process: during wafer sort, the bare chip (die) is tested, and during package test, the packaged IC is tested. For non-stacked ICs, the same tests are applied to the chip both during wafer sort and package test; hence, the same test schedule is used twice. However, for testing 3D SICs it is different. First, the test-flow is not well-defined. For 3D SICs, there are more test alternatives; testing can be performed on each individual IC, partial stacks, and/or the final stack [7]. Second, as the number of tests are different in each of these steps, test schedules are to be developed for each step (each individual IC, partial stacks, and the final stack), which is the focus of this paper.

Much work on test scheduling for non-stacked ICs have been performed [8]–[11]. For example, Chou *et al.* proposed a test scheduling technique that organized the tests in sessions such that the test time is minimized while power constraints are met [9]. Muresan *et al.* [8] proposed a test scheduling technique with the same optimization goal as Chou *et al.* While, the test architecture is unclear in the approach by Muresan *et al.* [8], Iyengar *et al.* [12]–[14] and Marinissen *et al.* [15] proposed test scheduling techniques and test architecture optimization for IEEE 1500. However, no work has addressed test scheduling in an IEEE 1149, under power constraint.1 environment. An increasing amount of work address testing of 3D SICs [1]–[4], [7], [16], [17].

In our previous work [7], we have defined a cost efficient test flow, while maximizing the yield. The test flow proposes that each individual IC is tested individually and then the complete stack is tested [7]. Marinissen *et al.* accounted for the variations in hardware required for various test schedules, although the overall test cost has not been optimized [16]. DfT hardware optimization has been addressed in [15], [18]–[20]. However, no work has addressed test scheduling for scan tested core based ICs under power constraints. And, no work has defined test cost models and test planning algorithms that optimizes the overall test cost for 3D SICs in an IEEE 1149.1 environment.

In this paper, we assume the test flow that we introduced in our previous works [7], [21], an IEEE 1149.1 environment, and we define test cost functions and test planning optimization algorithms for non-stacked ICs, 3D SICs with two chips and 3D SICs with an arbitrary number of chips.

The rest of the paper is organized as follows. In Section II, the JTAG test architecture assumed in our work is detailed. The problem definition is in Section III. In Section IV, we show a motivational example on the test scheduling problem for 3D SICs. The proposed test scheduling techniques are in Section V. The paper is concluded in Section VI.

II. Test Architecture

The test architecture of a non-stacked IC, that has been assumed in this paper, is shown in Fig. 1. A chip is considered to consist of a number of cores that are accessed by an on-chip JTAG infrastructure [7]. The JTAG test access port (TAP) may have up to five terminals, namely Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), Test Clock (TCK) and an optional Test Reset (TRST). In Fig. 1 only the TDI and TDO pins are shown, as the test interface terminals. Each core on a chip is accessed by the JTAG TAP via test data registers (TDRs). One TDR may be used to connect multiple cores on a single chip. In Fig. 1, the IC contains three cores: Core1, Core2 and Core3. Core1 and Core2 share a common TDR, while Core3 has an exclusive TDR. Only one TDR can be accessed at a time. Thus, if tests for more than one core of a chip are to be executed concurrently, in a session, as shown in Fig. 2, these cores are to be connected in series on the JTAG interface in one TDR. Since, Core1 and Core2 are tested in

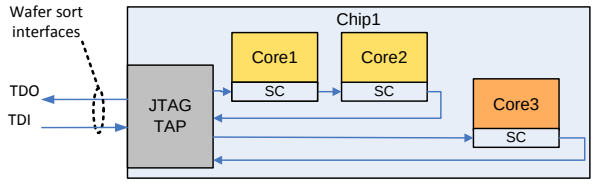

Fig. 1. Test architecture of a non-stacked chip with JTAG

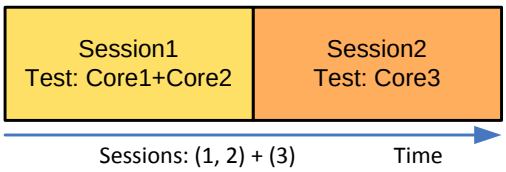

Fig. 2. Sessions formed by core tests

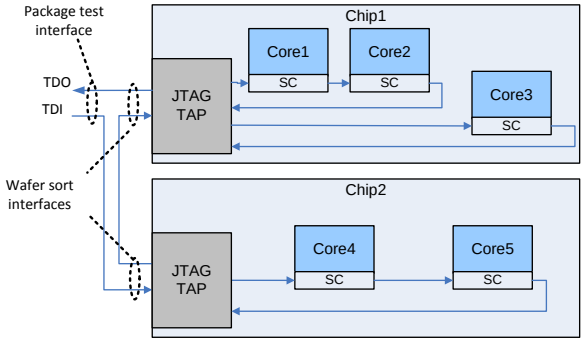

Fig. 3. Test architecture of 3D SIC with JTAG

the same session, denoted by $(1 + 2)$, as in Fig. 2, the two cores are connected to the JTAG TAP by the same TDR, as seen in Fig. 1. Correspondingly, in Session2, denoted by (3), only Core3 is tested, which is connected to the JTAG TAP by a single TDR.

During package test of the 3D SIC, the TDO of the lower JTAG TAP in the stack serves as the TDI of the JTAG TAP of the chip on top. The TDO of the topmost chip is directed out via TSVs. The TDI of the lowermost chip and the TDO of the topmost chip serve as the package test interfaces as shown in Fig. 3. A session of tests from one chip can be performed concurrently with a session of tests from another chip by selecting the corresponding TDRs by the respective on-chip JTAG TAPs of to the two chips.

III. Problem Definition

In this section the test cost for non-stacked IC, 3D SIC with two chips in the stack and 3D SIC with N chips in the stack, are defined. The overall objective is a test plan with a minimal cost in terms of test application time (TAT) and hardware (number of TDRs), defined as:

$$Cost(TAT, TDR) = \alpha \cdot TAT + \beta \cdot TDR \tag{1}$$

where, α and β are constants set by the designer depending on the particular system.

A. Non-stacked IC

For a non-stacked IC with C cores, we assume for a core c_{ij}, $1 \leq i \leq C$, $1 \leq j \leq S$, having a scan chain of length l_{ij} and requiring p_{ij} test patterns. The power required by the core during testing is given by w_{ij}. The test time for a core c_{ij} is given by:

$$Time(c_{ij}) = (l_{ij} + \delta) \cdot p_{ij} + l_{ij} \tag{2}$$

where, δ accounts for the number of clock cycles required by the JTAG for apply and capture, which is equal to 5.

A test schedule for the C cores consists of S sessions, where each core c_{ij} belongs to an unique session s_j. The number of cores that are tested in a session s_j is given by the set M_j. The test time T_j for a session s_j is denoted by:

$$T_j = \left(\delta + \sum_{\forall i \in M_j} l_{ij} \right) \cdot max_{\forall i \in M_j}(p_{ij}) + \sum_{\forall i \in M_j} l_{ij} \tag{3}$$

The power dissipated while testing the session s_j, is given by w_j, the sum of the power required by all the cores tested in the session:

$$w_j = \sum_{\forall i \in M_j} w_{ij} \tag{4}$$

The overall test time for a test schedule is given as:

$$Time = \sum_{j=1}^{S} T_j \tag{5}$$

The hardware cost is directly related to the number of sessions, since each session corresponds to a TDR; hence, $TDR = S$.

In the case of non-stacked ICs, the same schedule is applied at wafer sort and at package test; hence, $TAT = 2 \cdot Time$.

The cost function in Eq.1 is in the case of non-stacked ICs given as:

$$\begin{aligned} Cost(TAT, TDR) &= \alpha \cdot TAT + \beta \cdot TDR \\ &= \alpha \cdot 2 \cdot Time + \beta \cdot S \end{aligned} \tag{6}$$

The problem is to find a test schedule such that the TAT and the number of TDRs required result in a minimized cost within the power constraint.

B. 3D SIC with two chips in the stack

For a 3D SIC design having a stack of two chips, Chip1 and Chip2, we assume that Chip1 and Chip2 have C_1 and C_2 cores, respectively. For each core c_{1im} in Chip1, $1 \leq i \leq C_1$, $1 \leq m \leq S_1$, the length of the scan chain is l_{1im}, the number of patterns required is p_{1im} and the testing power is w_{1im}, while for each core c_{2jn} in Chip2, $1 \leq j \leq C_2$, $1 \leq n \leq S_2$, the length of the scan chain is l_{2jn}, the number of patterns required is p_{2jn}, and the testing power is w_{2jn}.

For wafer sort, Chip1 and Chip2 have test schedules with S_1 and S_2 sessions respectively. Each core c_{1im} belongs to an unique session s_{1m}, and each core in Chip2 c_{2jn} belongs to an unique session s_{2n}. The number of cores that are tested in a session s_{1m} (s_{2n}) is given by the sets M_{1m} (M_{2n}). The test time T_{1m} for a session S_{1m} session is denoted by:

$$T_{1m} = \left(\delta + \sum_{\forall i \in M_{1m}} l_{1im}\right) \cdot max_{\forall i \in M_{1m}}(p_{1im}) + \sum_{\forall i \in M_{1m}} l_{1im} \tag{7}$$

and the test time T_{2n} for a session S_{2n} session is denoted by:

$$T_{2n} = \left(\delta + \sum_{\forall j \in M_{2n}} l_{2jn}\right) \cdot max_{\forall j \in M_{2n}}(p_{2jn}) + \sum_{\forall j \in M_{2n}} l_{2jn} \tag{8}$$

The power dissipated while testing the session S_{1m} (S_{2n}), is given by w_{1m} (w_{2n}), the sum of the power required by all the cores tested in the session:

$$w_{1m} = \sum_{\forall i \in M_{1m}} w_{ijm} \tag{9}$$

Given Eq.7, the test time for wafer sort for Chip1 is given as:

$$T_{1ws} = \sum_{m=1}^{S_1} T_{1m} \tag{10}$$

and given Eq.8, the test time for wafer sort for Chip2 is given as:

$$T_{2ws} = \sum_{n=1}^{S_2} T_{2n} \tag{11}$$

The total time taken for wafer sort is:

$$T_{ws} = T_{1ws} + T_{2ws} \tag{12}$$

For package test of Chip1 and Chip2 a test schedule with S_3 sessions is formed. Each core c_{1im} (c_{2jn}) belongs to a unique session s_{3t}, $1 \leq t \leq S_3$. The number of cores that are tested in a session s_{3t} is given by the set M_{3t}. The test time T_{3t} for a session s_{3t} is denoted by:

$$T_{3t} = \left(\delta + \sum_{\forall i,j \in M_{3t}} (l_{1im} + l_{2jn})\right) \cdot max_{\forall i,j \in M_{3t}}(p_{1im}, p_{2jn}) + \sum_{\forall i,j \in M_{3t}} (l_{1im} + l_{2jn}) \tag{13}$$

Given Eq.13, the test time for package test for Chip1 and Chip2 is given as:

$$T_{pt} = \sum_{t=1}^{S_3} T_{3t} \tag{14}$$

The TAT is given by

$$TAT_{2chip} = T_{1ws} + T_{2ws} + T_{pt} \tag{15}$$

The hardware required is the sum of the number of TDRs required, which is equal to the sum of the number of sessions during wafer sort of Chip1 and Chip2:

$$TDR = S_1 + S_2 \tag{16}$$

The overall test cost can be expressed by the following equation:

$$\begin{aligned} Cost_{2chip}(TAT, TDR) &= \alpha \cdot TAT + \beta \cdot TDR \\ &= \alpha \cdot TAT_{2chip} + \beta \cdot (S_1 + S_2) \end{aligned} \tag{17}$$

The problem is to find the test schedules for wafer sort of Chip1 and Chip2 individually, and package test for jointly testing Chip1 and Chip2 such that the TAT and the total number of TDRs required by Chip1 and Chip2 during wafer sort result in a minimized cost within the power constraint.

C. 3D SIC with N chips in the stack

The cost minimization problem for a 3D SIC with N chips forming the stack can be generalized from the two problems stated above. Any chip in the stack n_i, $1 \leq i \leq N$, has C_i cores, each denoted by c_{ijk}, each having a scan chain of length l_{ijk}, requires p_{ijk} patterns, and the power dissipated is w_{ijk}, $1 \leq j \leq C_i$. During wafer sort, the test schedule of a chip n_i has S_i sessions, each denoted by s_{ik}, for $1 \leq k \leq S_i$, with M_{ik} tests in each session. Then, we can calculate the test time T_{ik} for a session s_{ik} by

$$T_{ik} = \left(\delta + \sum_{\forall j \in M_{ik}} l_{ijk}\right) \cdot max_{\forall j \in M_{ik}}(p_{ijk}) + \sum_{\forall j \in M_{ik}} l_{ijk} \tag{18}$$

The power dissipated while testing session s_{ik}, is given by w_{ik}, the sum of the power required by all the cores tested in the session:

$$w_{ik} = \sum_{\forall j \in M_{ik}} w_{ijk} \tag{19}$$

The time taken by each chip n_i during wafer sort is

TABLE I
GIVEN L, P VALUES FOR EACH CORE OF THE 3D SIC

	Chip 1			Chip 2	
	Core1	**Core2**	**Core3**	**Core4**	**Core5**
Scan chain length (l_{ijk})	50	40	30	20	10
Patterns required (p_{ijk})	50	40	30	20	10
Power dissipated (w_{ijk})	50	40	30	20	10

TABLE II
TEST SESSION ALTERNATIVES

Cases	**Wafer Sort** (T_{ws})		**Package Test** (T_{pt})	**Total Time**	**Cost**	**No. of TDRs**
	Chip 1	**Chip 2**				
1	(1, 2, 3)	(4, 5)	(1, 2, 3)+(4, 5)	14200	15000	2
2	(1, 2, 3)	(4)+(5)	(1, 2, 3)+(4) + (5)	14100	15300	3
3	(1, 2)+(3)	(4, 5)	(1, 2)+(3)+(4, 5)	13300	14500	3
4	(1)+(2)+(3)	(4, 5)	(1)+(2)+(3)+(4, 5)	12900	14500	4
5	(1, 2)+(3)	(4)+(5)	(1, 2)+(3)+(4)+(5)	13200	14800	4
5	(1)+(2)+(3)	(4)+(5)	(1)+(2)+(3)+(4)+(5)	12800	14800	5

$$T_{iws} = \sum_{k=1}^{S_i} T_{ik} \tag{20}$$

Thus, the total time taken for wafer sort of the 3D SIC is

$$T_{Nws} = \sum_{i=1}^{N} T_{iws} = \sum_{i=1}^{N} \left(\sum_{k=1}^{S_i} T_{ik} \right) \tag{21}$$

For package test of the 3D SIC, a test schedule is formed with S_N sessions. Each core c_{ijk} belongs to a unique session s_t, $1 \leq t \leq S_N$. The number of cores that are tested in a session s_t is given by M_t. The test time T_t is denoted by:

$$T_t = \left(\delta + \sum_{\forall j \in M_t} \sum_{i=1}^{N} l_{ijt} \right) \cdot max_{\forall j \in M_t}(p_{ijt}) + \sum_{\forall j \in M_t} \sum_{i=1}^{N} l_{ijt} \tag{22}$$

Given Eq.22, the test time for package test is given as:

$$T_{Npt} = \sum_{t=1}^{S_N} T_t \tag{23}$$

Hence, the overall cost is

$$\begin{aligned} Cost_N(TAT, TDR) &= \alpha \cdot TAT + \beta \cdot TDR \\ &= \alpha \cdot TAT_N + \beta \cdot \left(\sum_{\forall i \in N} S_i \right) \end{aligned} \tag{24}$$

The problem is to find the test schedules with S_1 sessions for wafer sort of Chip1, S_2 sessions for wafer sort of Chip2, and S_3 sessions for package test for jointly testing of Chip1 and Chip2 such that the TAT and the total number of TDRs required by all the N chips during wafer sort result in a minimized cost within the power constraint.

IV. MOTIVATIONAL EXAMPLE

Here we present an example to demonstrate the variation of cost incurred due to the trade-off between test time and hardware required. Given is a 3D SIC with two chips in the stack, illustrated in Fig. 3. The lengths of the scan chains, the number of patterns required and the power dissipated for each core is listed in Table I. We assume that the maximum power constraint $w_{max} = 75\ units$, and that the cost of a single TDR is equivalent to 400 time units.

The time taken for wafer sort, T_{ws}, for the configuration shown, as in case 3, $i.e.$, Core1 and Core2 with a common TDR, forming session s_{11}, Core3 forming session s_{12}, Core4 and Core5: session s_{21} is:

$$\begin{aligned} T_{ws} &= T_{11} + T_{12} + T_{21} \\ &= max(p_{111}, p_{121}) \cdot (l_{111} + l_{121} + 5) + (l_{111} + l_{121}) \\ &+ (l_{132} + 5) \cdot p_{132} + l_{132} \\ &+ max(p_{241}, p_{251}) \cdot (l_{241} + l_{251} + 5) + (l_{241} + l_{251}) \\ &= 50 \cdot 95 + 90 + 30 \cdot 35 + 30 + 20 \cdot 35 + 30 \\ &= 6650\ time\ units\ (t.u.) \end{aligned}$$

Performing the tests in the same order on package test as in wafer sort would result in this case

$$T_{ws} = T_{pt} \tag{25}$$

Therefore the total test time becomes,

$$T = T_{ws} + T_{pt} = 6650 + 6650 = 13300\ t.u. \tag{26}$$

In this case we require three TDRs for testing the chip. Hence, we can calculate the total test cost from Eq.1:

$$\begin{aligned} Cost_{case3} &= \alpha \cdot TAT + \beta \cdot TDR \\ &= 13300 + 400 \cdot 3 \\ &= 14500\ units \end{aligned}$$

But, we observe that in the session including the tests for Core1 and Core2 that the power dissipation is $w_{11} = 50{+}40 = 90$ units, which is more than the maximum power constraint. Therefore, case3, in Table II, should not be a valid solution.

Similarly, considering separate TDRs for all five cores would give, $T = 12800\ t.u$, as shown in case6 in Table II. But, the schedule results in more sessions, thus an increased hardware cost. The total cost incurred in case6 is $Cost_{case6} = 14800$ units. In this case we can see that the maximum power dissipated in any session is $w_{11} = 50$ units. Therefore, case6 does not provide a valid test schedule.

The minimum number of sessions is obtained when during wafer sort Core1, Core2 and Core3 are in s_{11} and Core4 and Core5 are in s_{21}, while during package test all five cores are in the same session. The total time leads to $T = 14200\ t.u.$, which is significantly higher than the alternative distribution of sessions discussed above. Although, in this case, the hardware requirement is minimum. The overall cost incurred in case1 is $Cost_{case1} = 15000$, which is higher than case3 and case6 discussed above. Additionally, when Core1, Core2 and Core3 are tested in the same session, the power dissipated is $w_{11} = 50{+}40{+}30 = 120$ units, which is above the maximum power limit. Hence case1 is also disregarded.

In case2, where Core1, Core2 and Core3 are tested in session s_{11}, while Core4 is tested in session s_{21} and Core5 in session s_{22}, the cost incurred is $Cost_{case2} = 15300$ units. In this case, the maximum power dissipated in session s_{11} is, $w_{11} = 50+40+30 = 120$ units, which is above the maximum power limit. Therefore, case2 is also disregarded.

In case4, where Core1, Core2 and Core3 are tested in three different sessions, while Core4 and Core5 are tested in the same session, the total test cost is $Cost_{case4} = 14500$ units. We can see that the cost incurred in performing case4 is minimum compared to the rest of the five cases in Table II. The maximum power dissipation is $w_{11} = 50$ units, which is within the power limit.

Therefore, from the above studies on the distribution of TDRs in a 3D SIC it was seen that the test time can be reduced by increasing the number of TDRs, thereby increasing the number of sessions. Although, an increased number of sessions implies increased hardware cost. Hence, in this paper, we try to obtain a trade-off between the hardware cost and the test time, within a power constraint, in order to give the minimum total effective cost.

V. Proposed Approaches

In this section we propose three algorithms, for non-stacked IC, 3D SIC with two chips in the stack and 3D SICs with any number of chips in the stack, to arrive at a test plan which requires minimal overall test cost, in terms of TAT and the number of TDR, as defined in Eq.1.

A. Non-stacked IC

By the following steps of the algorithm we arrive at the reduced cost for non-stacked ICs.

- Given is the list of C cores c_{ij}, $1 \leq i \leq C$, in a chip, sorted by the number of patterns required p_{ij}. The length of the scan chains are denoted by l_{ij}.
- The constants of the cost function defined by Eq.1, α and β are also provided.
- Initially, TAT is set equal to the test time of core c_1.
- The number of sessions, S is initially set equal to one. The first session, S_1, in the test schedule contains the test of core c_{1j}. Core c_{1j} is then removed from the sorted list.
- Each core c_{ij}, remaining in the sorted list, is descended in the following way:
  The power of each session is calculated after including the test of core c_{ij} and then is compared to the power constraint. If the power of the session is within the defined power limit, then the increase in TAT for each core c_{ij} is calculated by including it in all existing sessions. If the cost of a single TDR is less than the cost incurred by including the core test in any of the existing sessions due to the increased test time, the core test forms a new session.
  Once the core is assigned a session, it is excluded from the sorted list.
- The test plan is achieved when test of each core c_{ij}, $1 \leq i \leq C$, has been assigned its respective session S_j.

B. 3D TSV-SIC with two chips in the stack

The wafer sort test schedules for the two chips forming the 3D TSV-SIC, Chip1 and Chip2 are obtained by applying the algorithm for test scheduling of non-stacked ICs. The test planning algorithm for package test is discussed below:

- Given is the list of the test time taken by S_1 sessions of Chip1 and S_2 sessions of Chip2, denoted by T_{1m} and T_{2n} respectively.
  The lists of sessions of Chip1 and Chip2, S_{1m} and S_{2n}, are sorted in descending order of their test times, T_{1m} and T_{2n}.
- The test schedule for the package test is obtained by sequentially initiating the sessions S_{1m} and S_{2n} for all $m = n$, if the power constraints are met. Otherwise, they are performed in different package test sessions. The total number of sessions during package test is S_1 if $S_1 > S_2$, and S_2 otherwise.
- The reduction in test time for each new session formed during package test of the two chip 3D TSV-SIC is the test time of the session S_{1m}, if $S_{1m} < S_{2n}$ and S_{2n} otherwise.
  The sum of the reduction in test time over all the sessions formed during package test gives the overall reduction in the TAT.

C. 3D TSV-SIC with N chips in the stack

The algorithm used for scheduling tests for 3D TSV-SICs with two chips in the stack can be extended for 3D TSV-SICs with N chips in the stack.

- Given is the list of sessions S_i of each chip n_i, each denoted by S_{ik}, $1 \leq k \leq S_i$.
  All the sessions of each chip n_i are sorted in descending order of their test times.
- The test schedule for the package test is obtained by sequentially initiating the k^{th} session, S_{ik} of each chip n_i, $\forall i \in (1\ to\ N)$, untill the power constraints are met. Otherwise they are performed in separate package test sessions.
  The total number of sessions during the package test of the 3D TSV-SIC with N chips in the stack is $max(S_i)$ and the time taken by each session is $max(T_{ik})$, $1 \leq k \leq max(S_i)$.

VI. Conclusion

In this paper, we define test cost as a function of TAT and the number of TDRs for non-stacked ICs, 3D SIC with two chips in the stack and 3D SIC with N chips in the stack. The test cost is minimized by co-optimizing TAT and the number of TDRs, while meeting a power constraint. We have compared various test schedules and finally propose an algorithm for scheduling tests, to minimize the cost under power constraints.

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