Test Planning for 3D SICs using ILP

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***Abstract*—In this paper we propose a test planning scheme for core-based 3D stacked integrated circuits where the total test cost for wafer sort of each individual chip and the test cost of the complete stack at package test is minimized. We use an Integer Linear Programming (ILP) model to find the optimal test cost, which is given as the weighted sum of the test time and the test access mechanism (TAM). As ILP is time consuming, we use a scheme to bound the test time and the TAM such that the search space is reduced. The proposed bounding scheme and the ILP model were applied on several ITC'02 benchmarks and the results show that optimal solutions were obtained at low computation time.**

I. Introduction

3D Stacked Integrated Circuits (ICs) with Through-Silicon Vias (TSVs) have benefits such as enhanced performance, reduced power consumption and form factor [1]–[5]. However, additional manufacturing process steps like, insertion of TSVs, thinning, alignment and bonding of the chips forming the 3D SIC bear the potential to introduce defects formerly unknown for non-stacked ICs or 3D SICs is complicated [2]. Approximately 85% of IC manufacturers expect test cost to be the bottleneck in the production of 3D SICs in the forthcoming years [6]. Test planning is one alternative to reduce test cost.

Recent research addresses various aspects of testing 3D SICs, including test architecture design [7]–[11] and new challenges for 3D SICs with TSVs [1]–[5]; yet the issue of test planning, considering various contributors to test cost, remains fairly unexplored with only limited research works [9], [10].

The test cost is highly related to the test time and the test hardware. Thus, it is important to co-optimize both test time and test hardware while devising a test plan. For single chip ICs, so called unSICs, the test flow is well-defined. The test flow typically consists of wafer sort and package test, and the test plan is typically the same at wafer sort and package test. Hence, it is sufficient to find one single test plan; an order in which the cores of the IC are tested, and apply first at wafer sort and then at package test. For 3D SICs it is different. There are four possible test instances for the test flow:

1) Wafer sort: Testing the individual chip prior to integration into the stack to sort out known good dies (KGDs).
2) Intermediate test: Testing the partially constructed chip stack.
3) Post-bond test: Testing the complete chip stack assembly.
4) Package test: Testing the packaged assembly.

The more test instances that are used, the higher is the chance to detect manufacturing defects early, but it leads to a higher test cost. However, reducing the number of test instances may lead to a higher manufacturing cost per 3D SIC. For example, if only package test is performed, all stacked chips are wasted if one chip is defective. In our previous work [12], we studied the test flow problem and found it most suitable to use a test flow where the test flow comprises the wafer sort of each individual chip and package test of the complete stack. In this paper, we assume such a test flow.

The problem that is addressed in this paper is to find the most suitable test plan for testing the cores of each chip individually during wafer sort and for testing all cores of the complete chip stack during package test such that the overall test cost, given in test time and TAM wires, is minimal.

To address the problem, we propose an Integer Linear Programming (ILP) model to minimize the linear objective function of the overall test cost which is formulated as the weighed sum of the test time and the test hardware needed to test the cores of each individual chip at wafer sort and all cores of the complete chip stack at package test. As the search space is large, we use a scheme to bound the variables contributing to the test cost. A near optimal TAM width is estimated from the test cost function and the maximal test time at any TAM line is bounded by an upper limit. We have applied our scheme on several designs constructed from ITC'02 benchmarks and the results show that optimal solutions were obtained at low computation time.

The rest of the paper is organized as follows. In Section II, related works are reviewed. The test architecture of 3D SICs with IEEE 1500 is described in following section. The problem of test planning is defined in Section IV followed by a motivational example in Section V. An ILP fiorimulation and bounding approach is proposed to address the test planning problem in Section VI. The experimental results are presented in Section VII and the paper is concluded in Section VIII.

II. Related Work

A brief discussion of previous studies on test scheduling and test architecture of non-stacked ICs and 3D SICs is presented in this section.

Scheduling tests to reduce test time for non-stacked ICs has been addressed in [11], [13]–[20]. For core-based ICs, test scheduling under resource constraints is addressed in [14]–[16] by performing core tests concurrently, in sessions. A session is defined as a group of tests that start simultaneously and no other tests are initiated until all tests of the session are finished. The approaches perform well for non-stacked ICs, where the same schedule is applied both at wafer sort and package test.

Test planning to reduce the overall test cost for 3D SICs, considering both test time and test hardware has been addressed in [9], [10]. However, the proposed approach is rendered inefficient due to the inability to re-use wafer sort test hardware while performing package test, and is not scalable in case intermediate tests are necessary. In addition, for 3D SICs with TSVs, all test data commute via the lowermost chip [1], [2], [8] unlike illustrated in [9], [10], where the wide test data buses called TAMs start and end on any chip. Thus, it is important to provide a standardized and scalable test architecture for each chip forming the 3D SIC, which reuses the test infrastructure during all test instances.

The IEEE 1500 standard provides a platform for testing core-based non-stacked ICs with minimized test time and minimal test hardware overhead [21]–[29]. Design and optimization of test architecture for non-stacked ICs with IEEE 1500 is described in [18], [28]–[30]. In [18], Iyengar *et al.* address optimization of TAMs for System-on-Chips (SoCs) by designing wrappers to reduce core-test time by balancing core scan chains. Mullane *et al.* in [29] propose a hybrid scan for non-stacked ICs provided with IEEE 1500 core wrappers, by combining the serial and parallel ports of the wrapper, resulting efficient test vector access and reduced test time. However for 3D SICs, test architecture optimized for each chip in the stack during wafer sort may not lead to a optimized test architecture when all the chips are tested jointly during package test. Furthermore, unlike 3D SICs with TSVs, where each chip in the stack sends and receives data only via the lowermost chip, for 3D SICs not bonded with TSVs, such as System-in-Package (SiPs) and Package-on-Package (PoPs), data

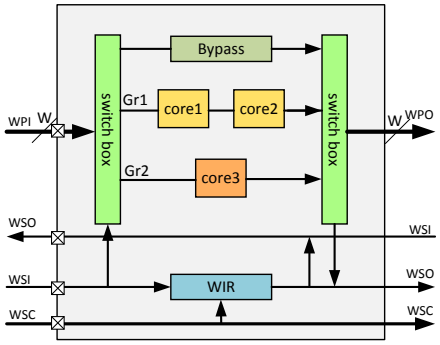

Fig. 1. Test architecture of a non-stacked chip

can be communicated to each chip via dedicated wire bonds. Thus, 3D SICs with TSVs require a test architecture standardized over all the chips in the stack that allows test access for all test instances.

Optimization of test architecture for 3D SICs with TSVs, has been addressed in [7], [8], [11], [18]. Marinissen *et al.* in [8] proposed a scalable test architecture based on IEEE 1149.1, IEEE 1500, and wide TAMs, which re-uses the test hardware for wafer sort during package test. However, test planning for 3D SICs supported by IEEE 1500, to reduce the overall test time, while re-using the wafer sort test architecture during later test instances has not yet been addressed, which is the goal of this paper.

III. Test Architecture

In this section we first discuss the test architecture for a non-stacked IC with an IEEE 1500 based test infrastructure, followed by a 3D SIC, where each chip of the stack is supported by the IEEE 1500 infrastructure.

A. non-stacked IC

Cores of an IC can be accessed during test by the TAMs of an on-chip IEEE 1500 test architecture. A non-stacked IC, supported with an IEEE 1500 based test infrastructure, is illustrated in Fig. 1. The chip consists of three cores, *viz.*, core1, core2 and core3, which are accessed by the TAMs. The Wrapper Parallel Port (WPP), comprising the Wrapper Parallel Input (WPI) and the Wrapper Parallel Output (WPO) in the figure, depicts a TAM of width W, to be decided by the user. The TAM width W is partitioned among Gr_1, which concatenates the scan chains of core1 and core2 serially, and Gr_2 connecting core3 to the switch boxes. The switch boxes select, depending on the instruction in the WIR, the bypass register or all the TAM lines. The Wrapper Serial Port (WSP), comprising of Wrapper Serial Input (WSI), Wrapper Serial Output (WSO), and Wrapper Serial Control (WSC) terminals, as shown in Fig. 1, supports the serial test mode. The instruction to be executed in a chip is stored in the corresponding Wrapper Instruction Register (WIR).

B. 3D SIC

Fig. 2 illustrates a 3D SIC with two chips, where Chip2 is stacked on top of Chip1. Chip1 contains core1, core2 and core3, while Chip2 hosts core4 and core5.

At wafer sort, Chip1 and Chip2 each use an IEEE 1500 based test infrastructure as described in Section III-A. Chip1 would require an optimal TAM width of m_1 during wafer sort, which is split among Gr_1 connecting core1 and core2 in series, and Gr_2 to core3, while Chip2 requires an optimal TAM width m_2, which is split among Gr_3 and Gr_4 to core4 and core5, respectively.

During package test of the 3D SIC in Fig. 2 a TAM of width W is provided to all the chips in the stack, which concatenates the cores of Chip1 and Chip2. The TAM width W in this case can be determined by $max(m_1, m_2)$, which is the maximum TAM width required by any chip forming the 3D SIC. This may however result in unused TAM lines in several chips in the stack, if during wafer sort the chip does not utilize the total TAM width provided.

In addition, the WPOup, WSOup and WSCup of Chip1, *i.e.*, the lower chip in the stack, is interconnected to the WPIdown, WSIdown and WSCdown of Chip2, respectively, *i.e.*, the chip on top. The WPOup, WSOup and WSCup of the topmost chip, Chip2, are directed out via the WPOdown, WSOdown and WSCdown, respectively, of the lowermost chip in the stack, Chip1. The WPOdown, WPIdown, WSOdown, WSOdown and WSCdown of the lowermost chip, Chip1, serve as the package test interface for the 3D SIC. As illustrated in [8], in this paper we assume equal number of WPIs and WPOs for each chip.

The TSV interconnect between chips may be tested using the boundary scan registers, which connects all input/output pins and TSVs. Boundary scan registers are implemented on both chips and are used in TSV interconnect test. Test stimuli are applied on outgoing TSVs and test responses are captured on in-coming TSVs. Since the boundary scan register is a separate register, testing of TSVs cannot be performed concurrently with core tests.

The TSV interconnect tests contribute with a constant term to the overall test time and could not be scheduled with any core tests. During TSV interconnect testing, the BYPASS mode is selected for each chip in the stack. As illustrated in Fig. 2, the WIR selects the bypass register for both Chip1 and Chip2 simultaneously. Therefore, the time required to perform TSV interconnect tests are overseen while addressing the total test time in the remainder of the paper.

IV. Problem Definition

In this section the test planning problem for 3D SICs has been formulated, where the test cost components, *viz.*, test time and test hardware must be co-optimized to achieve the optimal test plan.

For a 3D SIC, where each chip is supported by the IEEE 1500 based test infrastructure, the assignment of scan chains to respective TAM lines (core-scan chain configuration) within core1 of Chip1 of Fig. 2 is shown in Fig. 3. The routing of the IEEE 1500 test architecture is overlooked in the figure. We assume the following regarding the 3D SIC configuration:

- D chips in the stack, where each chip is denoted as $Chip_d$, $1 \leq d \leq D$. In Fig. 3, the 3D SIC consists of two chips, *viz.*, Chip1 and Chip2.
- $Chip_d$ has C_d cores, each denoted by $core_{dcn}$, $1 \leq c \leq C_d$, $1 \leq n \leq N$, where N is the TAM width of the core, explained below. For example, Chip1 has three cores, denoted by core1, core2 and core3 in Fig. 3.
- $core_{dcn}$ has S_{dcnb} scan chains, each denoted by sc_{dcnbs}, $1 \leq s \leq S_{dcnb}$ and requires p_{dcnb} test patterns, where b denotes the number of TAM lines, explained below. The three scan chains of $core1$ of $Chip1$ are shown in Fig. 3, labeled as A, B and C, respectively, for ease of reference.
  - each functional input or output is equivalent to an internal scan chain of length 1, and are included within S_{dcnb}
- scan chain sc_{dcnbs} is of length l_{dcnbs}
- scan chain sc_{dcnbs} takes Tsc_{dcnbs} time units, and is computed as:

$$Tsc_{dcnbs} = (1 + l_{dcnbs}) \cdot p_{dcnb} + l_{dcnbs} \quad (1)$$

For the IEEE 1500 test infrastructure to be optimized, for any given configuration we assume:

- W TAM lines as shown in Fig. 3, where $Chip_d$ receives a WPIdown of width W
- width of the TAM W, is divided into N groups of TAMs, each denoted by Gr_n and has B_n TAM lines, *i. e.*,

$$W = \sum_{n=0}^{N} B_n \quad (2)$$

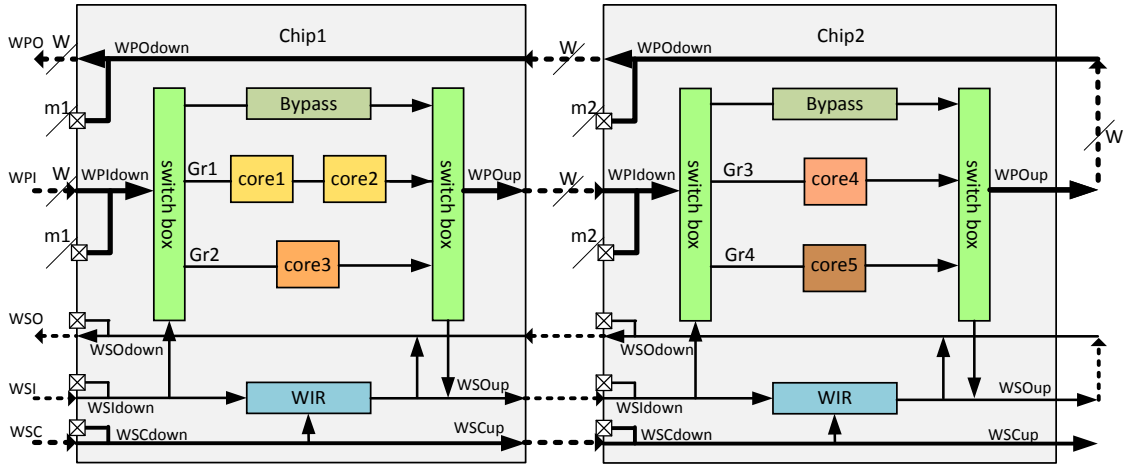

Fig. 2. Test architecture of 3D SIC

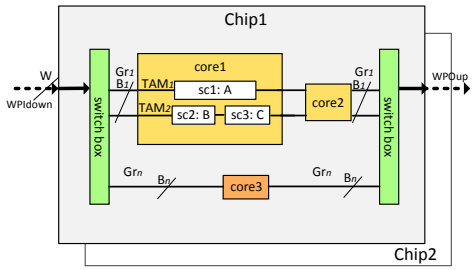

Fig. 3. Scan-chains configured into wrapper-chains in core1 of Chip1

As seen in Fig. 3, $core1$ is accessed by TAM group Gr_1 which has $B_1 = 2$ TAM lines.

- $core_{dcn}$ is accessed by TAM, Gr_n
  - multiple cores, $\{core_{dcn} | \forall d,c\}$, may be accessed in series by a single TAM, Gr_n, as seen in Fig. 3, where Gr_1 concatenates $core1$ and $core2$.
- each scan chain sc_{dcnbs} of $core_{dcn}$ is accessed by a single TAM line, TAM_{nb}, $1 \leq n \leq N$, $1 \leq b \leq B_n$ as visible in Fig. 3, where TAM_1 accesses scan chain A.
  - multiple scan chains, $\{sc_{dcnbs} | \forall d,c,s\}$, may be accessed in series by a single TAM line, TAM_{nb}, which is shown by TAM_2, which concatenates scan chains B and C.
  - Time required to execute tests $\{sc_{dcnbs} | \forall d,c,s\}$ on a single TAM line TAM_{nb} is given by $Ttam_{nb}$, the sum of the time taken by each individual scan chain Tsc_{dcnbs}:

$$Ttam_{nb} = \left\{ \sum_{s=0}^{S_{dcnb}} Tsc_{dcnbs} | \forall d,c \right\} \tag{3}$$

In the rest of the paper, wherever the length of each scan chain l_{dcnbs} and the number of patterns required by each core p_{dcnb} are provided, we have subsequently stated the respective test time obtained Tsc_{dcnbs} as given.

The test cost for any given configuration of the IEEE 1500 test infrastructure is obtained as below:

- Time taken to test $Chip_d$ in the stack, *i. e.*, the wafer sort time for any chip, Tws_d, is given by the maximum time at any TAM line TAM_{nb}:

$$Tws_d = \left\{ max \sum_{\forall c,s} Tsc_{dcnbs} | \forall n,b \right\} \tag{4}$$

- In a similar manner, the package test time Tpt, of all the stacked, bonded and packaged chips tested simultaneously is bounded by the maximum time taken at any TAM line TAM_{nb}, in the 3D SIC:

$$Tpt = \left\{ max \sum_{\forall d,c,s} Tsc_{dcnbs} | \forall n,b \right\} \tag{5}$$

- The overall test time of the 3D SIC, T, is given by the sum of the wafer sort time of each chip in the stack Tws_d, and the package test time Tpt, when all chips are tested jointly after stacking, bonding and packaging:

$$T = \sum_{d=0}^{D} Tws_d + Tpt \tag{6}$$

- Besides the routing, each TAM line requires dedicated chip pins (ATE pins during wafer sort) for transfer of test stimuli. Therefore, the number of TAM lines W corresponds directly to the hardware cost of each chip. Since, each chip in the stack has equal number of TAM lines, the total hardware cost P, is the product of the number of chips in the stack D and the width of the TAM W:

$$P = D \cdot W \tag{7}$$

- Thus, the cost of testing a 3D SIC can be defined as the cumulative cost of the total test time T, as obtained in Eq. 6, and the required test hardware P, from Eq. 7:

$$Cost(T,P) = T + \kappa \cdot P \tag{8}$$

where κ is the weighting factor for the test hardware, *i.e.*, the time equivalent for each unit of hardware.

Given the 3D SIC supported by the IEEE 1500 test architecture, a test plan is developed to minimize the overall test cost, defined by Eq. 8, which is achieved by optimizing the following parameters

1 width of the TAM, W
2 number of TAMs, N
3 determining the width of each TAM, B_n
4 assigning each core $core_{dcn}$ to a single TAM Gr_n
5 assigning each scan chain sc_{dcnbs} to respective TAM lines TAM_{nb}

TABLE I
GIVEN DATA FOR 3D SIC

Chip no.	Core no.	Scan Chain no.	Test Time	Label
d	c	s	Tsc_{dcnbs}	
1	1	1	600	A
		2	500	B
		3	500	C
	2	4	200	D
		5	200	E
	3	6	1000	F
2	4	1	600	X
		2	500	Y
	5	3	1000	Z
Time equivalent of each TAM, κ				200

TABLE II
TEST COST VARIATION FOR EACH CHIP

Chip no.	TAM Width	Test Time	Cost Achieved	Configuration
d	W	T_{ws}	$Tws_d + \kappa \cdot W$	
1	1	3000	3200	{A, B, C, D, E, F}
	2	1600	2000	{A, B, C}, {D, E, F}
	3	1400	2000	{A, B}, {C}, {D, E, F}
	4	1000	1800	{A}, {B, C}, {D, E}, {F}
	5	1000	2000	{A}, {B}, {C}, {D, E}, {F}
	6	1000	2200	{A}, {B}, {C}, {D}, {E}, {F}
2	1	2100	2300	{X, Y, Z}
	2	1100	1500	{X, Y}, {Z}
	3	1000	1600	{X}, {Y}, {Z}

V. MOTIVATIONAL EXAMPLE

In this section an example is illustrated to motivate the significance of test planning by finding the optimal trade-off between test time and test hardware while considering both wafer sort and package tests simultaneously. The following example shows that an improper co-optimization of the test time and test hardware leads to a higher test cost for the 3D SIC. The optimal TAM width required by the 3D SIC for wafer sort and package test is determined and the scan chains are assigned to the respective TAM line minimizing the test time to arrive at the minimal test cost.

In this example, the 3D SIC shown in Fig. 2 has been considered. Table I shows the given parameters for the 3D SIC. The first column from the left divides the table for either chip, *viz.*, Chip1 and Chip2, respectively. The second column lists the cores in the 3D SIC, as seen in Fig. 2. The third column lists the number of scan chains per chip, as well as scan chains per core. As can be seen, in Table I, core1 has three scan chains, $\{A,B,C\}$ which is also visible in Fig. 3, core2 has two: $\{D,E\}$, core3 contains one scan chain: $\{F\}$, core4 has two: $\{X,Y\}$, while core5 has one: $\{Z\}$. In the next column the time taken by each scan chain is tabulated, which is derived from a given length of the respective scan chain and the number of patterns required by the corresponding core, which have been concealed from the table. The rightmost column labels each scan chain in Chip1 as $A-F$ while for Chip2 $X-Z$, for ease of reference. The constant, κ of Eq. 8 is assumed to be 200 *units*, as the lowermost row of Table I depicts.

Table II depicts the variation in the test cost with increasing TAM width for the wafer sort of each chip. The first column of Table II divides the table for Chip1 and Chip2. The second column depicts all possible TAM widths for each chip. We can see that the maximum possible number of used TAM lines for Chip1 is 6 while that of Chip2 is 3, when each scan chain has a dedicated TAM line, depicted by the last row of each chip in Table II. On the other hand, the first row of each chip depicts the scenario where all scan chains of either chip are connected in series on a single TAM line. The third column shows the minimum test times achieved with the corresponding TAM widths. As stated by Iyengar *et. al.* in [18], the test time of either chip is lower bounded by the scan chain with the longest test time. It is seen that for both Chip1 and Chip2, the scan chain with the longest test time is 1000 *time units*. Thus, for Chip1 and Chip2 we see that with a TAM width of 4 and a TAM width of 3 respectively, the test time reaches the minimum, *i.e.*, 1000 *time units*. The fourth column lists the cumulative cost obtained from the given TAM width and the minimum test time hence obtained. It is seen that for Chip1 the cost reaches a minimum with a TAM width of 4, for 1800 *units*, while for Chip2 it is 1500 *units* with a 2 TAM lines. Intuitively, the cost reaches a minimum possible value, *i.e.*, the best trade-off, with a certain TAM width and the corresponding minimal test time, following which, increasing the TAM width results in increasing the cumulative test cost, as the corresponding reduction in the test time is insufficient to balance the trade-off. The last column in Table II shows the assignment of scan chains to respective TAMs, to arrive at the minimum test time with the given TAM width mentioned in the second column. For example, in case of Chip1 with two TAM lines, the minimum test time is obtained when scan chains A, B, and C are connected in series in the first TAM line, while scan chains D, $E$and F are assigned to the second, denoted by: $\{A,B,C\},\{D,E,F\}$. Thus the wafer sort time in this case is given by:

$$\begin{aligned} T_{ws1} &= max\{(T_A+T_B+T_C),(T_D+T_E+T_F)\} \\ &= max\{(600+500+500),(200+200+1000)\} \\ &= max\{1600,1400\} = 1600 \end{aligned} \tag{9}$$

While the wafer sort cost for Chip1 can be calculated as:

$$\begin{aligned} Cost_{ws1} &= T_{ws1} + \kappa \cdot W \\ &= 1600 + 200 \cdot 2 = 2000 \end{aligned} \tag{10}$$

During package test of the 3D SIC considered in this example, the TAM lines of Chip1, which exit through WPOup to that of the WPIdown entering Chip2 are integrated. The cores on each group of TAM for either chip forming the 3D SIC are concatenated to arrive at the package test schedule. During package test each core within a chip must be tested in the same order as they were tested during wafer sort. However, if the wafer sort schedule providing the optimal test cost of each chip is assumed, the TAM width W required by the 3D SIC is upper bounded by the maximal TAM width required by any chip in the stack to arrive at the optimal wafer test cost. Therefore, a number of redundant TAM lines must be routed through the chips forming the 3D SIC that require a lower TAM width during wafer sort to arrive at the respective optimal test cost. On the other hand, if the test time of each chip in the 3D SIC is distributed over the whole TAM width W, the package test time can be minimized by evenly distributing the test time over the total TAM width W, resulting in a lower overall test cost.

For example, in Table II it can be seen that the minimum cost obtained for Chip1 is with 4 TAM lines, whereas that of Chip2 is with 2 TAM lines. Therefore, during wafer sort, if either chip utilizes the TAM width that provides the minimal wafer sort cost, Chip1 would utilize 4 TAM lines, while Chip2 utilizes just 2 of the lines. However, the hardware cost would still be accounted for 4 TAM lines. On the other hand, during wafer sort the test time for Chip2 remains 1100 *time units*, which is longer than the time taken by utilizing all 3 TAM lines, *i.e.*, 1000 *time units*. Furthermore, WITH A tam WIDTH OF 2, the minimum package test time achieved by interconnecting respective TAM lines is 2600 *time units*, obtained as a result of concatenating the TAMs of core1 and core5. The minimal package test time is obtained by interconnecting the TAMs of Chip1 and Chip2 in the following manner: $\{A,B,C,Z\},\{D,E,F,X,Y\}$.

To arrive at the minimal cost for the 3D SIC described above, we have:

$$\begin{aligned} Cost_{\#case} &= T + \kappa \cdot P \\ &= \left(\sum_{d=0}^{D} Tws_d + Tpt \right) + \kappa \cdot (D \cdot W) \\ &= \left(\sum_{d=0}^{2} Tws_d + Tpt \right) + 200 \cdot (2 \cdot W) \\ &= (Tws_1 + Tws_2 + Tpt) + 400 \cdot W \end{aligned} \tag{11}$$

Three possible scenarios are hereby presented, for which the test cost is determined by substituting the values in Eq. 11:

i. *TAM width* $W = 2$

$$\begin{aligned} Cost_i &= (1600 + 1100 + 2600) + 400 \cdot 2 \\ &= 1000 + 1100 + 2600 + 800 = 5500 \ units \end{aligned} \tag{12}$$

ii. *TAM width* $W = 3$

$$\begin{aligned} Cost_{ii} &= (1400 + 1000 + 2100) + 400 \cdot 3 \\ &= 1400 + 1000 + 2100 + 1200 = 5700 \ units \end{aligned} \tag{13}$$

iii. *TAM width* $W = 4$

$$\begin{aligned} Cost_{ii} &= (1000 + 1000 + 1600) + 400 \cdot 4 \\ &= 1000 + 1000 + 1600 + 1600 = 5200 \ units \end{aligned} \tag{14}$$

It is seen that *Case iii*. gives the minimum test cost. It can be seen that, minimizing the wafer sort cost of each chip in the stack may not minimize the overall test cost. The optimized parameters mentioned in Section IV, for the given 3D SIC are:

1. bit width of the TAM: $W = 4$
2. number of TAMs: $B = 3$
3. partition of the total TAM width W, among number of TAMs: $B_1 = 2$, $B_2 = 1$ and $B_3 = 1$
4. assigning each core to a single TAM: core1 to Gr_1, core2 to Gr_2, core3 to Gr_3, core4 to Gr_1 and core5 to Gr_2
5. designing a test wrapper for each core by assigning scan chains to respective TAM lines: $\{A, X\}$ to TAM_{11}, $\{B, C, Y\}$ to TAM_{12} and $\{D, E, Z\}$ to TAM_{21} and $\{F\}$ to TAM_{31}

It is seen that to arrive at the minimum test cost for a 3D SIC supported by the IEEE 1500 based test infrastructure, it may be insufficient to minimize either the wafer sort cost of each chip or the package test cost. Thus, the test cost is minimized by co-optimizing the test time and hardware cost, while considering both the wafer sort and package test instances simultaneously.

VI. Proposed Approaches

In this section the test planning problem for 3D SICs is formulated as an ILP model and bounds are ascribed to the variables. Eventually, an algorithm to implement the ILP model has been presented.

ILP can be applied to find an optimal solution. However, the computation time sets a major drawback. Therefore, to reduce the computation time, we define constraints, thus minimizing the search space.

In [18], [31], for non-stacked ICs, the problem of wrapper-TAM co-optimization was stated to be *NP*-hard and a solution was proposed using ILP. Since, 3D SICs are manufactured by stacking non-stacked ICs, the problem can be extended to 3D SICs to state that, minimizing the cost while considering both the test time cost and the optimized wrapper-TAM as the hardware cost is *NP*-hard as well. Hence, in the following, an ILP model is detailed.

ILP is applied to minimize a linear objective function on a set of integer variables, while satisfying a set of linear constraints. The ILP model, as explained in [32], can be generalized as :

$$\begin{aligned} &\text{Minimize:} \quad A \cdot x \\ &\text{subject to:} \quad B \cdot x \leq C, \quad \text{s.t.,} \quad x \geq 0 \end{aligned}$$

where A is the linear objective function, B defines the constraints, C is a set of constants, and x is a vector of integer variables.

To reach at the minimal cost, the objective function to be minimized is in Eq. 8. The function can be expanded to contain the optimizing factors in the following way:

$$\begin{aligned} Cost &= T + \kappa \cdot P \\ &= \left(\sum_{d=0}^{D} Tws_d + Tpt \right) + \kappa \cdot (D \cdot W) \\ &= \sum_{d=0}^{D} max \left(\sum_{\forall c,s} Tsc_{dcnbs} | \forall n, b \right) \\ &+ max \left(\sum_{\forall d,c,s} Tsc_{dcnbs} | \forall n, b \right) + \kappa \cdot D \cdot \sum_{n=0}^{N} B_n \end{aligned} \tag{15}$$

subject to the following constraints

- Each scan chain sc_{dcnbs} is assigned to exactly one TAM line TAM_{nb}, *i.e.*, n, b are unique
- Each $core_{dcn}$ is assigned to exactly one TAM group Gr_n
- Sum of the TAM width for each chip is W, *i.e.*, $\sum_{n=0}^{N} B_n = W \forall c, s$
- Sum of the TAM width for the 3D SIC is W, *i.e.*, $\sum_{n=0}^{N} B_n = W \forall d$

The large search space of the ILP model can be reduced by an upper and a lower bound to several variables:

- Achieving a trade-off between the test time and the test hardware, can be portrayed as dividing the cumulative test time of all the scan chains in the 3D SIC into as many equal (or as nearly equal as possible) groups as the number of TAM lines. It can be formulated as:

$$Cost = \frac{2 \sum_{\forall d,c,s} Tsc_{dcnbs}}{W} + \kappa \cdot D \cdot W \tag{16}$$

To find the minima of the cost function in Eq. 15, we differentiate Eq.16, *wrt* W and equate it to *zero*:

$$\begin{aligned} 0 &= \frac{d}{dW} Cost \\ &= \frac{d}{dW} \left(\frac{2 \sum_{\forall d,c,s} Tsc_{dcnbs}}{W} + \kappa \cdot D \cdot W \right) \\ &= \frac{-2 \sum_{\forall d,c,s} Tsc_{dcnbs}}{W^2} + \kappa \cdot D \\ \Rightarrow W_{est} &= \left(\frac{2 \sum_{\forall d,c,s} Tsc_{dcnbs}}{\kappa \cdot D} \right) \end{aligned} \tag{17}$$

In the best case scenario, the scan chains in each chip can be categorized into W_{est} equal groups to give the optimal test cost. Although, in practice it might not always be plausible to complement Eq. 15 with exactly W_{est} to give the optimal cost.

- The maximum TAM width cannot exceed the ratio of the maximum possible test time to that of the minimum possible test time, *i.e.*,

$$W_{max} = \frac{\sum_{\forall d,c,s} Tsc_{dcnbs}}{max(Tsc_{dcnbs} | \forall d, c, s)} \tag{18}$$

- Number of partitions of the TAM width, N does not exceed the minimum number of cores in any chip, *i.e.*,

$$N_{max} = min(C_d | \forall d) \tag{19}$$

- Maximum width of any group of TAM B_{max} is the lowest ratio between the total time taken of all the scan chains to the longest scan chain for any chip in the 3D SIC, *i.e.*,

$$B_{max} = min\left(max(\frac{\sum_s Tsc_{dcnbs}}{max(Tsc_{dcnbs}|\forall d,c)}\right) \quad (20)$$

- The test time of any scan chain on any chip may not surpass the sum of the maximum time taken by any scan chain in the chip with the ratio of the total test time on the chip to that of the provided TAM width, *i.e.*,

$$T_{chip} = \frac{\sum_{\forall c,s} Tsc_{dcnbs}}{W} \quad (21)$$

The ILP is implemented on the test function while considering the constraints and bounds mentioned above, as in Algorithm 1 to obtain the optimal test cost, $Cost_{ILP}$, optimal TAM width, W_{ILP}, partitions of the TAM width Gr_n and the width of each partition, B_n. The allocation of scan chains to respective TAM wires is performed by a bin packing approach motivated by [33], *viz.*, the Best Fit Decreasing (BFD) algorithm, as detailed in Algorithm 2.

Algorithm 1 ILP model for test planning of 3D SICs

Given bounds: $W_{est}, W_{max}, \alpha, N_{max}, B_{max}$
if $W_{est} \leq W_{max}$ **then**
  $W_1 = W_{est}$
  $W_2 = W_{max}$
else
  $W_1 = W_{max}$
  $W_2 = W_{est}$
end if
for $W = (W_1 - \alpha)$ to $(W_2 + \alpha)$ **do**
  if $W < N_{max}$ **then**
    $N^* = W$
  else
    $N^* = N_{max}$
  end if
  for $N = 1$ to N^* **do**
    while All partitions of W have not been explored **do**
      for $B = 1$ to B_{max} **do**
        while $max \sum_{\forall c,s} Tsc_{dcnbs} | \forall n,b) \leq T_{chip}$ **do**
          Scan chains of each chip are assigned to each TAM line as per Algorithm 2
        end while
        Save B
      end for
    end while
    Save N
  end for
  if $Cost \leq Cost_{ILP}$ **then**
    $Cost_{ILP} = Cost$
  end if
end for

VII. Experimental Results

The proposed ILP model for test planning of 3D SICs with TSVs was implemented to achieve the minimal test cost for several 3D SICs with up to four chips in the stack. The wafer sort time for each chip, the package test time, and width of the TAM for the 3D SIC are accounted at the lowest obtained test cost. To highlight the efficiency of the proposed ILP model, experiments are detailed to compare the test cost obtained for 3D SICs with varying TAM widths.

The 3D SICs in the experiments are obtained by combining several ITC'02 benchmarks. Each benchmark represents a chip in the stack. The four designs listed in Table III have been considered.

The minimal test costs obtained by implementing the ILP model on 3D SICs with two, three and four chips in the stack are shown in

Algorithm 2 Scan Chain Allocation

Given from Algorithm 1: B
Sort Scan chains of each core $(sc_{dcnbs} \forall d,c)$ in descending order of time taken
for $max(sc_{dcnbs}|\forall d,c)$ to $min(sc_{dcnbs}|\forall d,c)$ **do**
  Sort TAM lines TAM_{nb} in descending order of time taken at present
  for $max(TAM_{nb})$ to $min(TAM_{nb})$ **do**
    Concatenate sc_{dcnbs} to TAM_{nb} to minimize $max(Ttam_{nb})$
  end for
  Save core-scan chain configuration
end for

TABLE III
Designs

Label	Design	Cores	Contributor
D	d695	11	Duke University
G	g1023	15	University of Stuttgart
P	p34392	20	Philips Semiconductors
T	t512505	32	Texas Instruments

Table IV, Table V, and Table VI respectively. The first column from the left mentions the designs from Table III that have been stacked to achieve the 3D SIC. In the first row of Table VI it can be seen that the 3D SIC obtained by stacking all four chips in Table III is listed as DGPT. The second column in each table lists the total number of cores, obtained as the sum of the cores in each design forming the 3D SIC. In case of DGPT in Table VI, it can be seen that the total number of cores in the 3D SIC is 78, while that of DP in the first row of Table IV is 31. The minimal cost obtained by the proposed ILP model, $Cost_{ILP}$, is listed in the third column from the left. The rest of the columns list the various components of the minimal test cost obtained. The test cost is obtained as a weighed sum of the total test time and the TAM width W, where a suitable value for the weighting factor κ defined in Eq. 8 was determined from several experiments to ensure that the hardware cost is comparable to the test time.Designers may vary the value of κ based on the given cost model. The next group of two columns show the optimal TAM width W_{est} as calculated from Eq. 17, followed by the TAM width W_{ILP} for which the minimal cost was obtained, respectively. The near-optimal width of the TAM was determined to be 27 in case of DGPT, as described in Section VI, and complemented by the other constraints, the search space was restricted to a TAM width in the range of $25 \leq W \leq 35$. The allocation of scan chains to respective TAM lines was recorded and finally the test cost was computed for each W. It was found that the minimum test cost was obtained at $W = 28$. The next group of two, three or four columns

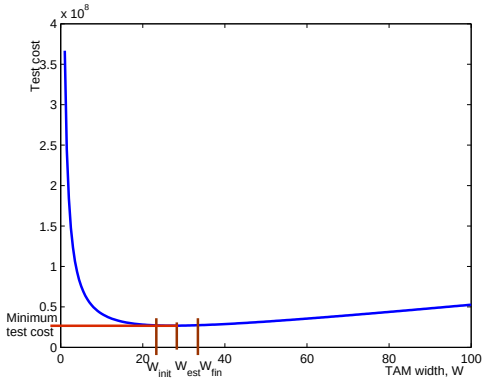

Fig. 4. Test Cost variation with TAM Width

TABLE IV
TEST PLANNING WITH TWO CHIPS IN THE STACK

Design	Cores	Cost	TAM width		Test time by ILP model		
		$Cost_{ILP}$	W_{est}	W_{ILP}	T_{ws1}	T_{ws2}	T_{pt}
DP	31	8534358	8	8	86979	2046611	2133589
DT	43	47434247	12	14	49702	11808860	11858562
GP	35	3257964	22	21	34830	779661	814491
GT	47	33211092	18	20	36571	8266202	8302773

TABLE V
TEST PLANNING WITH THREE CHIPS IN THE STACK

Design	Cores	Cost	TAM width		Test time by ILP model			
		$Cost_{ILP}$	W_{est}	W_{ILP}	T_{ws1}	T_{ws2}	T_{ws3}	T_{pt}
DGP	46	3095676	22	23	30253	31801	711865	773919
DGT	58	26680206	24	25	27833	29257	6612961	6670052
DPT	63	22799094	35	32	21745	511653	5166376	5699774
GPT	67	60809449	11	12	60952	1364407	13777003	15202362

TABLE VI
TEST PLANNING WITH FOUR CHIPS IN THE STACK

Design	Cores	Cost	TAM width		Test time by ILP model				
		$Cost_{ILP}$	W_{est}	W_{ILP}	T_{ws1}	T_{ws2}	T_{ws3}	T_{ws4}	T_{pt}
DGPT	78	26160610	27	28	24851	26122	584746	5904430	6540149
DDDD	44	1391660	8	8	86979	86979	86979	86979	347914

TABLE VII
TEST COST COMPARISON FOR DIFFERENT TAM WIDTHS

Design	Initial TAM width		Final TAM width		Optimal TAM width		Cost Difference (%)	
	W_{init}	$Cost_{init}$	W_{fin}	$Cost_{fin}$	W_{ILP}	$Cost_{ILP}$	$\frac{Cost_{init}-Cost_{ILP}}{Cost_{ILP}}$ %	$\frac{Cost_{fin}-Cost_{ILP}}{Cost_{ILP}}$ %
DP	5	9494471	10	8747713	8	8534358	11.25	2.50
DT	10	50144773	20	50483587	14	47434247	5.71	6.43
GP	15	3444140	25	3307620	21	3257964	5.71	1.52
GT	15	34594883	25	34041362	20	33211092	4.17	2.50
DGP	20	3125954	25	3106436	23	3095676	0.98	0.35
DGT	20	27347209	30	27124873	25	26680206	2.50	1.67
DPT	25	23497320	35	24041232	32	22799094	3.06	5.45
GPT	10	61822939	15	62329685	12	60809449	1.67	2.50
DGPT	25	26328784	35	26814629	28	26160610	0.64	2.50
DDDD	5	1548220	10	1426452	8	1391660	11.25	2.50
						Average:	4.69	2.79

for Table IV, Table V, and Table VI respectively, list the wafer sort times for each chip forming the 3D SIC obtained by the ILP. Chip1 refers to the first chip mentioned in the respective design, while Chip2 refers to the second chip, and so on. For example, in Table VI, T_{ws1} refers to the wafer sort time of D, T_{ws2} to that of G, T_{ws3} to P, and T_{ws4} to T. The rightmost column lists the package test times T_{pt}, for the respective 3D SIC. The total test time is obtained as a sum of the wafer sort time of each chip constituting the stack, and the package test time.

In addition to the test plans obtained by the ILP model, for the purpose of comparison, the test cost of the 3D SIC obtained with the starting and ending widths of TAM for which the ILP was executed, are accounted in Table VII. Extensive search was done to find a suitable range of TAM width between which the optimal cost was obtained by the ILP. It was found that the optimal solutions for all benchmarks were obtained with $\alpha = 0.1 \cdot W_{est}$. The first group of two columns show the test cost obtained with the initial TAM width W_{init} used during the ILP. The next group of columns show the test cost at the TAM width W_{fin} when the ILP was halted. The next group of columns termed optimal TAM width show the minimal cost obtained with the ILP. The last group of columns, *viz.*, cost difference, shows the percentage decrease of the minimal test cost obtained, $Cost_{ILP}$, with respect to $Cost_{init}$ and $Cost_{fin}$. As can be seen in case of DGPT, the cost obtained for a TAM width of $W = 25 < W_{opt}$ is 0.64% higher than the test cost obtained with optimized hardware. On the other hand, for a TAM width of $W = 35 > W_{opt}$ the test cost obtained for DGPT is 2.50% higher than the minimal test cost obtained. The last row depicts an average increase in the test cost, both by minimizing the test hardware and the test time of the 3D SIC respectively. At an average, the test cost obtained with the initial TAM width W_{init} considered for the ILP is higher than the minimal test cost by 4.69%, while that with the TAM width W_{fin} at which the ILP was halted is 2.79%.

From Table VII, it can be observed that a minima of the test cost is reached between the initial TAM width assumed for the ILP W_{init} and the TAM width for which the ILP was halted W_{fin}. It can be further complemented by Fig. 4, which illustrates an estimated variation of the test cost *Cost* with the TAM width W for DGPT obtained from Eq. 16. The test cost is plotted against a TAM width varying from $W = 1$ to $W = 100$. The sum of the test time of all the scan chains in the 3D SIC is ideally assumed to be divided equally among the total TAM width W. From the graph it can be seen that the test cost reduces exponentially with increasing TAM width W, until it reaches a minima, and following that, with increasing W the test cost rises, almost linearly. The trend is noticeable in all the results obtained in Table VII. This can be explained by the fact that in the beginning the cost is dominated by the test time, which splits up rapidly with increasing TAM width W until an optimal TAM width W is obtained, for which the test time is minimum. As the TAM width is further increased, the corresponding reduction in the test time as compared to the cost incurred by the additional TAM line keeps decreasing.

VIII. Conclusion

As test planning for 3D SICs with TSVs is different from test planning for non-stacked ICs, we address in this paper the problem of test planning for 3D SICs. We assume that each chip in the stack is supported by an IEEE 1500 based test architecture, and we model the test planning problem, which is known to be *NP*-hard, with ILP. The aim is to minimize the overall test cost given as the test time and TAM for each individual chip at wafer sort and the complete stack of chips at package test. As ILP is very time consuming, we reduce the search space by determining a near-optimal TAM width through a bounding scheme. The proposed ILP model and the bounding scheme was simulated on a 3D SIC obtained by stacking up to four ITC02 benchmarks. A reduction in the test cost was accounted for each instance.

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