No Fault Found: The Root Cause

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Abstract—No Trouble Found (NTF) has been discussed for several years [1]. An NTF occurs when a device fails at the board/system level and that failure cannot be confirm by the component supplier. There are several explanations for why NTFs occur, including: device complexity; inability to create system level hardware/software transactions which uncover hard to find defects; different environments during testing (power, thermal, noise). More recently a new concept, No Fault Found (NFF), has emerged. A NFF represents a defect which cannot be detected by any known means so far. The premise is that at some point the defect will be exposed - most likely at a customer site when the device is in a system. Given that we looking for a defect that we know nothing about and are theoretically undetectable it will be interesting to see what the panel has to say about the nature of these defects and how we intend to find them.

The panel is organized by Erik Larsson and moderated by Bill Eklow. The statements from the panel are:

1 Scott Davidsson

In my experience NFFs have many root causes [2]. The biggest is that board and system test exercise the part in ways a chip tester cant. Another cause is poor fault coverage. It sometimes pays to test a returned part with the test program it was tested to before shipment, and then retest with the latest. The reduction in NFFs with the newest one proves that the cause was coverage. There are other reasons. The diagnostic process is imperfect, and some returned parts are good. There might be psychology involved. If your last revision had problems, repair people will tend to replace your part just to be safe, even if the quality has improved. But a low NFF rate on the original test program is not something to be wished for. If the part passed and now fails, you have a reliability problem and none of us wants that.

2 Rob Aitken

Broadly speaking, NFFs fall into three categories: test escapes, marginal chips, and type 1 errors (working parts mistakenly believed to be failures). The relative abundance of each category depends on the type and complexity of the product, the maturity of the manufacturing process, and the robustness of the test flow. A recent consultant's study [3] determined that the vast majority of NFF returns for consumer products appear to be type 1 errors. Specifically, 68% of NFF parts met all specs but somehow don't meet consumer expectations, 27% were "buyer's remorse" (falsely reported as bad in order to return part), leaving a surprisingly low 5% as test escapes or marginal parts. This report also found that a 1% reduction in the rate of NFF parts led to a 4% reduction in return and repair costs. This leads to two interesting areas for further discussion: How many of the 68% of parts could potentially be found by improved screening, and for chip vendors, are there failure modes that are only observable at a higher level of the system, and if so, how can they be mitigated or avoided? Providing good answers to these questions can have a substantial effect on perceived quality while at the same time helping to control costs.

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3 Artur Jutman

A certain portion of NFFs could be due to the lack of Board-level defect or fault coverage. The incompleteness of existing board-level test coverage metrics could simply appear e.g. due to the combination of the following two factors. First, the inability of the classical structural test techniques to apply test patterns at-speed, hence limiting the covered fault spectrum to static faults leaving the delay and performance fault domain traditionally to the functional tests, which in its turn do not produce measurable coverage of structural faults (e.g. delays on the board). As the result, the quality of the functional test sets depends highly on the human factor and statistics (experience, field returns, yield learning) providing no guaranteed quality. The latter fact represents the second factor contributing to the potentially missing fault coverage at the board level, while also creating problems for technology transfer and production outsourcing.

4 Christophe Lotz

Test strategy and defect occurrence should be tied together: (1) High test coverage should be applied for defects that occur frequently, (2) Lack of coverage on defects that never occur, has no consequence to the final quality. It is usually unknown, precisely, where the defect really occurs. We will have to qualify the test strategy against the true defects. In the BASTION project [4] we are developing the tool QuadDPMO to extract the true Defect Per Million Opportunities from a traceability database, with data collected from the production line and throughout the product life. The analysis combines repair information, board modelization and test coverage data. Linking test coverage and true DPMO provides new business opportunities such as: test cost reduction, improved tests that target the true defects, new opportunities for adaptive test, test overlap reduction, lower escape rates and culminating in fewer NFF.

References

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[4] BASTION (http://fp7-bastion.eu)