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Vertical InAs Nanowire Devices and RF Circuits

Martin Berg

LUND UNIVERSITY

Doctoral Thesis
Electrical Engineering
Lund, September

Academic thesis which, by due permission of the Faculty of Engineering at Lund University, will be publicly defended on Weekday, September 29, 2015, at 10^{15} a.m. in lecture hall E:1406, Department of Electrical and Information Technology, Ole Römers väg 3, 223 63 Lund, Sweden, for the degree of Doctor of Philosophy in Electrical Engineering. The academic thesis will be defended in English.

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Abstract:

Recent decades have seen an exponential increase in the functionality of electronic circuits, allowing for continuous innovation, which benefits society. This increase in functionality has been facilitated by scaling down the dimensions of the most important electronic component in modern electronics: the Si-based MOSFET. By reducing the size of the device, more transistors per chip area is possible. Smaller MOSFETs are also faster and more energy-efficient. In state of the art MOSFETs, the key dimensions are only few nanometers, rapidly approaching a point where the current scaling scheme may not be maintained. Research is ongoing to improve the device performance, mainly focusing on material and structural improvements to the existing MOSFET architecture. In this thesis, MOSFETs based on nanowires, are investigated. Taking advantage of the nanowire geometry, the gate can be wrapped all-around the nanowires for excellent control of the channel. The nanowires are made in a high-mobility III-V semiconductor, InAs, allowing for faster electrons and higher currents than Si. This device type is a potential candidate to either replace or complement Si-based MOSFETs in digital and analogue applications. Single balanced down-conversion mixer circuits were fabricated, consisting of three vertically aligned InAs nanowire MOSFETs and two nanowire resistors. These circuits are shown to operate with voltage gain in the GHz-regime. Individual transistors demonstrated operation with gain at several tens of GHz. A method to characterise the resistivity and metal-semiconductor contact quality has been developed, using the transmission line method adapted for vertical nanowires. This method has successfully been applied to InAs nanowires and shown that low-resistance contacts to these nanowires are possible. To optimise the performance of the device and reach as close to intrinsic operation as possible, parasitic capacitances and resistances in the device structure need to be minimised. A novel self-aligned gate-last fabrication method for vertical InAs nanowire transistors has been developed, that allows for an optimum design of the channel and the contact regions. Transistors fabricated using this method exhibit the best DC performance, in terms of a compromise between the normalised transconductance and sub-threshold swing, of any previously reported vertical nanowire MOSFET.

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Vertical InAs Nanowire Devices and RF Circuits

Martin Berg

LUND UNIVERSITY

Doctoral Thesis
Electrical Engineering
Lund, September 2015

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Abstract

Recent decades have seen an exponential increase in the functionality of electronic circuits, allowing for continuous innovation, which benefits society. This increase in functionality has been facilitated by scaling down the dimensions of the most important electronic component in modern electronics: the Si-based metal-oxide-semiconductor field-effect transistor (MOSFET). By reducing the size of the device, more transistors per chip area is possible. Smaller MOSFETs are also faster and more energy-efficient. In state of the art MOSFETs, the key dimensions are only few nanometers, rapidly approaching a point where the current scaling scheme may not be maintained. Research is ongoing to improve the device performance, mainly focusing on material and structural improvements to the existing MOSFET architecture.

In this thesis, MOSFETs based on nanowires, are investigated. Taking advantage of the nanowire geometry, the gate can be wrapped all-around the nanowires for excellent control of the channel. The nanowires are made in a high-mobility III-V semiconductor, indium arsenide (InAs), allowing for faster electrons and higher currents than Si. This device type is a potential candidate to either replace or complement Si-based MOSFETs in digital and analogue applications. Single balanced down-conversion mixer circuits were fabricated, consisting of three vertically aligned InAs nanowire MOSFETs and two nanowire resistors. These circuits are shown to operate with voltage gain in the GHz-regime. Individual transistors demonstrated operation with gain at several tens of GHz.

A method to characterise the resistivity and metal-semiconductor contact quality has been developed, using the transmission line method adapted for vertical nanowires. This method has successfully been applied to InAs nanowires and shown that low-resistance contacts to these nanowires are possible. To optimise the performance of the device and reach as close to intrinsic operation as possible, parasitic capacitances and resistances in the device structure need to be minimised. A novel self-aligned gate-last fabrication method for vertical InAs nanowire transistors has been developed, that allows for an optimum design of the channel and the contact regions. Transistors fabricated using this method exhibit the best DC performance, in terms of a compromise between the normalised transconductance and subthreshold swing, of any previously reported vertical nanowire MOSFET.

Populärvetenskaplig Sammanfattning

Under de senaste årtiondena har prestandan i elektriska kretsar växt i en rasande takt. Detta har lett till otaliga innovationer som har förbättrat samhället. Grunden till denna utveckling grundar sig i två uppfinningar: transistorn och den integrerade kresten.

Till skillnad från många andra grundläggande elektroniska komponenter har en transistor tre elektroder. En elektrisk ström skickas mellan två av elektroderna, såsom i ett motstånd, medans den tredje elektroden används för att styra hur stor denna ström ska vara. Det är detta styre, även kallad gate, som gör det möjligt att använda transistorn till digitala beräkningar, som är grunden i datorer, och till analoga applikationer, såsom radiosändare och mottagare. I en integrerad krets tillverkas idag miljardtals transistorer sida vid sida i halvledarmaterialet kisel. Att tillverka transistorerna på detta sätt är väldigt kostnadseffektivt och gör det möjligt att tillverka stora kretsar, såsom processorer. Under åren har tillverkningsmetoderna av integrerade kretsar utvecklats och lett till en förminskning av transistorernas storlek. De minsta dimensionerna i en modern transistor motsvarar idag ett par tiotal atomer i bredd. Ytterligare miniatyrisering är komplicerad och detta har lett till mycket forskning kring alternativa material och transistorstrukturer.

I detta arbete studeras användandet av halvledande nanotrådar i transistorer. Nanotrådar är cylindriska pelare i nanometerskalan. Genom att linda styret kring den nanotråden kan styrningen av strömmen göras effektivare än i konventionella transistorer. Nanotrådar kan byggas av flera halvledarmaterial, där indiumarsenid är ett av de materialen som har högst rörlighet för elektroner. Genom att kombinera materialegenskaperna av indiumarsenid med fördelarna av att nyttja en nanotråd, har välfungerande transistorer tillverkats. Under arbetets gång har InAs-transistorerna flyttats till kisel för att visa på ett kostnadseffektivt sätt att tillverka högprestandatransistorer.

Acknowledgments

RESEARCH is not the one-man show that it was in past times. Several people have contributed to the work presented in this thesis and I would like to take this opportunity to acknowledge them.

Lars-Erik, my main supervisor; you have helped me immensely by teaching me how to see the larger picture of our research and guided me in new and exciting directions. My supervisor Erik, I thank you for sharing your gigantic knowledge about semiconductor devices and helping me to be mindful of the details. Johannes, you may not have been one of my official supervisors, but you have largely functioned as one. You deserve much recognition for your innovative ideas, making it possible to do interesting research.

My fellow PhD students in the nanoelectronics group have all contributed to this work in some way, either through fruitful discussions or in tighter collaborations. I thank you for maintaining a great research environment and would consider it an honour to work with you all again in the future. My gratitude also extends to teachers, lab staff and co-workers I have had the pleasure of encountering over the years.

Especially I would like to thank my friend Kristofer Jansson. During our years of PhD studies, you have been a great help in always offering invaluable office discussions and off-work future studies. For me, it is evident that you have all the characteristics of a true scientist. I regret that we never co-wrote a paper, but I hope that we can work together in the future and make it so.

Finally, my thoughts go to my family and my girlfriend. You have made me the person I am today and encouraged me to pursue my dreams. Your support during these years have been invaluable and even though you have not seen much of me at times, you are always with me.

Peace and long life,
Martin Berg

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Preface

This thesis marks the final part of five years work towards the understanding and development of nanowire-based devices and circuits. The work has been performed within the nanoelectronics group at Lund University under the supervision of Professor Lars-Erik Wernersson and Associate Professor Erik Lind.

STRUCTURE OF THE THESIS

This thesis is divided into three main parts: introduction, appendix, and the included papers.

- **INTRODUCTION**
  In this part, common concepts within the research field is defined, and explained towards the goal of further understanding the papers that are included in the thesis. The content of the different chapters are stated below.

  1: **Background**
  In this chapter, a historical background to the semiconductor field is presented with the main emphasis of important innovations that are still heavily influencing the research field. The basic operation of a MOSFET is briefly discussed together with the main motivations for the work.

  2: **MOSFET Parasitics and Performance Metrics**
  This chapter defines and introduces the parameters commonly used to establish the DC and RF-performance of MOSFETs. Furthermore, the typical parasitic contributions for vertical nanowire

transistors are presented.

3: Vertical Nanowire MOSFET Fabrication
In this chapter, the fabrication of vertical nanowire transistors are discussed. Existing technologies before the thesis work and competing technologies is presented together with newly invented fabrication methods.

4: MOSFET Characterisation
The transistor performance for several types of nanowire transistors, fabricated using different approaches are compared to highlight the importance of minimising parasitic contributions. The latest transistor results are finally benchmarked against competing technologies.

5: Mixer Circuit
The importance and basic operation of a mixer circuit is explained. Specifically, the nanowire-based mixer implementation is presented and its performance metrics are defined.

6: Material characterisation
This chapter presents some standard semiconductor characterisation metods, often used to characterise planar semiconductor devices. These methods are implemented on InAs epitaxial layers on silicon (Si). Furthermore, a new method for the characterisation of metal contacts on vertical nanowires are presented and discussed.

7: Conclusion and Outlook
The introduction part is ended with the main conclusions from the work together with an outlook for the future of the research field and semiconductor industry.

- **APPENDICES**
  Further details on various aspects of the work can be found in the appendices.

  A: MOSFET Fabrication Using the Self-Aligned Gate-Last Process
  The exact fabrication steps for the latest generation of vertical InAs nanowire MOSFETs are reproduced.

- **PAPERS**
  The included papers are reproduced in the back of the thesis.

INCLUDED PAPERS

The following papers are included in this thesis and the respective published or draft versions are appended at the back of this thesis.

Paper I: M. Berg, K.-M. Persson, O.-P. Kilpi, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Gate-Last Fabrication of Enhancement Mode Vertical InAs Nanowire Transistors," *IEEE Electron Device Lett.* Manuscript

▶ *I co-fabricated the devices, collaborated on the measurements, did most of the analysis, and wrote most of the paper.*

Paper II: M. Berg, J. Svensson, E. Lind, and L.-E. Wernersson, "A transmission line method for evaluation of vertical InAs nanowire contacts," *Appl. Phys. Lett.*. Submitted manuscript in June 2015, undergoing review

▶ *I performed almost all of the work on this paper.*

Paper III: M. Berg, K.-M. Persson, J. Wu, H. Sjöland, E. Lind, and L.-E. Wernersson, "InAs nanowire MOSFETs in three-transistor configurations: single balanced RF down-conversion mixers," *Nanotechnology*, vol. 25, no. 48, Dec. 2014.

▶ *I co-fabricated the devices, did the RF and DC measurements in collaboration, did half of the analysis, and wrote the paper.*

Paper IV: K.-M. Persson, M. Berg, H. Sjöland, E. Lind, and L.-E. Wernersson, "InAs nanowire MOSFET differential active mixer on Si-substrate," *Electron. Lett.*, vol. 50, no. 9, pp. 682–+, Apr. 2014.

▶ *I co-fabricated the devices, did the RF and DC measurements in collaboration, did half of the analysis, and co-edited the article.*

Paper V: K.-M. Persson, M. Berg, M. B. Borg, J. Wu, S. Johansson, J. Svensson, K. Jansson, E. Lind, and L.-E. Wernersson, "Extrinsic and Intrinsic Performance of Vertical InAs Nanowire MOSFETs on Si Substrates," *IEEE Trans. Electron Dev.*, vol. 60, no. 9, pp. 2761–2767, Sep. 2013.

▶ *I co-fabricated the devices, collaborated on the RF and DC measurement, and co-edited the article.*

Paper VI: S. G. Ghalamestani, M. Berg, K. A. Dick, and L.-E. Wernersson, "High quality InAs and GaSb thin layers grown on Si (111)," *J. Cryst. Growth*, vol. 332, no. 1, pp. 12–16, Oct. 2011.

▶ *I fabricated Hall devices, did all electrical characterization and analysis, and co-wrote the article.*

Paper VII: S. Johansson, M. Berg, K.-M. Persson, and E. Lind, "A High-Frequency Transconductance Method for Characterization of High-κ Border Traps in III-V MOSFETs" *IEEE Trans. Electron Dev.*, vol. 60, no. 2, pp. 776–781, Feb. 2013.

► *I co-fabricated the nanowire MOSFETs characterized and co-edited the article.*

EXTRANEOUS PAPERS

The following papers are not included in the thesis, but summarise related work which I have contributed to.

Paper viii: M. Berg, K.-M. Persson, O.-P. Kilpi, J. Svensson, E. Lind, and L.-E. Wernersson, "Self-Aligned, Gate-Last Process for Vertical InAs Nanowire MOSFETs on Si," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 7-9, 2015, Accepted for oral presentation.

Paper ix: M. Berg, K.-M. Persson, E. Lind, H. Sjöland, and L.-E. Wernersson, "Single Balanced Down-Conversion Mixer Utilizing Indium Arsenide Nanowire MOSFETs," in *26th Int. Conf. on Indium Phosphide and Related Materials (IPRM)*, May. 11-15, 2014, presented.

Paper x: M. Berg, J. Svensson, S. G. Ghalamestani, E. Lind, and L.-E. Wernersson, "Doping Control in InAs Epitaxial Layers on Si," *39th International Symposium on Compound Semiconductors (ISCS)*, Aug. 27-30, 2012, poster presentation.

Paper xi: K.-M. Persson, M. Berg, M. Borg, J. Wu, H. Sjöland, E. Lind, and L.-E. Wernersson, "Vertical InAs Nanowire MOSFETs with $I_{DS} = 1.34$ mA/µm and $g_m = 1.19$ mS/µm at $V_{DS} = 0.5$ V," in *70th Annual Device Research Conf. (DRC)*, Jun. 18-20, 2012, pp. 195–196.

Paper xii: K.-M. Persson, M. Berg, E. Lind, and L.-E. Wernersson, "$1/f$-noise in Vertical InAs Nanowire Transistors," in *25th Int. Conf. on Indium Phosphide and Related Materials (IPRM)*, May. 19-23, 2013.

Paper xiii: J. Wu, K. Jansson, A. S. Babadi, M. Berg, E. Lind, and L.-E. Wernersson, "RF-Characterization of Vertical Wrap-gated InAs/high-k Nanowire Capacitors," *IEEE Trans. Electron Dev.*, vol. 59, no. 10, pp. 2733–2738, Oct. 2011. Submitted manuscript in August 2015, undergoing review

Paper xiv: S. Johansson, M. Egard, S. G. Ghalamestani, M. Borg, M. Berg, L.-E. Wernersson, and E. Lind, “RF Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates,” *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2733–2738, Oct. 2011.

Paper xv: S. Johansson, S. G. Ghalamestani, M. Egard, M. Borg, M. Berg, L.-E. Wernersson, and E. Lind, “High frequency vertical InAs nanowire MOSFETs integrated on Si substrates,” in *Physica Status Solidi C*, vol. 9, no. 2, 2012.

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Abbreviations and Symbols

ABBREVIATIONS

ADC Analogue-to-digital converter
AFM atomic force microscopy
ALD atomic layer deposition
Ar argon
As arsenic
AsH_3 arsine
Au gold

BDEAS bis(diethylamino)silane
BOE buffered oxide etch

CB conduction band
CVD chemical vapour deposition

DIW de-ionized water
DR double-row array

EBL electron beam lithography
EOT effective oxide thickness

GAA gate all-around
Ge germanium

HBT heterojunction bipolar transistor
HEMT high-electron-mobility transistor
HEX hexagonal array
HSQ hydrogen silsesquioxane

ICP-RIE inductively coupled plasma reactive-ion etching
IF intermediate frequency
In indium
InAs indium arsenide
InGaAs indium gallium arsenide
InP indium phosphide
InSb indium antimonide
IPA 2-propanol
ITRS international technology roadmap for semiconductors

LNA low-noise amplifier
LO local oscillator

MESFET metal-semiconductor field effect transistor
MIBK methyl isobutyl ketone
MOSFET metal-oxide-semiconductor field-effect transistor
MOVPE metalorganic vapour phase epitaxy

N_2 nitrogen
Ni nickel
NW nanowire

O oxygen

Pd paladium
PEALD plasma-enhanced atomic layer deposition
PMMA poly(methyl methacrylate)

RF radio frequency
RIE reactive-ion etching

SEM scanning electron microscopy
Si silicon
SIMS secondary ion mass spectrometry
Sn tin

TDMAHf tetrakis(dimethylamino)hafnium
TDMATi tetrakis(dimethylamido)titanium
TESn tetraethyltin
Ti titanium
TLM transmission line model
TMA trimethylaluminium
TMAH tetramethylammonium hydroxide

TMIn trimethylindium

UV ultraviolet

VLS vapor-liquid-solid

W tungsten

GREEK SYMBOLS

$\boldsymbol{\epsilon_0}$ ($A^2s^4kg^{-1}m^{-3}$) Vacuum permittivity: approximately equal $8.854 \cdot 10^{-12}$
$\boldsymbol{\epsilon_r}$ (unitless) Relative permittivity

$\boldsymbol{\mu}$ ($m^2/(Vs)$) Mobility
  $\boldsymbol{\mu_e}$ Electron mobility
  $\boldsymbol{\mu_p}$ Hole mobility

$\boldsymbol{\eta}$ (unitless) Ideality factor

$\boldsymbol{\rho}$ (Ωm^2) Resistivity
  $\boldsymbol{\rho_c}$ Specific contact resistivity
  $\boldsymbol{\rho_s}$ Semiconductor resistivity

LATIN SYMBOLS

$\boldsymbol{A_{V,OC}}$ (unitless) Open-circuit voltage gain. Transistor self-gain.

$\boldsymbol{B}$ (T) Magnetic field

$\boldsymbol{C}$ (F) Capacitance
  $\boldsymbol{C_{DS}}$ Drain-soue capacitance
  $\boldsymbol{C_{GD}}$ Gate-drain capacitance
  $\boldsymbol{C_{GS}}$ Gate-source capacitance
  $\boldsymbol{C_{ox}}$ Gate oxide capacitance

e (unitless) Euler′s number: approximately equal to 2.71828
$\boldsymbol{E_g}$ (J) Band gap energy

$\boldsymbol{f}$ (Hz) Frequency
  $\boldsymbol{f_{IF}}$ Intermediated frequency
  $\boldsymbol{f_{LO}}$ Local oscillator frequency
  $\boldsymbol{f_{max}}$ Maximum oscillation frequency
  $\boldsymbol{f_{RF}}$ Radio frequency (often input signal)

- **f_{T}** Transition frequency

F (N) Lorentz force

g (S) Conductance
- **g_{d}** Output conductance
- **g_{m}** Transconductance
- **$g_{\mathrm{m,i}}$** Intrinsic transconductance
- **$g_{\mathrm{m,max}}$** Maximum transconductance
- **$g_{\mathrm{m,RF}}$** Transconductance of the RF-transistor

G_{VC} (unitless) Voltage conversion gain

h_{21} (unitless) Current gain from hybrid parameter

I (A) Current
- **I_{DS}** Drain-source current
- **I_{D}** Drain current
- **I_{off}** Off-current
- **I_{on}** On-current

IIP_3 (W) Input referred third-order intercept point
IM_3 (W) Third-order intermodulation product

k (m^2 kg s^{-2} K^{-1}) Boltzmann constant

L (m) Length
- **L_{c}** Contact length
- **L_{G}** Gate length
- **L_{T}** Transfer length

n (m^{-3}) Carrier concentration
n_{s} (m^{-2}) Sheet carrier concentration

OIP_3 (W) Output referred third-order intercept point

$P_{\mathrm{in},-1\mathrm{dB}}$ (W) Input referred 1 dB-compression point

q (As) Elementary charge
Q (kS dec./(Vm)) Quality factor, $g_{\mathrm{m,max}}/SS_{\mathrm{min}}$

r_{NW} (m) Nanowire radius
R (Ω) Resistance
- **R_{c}** Contact resistance
- **R_{D}** Drain resistance
- **R_{G}** Gate resistance
- **R_{L}** Load resistance

- R_{NW} Nanowire resistance
- R_{on} On-resistance
- R_{s} Semiconductor resistance
- R_{S} Source resistance
- R_{SH} Sheet resistance
- R_{tot} Total resistance

s (m) Width of the center conductor in a co-planar waveguide

SS (mV/decade) Sub-threshold swing
- SS_{min} Minimum sub-threshold swing

t (m) Thickness
- t_{ox} Gate dielectric thickness
- t_{s} Semiconductor thickness

T (K) Temperature

U (unitless) Unilateral power gain

$v_{\mathrm{inj,e}}$ (m/s) Electron injection velocity

V (V) Voltage
- V_{DD} Supply voltage
- V_{DS} Drain-source voltage
- V_{GS} Gate-source voltage
- V_{H} Hall voltage
- V_{out} Output voltage
- V_{RF} AC voltage at the gate of the RF-transistor
- V_{T} Threshold voltage

w (m) Gap distance between the center conductor and the ground plane in a co-planar waveguide

W_{s} (m) Width of semiconductor resistor

Y (S) Admittance
- Y_{11} Short-circuit input admittance parameter
- Y_{12} Short-circuit reverse transfer admittance parameter
- Y_{21} Short-circuit forward transfer admittance parameter
- Y_{22} Short-circuit output admittance parameter

FUNCTIONS AND OPERATORS

$\coth(\cdot)$ hyperbolic cotangent

$\ln(\cdot)$ logarithm with the base e

$\mathbf{log_{10}}(\cdot)$ logarithm with the base 10

$\mathbf{Re}(\cdot)$ Real part of a complex number

INTRODUCTION

1

Background

FOR many decades, the semiconductor technology have seen a tremendous development, with continuous improvements to established ideas or the invention of completely new devices or applications. This development has had a great impact on society through high data rate communications and computing.

This chapter consists of an overview of semiconductor history, recent developments in the field, and an introduction to the main concepts that serves as motivation for the work presented in this thesis.

1.1 THE EMERGENCE OF SEMICONDUCTOR ELECTRONICS

The first transistor was fabricated in 1947 at Bell Lab [1], with the work later being awarded with the Nobel physics prize 1956. In that effort, the research team led by William Shockley tried to produce the first functioning field-effect transistor, which was already conceived on a theoretical level decades earlier. The integrated circuit was invented by Kilby in 1958 and patented in 1959 [2], with the idea that all the electronic building blocks could be fabricated on the same semiconductor substrate with metals connecting them, forming circuits. This new fabrication method allowed for many components to be manufactured simultaneously while at the same time connecting them to form more complex circuits than had previously been produced using individually package components. The vast majority of transistors used in today's integrated circuits are metal-oxide-semiconductor field-effect transistors (MOSFETs), which were invented in 1959 and patented in the following year [3].

1.2 METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

The active region of the MOSFET is called the channel and is made in a semiconductor material, with silicon (Si) being the most commonly used. Semiconductors are intrinsically highly resistive materials as they, compared to metals, have few free electrons that can flow with an applied voltage. This stems from the energy band gap (E_g) for semiconductors. The band gap, depicted in Figure 1.1a, is a range of energies, which no electrons can occupy. In an intrinsic semiconductor, almost all electrons occupy states in the valence band, but in order for the electrons to contribute to a current, they have to be excited to the conduction band. By heating or illuminating the semiconductor, electrons can absorb energy which can give them enough potential energy to instead occupy a free state in the conduction band. Another way to control the conductivity, is by a process called doping, in which atoms in the crystal lattice are substituted by atoms with more or fewer valence electrons, resulting in n-doping and p-doping, respectively. The resulting crystal thus have a surplus of mobile charges in the conduction or valence band for n-type or p-type semiconductors, respectively. One way to characterise how the semiconductor is doped, is by using the Fermi level, which illustrates the highest occupied energy level at the absolute zero temperature with some spreading occurring at elevated temperatures [4]. The Fermi levels for three types of dopings are illustrated in Figure 1.1a, denoted by $E_{F,i}$, $E_{F,n}$, and $E_{F,p}$ for an intrinsic (undoped), n-type, and p-type semiconductor, respectively.

In a MOSFET, the semiconductor channel is covered by a conductive electrode, called the gate, which is usually made using a metal. The gate and the channel are electrically isolated from each other by an insulating dielectric layer, often an oxide, and thus building up the metal-oxide-semiconductor (MOS) structure. The semiconductor channel is contacted to two terminals at either end of the device, called the source and the drain. With an applied voltage between drain and source, V_{DS}, a current, I_{DS}, can flow between the electrodes, similar to a resistor. MOSFETs come in two main types: n-type, where electrons are the main charge carriers flowing in the conduction band; and p-type, where instead holes are transported in the valence band.

The magnitude of I_{DS} is controlled, in part by V_{DS}, but also with the third electrode, the gate. The MOS-structure give rise to a capacitance, which makes it possible to control the potential and thus the energy of the channel as illustrated in Figure 1.1b) for an n-type device. For a constant V_{DS}, an electric field exists between the drain and source. The mobile electrons in the conduction band will flow against the field, achieving lower potential energy, i.e. flowing from source to drain. By varying the gate voltage (V_{GS}), and thus the conduction band energy alignment to the source, it is possible to tune the height of the energy barrier between the drain and source. By increasing V_{GS},

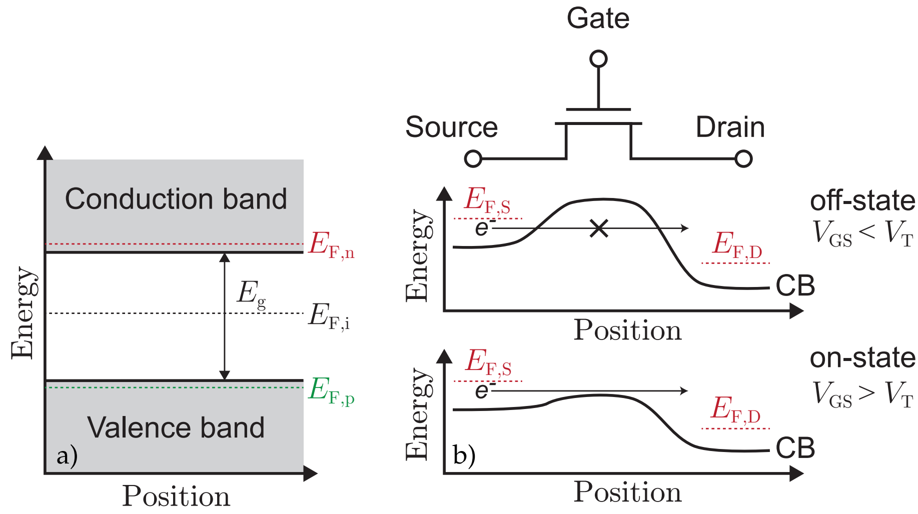

Gate
Source
Drain
Energy
Conduction band
$E_{\mathrm{F,n}}$
E_{g}
$E_{\mathrm{F,i}}$
$E_{\mathrm{F,p}}$
Valence band
a)
Position
$E_{\mathrm{F,S}}$
e^-
$E_{\mathrm{F,D}}$
CB
off-state
$V_{\mathrm{GS}} < V_{\mathrm{T}}$
Energy
Position
$E_{\mathrm{F,S}}$
e^-
$E_{\mathrm{F,D}}$
CB
on-state
$V_{\mathrm{GS}} > V_{\mathrm{T}}$
Energy
b)
Position

Figure 1.1: a) Band diagram of a semiconductor depicting the band gap between the valence and conduction bands. Also depicted is three Fermi level energies corresponding to n-type (red), intrinsic (black), and p-type semiconductors (green). b) The on- and off-states illustrated along the nanowire channel as an energy band diagram for an n-type transistor with an applied V_{DS}. Only the conduction band (CB) is shown as negligible transport occurs in the valence band.

the potential barrier is lowered, resulting in that more electrons reaches the drain and thus an increased current. If instead V_{GS} is lowered, the energy barrier is raised, thus turning the transistor off [5]. This switching between the on- and off-states can be done in a very energy-efficient way in a well-designed MOSFET.

Compared to other types of transistors the MOSFET offer low leakage currents from the gate electrode, due to the insulating layer between gate and semiconductor. Other types of field-effect transistors, like high-electron-mobility transistors (HEMTs) and metal-semiconductor field effect transistors (MESFETs), uses a semiconductor barrier or a Shottky barrier, respectively, instead of an insulating oxide [6]. These barriers offer less insulation than popular gate dielectrics, which results in higher gate currents [7]. The combined properties of energy-efficient on/off-switching and low gate leakage allows for low-power computing.

1.3 MOORE'S LAW

The framework established by the invention of the integrated circuit allowed for shrinking, also called scaling, of device dimensions, with the main driving force of the shrinking being more functionality per chip area and faster MOSFET switching speed. The rate of the dimension scaling led to the famous prediction coined by Gordon E. Moore in 1965 [8]. He stated that the number of transistors per chip area would double every year, which eventually was restated as a doubling in transistor count every two years in 1975 [9]. This prediction, often referenced as Moore's law, was estimated to hold for the following decade and was quickly adopted by industry as a self-fulfilling prophecy that guided the investments and goals for the semiconductor industry. The clock frequency, which roughly translates to the speed of the integrated circuit, doubled about every three years, originating from the shortening of the gate length (L_G). This was sustained up until about 2003, when the amount of power dissipated as heat of a processor reached close to $100\,\mathrm{W\,cm^{-2}}$, resulting in too high requirements of circuit cooling for many commercial applications. State of the art MOSFETs could potentially run at much higher clock frequency than the 3 to 4 GHz of today's high-performance processors.

Moore's law continued, but instead of clock frequency scaling, the performance increase was accomplished by increasing the number of processor "cores" on the same chip. The performance increase with the number of cores is decided by how much of the calculations that can be performed in parallel for a specific software application [10]. The prediction set up by Moore endured until about 2010, with the current scaling rate now following closer to a doubling of the number of transistors every two and a half years.

1.4 MOSFET EVOLUTION

Over the decades, the MOSFET has evolved by implementing new technologies and fabrication methods when the need was present, in order to maintain Moore's scaling law. During device scaling of the gate length, L_G, and other dimensions, the oxide capacitance, C_{ox}, is increased to maintain electric field patterns within the device [11]. One way to accommodate this is by a decrease in the oxide thickness, t_{ox}, evident from

$$C_{\mathrm{ox}} = \frac{\epsilon_0 \epsilon_{\mathrm{r}}}{t_{\mathrm{ox}}}. \tag{1.1}$$

At thicknesses of just a few nm, however, quantum mechanical tunnelling of charge carriers through the oxide becomes noticeable, resulting in higher off-state leakage and thereby less energy efficient computing. One way to solve the tunnelling problematic is by increasing the relative permittivity, ϵ_r, of the oxide layer, allowing for a thicker oxide layer.

Indeed, the problem with tunnelling was observed during the 1990s, which saw the evolution from SiO_2, with $\epsilon_r = 3.9$, to SiO_xN_y, which has a ϵ_r ranging between 3.9 and 7.8 with the higher numbers obtained with high nitride content. In the years following 2007, materials with even higher ϵ_r, such as HfO_2, were implemented and continually used by industry. The relative dielectric constant may also be denoted by κ, thus the term high-κ dielectrics.

1.4.1 GEOMETRY OF TRANSISTOR CHANNEL

Until 2011, MOSFETs were more or less planar devices with a gate controlling the channel potential from one direction, similar to the schematic illustration of Figure 1.2a.

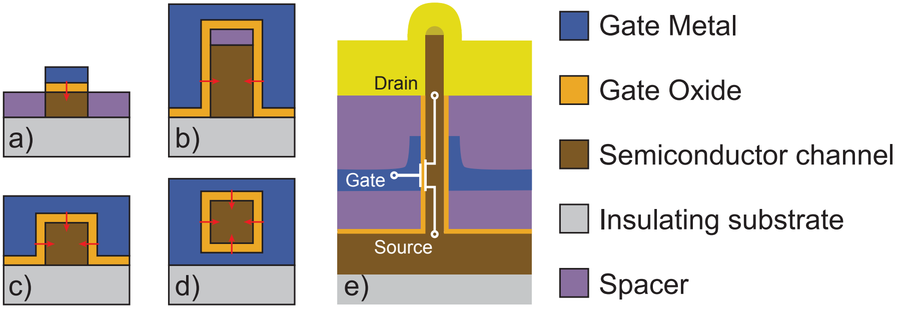


Figure 1.2: Schematic cross-sectional illustration of different nanowire channel geometries: a) Single-sided gate, b) Fin-, c) Tri-gate-, d) lateral gate-all-around, and e) vertical gate-all-around MOSFET. The red arrows illustrate the direction of the electric field at the different surfaces. For the first four lateral architectures, the source and drain regions are situated normal to the paper.

The last couple of years have seen the introduction of multi-gate devices, in which the gate controls the channel potential from several surfaces. Such a device offers better electrostatic control of the semiconductor channel as the capacitance to channel volume ratio is larger. Furthermore, the extra gate area have only a small impact on the device area as seen from the top, i.e. the footprint area, resulting in a large performance boost per device area. A multi-gate device, with gate control from two sides, is called a Fin-FET (Figure 1.2b), with the name originating from the shape of the semiconductor channel sticking up from the planar substrate. A tri-gate MOSFET (Figure 1.2c), is a similar device but the gate also operates on the top side. Compared to a Fin-FET, a tri-gate is almost symmetrical in terms of the length of the gating sidewalls. The tri-gate structure has recently been introduced in industrial fabrication.

The best electrostatic gate control is obtained by surrounding the gate around the entire semiconductor channel [12, 13], often referred to as a gate all-around (GAA) design. In this gate architecture the semiconductor is referred to as a nanowire, which can either be aligned laterally or vertically, with the lateral version illustrated in Figure 1.2d. The potential benefit of using a vertical structure is the possibility of designing L_G and metal contact lengths without affecting the device footprint area. A vertical nanowire MOSFET is shown in Figure 1.2e with an overlay of the circuit symbol to illustrate the different electrodes.

1.4.2 SEMICONDUCTOR MATERIALS

There is a number of material properties that determine the intrinsic performance of the transistors. For a long-channel device (L_G longer than the mean free path) an important parameter is the charge carrier mobility, μ, which is a measure of how easily mobile charges are transported in the material. With an applied electric field, the charges are accelerated to a certain velocity, with charges in a material with high mobility reaching higher velocities. For a short-channel device, where ballistic carrier transport dominates, the velocity is instead set by the injection velocity. The velocity of the charges correlate roughly to the current flowing through the device.

In today's semiconductor industry, MOSFETs are based on Si, which has been extensively used for over 50 years with its main advantage over many other semiconductors being the formation of a native oxide with a good oxide-semiconductor interface. Germanium (Ge) is used in industry [14, 15] in the contact regions to achieve a higher channel mobility, and therefore higher currents. Si and Ge does not, however, have the highest mobilities for all semiconductors as observed in Table 1.1.

Here, the electron and hole mobilities are provided together with the electron injection velocity for a number of semiconductors extensively studied in transistors. The highest electron mobilities, μ_e, can be found in compound semiconductors, consisting of group III and group V elements, such as indium antimonide (InSb) and indium arsenide (InAs) with values of about $70\,000\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ and $40\,000\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, respectively. Both of these semiconductors have narrow band gaps and a light electron mass, which translates to fast carriers under an applied electric field. Generally, hole mobilities, μ_p, are much lower than the electron mobilities with Ge having the highest hole mobility at about $1900\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$. At small semiconductor dimensions, as in ultra-scaled MOSFETs, the surface to volume ratio is large, which results in increased surface scattering. For these small dimensions, the

Table 1.1: Intrinsic semiconductor parameters where μ_e is the electron mobility, μ_p is the hole mobility, and $v_\mathrm{inj,e}$ is the electron injection velocity [16].

Semiconductor	μ_e [cm^2/(Vs)]	μ_p [cm^2/(Vs)]	$v_\mathrm{inj,e}$ at L_G= 30 nm [cm/s]
Si	1400	450	$1.2 \cdot 10^7$
InAs	40000	500	$3.7 \cdot 10^7$
$\mathrm{In_{0.53}Ga_{0.47}As}$	12000	300	$2.8 \cdot 10^7$
Ge	3900	1900	
InSb	70000	1000	
GaSb	7000	1000	
GaAs	8500	400	

mobility is much smaller than the bulk values reported in Table 1.1, but the general trend still applies. It is therefore assumed that higher performance, in terms of speed and energy efficiency, can be expected by utilizing these high-mobility materials [17].

III-V semiconductors are expected to be introduced in the large-scale semiconductor industry in a couple of years with the International Technology Roadmap for Semiconductors (ITRS) predicting the introduction occuring already in 2018 [18]. The III-V semiconductors would be utilized for the n-type transistor with its p-type companion probably based on Ge. An expected speed boost of 50 % and 40 % lower switching energy compared to high-performance Si, is expected for this change of material. It is likely that tri-gate MOSFETs will be the geometry of choice with a possibility for GAA nanowires a few years later.

2

MOSFET Parasitics and Performance Metrics

In order to characterise MOSFET devices, different standardised metrics have been established. Some of the metrics are shared with other types of transistors, whereas others are mostly attributed only to field-effect transistors. Characterisation and the extraction of various performance metrics are integral to the general understanding of the intrinsic device and its limitations. Furthermore, it allows for benchmarking to other similar devices [19], and imperative for circuits design. The performance of a transistor is always limited by parasitic elements [20]. By analysing the transistor characteristics and by device modelling, knowledge about these parasitics can be extracted, and in turn making it possible to limit their impact.

In this chapter, an overview of the parasitics in vertical nanowire MOSFETs is presented followed by a walkthrough of some of the most important MOSFET performance metrics, used throughout the thesis.

2.1 PARASITICS

In vertical nanowire MOSFETs, the main parasitic contributions come from resistances and capacitances in series or in parallel with the active device. The vertical architecture has been shown, through modelling, to be highly competitive compared to alternative device layouts for highly scaled device dimensions [21].

2.1.1 RESISTANCES

Parasitic resistances connected to the active device limit the effective voltage drops across the device. Their effect on the transistor performance can vary depending on their linearity, at what frequency the device is run at, and temperature.

The major parasitic resistance contributions for a vertical nanowire MOSFET can be seen in Figure 2.1a. Several resistive elements are positioned in series with the intrinsic transistor, resulting in voltage division and therefore a lower effective V_{DS} over the channel. On the drain side, the resistance can be divided into three elements $R_{\mathrm{D,m}}$, $R_{\mathrm{D,c}}$, and $R_{\mathrm{D,s}}$; corresponding to resistive paths in the metal electrode, the metal-semiconductor interface, and the ungated spacer segment, respectively. Similar elements can be found on the source side, where the ungated spacer and the bottom electrode (in this case the same semiconductor as the nanowire), are the main contributors. At high frequency operation, the gate resistance R_{G} can have an impact on the performance. It should be noted that these resistive elements are not necessarily linear in terms of their I-V characteristics. Especially metal-semiconductor contacts often exhibit non-ohmic behaviour.

One of the main benefits of a vertically aligned MOSFET is the potential for longer metal contacts without affecting the footprint area. This applies to contacts implemented on both the top and bottom part of the nanowire. An additional benefit originates from the growth of nanowires, where high-quality materials of different lattice constants can be grown on top of each other. This allows for the use of specific materials for ungated or contact regions in order to minimise the series resistances.

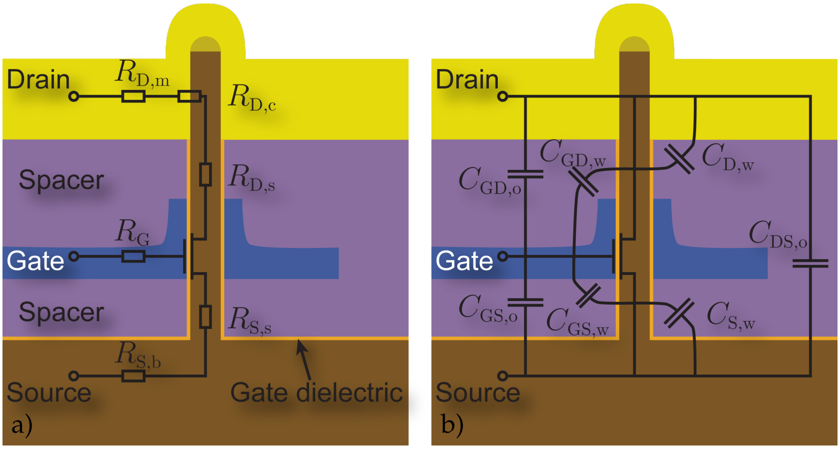

Drain
$R_{\mathrm{D,m}}$
$R_{\mathrm{D,c}}$
Spacer
$R_{\mathrm{D,s}}$
R_{G}
Gate
Spacer
$R_{\mathrm{S,s}}$
$R_{\mathrm{S,b}}$
Source
Gate dielectric
a)
Drain
$C_{\mathrm{GD,w}}$
$C_{\mathrm{D,w}}$
$C_{\mathrm{GD,o}}$
$C_{\mathrm{DS,o}}$
Gate
$C_{\mathrm{GS,o}}$
$C_{\mathrm{GS,w}}$
$C_{\mathrm{S,w}}$
Source
b)

Figure 2.1: Schematic images of a vertical nanowire MOSFET with an overlay illustrating the effective transistor together with a) parasitic resistance elements and b) parasitic capacitances. In the subscripts; s, m, b, w, and o, denotes contact, metal, bottom, wire, and overlap, respectively.

2.1.2 CAPACITANCES

Capacitances in the vertical nanowire architecture can be divided into two groups: overlap capacitances and fringing capacitances between electrodes or between electrode and nanowire (Figure 2.1b). The overlap capacitances can easily be calculated by the overlapping area, the permittivity of the spacer layers and their thicknesses, assuming a parallel-plate model. More complicated is the calculation of fringing capacitances, but approximative analytical calculations are easily performed [22]. For accurate determination of the capacitances, the entire electric field need to be solved numerically [23].

The parasitic capacitances can be minimised by a large spacing between electrodes, resulting in thick spacer layers and instead large series resistances. An optimum spacer layer thickness exist which is dependent on the permittivity of the spacer layer and resistivity of the ungated regions. The best possible spacer is air, with its low relative permittivity of close to 1. Other materials are, however, usually used for mechanical stability, such as SiO_2 or Si_3N_4. The overlap capacitance is most effectively minimised by the reduction of the overlap between source, gate, and drain. This was successfully performed in [24] using electron beam lithography (EBL).

2.2 DC METRICS

The drain current, I_D, of a MOSFET is, in common-source configuration, dependent on both the gate-source voltage, V_GS, and the drain-source voltage, V_DS. One way to depict I_D, would be as three-dimensional graphs with V_DS and V_GS occupying the two remaining axes. Three-dimensional graphs are, however, more difficult to grasp than their two-dimensional counterparts. Commonly, the current is instead illustrated using two different two-dimensional graphs: the output characteristics, I_D represented as a function of V_DS at a constant V_GS, and the transfer characteristics, I_D as a function of V_GS at a constant V_DS.

2.2.1 TRANSCONDUCTANCE

An important transistor metric, especially in radio frequency (RF) applications, is the transconductance, g_m. It is defined as the partial derivative of the drain current with respect to the gate-source voltage, defined as

$$g_\text{m} \equiv \frac{\partial I_\text{D}}{\partial V_\text{GS}}. \tag{2.1}$$

From this definition, the transconductance can be understood as the current amplification acquired with a small-signal voltage on the gate electrode. In a circuit, the resulting current can drive some load, e.g. a resistor, and thus give rise to a voltage or power at the load. A high transconductance is favourable in RF-circuits as it allows for high low-frequency gain. For digital applications, a high g_m is important since a lower supply voltage, V_DD, could be used while maintaining a certain drive current. A typical transconductance curve, together with its corresponding transfer characteristics, is illustrated in Figure 2.2a. A clear peak is observed, often denoted as $g_\mathrm{m,max}$.

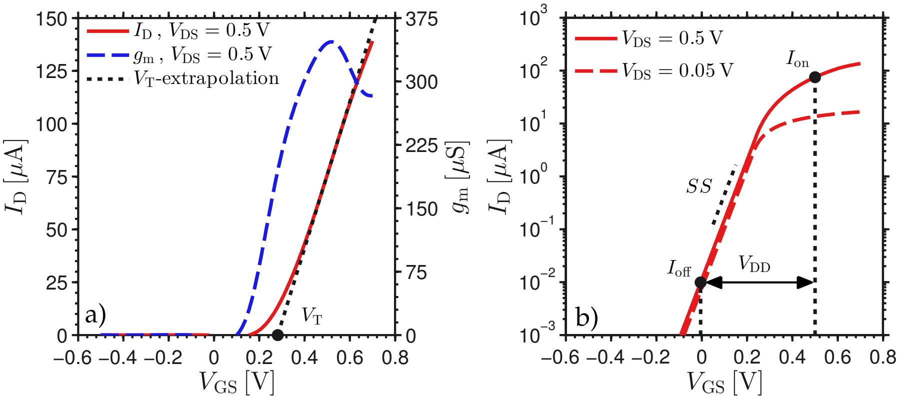


Figure 2.2: Transfer characteristics of a MOSFET in linear scale, a), and logarithmic scale, b). The MOSFET characteristics are calculated from a simple MOSFET-model with added series resistances on both the source and drain side. a) g_m is shown together with I_D and V_T is extrapolated from $g_\mathrm{m,max}$. b) The sub-threshold characteristics are seen as the linear slope for $V_\mathrm{GS} < 0.2\,\mathrm{V}$. SS corresponds to the slope of the exponentially increasing current in logarithmic scale. Also plotted in b) are I_off corresponding to $100\,\mathrm{nA}\,\mu\mathrm{m}^{-1}$ and its related I_on for a V_DD of 0.5 V

2.2.2 THRESHOLD VOLTAGE

The threshold voltage, V_T, signifies the gate-source voltage in which the transistor transitions between the on-state and the off-state. This transition does not occur abruptly and its extraction from measurement data can thus be somewhat arbitrary. One popular extraction method is to linearly extrapolate the current in the saturation region as a function of V_GS. The transfer characteristics does not, however, necessarily follow a linear relation to V_GS and often the maximum transconductance peak is used as the anchor point for the extrapolation. An example of a V_T-extraction can be seen in Figure 2.2a.

2.2.3 SUB-THRESHOLD SWING

One of the most important MOSFET metrics for digital applications is the sub-threshold swing (SS). At gate voltages below the threshold voltage, I_D increases exponentially with V_GS as seen in Figure 2.2b. On a logarithmic scale, the linear current increase is called the sub-threshold slope which is the inverse of the sub-threshold swing. SS is modelled as a thermionic injection over a potential barrier and expressed as

$$SS = \frac{1}{\log_{10}(\mathrm{e})} \frac{\eta k T}{q}. \tag{2.2}$$

Here q is the elementary charge, k is the Boltzmann constant, T is the temperature, e is Euler's number and η is the ideality factor, which can vary from the ideal value of 1 to higher values. For an ideal MOSFET, with $\eta = 1$, an SS of $60\,\mathrm{mV\,decade^{-1}}$ is obtained at room temperature. The sub-threshold current increases by a factor of 10 (one decade) over a V_GS range of 60 mV.

SS determines the effectiveness of the MOSFET as a switch. A steep sub-threshold slope results in a large ratio between the on-current, I_on, and the off-current, I_off. If SS deviates too much from the ideal $60\,\mathrm{mV\,decade^{-1}}$, either the off-state leakage increases or on-state current decreases dependent on the choice of threshold voltage. An increased off-state leakage current results in high power dissipation, which is unacceptable for large circuits, e.g. a processor, or circuits aimed for low-power applications. The international technology roadmap for semiconductors (ITRS) states a maximum I_off of $100\,\mathrm{nA\,\mu m^{-1}}$ for high-performance devices, whereas MOSFETs aimed for low-power implementations have maximum I_off of $10\,\mathrm{nA\,\mu m^{-1}}$ [18]. I_on is determined by the supply voltage, and is ideal as high as possible for faster switching or higher operation frequency of the MOSFETs.

2.2.4 OUTPUT CONDUCTANCE

A typical MOSFET output characteristic can be seen in Figure 2.3. The output conductance, g_d, is defined in the same way as g_m, as a partial derivative, but now instead with respect to V_DS,

$$g_\mathrm{d} \equiv \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{DS}}. \tag{2.3}$$

The output conductance is important to consider for RF applications. In a common-source stage, e.g. in an amplifier, the low-frequency open-circuit voltage gain, $A_\mathrm{V,OC}$, can be calculated as

$$A_\mathrm{V,OC} = \frac{-g_\mathrm{m}}{g_\mathrm{d}}. \tag{2.4}$$

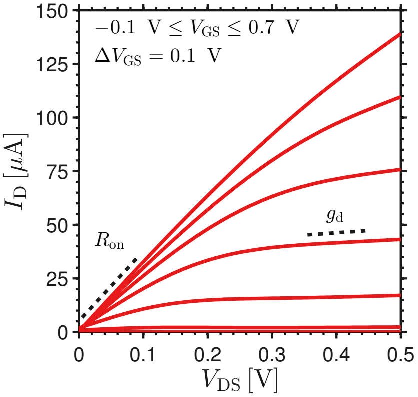


Figure 2.3: Output characteristics of a MOSFET, based on the same model as depicted in the transfer characteristics of Figure 2.2. g_d is defined as the derivative of the output characteristics, with R_on being defined only in linear region.

The ratio of (2.4) is commonly referred to as the transistor self gain and can be utilised to find optimum biasing conditions or benchmarking against other MOSFETs. Ideally, the saturation current is independent of V_DS, resulting in infinite $A_\mathrm{V,OC}$, but is in reality finite for scaled MOSFETs due to the influence of the drain voltage on the potential in the channel.

2.2.5 ON-RESISTANCE

The current in a MOSFET is very dependent on its extrinsic series resistances. One way to estimate the magnitude of these resistances is to extract the on-resistance, R_on, which is defined as the inverse output conductance at a V_DS of 0 V. For ohmic series resistances, the contribution of the extrinsic resistances to the total device resistance is higher for larger V_GS. As seen in the output characteristics of Figure 2.3, R_on varies as a function of V_GS but approaches, for large voltages, a saturated value corresponding to the total series resistance of the device.

2.2.6 Q

One popular performance metric, that takes both on- and off-performance into account, is the quality value [25],

$$Q \equiv \frac{g_\mathrm{m,max}}{SS_\mathrm{min}} = \left[\frac{\mathrm{mS/mm}}{\mathrm{mV/dec.}}\right] = \left[\frac{\mathrm{kS\,dec.}}{\mathrm{Vm}}\right]. \tag{2.5}$$

The metric is usually presented without a unit and it is understood that the units and normalisation used during its calculations is defined as in (2.5).

2.3 RF METRICS

A transistor is very much a non-linear component but can be linearised if the operation window is small enough. This means that a transistor biased at some fixed DC voltages with superposed time-varying signals of very small amplitudes, can be described by linear circuit elements, such as resistors, capacitors etc. One such simple model is depicted in Figure 2.4 [26–28].

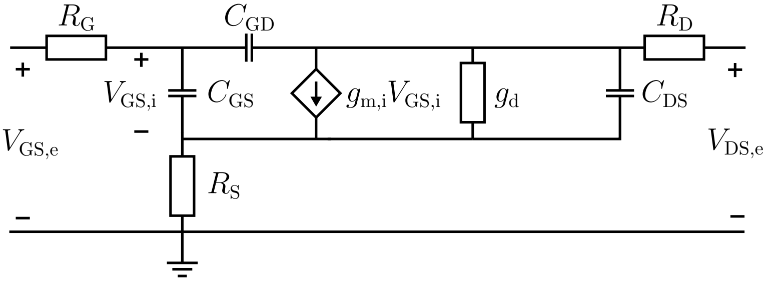


Figure 2.4: A small-signal model of a MOSFET built up by linear circuit elements. The device is illustrated as a 2-port with the input between gate and source (left), and output between drain and source (right). Due to series resistances, the extrinsic voltages ($V_{GS,e}$ and $V_{DS,e}$) are not identical to the intrinsic voltages ($V_{GS,i}$ and $V_{DS,i}$). More circuit elements can be incorporated for a more accurate description of the high-frequency performance.

At the core of the transistor is the voltage-controlled current source with a parallel series resistor, g_d. With transistors operating at high frequencies, capacitances start to affect the performance of the device. Dependent on the device architecture, these capacitances can sometimes be lumped together into three elements situated between the three electrodes: C_{GS}, C_{GD}, and C_{DS}. In series with the device, out towards the electrodes are the three series resistances (R_G, R_D, and R_S) situated, which together with the capacitances affect the internal voltage nodes and, in turn, the performance. The values for all these components vary with the chosen DC bias and some, like g_m, can potentially be frequency dependent.

For high-frequency MOSFET characterisation, mainly two metrics are important in terms of benchmarking: f_T and f_{max}. The first, f_T, is the transition frequency, which is defined as the frequency, at which the current gain reaches unity, i.e. 0 dB. It can be estimated using (2.6) or extracted from a measurement of the device scattering parameters (S-parameters) followed by calculation of the hybrid parameter h_{21}, i.e. the current gain, with an extraction illustrated in Figure 2.5. The current gain is observed to fall with a constant decay of 20 dB decade^{-1}, originating from the first order filtering of the RC-network.

$$\frac{1}{2\pi f_T} = \frac{C_{GS}+C_{GD}}{g_{m,i}} + \frac{(C_{GS}+C_{GD})(R_S+R_D)g_d}{g_{m,i}} + (R_S+R_D)C_{GD} \tag{2.6}$$

$$f_{max} = \frac{1}{2}\sqrt{\frac{f_T}{2\pi C_{GD}(R_S+R_G)+\frac{g_d(R_S+R_G)}{f_T}}} \tag{2.7}$$

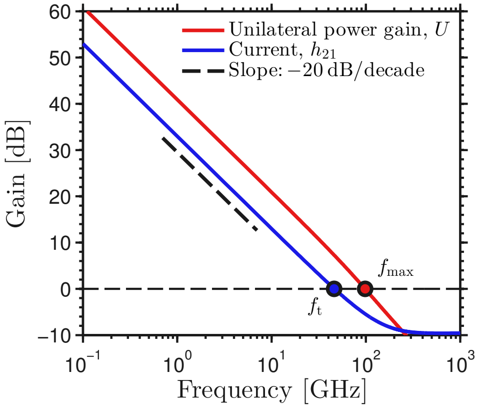


Figure 2.5: Current gain and unilateral power gain as a function of frequency, calculated using the small-signal MOSFET model shown in Figure 2.4, with the correspondingly extracted f_T and f_{max}.

The second important RF-metric is the maximum oscillation frequency, f_{max}. It is defined as the frequency at which the unilateral power gain, U, reaches 0 dB. The maximum oscillation frequency can roughly be calculated from f_T using (2.7). The unilateral power gain is defined as the power gain when any feedback path for the power is neglected. From measured S-parameters, transformed to Y-parameters, U can be calculated as

$$U = \frac{|Y_{21}-Y_{12}|^2}{4\left(\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12})\,\mathrm{Re}(Y_{21})\right)}, \tag{2.8}$$

with an example characteristic illustrated in Figure 2.5.

2.4 NORMALISATION

In benchmarking of transistors, the metrics such as $g_{\mathrm{m,max}}$ and I_{on}, are often normalised to the gate width. For a planar surface channel MOSFET architecture, the transistor performance and footprint area scales linearly with the width of the device. In this case, for a fixed gate length, this corresponds to a normalisation to the gate area. Often in industrial applications, it is the performance per unit area that matters, which means that vertical stacking of lateral transistors or vertically aligned nanowires have competitive advantages compared to other device architectures.

In multi-gate MOSFET architectures, the normalisation is performed in the same way, to the gate width. For nanowire MOSFETs, normalisation is performed with the circumference, and for tri-gate MOSFETs, using the sum of the three gates, as though they have surface channels. For these multi-gate devices, the gating from different sides extends through the semiconductor so that more of the current is transported deeper in the semiconductor. When comparing a tri-gate to a GAA device, the electrostatic control is improved in the GAA-case. This improvement is, however, less than the added gated width [12], resulting in an underestimated performance for GAA devices.

3

Vertical Nanowire MOSFET Fabrication

VERTICAL nanowires allow a possible development path for future ultra-scaled MOSFETs, promising a high scalability in terms of metal contacts and gate lengths. In this chapter, an overview of established techniques for the fabrication of vertical nanowire MOSFETs is given, followed by a brief description of the improvements established during the thesis work. In the main part of the chapter, the fabrication steps of a self-aligned gate-last process for vertical nanowires are presented.

3.1 NANOWIRE FABRICATION TECHNOLOGIES

Nanowires can be formed either using various epitaxial growth methods or etching processes. One popular way is to grow nanowires using metalorganic vapour phase epitaxy (MOVPE), exploiting the vapor-liquid-solid (VLS) growth mechanism. Using this method, metallic catalyst particles, usually gold (Au), are positioned on a semiconductor substrate, serving as a template with the same crystal direction as the one wanted for nanowire growth. Growth is initiated by the introduction of metal-organic precursor molecules at elevated temperatures. At some specific temperatures and pressures, the liquid catalyst particle absorbs more vapour-phase semiconductor material than what is possible in equilibrium, making the metal catalyst go into a supersaturated state. Due to this unstable state, precipitation of solid semiconductor material is started and a nanowire is grown from the semiconductor template [29].

Another way of growing nanowires is through selective area growth. Small openings are made in a dielectric mask down to the semiconductor substrate and, similarly as when using catalyst particles, precursor molecules are utilised at elevated temperatures with growth only taking place inside the openings [30,31]. An extension of the same approach is to grow the nanowires inside dielectric tubes [32].

Instead of growth, nanowires can also be formed by wet or dry etch procedures. One possible way is to start from a high-quality substrate, which could consist of various doping profiles and different semiconductors. An etch mask is deposited onto this substrate, defined using high-resolution lithography such as EBL. The etch mask is easiest created in a positive resist, such as hydrogen silsesquioxane (HSQ) [33, 34]. Finally, the substrate is etched using a highly anisotropic dry etch process, forming the nanowires underneath the etch mask [35].

All of these nanowire fabrication technologies are applicable to silicon (Si) substrates, which is required for low-cost device fabrication [36], but consideration has to be taken to the bottom contact to the nanowire devices. If III-V nanowires are used on Si, which also functions as a bottom contact, charge transport will occur over a potential barrier at the III-V/Si heterojunction [30, 31]. This appear as a highly non-linear resistance in series with the active device, limiting I_D and increasing g_d. A potential barrier can also arise from other substrates than Si, e.g. indium phosphide (InP). The heterojunction barrier can, however, be avoided altogether by fabricating a metal bottom contact to the nanowires [37] or by growing the nanowires on a planar buffer layer, on top of Si, of the same material as the nanowires [28].

The most studied materials for vertical nanowire MOSFETs are Si, InGaAs, and InAs. Si has the main advantage of being directly compatible with established fabrication technologies in large-scale nanoelectronics. InGaAs and InAs are of interest, together with many other III-V semiconductors, for their advantageous transport properties, thus allowing for faster and more energy efficient electronic circuits.

Fabrication of vertical MOSFET devices distinguishes itself from lateral device fabrication in that the device, in general, has to be built up from the bottom to the top. After establishing the bottom contact scheme, i.e. using a metal socket or contacting via the substrate, a spacer is formed using an organic (e.g. a baked photoresist), a dielectric (e.g. $\mathrm{SiO_2}$ [38]), an exposed HSQ [39] or a high-κ oxide film [34]. This spacer should be thin in order to minimise the access resistance, although thick enough to not limit the device high frequency operation by parasitic capacitances [23]. For devices optimised for DC performance, using a high-κ is an attractive choice as it requires no extra fabrication steps other than those already needed to deposit the gate stack. After high-κ deposition, a gate metal is formed and the gate length defined either using an etch mask [40] or by the deposition thickness [38]. Before the top contact is fabricated, a second spacer is needed that usually consist of an organic spin-on resist [31, 34, 38, 40] or electron-beam defined

HSQ [39].

In lateral fabrication, device dimensions, such as the gate length, contact regions etc., are defined through lithographic processes. In a vertical geometry, however, these geometries roughly translates to the thickness of the different layers constituting the device. The thickness precision of evaporation, sputtering, atomic layer deposition (ALD), and chemical vapour deposition (CVD) can be very good, but this does not necessarily translate to the thickness precision close to the nanowires. Dependent on the deposition method, nanowires can shadow their surroundings due to the high aspect ratio of the structure. Often material deposition on the nanowire sidewalls is unwanted and need to be removed, resulting in extra fabrication steps. As a general observation, vertical fabrication is more challenging than lateral because of less developed fabrication methods.

3.2 PROGRESSION OF THE VERTICAL NANOWIRE MOSFETS

At the start of the work leading up to this thesis, vertical InAs nanowire MOSFETs had already been fabricated with an RF-compatible layout [37, 38, 41, 42], with the cross-sectional device architecture illustrated in Figure 3.1a. This is compared to a newer version of the same MOSFET in Figure 3.1b. The overall structure of the two types is the same: one source contact in the bottom, a drain contact in the top, and the gate situated in the middle with spacer layers in-between.

The nanowire doping has been changed from a uniform doping all through the nanowire, to nanowires with an undoped bottom part and a highly doped top part. This change is important as it allows for better control of the channel potential while at the same time contributes to low resistance in the contact regions. III-V substrates, either semi-insulating InP or conducting InAs, where originally used. For the semi-insulated substrate, a metal bottom contact was used. A large drawback using III-V substrates is the heavy costs involved, especially if large wafer sizes are needed. To demonstrate industrial compatibility of the technology, Si was introduced as the substrate. Instead of growing the nanowires directly from Si and using a metal bottom contact, the growth of an InAs buffer layer followed by InAs nanowire growth on the buffer layer, was implemented. This approach also allows for the use of the InAs epitaxial layer as a bottom contact to the nanowires and as interconnects between devices, simplifying the fabrication process. More details about the InAs epitaxial layers is discussed in material characterisations part of the thesis in Chapter 6.

During this work, a higher precision has been developed in defining the different layers of the structure, which has made it possible to shortening the

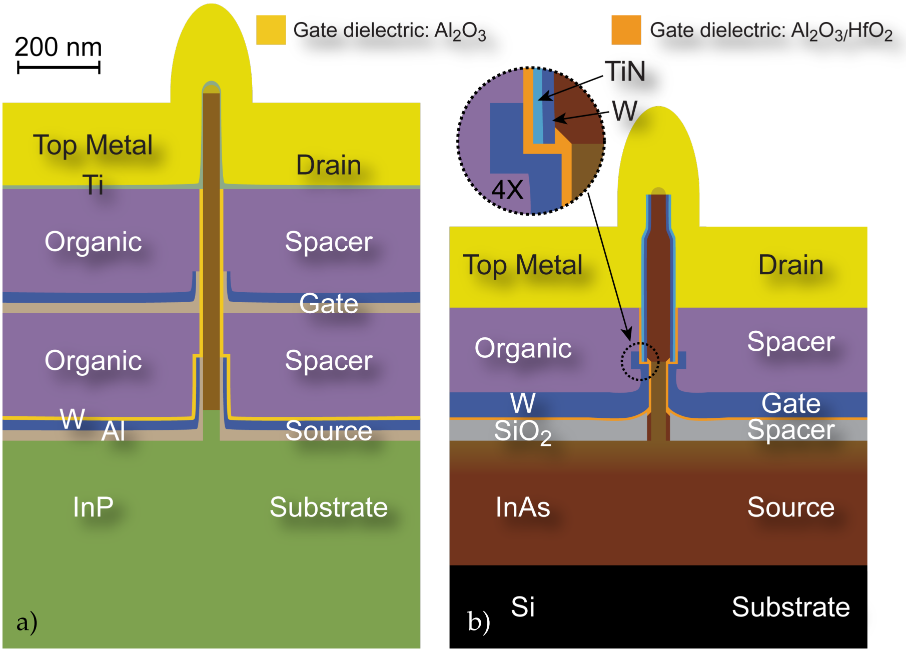

200 nm
Gate dielectric: Al_2O_3
Top Metal
Ti
Drain
Organic
Spacer
Gate
Organic
Spacer
W
Al
Source
InP
Substrate
a)
Gate dielectric: Al_2O_3/HfO_2
TiN
W
4X
Top Metal
Drain
Organic
Spacer
W
Gate
SiO_2
Spacer
InAs
Source
Si
Substrate
b)

Figure 3.1: Schematic cross-section of the vertical InAs nanowire MOSFETs, before a) and after b) the thesis work. The schematics are presented in the same scale for easy comparison.

nanowires, resulting in a more compact device. Comparing the two versions, it is obvious that the height at which the gate originally was situated, is now at the same height as the drain electrode for the newer design. In the old design, it was found that organic spacers can induce potential barriers in the ungated regions, due to charging, which makes them unsuitable as spacers. Over the course of the thesis, several dielectric materials have been investigated as suitable spacer materials, e.g. Si_3N_4 in Paper V, HSQ in Paper II, and SiO_2 in Paper I. The second spacer has been kept as an organic material in the new design due the ease of fabrication and that the effect of spacer charging is shielded by the top metal.

3.3 SELF-ALIGNED GATE-LAST FABRICATION PROCESS

One of the main innovations to the nanowire MOSFET structure during the thesis work is the development of a self-aligned gate-last process. The meaning of a "self-aligned" process is that the gate is positioned relative to the contact regions without the requirement of a high-precision alignment step.

By using a gate-last process, the contact regions are first formed, with the gate stack fabrication among the final steps in the process. The main benefit of such a process is the minimisation of access resistances to the active device as it allows for a gate overlapping the contact regions. The main fabrication steps are in this section explained in detail with the exact process parameters provided in Appendix A.

3.3.1 NANOWIRE DEFINITION AND GROWTH

Au discs are deposited on the InAs epitaxial layer either individually or in an array, using an electron-beam defined poly(methyl methacrylate) (PMMA)/Au lift-off process. Nanowires grown from these Au discs vary in length depending on the type of array they are positioned in. It is challenging to optimise growth for several types of nanowire arrays simultaneously and most focus have been put towards optimisation of nanowires placed in equilateral zigzag stripe arrays (also known as double-row arrays) with a spacing of 200 nm, as shown in Figure 3.2. Other array types have also been implemented, such as hexagonal arrays, where each nanowire is positioned in the centre of a hexagon of its closest neighbours.

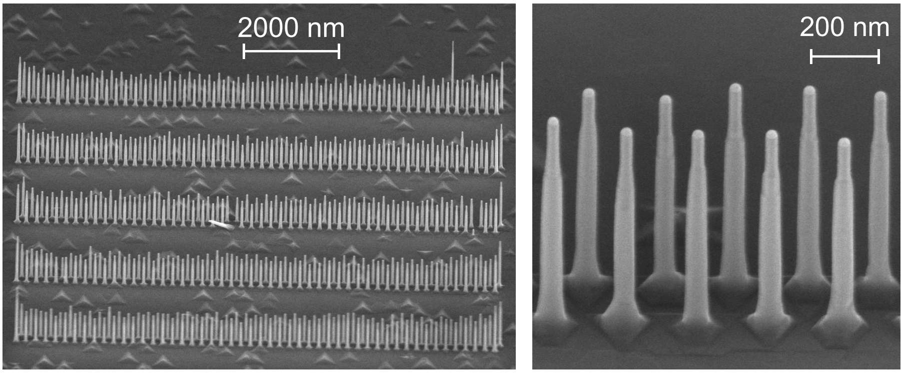


Figure 3.2: Nanowires positioned in equilateral zigzag stripe arrays with an inter-nanowire spacing of 200 nm.

InAs nanowires are grown using MOVPE with trimethylindium (TMIn) and arsine (AsH_3) as precursors at temperatures between 420 °C and 470 °C. Dopants can be applied during the growth by adjustment of the tetraethyltin (TESn) flow (n-type). In Paper V, uniformly doped nanowires along their length were used whereas in Paper I, a two-step growth was implemented. In the two-step growth, an undoped segment is first grown, followed by growth of a doped top part. This second step overgrows the undoped segment, creating a core-shell structure as seen in Figure 3.3a). The diameter of the inner undoped core is controlled by the Au disc size, which can range between 18 nm and 60 nm. The thickness of the doped shell is controlled by the growth time and the group V to group III molar ratio, with a thickness varied between 3 nm and 25 nm.

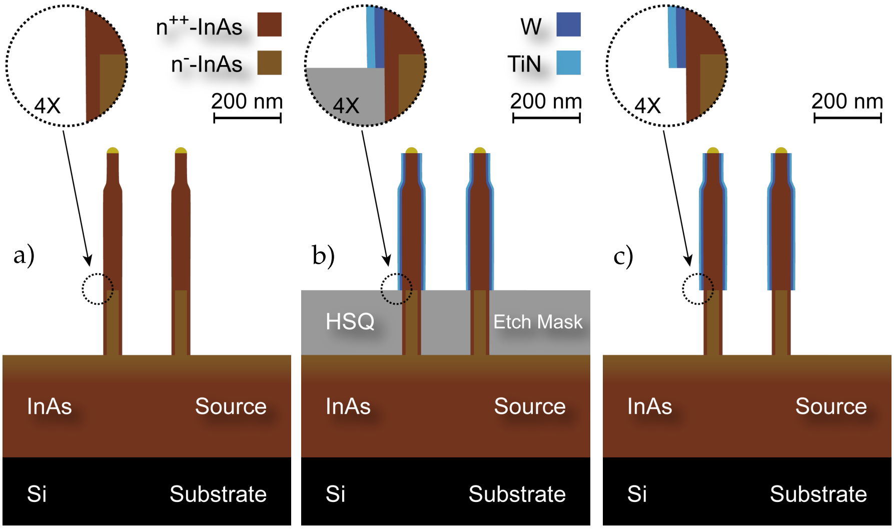


Figure 3.3: Schematic illustrations of the fabrication steps used in order to establish the top metal contact in the gate-last process: a) the nanowires after growth, b) after defining the top contact edge using anisotropic metal etching, and c) the fabricated top contact.

3.3.2 TOP METAL DEFINITION

In order to fabricate the top contact to the nanowires, an HSQ film is spun on followed by baking and electron beam exposure. The exposure dose determines the thickness of the HSQ after development and it is therefore possible to vary the eventual gate length of the MOSFETs. The top contact metal stack (W and TiN) is deposited by sputtering and ALD,respectively. This is followed by anisotropic inductively coupled plasma reactive-ion etching (ICP-RIE) to remove the planar layer and keep the metal on the nanowire sidewalls, as depicted in Figure 3.3b. After etching of the HSQ mask with HF, the top metal edge is defined as illustrated in Figure 3.3c and the scanning electron microscopy (SEM) image in Figure 3.4.

The reason for the TiN in the top metal stack is to serve as protection to the inner metal during the ICP-RIE in order to keep a uniform contact metal film. Instead of using a metal for this protection film, a dielectric could be

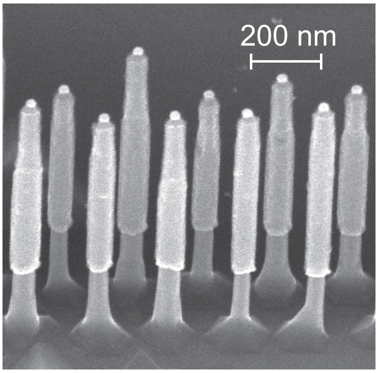


Figure 3.4: SEM image of a nanowire array with fabricated top contacts.

used as long as it is thick enough to ensure protection to the inner contact metal. Top metals consisting only of the inner contact metal, i.e. without the protection layer, has also been successfully implemented for nanowire arrays with spacings more than 300 nm. For closer nanowire spacing, significant shadowing occur during metal sputtering, resulting in thinner metal closer to the nanowire base, which is etched away during the ICP-RIE.

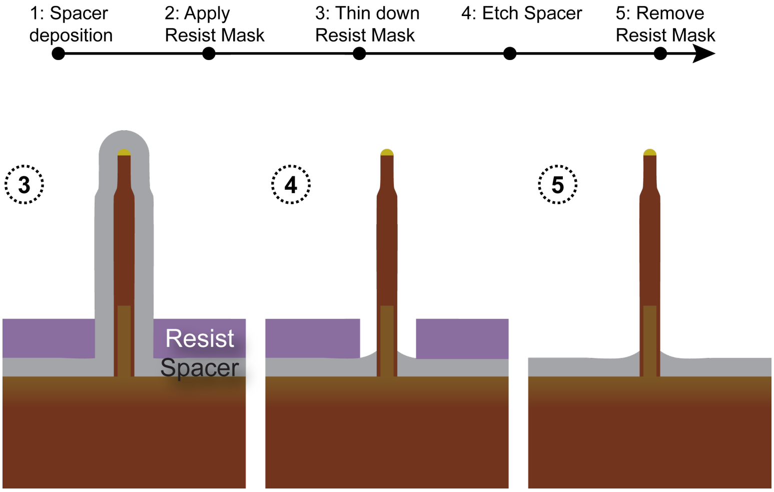

1: Spacer deposition
2: Apply Resist Mask
3: Thin down Resist Mask
4: Etch Spacer
5: Remove Resist Mask
3
4
5
Resist
Spacer

Figure 3.5: Schematic illustrations of the fabrication steps for the bottom spacer.

3.3.3 BOTTOM SPACER

A bottom spacer, separating the gate and the bottom contact is fabricated. Firstly, the spacer material (e.g. SiO_2 or Si_3N_4) is deposited, either by CVD, evaporation or ALD. The choice of method determines the amount of material deposited on the nanowire sidewalls relative to that deposited on the planar surface. If a large ratio exists between the vertical and lateral thicknesses, isotropic etching could be performed to remove all the material on the sidewalls, thinning down the planar layer to desired thickness. This method has, however, proven difficult to control as material deposited on the sidewalls have a different quality and etch rate than material deposited on a planar surface. A more controllable approach is illustrated in Figure 3.5

Here, a resist is spun on, baked, and thinned down to a desired thickness of about 200 nm using reactive-ion etching (RIE) in O_2-plasma. The spacer material is selectively etched, either using an isotropic dry etch or wet etch, to remove all material on the nanowire sidewalls. Etching occurs also underneath the resist edge and the etch time is therefore precisely controlled to acquire the wanted spacer thickness close to the nanowires. The area protected by the resist is not etched and the spacer is finalised by removing the resist mask.

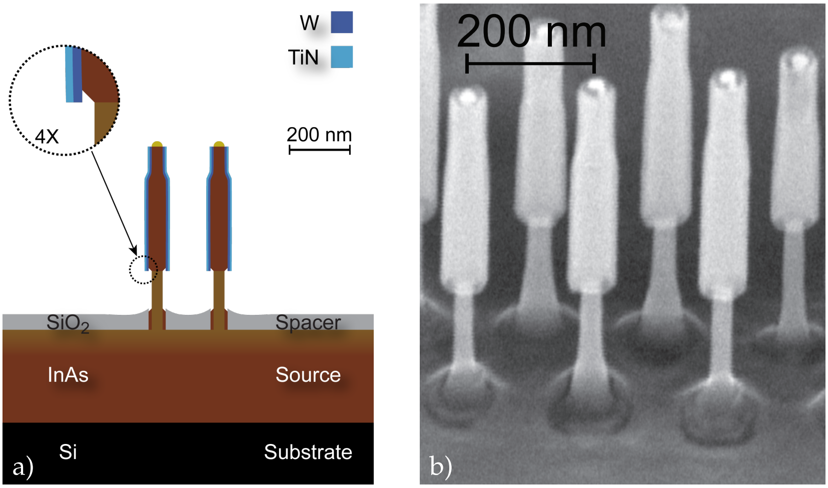


Figure 3.6: a) Schematic illustration of the fabrication after the digital etch step and b) the corresponding SEM image.

3.3.4 CHANNEL CONTROL

With the bottom spacer in place and the top metal previously fabricated, the effective gate length is already defined. In this stage, the channel thickness can be selectivity thinned down to allow for better electrostatic control with the bottom spacer and the top metal serving as etch masks. The thinning is performed by repeated surface oxidation and etching of the oxide (digital etching), with the result shown in the schematic and SEM image of Figure 3.6a and b), respectively. Observe that the doped shell is etched only at the channel region, keeping the doped shell and the thicker dimensions at the top and bottom, enabling low access resistance.

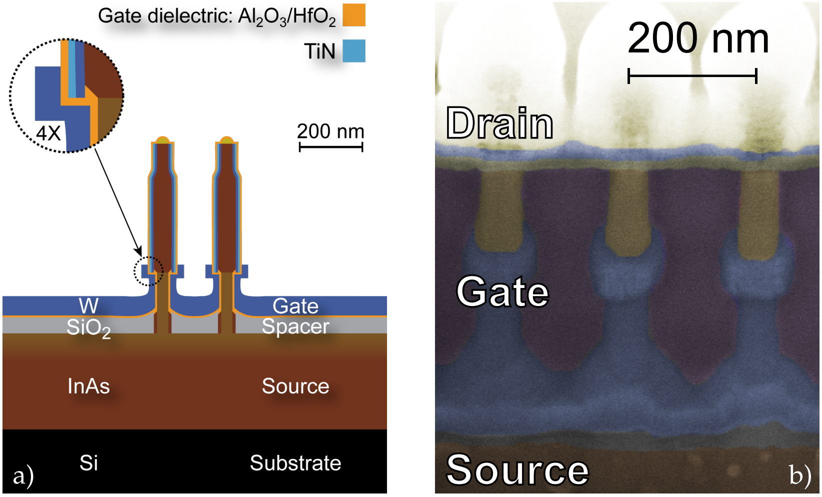


Figure 3.7: a) Schematic illustration of the fabrication after the gate formation and b) a SEM cross-section of a finished device.

3.3.5 GATE ELECTRODE AND DRAIN CONTACT

Immediately after thinning of the channel region, a high-κ is deposited by ALD. A gate metal (W) is sputtered and a similar process used to define the bottom spacer (Figure 3.5) is also applied for the gate metal definition, with the only difference being that a metal is etched instead of a dielectric. An overlapping gate can be formed to the top contact with the bottom of the gate metal almost being edge-to-edge with the highly doped shell, as seen in Figure 3.7a. Using this fabrication method, the length of the access regions are limited to the etching underneath the masks during channel thinning. For device isolation, the planar layer of the gate metal is etched out to form rectangular pads. The second spacer is defined using a spin-on resist followed by thinning using O_2-plasma etching. Via holes down to the different layers are opened up followed by deposition of a top metal stack, with the top layer being Au for ease of probing. This top metal is finally patterned and etched to form pads and interconnects. A SEM cross-sectional image of a fully fabricated device can be seen in Figure 3.7b.

3.4 LAYOUT

In all patterning steps used in the fabrication, except in the Au seed particle definition, ultraviolet (UV)-photolithography is used. Device isolation and interconnects are fabricated by resist patterning and etching of the different conductive layers, forming individual transistors, resistors or circuits. The RF-compatible layout uses a 50 Ω coplanar waveguide design in order to match to high-frequency measurement equipment and therefore avoid reflections of power waves. To achieve a 50 Ω waveguide, the width of the centre, s, conductor is sized relative to its gap to the ground plane, w, with the ratio $s/w = 1.5$, for a thick insulating Si substrate. The layout of a transistor utilising this design rule can be seen in Figure 3.8.

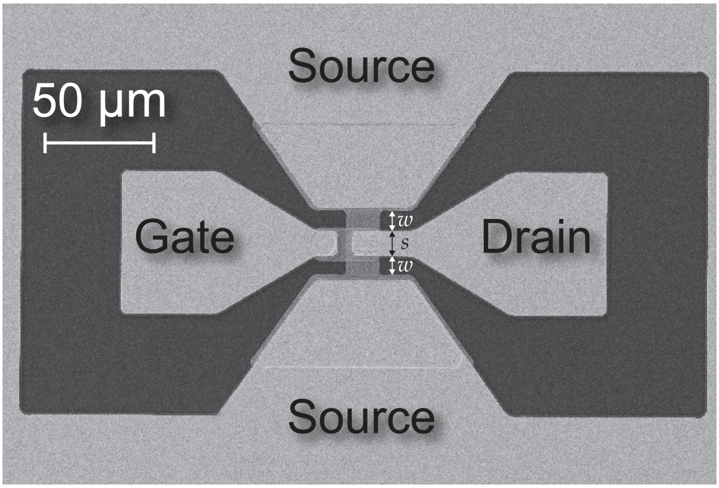


Figure 3.8: SEM top view images of a fabricated transistor. The layout utilizes a co-planar waveguide design for 50 Ω matching in a common-source configuration.

4

MOSFET Characterisation

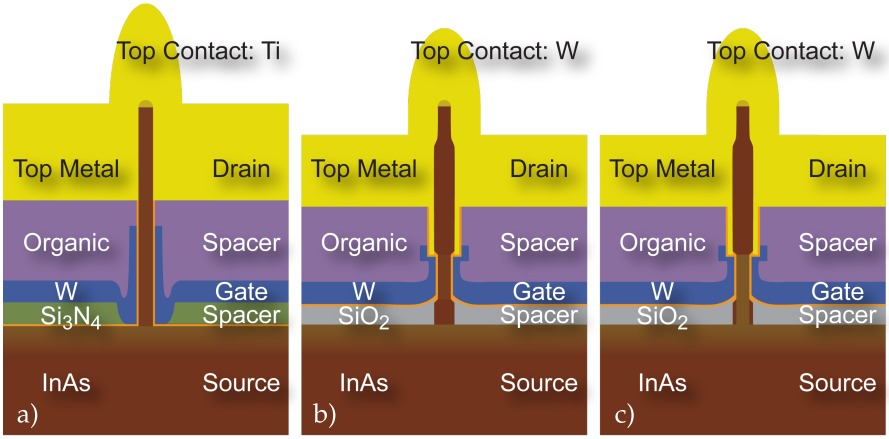
In order to establish the performance of the fabricated vertical InAs nanowire MOSFETs, they are characterised both at DC and RF. In this chapter, key performance metrics are evaluated and analysed for increased understanding of the transistor structure, thus allowing for continuous improvements. The device performance is also benchmarked to study how the transistor operation compares to competing technologies and research groups around the world.

4.1 DECOUPLING THE TRANSCONDUCTANCE AND SUB-THRESHOLD SWING

In transistor technologies, in which the doping control is limited, a trade-off is often observed between on- and off-performance. By studying literature, this is exemplified by a correlation between transconductance (g_{m}) and the sub-threshold swing (SS) [34]. This supposed trade-off can be understood in terms of access resistances to the intrinsic device. For undoped nanowires biased above the threshold voltage, V_{T}, these series resistances can be very large compared to the gated channel segment. A voltage drop occurring over the ungated segments limits the effective voltage drop over the channel, which leads to lower drain currents, I_{D}, and g_{m}. The effect of the series resistances are not as severe in the off-state ($V_{\mathrm{GS}} < V_{\mathrm{T}}$), as the effective resistance in the gated channel is high, leading to potentially good off-characteristics. For uniformly doped nanowires, however, things get somewhat reversed. With doping, the resistances of the ungated segments are much smaller, allowing for potentially higher current levels and transconductances. The electrostatic control decreases since the voltage drop occurs mainly over the oxide when there is considerable charge in the channel. For doped semiconductors the semiconductor capacitance increases due to the thinner depletion region [5]. This loss of control over the channel potential is most clearly observed as an increased SS.

One solution to this trade-off between on- and off-performance is the introduction of varying doping levels along the nanowires, with high doping in all access regions and lowly or undoped channel region. For nanowires grown using the VLS approach, abrupt doping profiles are challenging to achieve as dopant atoms are dissolved in the catalytic particle and give rise to memory effects. Abrupt junctions using this method is yet to be realised. An other method is to etch out nanowires from planarly grown substrates [33,34]. This method requires, however, very anisotropic etch properties and may impair on the device performance due to etch damaged surfaces.

Our approach to form a low-doped channel with high-doped access regions was presented in the device fabrication chapter (Chapter 3), as the self-aligned gate-last method.


Top Contact: Ti
Top Metal
Drain
Organic
Spacer
W
Gate
Si_3N_4
Spacer
InAs
Source
a)
Top Contact: W
Top Metal
Drain
Organic
Spacer
W
Gate
SiO_2
Spacer
InAs
Source
b)
Top Contact: W
Top Metal
Drain
Organic
Spacer
W
Gate
SiO_2
Spacer
InAs
Source
c)

Standard: All Doped nanowires

Gate-Last: Doped bottom part

Gate-Last: Un-doped bottom part

Figure 4.1: Three transistor configurations used in order to illustrate the effect of channel doping in vertical nanowire MOSFETs. In a) uniformly doped nanowires from Paper III are used. In the other two, the gate-last fabrication method is implemented for a doped bottom part b), and an undoped bottom part c). Other minor differences exists between the structure, e.g. spacer material and the choice of top metal.

4.2 COMPARISON OF THREE DEVICE ARCHITECTURES

In this section, the DC performance for three different types of vertical nanowire MOSFETs are compared. The difference between the three are illustrated in the schematic cross-sectional images shown in Figure 4.1.

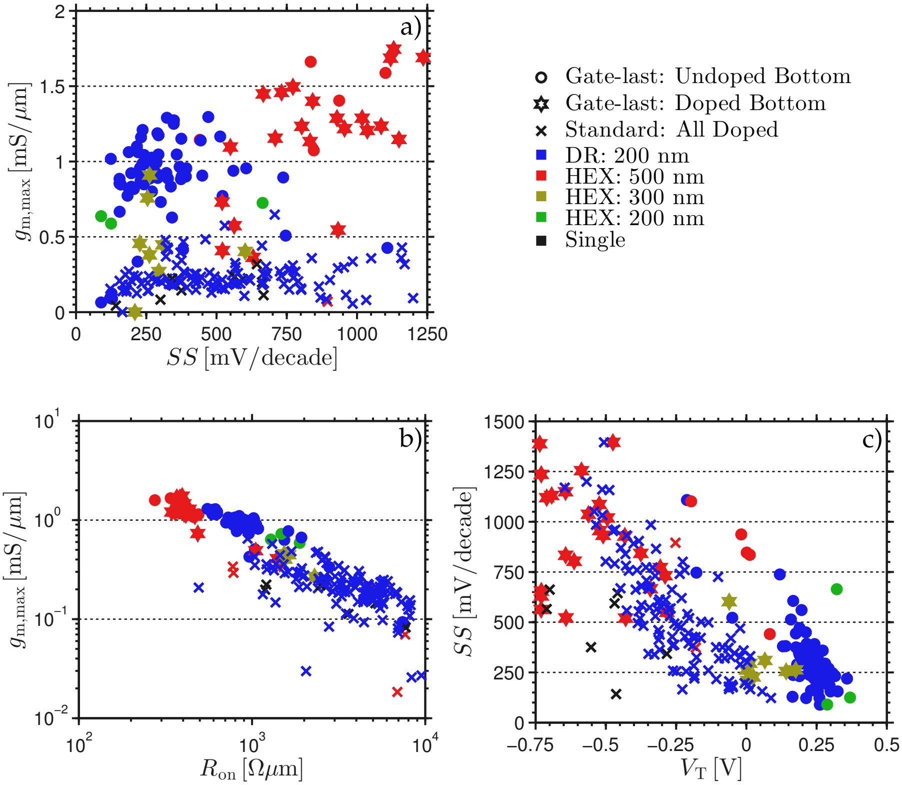


Figure 4.2: Scatter plots of the DC performance for three types of nanowires, symbolised by different markers. These three types of nanowires are positioned in various types of arrays, either in double-row arrays (DR) or in hexagonal arrays (HEX), of different distances to their closest neighbour. The different type of arrays are indicated by the marker colour. a) $g_{\mathrm{m,max}}$ as a function of SS_{min}. b) $g_{\mathrm{m,max}}$ as a function of R_{on}. c) The extracted V_{T} compared to the corresponding SS.

The main variation between them are the doping scheme used, where one is uniformly low doped (a), one utilises the novel gate-last fabrication method with a doped bottom part (b), and one is also using the same gate-last approach, but instead with an undoped bottom part (c). Note that in

Figure 4.1b, dopants may also incorporate in the channel region, whereas in (c) a more intrinsic semiconductor is maintained in the gated segment.

Figure 4.2a illustrates the DC performance difference between the structures in terms of g_m and SS. Uniformly doped nanowires with the standard fabrication process show relatively low transconductance values with a large variation in SS, which is attributed the use of varying diameters across the sample. Worse electrostatic control of the channel is obtained for thicker nanowires. In addition, threshold voltage variations indicate that thicker nanowires have a higher degree of dopant incorporation during growth, leading to even worse control by the gate.

Both types of MOSFETs fabricated using the gate-last method demonstrate high transconductance and low SS_min for arrays with inter-nanowire spacing below 300 nm. The best combination of on- and off-performance is achieved using an intrinsic bottom part. For wider spaced arrays, the doped shell is somewhat thicker and possibly more highly doped. Furthermore, spin-on resists during the device fabrication are thinner for the wider spaced arrays, resulting in a gated region closer to the nanowire foot. This foot has a considerably thicker shell than the rest of the nanowire. During the removal of this doped material, to reach the more lowly doped core, a thin shell might still exist on several nanowires, resulting in a parallel lowly-resistive conduction path. This conclusion is further observed in Figure 4.2b. Nanowire arrays with wider spacing exhibit low R_on, indicating a thicker and more highly-doped shell than tighter spaced nanowire arrays. A clear trend between R_on and $g_\mathrm{m,max}$ is observed, highlighting the importance of continuous reduction of series resistances during device optimisation. A dependency between the off-performance and V_T is observable in Figure 4.2c), which at least partly can be attributed to the doping underneath the gate. Enhancement-mode operation ($V_\mathrm{T} > 0\,\mathrm{V}$) is observed for closely packed arrays with the most positive threshold voltages obtained for undoped bottom parts. While utilising a doped bottom part, the threshold voltage is lower as the Fermi level is positioned higher in energy, resulting in a lower potential barrier. Much lower threshold voltages are observed for wider spaced arrays, which originates from the extraction method. These transistors never enters a proper sub-threshold region as is shown in the transfer characteristics of Figure 4.3a together with its corresponding output characteristics in (b).

In contrast, the much improved sub-threshold behaviour for MOSFETs with a closer inter-nanowire spacing, is observed in the DC characteristics of Figure 4.4. The two transistors of Figure 4.3 and Figure 4.4 are fabricated in parallel, demonstrating the challenge in fabrication of different array spacings.

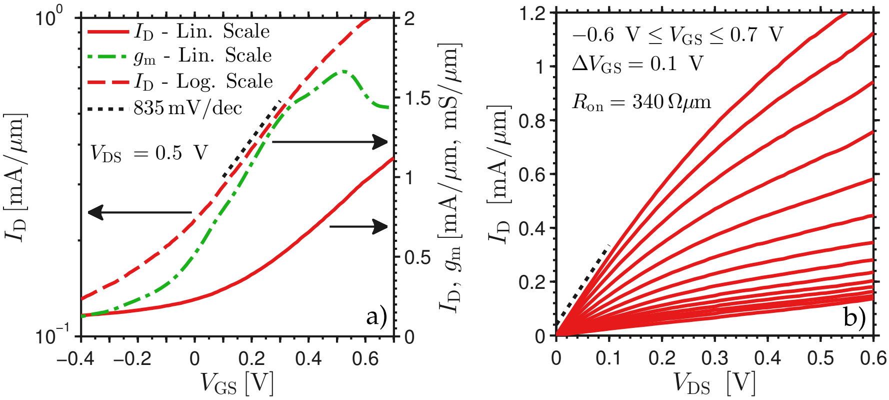


Figure 4.3: DC-characteristics of a MOSFET fabricated using the gate-last method on nanowires positioned in a hexagonal array with a spacing of 500 nm.

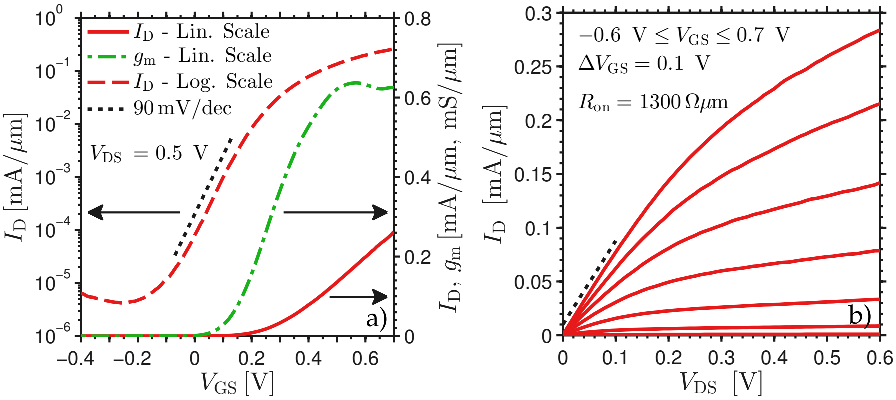


Figure 4.4: Transfer and output characteristics of a nanowire transistor fabricated using the gate-last method on nanowires positioned in a hexagonal array with a spacing of 200 nm.

4.3 BENCHMARKING

The performance of the vertical InAs nanowire MOSFETs, developed during the work leading up to this thesis, are benchmarked against some of the best competing vertical nanowire MOSFETs, in Table 4.1. The transistors fabricated using the gate-last process show favourable performance compared to the competition in terms of both on-state and off-state operation, exemplified by g_m and SS. The quality factor, Q, for some of these transistors are to the authors best knowledge the highest reported for any vertical nanowire MOSFET.

Table 4.1: Benchmarking vertical nanowire MOSFETs. The parameters $g_\mathrm{m,max}$ and SS_min are extracted at $V_\mathrm{DS} = 0.5\,\mathrm{V}$.

Channel	$g_\mathrm{m,max}$ mS/µm	SS_min mV/decade	Q kS/(Vm)	L_G nm	EOT nm	Reference
InAs	1.02	124	8.2	130	1.5	Paper I
InAs	1.09	420	2.6	200	1.7	Paper V
InAs	0.26	390	0.67	200	1.5	Paper III
InAs	0.52	88	5.9	50	2.3	[38]
InAs	0.26	119	2.2	35	1.6	[41]
$In_{0.7}Ga_{0.3}As$	0.11	85	1.3	200	2.8	[31]
$In_{0.53}Ga_{0.47}As$	0.73	305	2.4	80	2.2	[34]

The oxide capacitance, C_ox, has historically been importantsince it isone of the main parameters determining the current through the transistor, with larger values per unit area giving rise to higher current levels. When comparing modern MOSFETs a great variety is observed in the material choice for the gate dielectric between channel and gate. A parameter, the EOT, representing the thickness of the gate dielectric where the permittivity is translated to the corresponding thickness if SiO_2 instead was implemented, is often used to characterise the oxide capacitance. For a cylindrical geometry, C_ox can be expressed as:

$$C_\mathrm{ox} = \frac{2\pi\epsilon_0\epsilon_\mathrm{r}L_\mathrm{G}}{\ln((t_\mathrm{ox}+r_\mathrm{NW})\,/r_\mathrm{NW})}, \tag{4.1}$$

where ϵ_0 is the vacuum permittivity, t_ox is the oxide thickness, L_G is the gate length, and r_NW is the nanowire radius. If the thickness and relative permittivity of the used high-κ dielectric is known, effective oxide thickness (EOT) can be calculated assuming a $\epsilon_{\mathrm{r,SiO_2}} = 3.9$.

Concerning RF-performance, the full potential of using InAs nanowires transistors is yet to be realised. Record performance for these type of transistors was achieved in [24] with both f_T and f_max reaching above 100 GHz. The performance is however to a large extent limited by parasitic capacitances originating from the challenge of vertical fabrication. The nanowire performance is benchmarked against other transistors, in Table 4.2. Operation with gain over several hundred GHz have been accomplished for a multitude of technologies including both standard devices such as the Si-based MOSFETs, but also more exotic devices such as graphene-based MOSFETs. The fastest transistors are HEMTs using InGaAs as channel but similar performance can also be found in HBTs [43]. III-V trigate MOSFETs are also starting to show very impressive DC and RF-performance, utilizing their multi-gate architecture [44].

Table 4.2: Benchmarking DC and RF performance metrics for various transistor technologies. The parameters $g_{\mathrm{m,max}}$ and SS_{min} are extracted at $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$. If not stated otherwise, the devices are laterally oriented. In the table, V is short for vertical.

Technology	Channel	f_{T} GHz	f_{max} GHz	$g_{\mathrm{m,max}}$ mS/µm	SS_{min} mV/decade	L_{G} nm	Reference
V-NW MOSFET	InAs	31	50	1.02	124	130	Paper I
V-NW MOSFET	InAs	13	62	0.26	390	200	Paper III
V-NW MOSFET	InAs	103	155	0.73	420	150	[24]
Tri-gate MOSFET	InGaAs	281	365	2.85		32	[45]
MOSFET	InGaAs	370	280	2	110	60	[46]
MOSFET	Si	485		1.8		29	[47]
MOSFET	Graphene	427	10			67	[48]
HEMT	InGaAs	688	800	2.5	115	40	[49]

4.4 POSSIBLE IMPROVEMENTS

In order to improve the high-frequency performance of the vertical nanowire MOSFETs and be able to compete with lateral devices, several improvements need to be implemented. Considering the gate stack, more studies on the high-κ/InAs interface and the overall dielectric quality need to be improved. A method for investigating the border traps and interface traps of the these vertical nanowire structures was invented in Paper VII. More extensive studies are needed to fully investigate the optimal material and deposition conditions of these gate oxides. An improved gate stack will allow for better SS and g_{m}.

With the invention of the gate-last fabrication method, a framework is established for minimising access resistances, through the use of an overlapping gate. For devices with good combined on- and off-performance, discussed above, R_{on} is still too high in order to approach intrinsic performance [50]. Higher doping in the access regions and improved metal contacts are required. This will ensure higher current levels, higher g_{m}, and in turn higher

f_T and f_{max}.

It has previously been shown that the extrinsic capacitances can be reduced by high-resolution patterning of the metal electrodes [24]. Similar patterning can easily be implemented for the self-aligned gate-last transistors. To reach operation at frequencies of several hundred GHz, however, the existing technology will probably not be sufficient. Tighter nanowire spacings, smaller overlapping areas, and possibly patterning of the bottom electrode is needed to minimise the capacitances. To allow for easier patterning and etching of the bottom electrode in the established transistor architecture, the InAs epitaxial layer probably need to be made thinner. Another possibility is to grow the nanowires directly on the Si surface, skipping the InAs buffer layer, and instead create a bottom metal contact to the nanowires. This metal contact complicates the device fabrication but allows for easier etching of the bottom contact.

5

Mixer Circuit

DURING this thesis work, the vertical InAs nanowires were implemented in mixer circuits, both as MOSFETs and as resistors. The mixer is a widely used RF-circuit where both the transistor on- and off-performance is of interest. Prior to this work, very few circuit implementations of III-V nanowires had been reported [51–54], with the highest reported, to the authors knowledge, operating frequency of 108 MHz. In this chapter, some background and motivation to the nanowire-based mixer work from Paper III, is presented. Also, the main performance metrics are introduced to serve as introduction to the work.

5.1 RF FRONT END

Mixers are an integral part of the RF front end, depicted in Figure 5.1, which is the main part of a receiver circuit.

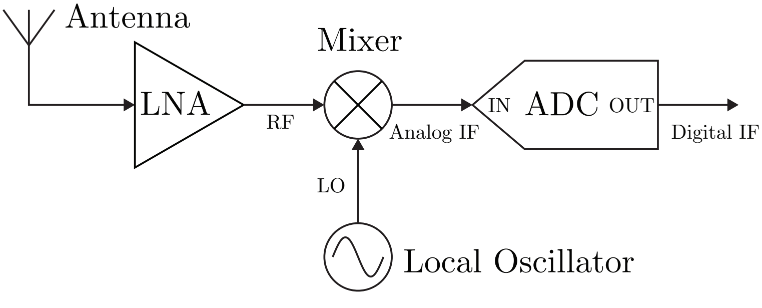


Figure 5.1: The RF front end omitting filtering in the signal pathway.

Here, an antenna serves as a signal source followed by amplification of the picked up signal. In the simplest case, the input signal has a single frequency, but more common is that it constitutes a band of frequencies, defined by filters in the signal path. For the amplification, a low-noise amplifier (LNA), optimised to add as little noise as possible to the amplified signal, is used. This is important as any noise added in the beginning of the signal path could affect signal processing in the later stages. The amplified signal serves as the input, denoted as RF in the figure, to the mixer, which uses a local oscillator (LO)-signal to create new frequencies. These new frequencies could be higher or lower than the RF input signal, referred to up-conversion or down-conversion, respectively. Down-conversion is a powerful tool as it allows for signal processing to be performed at much lower frequencies than the original signal, allowing for higher performance and potentially easier circuit implementations. Commonly, the signal processing is performed in the digital domain, resulting in the need for analogue-to-digital conversion (ADC) of the analogue mixer output intermediate frequency (IF)-signal.

5.2 SINGLE BALANCED DOWN-CONVERSION MIXERS

When studying the physics or performance of individual transistors, the yield can be of low importance. However, with the implementation of these devices in circuits, larger requirements are put on the device functionality. Not only is it necessary that the yield is high, but the device-to-device variation need to be small. With vertical fabrication methodologies of MOSFETs still being relatively unrefined, the device yield is low compared to more established lateral processes. For this reason, a simple mixer circuit containing only three transistors and two resistors is studied with the circuit diagram shown in Figure 5.2.

Transistor M_1 serves as the input common-source stage, with a resistive load (R_L). The two LO-transistors, M_2 and M_3, functions as switches with an high-amplitude input signal at a frequency not equal to the input frequency. The difference between the two signal pathways, through M_2 and M_3, respectively is a 180° phase shift, resulting in a differential output defined as $V_\mathrm{out} = V_\mathrm{IF+} - V_\mathrm{IF-}$. A capacitor, C, is placed between the outputs to serve as a high-pass filter. Compared to a single ended mixer, the use of a differential output allows for the doubling of the output signal amplitude, in addition to the suppression of externally originated noise and input signal leaking through transistors M_2 and M_3 (RF-leakage).

The mixing occurs during the switching of the LO devices, which mathematically can be viewed as multiplication of 1, if the LO-transistor is on, or 0, if the transistor is in its off-state. A multiplication of two sinusoidal signals

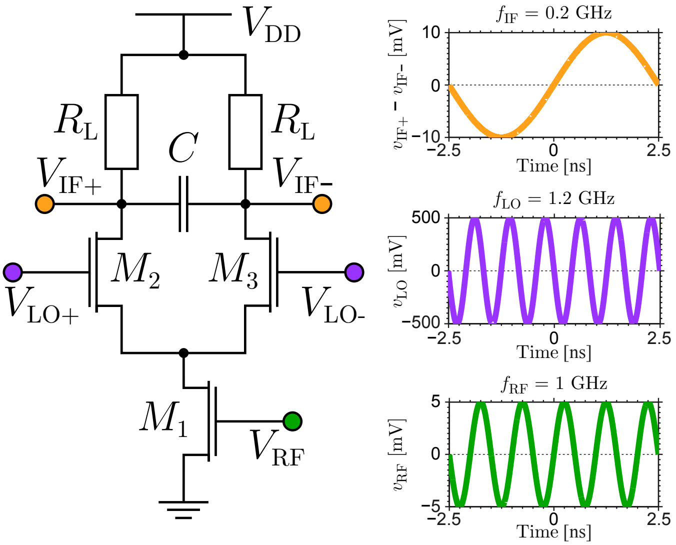

V_{DD}
R_{L}
R_{L}
C
$V_{\mathrm{IF+}}$
$V_{\mathrm{IF-}}$
M_2
M_3
$V_{\mathrm{LO+}}$
$V_{\mathrm{LO-}}$
M_1
V_{RF}
$f_{\mathrm{IF}} = 0.2$ GHz
$v_{\mathrm{IF+}} - v_{\mathrm{IF-}}$ [mV]
10
0
−10
−2.5
0
2.5
Time [ns]
$f_{\mathrm{LO}} = 1.2$ GHz
v_{LO} [mV]
500
0
−500
−2.5
0
2.5
Time [ns]
$f_{\mathrm{RF}} = 1$ GHz
v_{RF} [mV]
5
0
−5
−2.5
0
2.5
Time [ns]

Figure 5.2: The circuit diagram of a single balanced down-conversion mixer with its corresponding signals in the time domain, illustrating the mixing functionality. An RF-signal of 1 GHz is down-converted in frequency with an LO-signal of 1.2 GHz, creating a mixing product corresponding to the difference of the two frequencies, 0.2 GHz. Note that a large amplitude is used for the LO-signals to ensure proper switching of transistors M_2 and M_3.

results in new frequencies with the sum and difference of the two frequencies, such that $f_{\mathrm{IF}} = |f_{\mathrm{RF}} \pm f_{\mathrm{LO}}|$. An example of the three signals, represented in the time domain, can be seen in Figure 5.2.

One of the main performance metrics for this type of mixer is the voltage conversion gain, G_{VC}. It is defined as the ratio between V_{out} and the input voltage of the RF-transistor, V_{RF}. Note that these voltages are defined at different frequencies, f_{IF} and f_{RF}, respectively. The maximum low-frequency voltage conversion gain for this type of mixer can be derived as

$$G_{\mathrm{VC}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{RF}}} = \frac{2 g_{\mathrm{m,RF}} R_{\mathrm{L}}}{\pi}, \tag{5.1}$$

obtained using transistors with excellent saturation and sub-threshold characteristics [55].

In reality, however, the output conductance of the devices, the effective resistance of the LO-transistors and other leakage paths affect the low-frequency G_{VC}.

5.3 NON-LINEARITY

Apart from the fundamental frequency, $|f_{\text{RF}} \pm f_{\text{LO}}|$, other higher-order frequencies can be created. With switching occurring for large voltage swings, the transistor is going in and out of the highly non-linear sub-threshold region. This non-linearity give rise to integer harmonic frequencies of f_{LO}, which in return also can mix with the input signal. In addition, the RF-transistor and the load can behave non-linearly, which can give rise to even more complicated frequency response such that $f_{\text{IF}} = |mf_{\text{RF}} \pm nf_{\text{LO}}|$, where m and n are integer numbers. A measured output spectrum for one of the fabricated mixers is presented in Figure 5.3a.

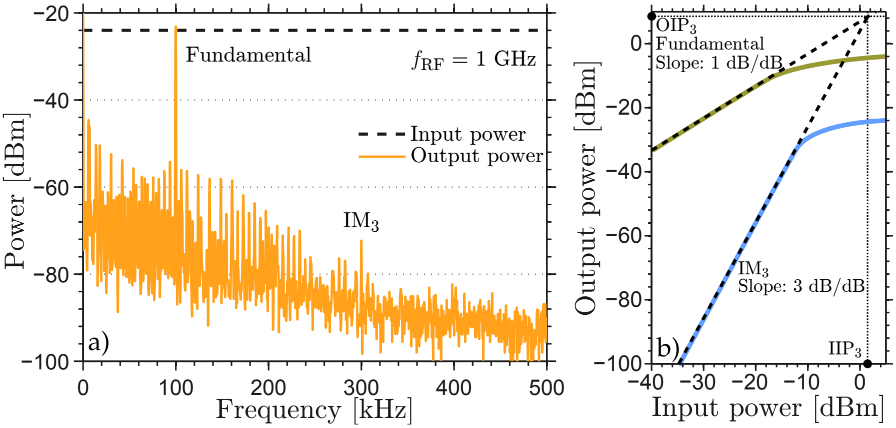


Figure 5.3: a) Measured output spectrum of a fabricated mixer circuit. The input frequency is set to 1 GHz and $f_{\text{LO}} = 1.0001$ GHz, resulting in a fundamental frequency of 100 kHz and IM$_3$ of 300 kHz. The extra frequency peaks located in the range of 0 - 250 kHz are attributed to the measurement setup. b) Illustration of the output power as a function of input power for the fundamental and IM$_3$. Compression can observed for both frequencies with extrapolations showing the extraction of IIP$_3$ and OIP$_3$. The input and output powers are corresponding to their respective voltages over a 50 Ω load.

The fundamental peak, corresponding to $m = 1$ and $n = 1$, is clearly observed at 100 kHz. Many smaller peaks can be discerned in the spectra, where especially the peak at 300 kHz ($m = 3$, $n = 3$) are of interest. This frequency is commonly called a third-order intermodulation product, IM$_3$, which are important as this type of frequencies often fall close the fundamental peak, and therefore are difficult to filter out. In addition, it can be shown that the magnitude of IM$_3$ grows as the cube of the input power, compared to the fundamental, which grows linearly. This is exemplified in Figure 5.3b. In logarithmic scale, the third-order intermodulation product grows three times faster than the signal compared to the fundamental frequency. A way to characterise the contribution of the third-order is to extrapolate the powers of the fundamental and IM_3 in their low-power regions to an intersect point. The input or output power of this intercept point are denoted as the IIP_3 and OIP_3, respectively. At sufficiently high input power, the circuit goes into compression, i.e. the gain is no longer linear with the input power. One popular metric to characterise the compression is the 1 dB-input referred compression point ($P_{\mathrm{in},-1\mathrm{dB}}$), referring to the input power when the measured output power deviates 1 dB from its ideal value.

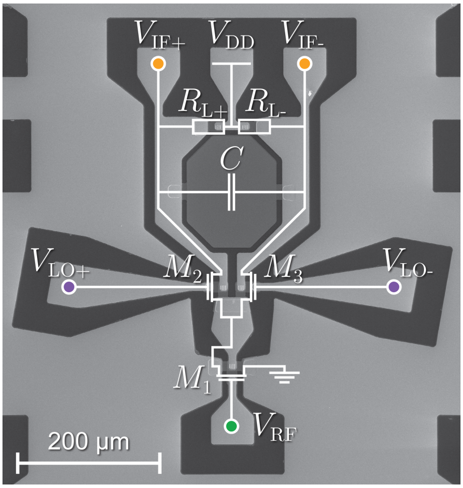


Figure 5.4: Fabricated mixer circuit using a 50 Ω co-planar waveguide design together with an overlay of the circuit diagram.

5.4 DESIGN

The MOSFETs and resistors in the circuit are all implemented using vertical InAs nanowires. The resistors are fabricated in the same way as the transistors with the main exception being that the gate metal is etched away. The capacitor is fabricated using the InAs epitaxial buffer layer as a bottom electrode and the gate layer as the top electrode with the bottom MOSFET spacer serving as dielectric. The layout follow the same design philosophy as the stand-alone transistors, shown in the MOSFET fabrication chapter, Chapter 3, using co-planar waveguide leads with a characteristic impedance of 50 Ω. A fabricated circuit is displayed in Figure 5.4 together with an overlay of the circuit diagram.

5.5 PASSIVE COMPONENTS

The passive components of the fabricated mixer circuits, i.e. the nanowire resistors and the parallel plate capacitor are characterised individually in order to ensure proper circuit operation and allowing optimisation on the device level. The two load resistors are characterised at DC as shown in Figure 5.5a, with the bottom of the nanowires grounded. The non-linear *I*-*V* characteristics observed indicate a potential barrier close to the top of the nanowires. This barrier can be attributed to either the top metal or, probably more plausible, charging effect in the organic top spacer in these devices. The two resistors depicted are from the same mixer, indicating small device variations.

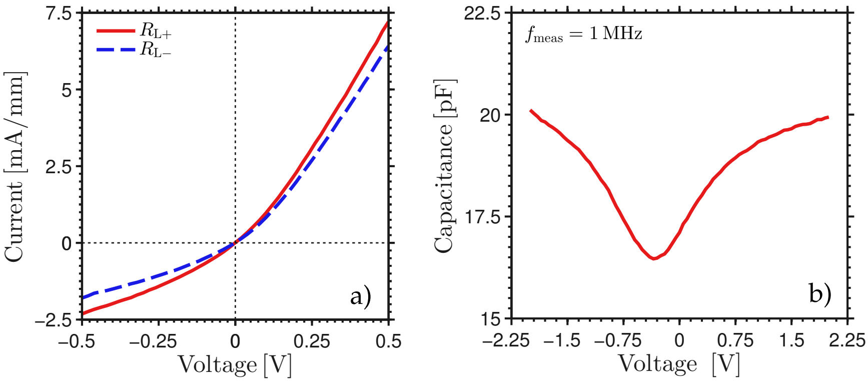


Figure 5.5: a) *I*-*V* characteristics of two load resistors in the same mixer circuit measured with the bottom grounded. The asymmetry of the characteristics indicate a potential barrier for electrons close to the nanowire top. b) *C*-*V* characteristics of the capacitor used for high-pass filtering in the mixers.

The capacitors are characterised using an impedance analyser for varying voltage at a fixed frequency of 1 MHz. A model including a capacitor in parallel with a resistor is applied to the measured impedance with the capacitance shown in Figure 5.5b. A weak voltage dependence is observed and attributed to the use of a semiconductor bottom plate. The maximum measured capacitance correspond well to expected values for this dielectric stack (Si_3N_4 and high-κ oxide) and overlapping area, calculated using a parallel-plate model.

6

Material characterisation

Semiconductor materials and their contacts have been characterised using standard methods, commonly used in industry and academia, and new methods, suited for vertical nanowire characterisation, have been introduced. This characterisation has allowed for integration of InAs nanowires on Si wafers and thus, preparation for industrial scale fabrication. It has also resulted in improved MOSFET and circuit performance and possibly setting new standards for contact characterisation in the vertical geometry.

6.1 INAS EPITAXIAL LAYERS ON SILICON

In order for III-V semiconductor transistors to be considered for mass production in industry, they need to be integrated on Si wafer for the cheap availability of high quality wafers and the possibility of co-integration of Si transistors. A good way to integrate III-V semiconductors on Si is through nanowires grown in the vertical direction. Due to the small diameters of nanowires, stress originating from different lattice constants can relax in the radial direction resulting in high-quality semiconductor crystals with small number of dislocations [56, 57]. A potential barrier at the Si/InAs heterojunction has been observed using this direct integration [30], which makes it unsuitable for high-performance MOSFETs.

Another integration scheme for nanowires is growth of planar InAs on Si, followed by nanowire growth from the planar InAs layer. Due to different thermal expansion coefficients, lattice constants and the growth of a polar semiconductor on a non-polar substrate, this task is not trivial. A high-quality growth of InAs on Si (111) was demonstrated in Paper VI, wherein a two-step growth consisting of several nucleation layers followed by normal high-temperature growth was used. An atomic force microscopy (AFM) image

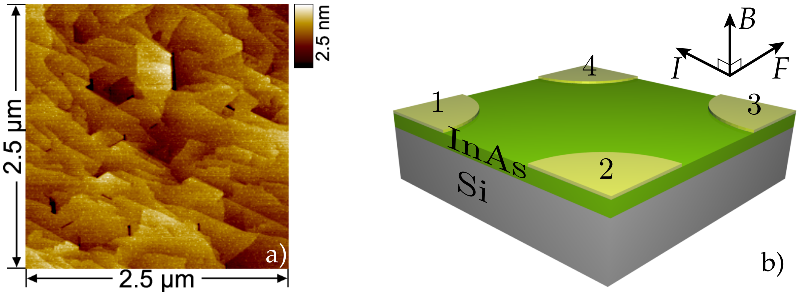


Figure 6.1: (Left) InAs epitaxial layer surface measured with AFM and (right) 3D illustration of a fabricated Hall sample

of the surface can be seen in Figure 6.1a, where atomic steps can clearly be observed.

6.2 HALL MEASUREMENTS USING THE VAN DER PAUW TECHNIQUE

A Hall measurement is a powerful tool to characterise planar semiconductor layers. The main principle is based on the Lorentz force acting on mobile charges travelling between two contacts under the influence of a magnetic field, B. The Lorentz force, F, is applied perpendicular to both the direction of B and the current, I, resulting in accumulation of charge carriers in the direction of the Lorentz force. These mobile charges give rise to a voltage drop called the Hall voltage, V_{H}, expressed as

$$V_{\mathrm{H}} = \frac{IB}{qn_{\mathrm{s}}}. \tag{6.1}$$

Here, n_{s} is the sheet carrier concentration of the semiconductor layer and q is the elementary charge. Hall samples, $2.4 \cdot 2.4$ mm^2 in size, were fabricated according to the design shown in Figure 6.1b. Four metal contacts are evaporated onto a HCl (1:10) etched InAs surface through a shadow mask forming contacts of a size large enough for any contact resistance to be negligible. The Si underneath the InAs is lowly n-doped, serving as an insulating substrate. After sample mounting and wire bonding to the contacts, the sheet resistance, R_{SH}, of the InAs layer can be calculated using

$$1 = \mathrm{e}^{-\pi R_{\mathrm{vertical}}/R_{\mathrm{SH}}} + \mathrm{e}^{-\pi R_{\mathrm{horizontal}}/R_{\mathrm{SH}}} = \begin{bmatrix} R_{\mathrm{vertical}} = \frac{V_{\mathrm{vertical}}}{I_{\mathrm{vertical}}} \\ R_{\mathrm{horizontal}} = \frac{V_{\mathrm{horizontal}}}{I_{\mathrm{horizontal}}} \end{bmatrix}. \tag{6.2}$$

V_{vertical} is the voltage measured over the opposing contacts of the current flow. As an example, the current flows between contacts 1 and 2 in Figure 6.1b and the voltage is then measured between contacts 4 and 3. This measurement can be performed in four separate ways by switching polarities and sides to get average values for R_{vertical} and $R_{\text{horizontal}}$.

Once R_{SH} is established, V_{H} is measured across the diagonal of the square samples and the current is applied between the other two contacts under the influence of the magnetic field. The Hall measurements can also be averaged by switching polarities of the current and magnetic field and switching the contacts used for measuring V_{H}. From V_{H}, n_{s} is calculated using (6.1). Knowing R_{SH} and n_{s}, μ is determined using

$$\mu = \frac{1}{q n_{\text{s}} R_{\text{SH}}}, \tag{6.3}$$

and if the thickness is known, the carrier concentration (n) can be calculated.

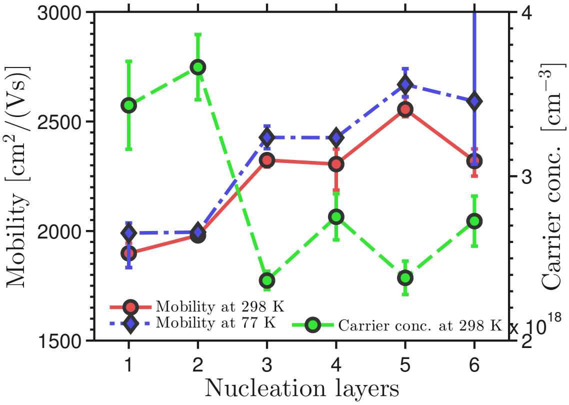


Figure 6.2: Hall mobility and carrier concentration for undoped InAs as a function of the number of nucleation layers during growth, measured both at room temperature and at 77 K.

6.2.1 HALL MEASUREMENTS ON INAS EPITAXIAL LAYERS

Undoped InAs layers grown with different number of nucleation steps are investigated using Hall measurements with the results presented in Figure 6.2. An increase of μ is observed up to about 4 nucleation layers, which is an indication of an improved crystal quality. Furthermore, n is reduced with more nucleation layers pointing towards a more defect-free material. A slightly higher mobility is observed for measurements performed in liquid nitrogen (N_2), corresponding to a temperature of 77 K, possibly due to less phonon scattering. The highest measured μ for the undoped InAs layers on Si is $2750\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at room temperature.

More interesting from a device perspective is the usage of doped InAs epitaxial layers to serve as low-resistance contacts to the nanowires. Doping is ensured by flowing tetraethyltin (TESn) together with the In and As precursors, resulting in a Sn-doped semiconductor. Similarly as the undoped layers, these doped layers are characterised using Hall measurements with a highest observed carrier concentration of $4.8 \times 10^{19}\,\mathrm{cm}^{-3}$. From a nanowire growth perspective, having dopants up to the epitaxial layer surface may unintentionally dope nanowires grown from the layer. Instead, InAs layers grown with a doping profile along the thickness of the layer, is studied. The layers are doped for most of the thickness, but with an undoped cap layer at the top, as seen in the schematic of Figure 6.3a. One way to study the doping is to remove material by etching some of the semiconductor using the metal contacts as etch masks followed by Hall measurements. By doing this repeatedly, a map over the mobility and carrier concentration as a function of depth can be calculated by modelling the layers as parallel sheets of different sheet resistances, i.e. different mobility and carrier concentrations, Figure 6.3b. This is performed for an undoped and a doped layer with the results shown in Figure 6.4.

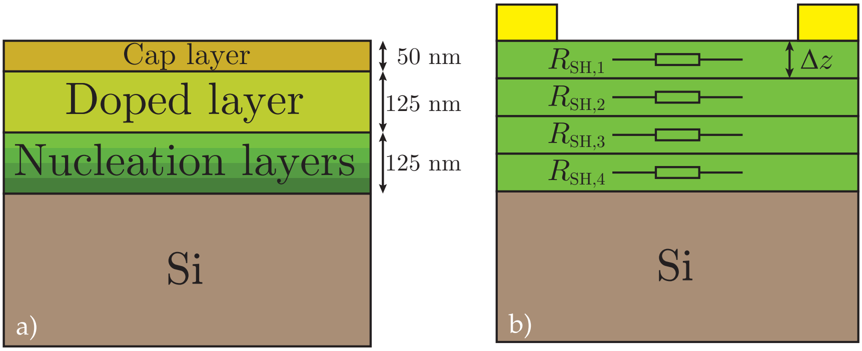


Figure 6.3: a) Schematic illustration of a doped epitaxial layer with an undoped cap layer in cross section. b) Characterisation of the doped layers is performed using a model consisting of separate conductive sheets, each with its corresponding carrier concentration and mobility.

The undoped sample of Figure 6.4a is observed to have a higher mobility and lower carrier concentration closer to the surface of the epitaxial layer.

This points toward an improved crystal quality with thicker layers, probably caused by high concentration of crystal defects close to the InAs/Si interface. Closest to the surface, μ is about $4000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. For the layer with varying doping, Figure 6.4b, a similar trend for μ is observed, but with overall lower values, going up to above $3000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ close to the surface. For the carrier concentration, a clear peak between 50 and 100 nm is seen indicating the doped region. The cap layer is indicated by the lower carrier concentration at the point closest to the surface. A large carrier concentration can be seen in the bottom of the layer, very similar in magnitude between the two samples.

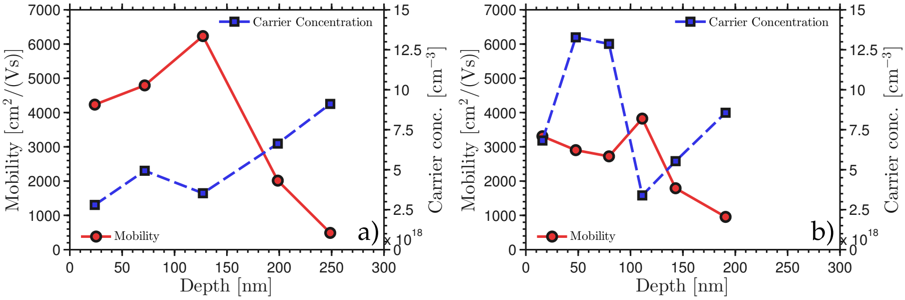


Figure 6.4: Hall mobility and carrier concentrations as a function of depth for an undoped a) and a doped b) InAs epitaxial layer.

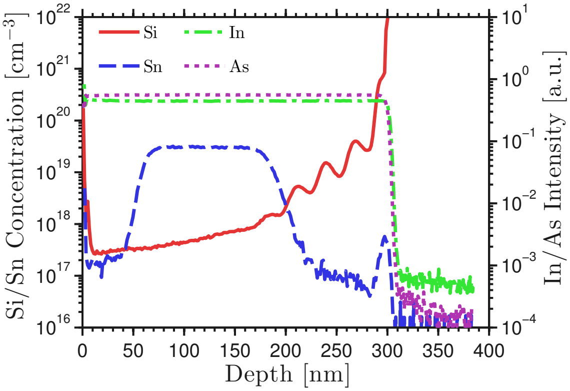


Figure 6.5: SIMS analysis performed on the modulation doped InAs epitaxial layer.

In order to verify these results, the modulation doped sample was sent for secondary ion mass spectrometry (SIMS) inspection, with the result plotted in Figure 6.5. A clear peak is seen for the dopant atoms, Sn, at about the same depth as suggested by the Hall measurements. The In and As traces indicate a layer thickness of 300 nm. According to the SIMS data, Si impurities are situated in the first 100 nm of the layer, which explains the carrier concentration increase close to the InAs/Si interface from Figure 6.4b.

6.3 STANDARD TLM MODEL

A common way of characterising the quality of semiconductors and their contacts is by applying the transmission line method (TLM) [58, 59]. The model is based on the fabrication of a series of resistors on an insulating substrate with contacts on top and is used to calculate the semiconductor resistivity, ρ_s, and the specific contact resistivity, ρ_c. A schematic illustration of one such resistor can be seen in Figure 6.6.

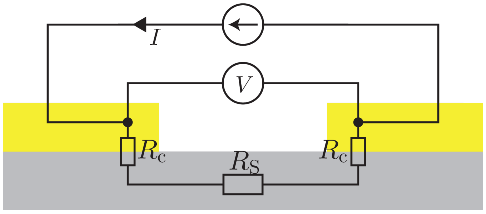


Figure 6.6: A schematic cross-sectional view of an isolated semiconductor resistor with two metal contacts. In a 4-point measurement approach, a current is applied with using a current source and the corresponding voltage is measured over the resistor.

A current is applied from one contact to the other using a current source and the resulting voltage is measured using a voltmeter. Using Ohm's law, the total resistance, R_tot, is calculated, which is the sum of the resistance in the semiconductor, R_s, and two distributed contact resistances, R_c. By varying the separation between the metal contacts, L, and assuming uniform semiconductor resistivity, R_s can be described as

$$R_\text{s} = \frac{\rho_\text{s} L}{W_\text{s} t_\text{s}}. \tag{6.4}$$

Here, W_s is the width and t_s is the thickness of the semiconductor. By varying the length of the resistors and keeping all other dimensions constant, a series similar to the one shown in Figure 6.7 can be created.

If R_c is fixed, i.e. constant contact length, for all resistor lengths, the derivative of the linear relation can be used to extract the sheet resistance

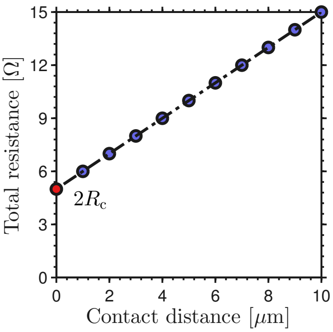


Figure 6.7: Theoretical TLM series.

and, in turn, ρ_s if t_s is known, (6.5).

$$\frac{\mathrm{d}R_{\mathrm{tot}}}{\mathrm{d}L} = \frac{\rho_{\mathrm{s}}}{W_{\mathrm{s}} t_{\mathrm{s}}} = \frac{R_{\mathrm{SH}}}{W_{\mathrm{s}}} \tag{6.5}$$

The total resistance for a contact separation of 0 corresponds to $2R_c$. If the contact length, L_c, is known and the sheet resistance underneath the contact, is equal to R_{SH}, then the transfer length, L_T, can be calculated using

$$R_{\mathrm{c}} = \frac{R_{\mathrm{SH}} L_{\mathrm{T}}}{W_{\mathrm{s}}} \coth\left(\frac{L_{\mathrm{c}}}{L_{\mathrm{T}}}\right). \tag{6.6}$$

L_T is the depth underneath an infinitely long contact at which $1 - \mathrm{e}^{-1} = 63\,\%$ of the total current flowing in the semiconductor has entered the metal contact. For long contacts (6.6), condenses down to

$$\lim_{L_{\mathrm{c}} \to \infty} R_{\mathrm{c}} = \frac{R_{\mathrm{SH}} L_{\mathrm{T}}}{W_{\mathrm{s}}}. \tag{6.7}$$

From L_T, the specific contact resistivity is calculated using

$$\rho_{\mathrm{c}} = R_{\mathrm{SH}} L_{\mathrm{T}}^2. \tag{6.8}$$

6.3.1 TLM CHARACTERISATION OF INAS EPITAXIAL LAYERS

In the nanowire device fabrication, metal contacts are fabricated down to the InAs epitaxial layers to serve as the bottom electrode. It is therefore of great importance to limit the resistance of these metal contacts. Resistors are fabricated with evaporated titanium (Ti)/paladium (Pd)/Au contacts using lift-off and semiconductor mesa isolation with $H_3PO_4 : H_2O_2 : H_2O$ (1:1:25).

Two different layers are investigated corresponding to different doping flow conditions: one undoped and one doped. Using the standard TLM model applied to measured resistances, the results can be seen in Figure 6.8.

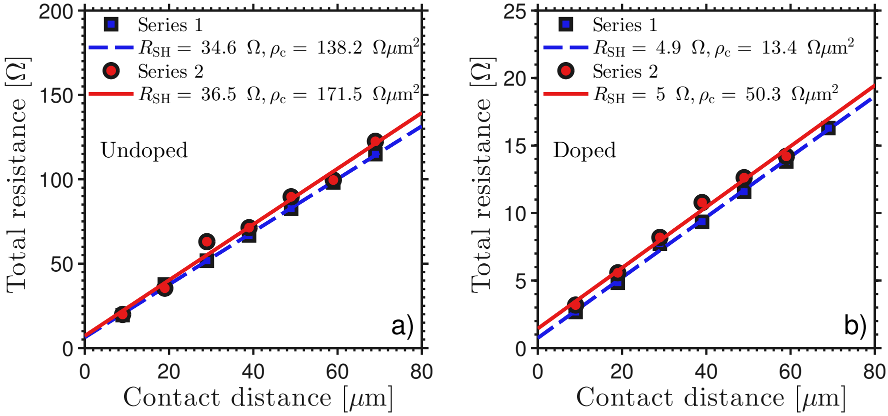


Figure 6.8: transmission line model (TLM) evaluation of two InAs epitaxial layers: a) an undoped and b) a doped. Two TLM sets are included to give an estimate of the parameter variation across the sample. Infinitely long contacts are assumed.

A high R_{SH} of about $35\,\Omega$ is observed for the undoped layer with a corresponding Ti/InAs ρ_{c} of $150\,\Omega\,\mu\mathrm{m}^2$. For a vertical nanowire device consisting of one semiconductor sheet access and a metal contact width of $5\,\mu\mathrm{m}$, an access resistance of about $45\,\Omega$ is calculated. For a device consisting of tens or hundreds of nanowires, this resistance seriously degrades the performance. The doped layer shows much improved resistance values with an R_{SH} of $5\,\Omega$ and ρ_{c} of $30\,\Omega\,\mu\mathrm{m}^2$. With the same access structure, the access resistance is just $2.5\,\Omega$, which makes these InAs epitaxial layers useful for high performance nanowires MOSFETs. A more extensive study of metal contacts on these InAs epitaxial layers has previously been published [60].

6.4 TLM ON VERTICAL NANOWIRES

The transmission line method can also be applied to nanowires. The same methodology used for planar resistors applies to nanowires, wherein resistors of different lengths are fabricated that allows for determination of ρ_{s} and ρ_{c}. Most methods for TLM evaluation on nanowires requires breaking the nanowires off, transferring them to an insulating substrate, and defining contact [61–63]. The results obtained from this fabrication method might, however, not be applicable to vertically fabricated devices, since the fabrication process differ significantly and the metal contact surfaces are not identical. For accurate determination of contact resistances, the TLM need to be applied on vertically aligned nanowires on the same chip and fabricates in the same way as the contacts for the real devices, such as MOSFETs.

6.4.1 TLM IN THE CYLINDRICAL GEOMETRY

The TLM model can be applied to a cylindrical geometry by some slight modifications of the standard planar model [62]. The nanowire resistance, R_{NW}, in the uncontacted regions is described using (6.9), with R_{c} and ρ_{c} calculated using (6.10) and (6.11), respectively.

$$R_{\mathrm{NW}} = \frac{\rho_{\mathrm{s}} L}{\pi r_{\mathrm{NW}}^2} \tag{6.9}$$

$$R_{\mathrm{c}} = \frac{\rho_{\mathrm{s}} L_{\mathrm{T}}}{\pi r_{\mathrm{NW}}^2} \coth\left(\frac{L_{\mathrm{c}}}{L_{\mathrm{T}}}\right) \tag{6.10}$$

$$\rho_{\mathrm{c}} = \frac{2 L_{\mathrm{T}}^2 \rho_{\mathrm{s}}}{r_{\mathrm{NW}}} \tag{6.11}$$

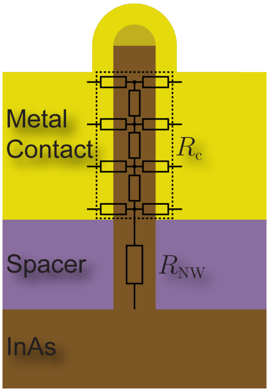


Figure 6.9: Schematic showing a nanowire resistor with a distributed metal contact at the top and a semiconductor contact at the bottom.

Here, r_{NW} is the nanowire radius. If all the geometrical parameters are known, the model can be applied to measured resistance values as a function of L. The analytical model has been validated using simulations of nanowire resistors, of a similar structure shown in Figure 6.9, with various ρ_{c} in COMSOL®.

6.4.2 NANOWIRE RESISTOR FABRICATION

Vertical nanowire resistors can be fabricated from different semiconductors on various substrates and using different metal contacts. Because of its narrow band gap and Fermi level pinning in the conduction band, InAs is a good choice for ohmic contacts [64]. Ni has shown to yield good contacts to both InAs, InGaAs, and other semiconductors especially when Ni is annealed into the semiconductor [65–67]. The main challenge for performing a TLM study in the vertical direction is to form a spacer between a bottom and top electrode and, in a controlled manner, vary its thickness and thereby fabricate the different resistor lengths needed for TLM.

Vertical InAs nanowire resistors are fabricated on the InAs epitaxial layers, using it both as a as a buffer layer for nanowire growth and as a low-resistive contact to the nanowires. The nanowire Au seed particles are defined in a similar way as the nanowire MOSFETs. Nanowire growth is performed using MOVPE at 420 °C with three different doping conditions corresponding to lowly, medium, and highly doped nanowires. For the spacer, HSQ is chosen for the possibility to control the thickness with the electron-beam exposure dose [39]. A 400-nm-thick HSQ is spun on, baked at 200 °C, and exposed with an acceleration voltage of 50 kV to transform the film into SiO_2. Development is performed in concentrated tetramethylammonium hydroxide (TMAH) for 60 s followed by water rinsing. The exposure dose is varied from 200 to 500 $\mu C\,cm^{-2}$, corresponding to thicknesses from 50 nm to 400 nm. After development, the HSQ is baked at 350 °C for 20 min. Before metal deposition, the nanowire surface not covered by the HSQ, i.e. the contact area, is etched in $HCl : H_2O$ (1:10) for 30 s to remove the native oxide and passivate the semiconductor surface. A top metal stack consisting of nickel (Ni), W, and Au (15, 30, 150 nm) is sputtered and patterned using UV-lithography. Au is etched using a KI-based wet etchant, W is dry etched in a mixture of SF_6 and argon (Ar) using RIE, and finally Ni is wet etched using $CH_3COOH : H_2SO_4 : HNO_3 : H_2O$ (1:2.5:2.5:15). The metal stack is used for contacts both to the InAs epitaxial layer and the nanowires so that no vias are necessary. A 3D illustration of the fabricated devices can be seen in Figure 6.10.

6.4.3 DETERMINATION OF HSQ THICKNESS

One of the main challenges in the vertical TLM study is to accurately determine the thickness of the HSQ spacer. The spun on film can vary in thickness across the sample due to edge effects, non-uniform effective spin-on speed and dirt particles. Also, small variations in the time between resist application and spinning affects the eventual thickness. Instead, the thickness is determined after development and baking by comparing the colour of the

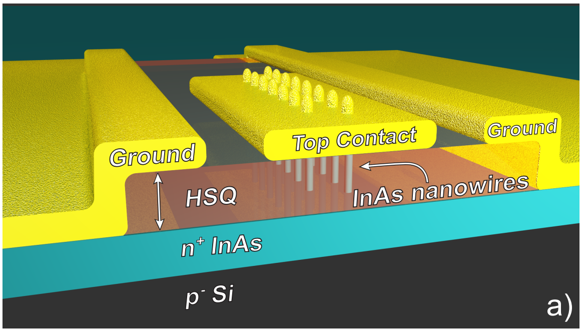


Figure 6.10: 3D illustration of a nanowire resistor used in TLM study.

thin film to a reference colourbar, similar to the spectral reflectance method. This colourbar can be seen in Figure 6.11 and was obtained by comparing the colour information from optical micrographs to measured heights using AFM and profilometer. It is imperative that identical lighting conditions are used when extracting the HSQ height as was used when calibrating the colourbar. Our determined colourbar corresponds very well to the expected thin film interference colours for a refractive index of 1.39, a previously reported value for HSQ from literature [68].

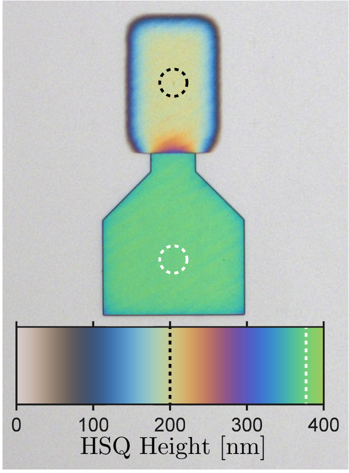


Figure 6.11: Top view optical micrograph of an HSQ pad, which forms the spacer between the bottom and top contact. The inset shows the thin-film colour of HSQ as a function of the HSQ thickness.

6.4.4 RESULTS

The *I*-*V* characteristics of three nanowire resistors, fabricated with the same HSQ thickness, are shown in Figure 6.12. A higher current is observed for higher-doped nanowires as expected, but more striking is the asymmetry of the currents at positive and negative biases. For the highly doped nanowires, a symmetric and ohmic behaviour is observed whereas for the lightly and undoped nanowires, non-linear characteristics are seen indicating a potential barrier close to the bottom of the nanowires.

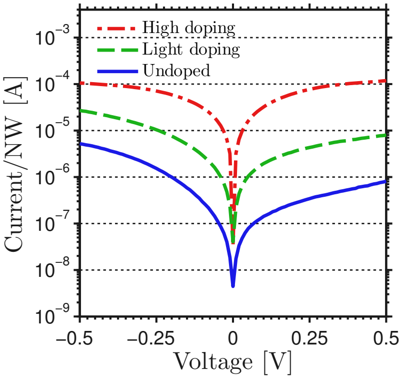


Figure 6.12: *I*-*V* characteristics of three devices with the same HSQ thickness for the different doping levels. The voltage is applied to the top of the nanowires with the bottom defined as ground.

Because of these non-linear *I*-*V* dependencies, TLM analysis is troublesome for the lightly and undoped sample. For the highly doped sample, however, the familiar TLM trend is depicted in Figure 6.13a. The same analysis is performed after annealing the devices in N_2 at some different temperatures. The resistivity and specific contact resistivity is extracted for the different annealing conditions, shown in Figure 6.13b. Better contacts are observed with higher annealing temperatures with a lowest obtained ρ_c of $0.6\,\Omega\,\mu\mathrm{m}^2$. This value corresponds well to what has previously been reported for annealed Ni/InAs planar contacts [69]. The resistivity is constant, and close to previously reported values for InAs nanowires [70], up to 350 °C where a substantial degradation is observed.

6.4.5 PROPOSED IMPROVEMENTS FOR THE VERTICAL TLM

With the demonstrated vertical nanowire TLM, a large number of different contact metals can be studied and with them various annealing conditions and surface preparations, as long as the process steps are compatible with

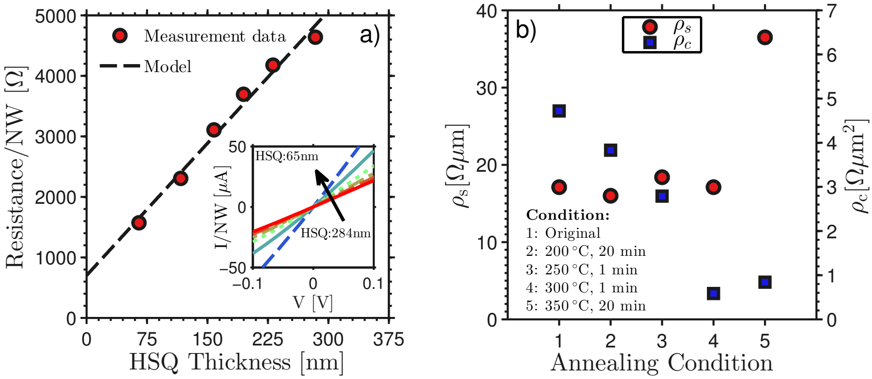


Figure 6.13: a) TLM series for highly doped nanowires. b) Resistivity and specific contact resistivity for highly doped nanowires as function annealing conditions.

material choices. The spacer in this study, HSQ, has some issues that should be addressed. For lowly doped nanowires, non-linear *I*-*V* characteristics are observed that indicate a potential barrier close to the bottom of the nanowire. This can be explained by charges situated in the HSQ. This effect disappears with annealing of the resistors, which could mean that the 20 min HSQ baking after development is insufficient. A specific study of the HSQ is needed in order to be able to optimize its characteristics.

Another issue, as with all spin-on spacers, is the accumulation of material close to densely packed or high aspect ratio features. If the nanowires are longer than the spin-on spacer thickness, a locally thicker spacer can be observed. For any exposure dose, this will result in thicker film also post-development. This very local change in thickness can be hard to accurately determine. The solution is to always work with short nanowires, shorter than the originally spun on spacer thickness.

In the present analysis, 6 resistor lengths are fabricated per TLM series. By fabricating more of them, a larger certainty can be obtained for the calculated parameters and error margins can be estimated.

7

Conclusion and Outlook

In the work presented in this thesis, vertical InAs nanowire MOSFETs, operating with a higher combined on- and off-performance than any previously reported vertical nanowire MOSFETs. A method for the characterisation of nanoscale contacts is demonstrated that makes it possible to further reduce the access resistance and approach the intrinsic performance limit for this type of devices. Furthermore, an RF-circuit implementation of vertical nanowire devices on Si is demonstrated, highlighting the maturity of the technology. During the years leading up to this thesis, the vertical nanowire technology has improved considerably, offering high performance in both DC and RF.

One of the main challenges to integrate III-V semiconductors on silicon, at an industrial scale, is to do this in an economically viable way, while still maintaining high-quality materials. Both of these conditions could be met by vertical III-V nanowires, grown either from catalytic seed particles or from selective area growth. Both methods could also be used for growth of heterostructures, consisting of several semiconductor materials, allowing for band engineering.

One main motivation for the use of vertical nanowires is that the device architecture allows for relatively easy fabrication of gate-all-around structures, offering better scalability than competing technologies. The electrostatic is much improved compared to a planar device, but less pronounced when compared to e.g. a tri-gate device. Instead, the main advantage of a vertical transistor layout is the possibility to more freely optimise gate and contact lengths, without affecting the footprint area. It is likely that future transistor technologies will move closer to a vertical architecture. Several transistors may be stacked on top of each other in a single nanowire. It is also possible that laterally oriented nanowires, but stacked vertically, will prove to be a better alternative.

Personal experiences point towards more complex fabrication methods in vertical MOSFET fabrication, compared to lateral ones. The increased fabrication complexity is probably the main challenge restricting the performance at this time. Novel methods for this fabrication need to be invented together with further development of device characterisation. The MOSFET development in recent years has not only been based on the shrinking of device dimensions, but also by several paradigm shifts, such as the introduction of high-κ dielectrics and tri-gate MOSFET channels. It can therefore be expected that when nanowire-based MOSFETs move closer to large-scale production, industry will find a way to solve the remaining issues.

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APPENDICES

A

MOSFET Fabrication Using the Self-Aligned Gate-Last Process

THE detailed process flow used to fabricate the vertical indium arsenide (InAs) nanowire metal-oxide-semiconductor field-effect transistor (MOSFET)s, using the self-aligned gate-last process, is presented in this appendix. The aim of this description is to allow for future reproduction of the MOSFET results included in this thesis. The fabrication was performed at Lund Nano Lab and note should be taken that some processing parameters can vary over time and with the exact tools used.

A.1 SUBSTRATE

The MOSFETs are fabricated on externally fabricated silicon (Si) wafers with a (111) orientation, which is the desired orientation for the eventual nanowire growth. Si-wafers with low p-doping are used to induce a pn-junction at the interface to the n-type InAs epitaxial layers. A low doping of the Si is desired as it is used for inter-device isolation in circuits and to reduce the capacitance of contacting pads.

A.2 BUFFER LAYER GROWTH

InAs layers are grown on the Si wafers to serve as (111) buffer layers for nanowire growth and a low resistive interconnecting layer. A doping gradient is introduced during metalorganic vapour phase epitaxy (MOVPE) growth to reduce the resistance of the layers. For this work, the growth of the InAs epitaxial layers was performed by Sepideh Gorji Ghalamestani and Johannes Svensson.

A.3 CATALYST PARTICLE DEFINITION

gold (Au) discs are deposited onto the InAs surface to serve as catalytic particles during the nanowire growth. The particles are defined by electron beam lithography (EBL) single-pixel exposure in a positive resist. The exposure has recently been outsourced to Chalmers University of Technology with different parameters for exposure and resist development, but here the older in-house process is presented.

Step 4: Dehydrate the surface

- 5 min on 200 °C hotplate.
- Cool sample on a cold metal surface.

Step 5: Apply poly(methyl methacrylate) (PMMA) 200A5 in anisole (1:1)

- 30 s spin at 6000 rpm (1500 rpm s^{-1}).
- 40 min baking at 180 °C in oven.

Step 6: Apply PMMA 950A4 in anisole (1:1)

- 30 s spin at 6000 rpm (1500 rpm s^{-1}).
- 40 min baking at 180 °C in oven.

Step 7: EBL at 20 kV and beam current of 18 pA

- Dot exposure dose of 6 fC for arrays with a spacing of 200 nm.
- Dot exposure dose of 60 fC for single particles.

Step 8: Development

- 90 s in methyl isobutyl ketone (MIBK):2-propanol (IPA) (1:3), stirring 3 times.
- 30 s in IPA, continuous stirring.

Step 9: Semiconductor surface cleaning

- O_2-plasma ashing for 20 s at a pressure of 5 mbar.
- 30 s etching in buffered oxide etch (BOE) (1:10).
- 30 s in de-ionized water (DIW).

Step 10: Evaporation

- 15 nm Au evaporation (1 Å s^{-1}).

Step 11: Lift-off

- 15 min in 50 °C acetone, stirring at the end.
- 5 s in 50 °C acetone, stirring.
- 5 min in 50 °C acetone, stirring at the end.
- 5 s in IPA, stirring.
- 1 min in IPA.

Step 12: Organic cleaning to remove residual PMMA

- 15 min in 50 °C acetone and ultrasonic power bath.
- 1 min in IPA.
- O_2-plasma ashing for 20 s at a pressure of 5 mbar.
- 30 s etching in BOE (1:10).

A.4 NANOWIRE GROWTH PREPARATION

Nanowire growth is not performed on the entire wafer at the same time as the wafer is cut into $1 \cdot 1\ \text{cm}^2$-pieces. A protective organic coating is first applied, followed by dicing and cleaning of the surface.

Step 13: Dehydrate the surface

- 2 min on 115 °C hotplate.
- Cool sample on a cold metal surface.

Step 14: Apply S1818 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 15 min baking at 120 °C on hotplate.

Step 15: Dicing

- Wafer is cut into $1 \cdot 1\ \text{cm}^2$-pieces.

Step 16: Organic cleaning to remove S1818 and PMMA residuals

- Acetone spraying with squeeze bottle.
- 15 min in 50 °C acetone and ultrasonic power bath.
- 1 min in IPA.
- O_2-plasma ashing for 20 s at a pressure of 5 mbar.
- 30 s etching in BOE (1:10).
- 30 s in DIW

A.5 NANOWIRE GROWTH

Just before nanowire growth, the surface should be etched either by HF or diluted HCl to remove the native oxide. The growth is performed in two steps: Firstly a short undoped stem is grown and secondly a highly doped top segment, which also overgrows on the sidewalls.

A.6 GATE MASK DEFINITION

In order to define the edge of the top metal, hydrogen silsesquioxane (HSQ) is applied and exposed. Other resists than HSQ are conceivable for this process as long as it possible to perform 3D lithography using the exposure dose.

Step 19: Dehydrate the surface

- 2 min on 200 °C hotplate.
- Cool sample on a cold metal surface.

Step 20: Applying the HSQ (FOX-15)

- 60 s spin at 3000 rpm (1500 rpm s^{-1}).
- 2 min baking at 200 °C on hotplate.

Step 21: EBL at 50 kV and beam current of 430 pA

- $60 \cdot 60$ μm^2 area exposure with dose 210 μC cm^{-2} and 10 nm step size.

Step 22: Development

- 60 s in concentrated tetramethylammonium hydroxide (TMAH), no stirring in the first 15 s followed by slow continuous stirring.
- 30 s in DIW, continuous stirring.

A.7 TOP METAL FORMATION

The top metal is deposited followed by anisotropic dry etching and HSQ mask removal.

Step 19: Contact surface cleaning

- 30 s in $HCl:H_2O$ (1:10), continuous stirring.
- 30 s in DIW, continuous stirring.

Step 20: Metallization

- 15 nm tungsten (W) sputtering at 100 W DC power and 16 sccm argon (Ar)-flow (0.9 Å s^{-1}), rotation.
- 6 nm TiN plasma-enhanced atomic layer deposition (PEALD) at 250 °C using tetrakis(dimethylamido)titanium (TDMATi) precursor.

Step 21: ICP-RIE of metal stack

- 70 s + 30 s in 20 mTorr SF_6:C_4F_8:Ar (16, 32, 3 sccm) at an ICP power of 800 W and radio frequency (RF) power of 20 W.

Step 22: Cleaning of dry-etch residuals

- 60 s in acetone.
- 60 s in IPA.
- 60 s in DIW.
- 30 s in HCl:H_2O (1:100).
- 60 s in DIW, continuous stirring.

Step 23: Wet etching of HSQ

- 20 s in BOE.
- 60 s in DIW, continuous stirring.

A.8 INDIUM ARSENIDE SOURCE PAD DEFINITION

The bottom InAs epitaxial layer is patterned by UV-lithography and etched to form InAs mesas on the highly resistive Si.

Step 24: Dehydrate the surface

- 2 min on 115 °C hotplate.
- Cool sample on a cold metal surface.

Step 25: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 90 s baking at 115 °C on hotplate.

Step 26: Ultraviolet (UV) lithography (wavelength of 365 nm at 20 mW cm^{-2})

- Exposure for 4.2 s.

Step 27: Development

- 90 s in MF319, slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 28: Hardbaking

- 15 min at 120 °C on hotplate.

Step 29: Plasma ashing

- 30 s at 5 mbar O_2-pressure.

Step 30: Wet etching of InAs

- 150 s in H_3PO_4:H_2O_2:H_2O (1:1:25), slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 31: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

A.9 BOTTOM SPACER

The bottom spacer is deposited by atomic layer deposition (ALD), defined using an etched back organic resist, and wet etched, only at the unprotected nanowires.

Step 32: SiO_2 Deposition

- 50 nm PEALD at 250 °C using bis(diethylamino)silane (BDEAS) precursor.

Step 33: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 15 min baking at 120 °C on hotplate.

Step 34: Thinning of resist

- 1340 s reactive-ion etching (RIE) with oxygen $(O)_2$ at 300 mTorr, a flow of 15 sccm and power of 20 W.

Step 35: Wet etching of SiO_2

- 200 s in HF:H_2O (1:100), slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 36: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

A.10 THINNING DOWN CHANNEL AND GATE DIELECTRIC

After bottom spacer formation, the top and bottom of the nanowires are protected by etch masks. This means that the channel region can be etched selectively. To do this in a controlled way, cyclical oxidation and etching of the oxide is performed (digital etching). The following steps are repeated several times. Directly after thinning down the channel, a high-κ dielectric is deposited.

Step 37: Oxidation

- 10 min O_3-treatment at 50 °C.

Step 38: Oxide etching

- 15 s in $HCl{:}H_2O$ (1:10).
- 60 s in DIW, continuous stirring.

Step 39: Gate dielectric deposition

- 0.9 nm Al_2O_3 ALD at 300 °C using trimethylaluminium (TMA) and H_2O precursors.
- 5.5 nm Al_2O_3 ALD at 120 °C using tetrakis(dimethylamino)hafnium (TDMAHf) and H_2O precursors.

A.11 GATE EDGE DEFINITION

The gate edge is defined in the same way as the bottom spacer, i.e. by thinning down a resist and using it as an etch mask. An overlapping gate, aimed for reducing the access resistance, is implemented.

Step 40: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 15 min baking at 120 °C on hotplate.

Step 41: Thinning of resist

- 1250 s RIE with O_2 at 300 mTorr, a flow of 15 sccm and power of 20 W.

Step 42: Dry etching of W

- 45 s RIE with SF_6 and Ar at 185 mTorr, flows of 45 sccm and 10 sccm respectively and a power of 140 W.

Step 43: Plasma Ashing

- 60 s at 5 mbar O_2-pressure.

Step 44: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

A.12 GATE PAD FORMATION

Gate pads are etched out for device isolation. This here done using UV-lithography but can be done using EBL for the creating of a finger gates.

Step 45: Dehydrate the surface

- 2 min on 115 °C hotplate.
- Cool sample on a cold metal surface.

Step 46: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 90 s baking at 115 °C on hotplate.

Step 47: UV lithography (wavelength of 365 nm at 20 mW cm^{-2})

- Exposure for 4.2 s.

Step 48: Development

- 90 s in MF319, slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 49: Hardbaking

- 15 min at 120 °C on hotplate.

Step 50: Plasma ashing

- 30 s at 5 mbar O_2-pressure.

Step 51: Dry etching of W

- 45 s RIE with SF_6 and Ar at 185 mTorr, flows of 45 sccm and 10 sccm respectively and a power of 140 W.

Step 52: Plasma ashing

- 60 s at 5 mbar O_2-pressure.

Step 53: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

A.13 TOP SPACER FABRICATION

The top spacer is, again, defined by organic resist thinning using O_2-plasma.

Step 54: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 40 min baking at 200 °C on hotplate.

Step 55: Thinning of resist

- 700 s RIE with O_2 at 300 mTorr, a flow of 15 sccm and power of 20 W.

A.14 FORMATION OF VIAS

Two types of vias are formed: one down do the gate layer and one down to contact the InAs. The gate via is created using UV-lithography and resist ashing to reach the gate metal. The via down to the InAs is formed in the same way as the gate via.

Step 56: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 rpm s^{-1}).
- 90 s baking at 115 °C on hotplate.

Step 57: UV lithography (wavelength of 365 nm at 20 mW cm^{-2})

- Exposure for 8 s.

Step 58: Development

- 60 s in MF319, slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 59: Hardbaking

- 15 min at 120 °C on hotplate.

Step 60: Thinning of resist

- 800 s RIE with O_2 at 300 mTorr, a flow of 15 sccm and power of 20 W.

Step 61: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

A.15 TOP METAL DEPOSITION AND DEFINITION

High-κ oxide is etched from the top of the nanowires, not covered by the second spacer, and the via down to the InAs. This is followed by metal sputtering, which will contact the already established TiN/W top contact. The top metal stack is patterned and etched to form 50 Ω co-planar waveguide pads.

Step 62: Metallization

- 15 nm nickel (Ni) sputtering at 100 W DC power and 9 sccm Ar-flow (0.6 $\text{Å}\,\text{s}^{-1}$), rotation.
- 30 nm W sputtering at 100 W DC power and 16 sccm Ar-flow (0.9 $\text{Å}\,\text{s}^{-1}$), rotation.
- 150 nm Au sputtering at 100 W DC power and 9 sccm Ar-flow (3.4 $\text{Å}\,\text{s}^{-1}$), rotation.

Step 63: Apply S1813 resist

- 60 s spin at 4000 rpm (1000 $\text{rpm}\,\text{s}^{-1}$).
- 90 s baking at 115 °C on hotplate.

Step 64: UV lithography (wavelength of 365 nm at 20 $\text{mW}\,\text{cm}^{-2}$)

- Exposure for 4.1 s.

Step 65: Development

- 90 s in MF319, slow continuous stirring.
- 60 s in DIW, continuous stirring.

Step 66: Hardbaking

- 15 min at 120 °C on hotplate.

Step 67: Plasma ashing

- 30 s at 5 mbar O_2-pressure.

Step 68: Etching of metal stack

- Au wet etching: 30 s $KI:I_2:H_2O$ (1:2:17), slow continuous stirring.
- 60 s in DIW, continuous stirring.
- W dry etching: 45 s RIE with SF_6 and Ar at 185 mTorr, flows of 45 sccm and 10 sccm respectively and a power of 140 W.
- Ni wet etching: 60 s $CH_3COOH:HNO_3:H_2SO_4:H_2O$ (1:2.5:2.5:5).
- 60 s in DIW, continuous stirring.

Step 69: Plasma ashing

- 60 s at 5 mbar O_2-pressure.

Step 70: Resist stripping

- 2 min in acetone.
- 2 min in IPA.

PAPERS

Paper I

Gate-Last Fabrication of Enhancement Mode Vertical InAs Nanowire Transistor on Si

Martin Berg, Olli-Pekka Kilpi, Karl-Magnus Persson, Johannes Svensson, Markus Hellenbrand, Erik Lind, and Lars-Erik Wernersson,

***Abstract*—We present a new self-aligned, gate-last fabrication method for vertical nanowire transistors. The process allows for lithography-based control of the vertical gate length and selective trimming of the channel diameter, using digital etching. Core-shell nanowires consisting of an undoped InAs core and a highly doped InAs shell are used for reduced access resistance. Using this process, transistors are fabricated and characterised by DC and RF measurements. The best devices combine good on- and off-performance, exhibiting a transconductance of 0.64 mS/m and sub-threshold swing of 90 mV/decade. This corresponds to a Q-value of 7.1, which is higher than any previously reported vertical nanowire MOSFET.**

***Index Terms*—Vertical, Nanowire, InAs, MOSFET, Transistor, Gate-last, Self-aligned.**

I. INTRODUCTION

IN recent decades, the fast development of integrated circuits has been based on the scaling of planar Si metal-oxide-semiconductor field-effect transistors (MOSFETs). Extremely scaled devices often suffer from various short channel effects (SCEs), leading to larger power dissipation and lower operational frequencies. In order to reduce SCEs, new gate architectures and materials are implemented in order to improve the electrostatic control of the MOSFET channel and the carrier transport properties, respectively [1]–[4]. Vertical III-V compound semiconductor nanowire transistors are an attractive option for the next generation transistors due to integration compatibility of high electron mobility III-V materials on Si and straightforward fabrication of gate-all-around structures [5]–[7]. Furthermore, the vertical geometry allows for the use of large contact regions and the possibility for gate length optimization without affecting the device footprint.

The performance of vertical nanowire MOSFETs is commonly restricted by high access resistances situated in the ungated regions of the nanowires. These resistances can be lowered by highly doped access regions, strain engineering or through the use of heterostructures. However, in order to achieve a minimal resistive contribution of the access regions, a gate overlapping the contacts is needed. In this paper, vertical InAs nanowire MOSFETs fabricated using a novel self-aligned, gate-last process [8] are presented. The devices exhibit enhancement mode operation and have, to the authors knowledge, the highest reported Q-values [9] for any vertical nanowire MOSFET. The device is based on a core-shell structure, consisting of an intrinsic InAs core and a highly doped InAs shell. During the fabrication, the channel diameter is locally controlled by digital etching and a new kind of top contact structure is implemented, which allows overlap between the gate and the top contact. The process incorporates lithography-based control of the gate length in the vertical geometry. Furthermore, data is compared for devices with different spacing between nanowires, demonstrating the role of the access resistance on the transistor performance.

II. DEVICE FABRICATION

A cross-sectional scanning electron micrograph (SEM) of the fabricated nanowire MOSFETs is shown in figure 1a) with a corresponding schematic layer structure shown in Figure 1b). The devices are fabricated on $1 \cdot 1\,\mathrm{cm}^2$, highly resistive, $\{111\}$ p-type silicon substrates with a highly doped 300-nm-thick epitaxially grown InAs layer. InAs nanowires are grown in two types of arrays with a nanowire spacing of $200\,\mathrm{nm}$ and $500\,\mathrm{nm}$, respectively, using metalorganic vapor phase epitaxy (MOVPE). The growth is based on the vapor-liquid-solid (VLS) method, where Au particles are used as catalyst particles for nanowire growth. Electron beam lithography (EBL) and lift-off is used to define Au discs with a height

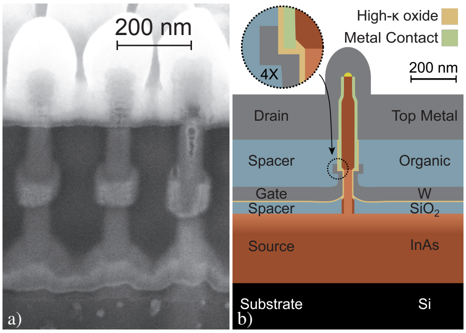

Fig. 1: a) Cross-sectional SEM of a fabricated device using the self-aligned gate-last process, clearly showing the gate overlapping the drain. The image is taken at a tilt of 52° from topview. b) Schematic cross section of the transistor architecture, with an inset highlighting the overlapping gate area.

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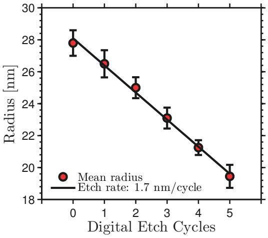

Fig. 2: Digital etching of InAs nanowires oxidized for $10\,\mathrm{min}$ in O_3 at $50\,^\circ\mathrm{C}$ followed by wet etching for $15\,\mathrm{s}$ in $\mathrm{HCl} : \mathrm{H_2O}$ (1:10). Each digital etch cycle removes about $1.7\,\mathrm{nm}$ on each side. The error bars indicate diameter variation for several nanowires.

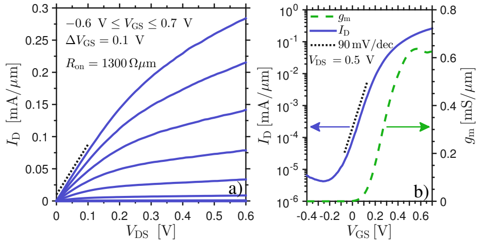

Fig. 3: a) Output and b) transfer characteristics of a nanowire MOSFET with $L_{\mathrm{G}} = 190\,\mathrm{nm}$ and fabricated using the self-aligned gate-last process. The nanowires are positioned in an hexagonal array with a spacing of $200\,\mathrm{nm}$. The current and transconductance are normalized to the circumference of the nanowires and the measurements are performed with the bottom of the nanowires grounded.

of $15\,\mathrm{nm}$ and a diameter of $28\,\mathrm{nm}$. The growth itself is a two-step process: 1) A 200-nm-long undoped InAs bottom part is grown at $470\,^\circ\mathrm{C}$ with a trimethylindium (TMIn) molar fraction of $30.4\,\mathrm{ppm}$ and an arsine ($\mathrm{AsH_3}$) molar fraction of $192\,\mathrm{ppm}$; and 2) a 400-nm-long highly Sn-doped top section is grown for which triethyltin (TESn) with a molar fraction of $16\,\mathrm{ppm}$ is added and the arsine ($\mathrm{AsH_3}$) molar fraction is increased to $577\,\mathrm{ppm}$. Due to the higher V/III ratio during the second growth step, the diffusion length is reduced promoting surface growth resulting in a 10-nm-thick highly doped shell around the undoped part.The final nanowires have a length of about $600\,\mathrm{nm}$, a core diameter of $35\,\mathrm{nm}$ and a shell thickness of about $10\,\mathrm{nm}$.

To define the extension of the top metal contact, and in turn control the gate length (L_{G}), hydrogen silsesquioxane (HSQ) is deposited by spin coating followed by electron-beam exposure and development, where the exposure dose determines the HSQ thickness [10]. Three different exposure doses are utilized, which correspond to gate lengths between $70-200\,\mathrm{nm}$. The top metal is fabricated in two steps; in the first step, $20\,\mathrm{nm}$ of W is sputtered, and in the latter step, $5\,\mathrm{nm}$ of TiN is deposited by atomic layer deposition (ALD). The top metal stack is dry etched anisotropically, leaving metal only on the sides of the nanowires with a planar HSQ surface where all of the metal has been removed. The top contact is finalized with HF etching of the HSQ layer.

A 50-nm-thick ALD $\mathrm{SiO_2}$ is deposited, serving as a first spacer layer. In order to protect the planar film layer, while removing the ALD film deposited on the sides of the nanowire structures, a thin spin-on resist layer is deposited followed by a selective HF etching of $\mathrm{SiO_2}$ around the unprotected nanowires. After removing the resist, only the channel region is revealed, as the bottom part is covered by $\mathrm{SiO_2}$ and the top part by the top metal. The channel region is digitally etched by oxidizing the InAs surface for $10\,\mathrm{min}$ in O_3 at $50\,^\circ\mathrm{C}$, followed by $\mathrm{HCl} : \mathrm{H_2O}$ (1:10) etching for $15\,\mathrm{s}$ to remove the formed oxide. The etch rate of this process has been calibrated to etch $1.7\,\mathrm{nm}$ per etch cycle on each side, as shown in Figure 2. The digital etching is repeated until the highly doped shell is removed and the desired nanowire diameter is reached, resulting in an intrinsic channel region with a diameter of about $28\,\mathrm{nm}$.

A high-κ gate oxide, consisting of a bi-layer of 10 cycles of $\mathrm{Al_2O_3}$ and 40 cycles of $\mathrm{HfO_2}$, is deposited by ALD at $300\,^\circ\mathrm{C}$ and $120\,^\circ\mathrm{C}$, respectively for the two materials. This dielectric has an estimated equivalent oxide thickness (EOT) of $1.5\,\mathrm{nm}$. The gate oxide deposition is followed by the sputtering of a 60-nm-thick W gate metal. An organic second spacer is deposited and followed by the sputtering of the top metal electrode.

III. DC CHARACTERIZATION

The output and transfer characteristics for one of the fabricated transistors can be seen in Figure 3. The device exhibit enhancement mode operation ($V_{\mathrm{T}} = 0.29\,\mathrm{V}$) and combine good on-performance, shown by the peak transconductance (g_{m}) of $0.64\,\mathrm{mS}\,\mu\mathrm{m}^{-1}$, and off-performance, characterized by the minimum sub-threshold swing (SS) of $90\,\mathrm{mV/decade}$. These values yield a transistor $Q = g_{\mathrm{m}}/SS$ of 7.1, which is higher than previously reported performance for vertical nanowire MOSFETs [11], [12]. The good sub-threshold behavior is attributed to the fabrication method, which allows for a close to an intrinsic semiconductor channel without too much degradation of the on-performance. Similar performance is obtained for several devices fabricated in parallel. What is mostly limiting the DC-performance is the relatively high on-resistance (R_{on}) at $1300\,\Omega\,\mu\mathrm{m}$. By comparing DC-measurements when keeping the bottom of the nanowires as ground to measurements when grounding the top, it is established that the majority of the access resistance is situated close to the top of the nanowires.

MOSFETs with other nanowire spacings are also fabricated. A transistor, positioned in a similar array, but with a spacing of $500\,\mathrm{nm}$ is presented in Figure 4. This device shows much improved drain currents (I_{D}) and a peak g_{m} of $1.6\,\mathrm{mS}\,\mu\mathrm{m}^{-1}$ is obtained. The on-performance is boosted by the much lower R_{on} of this device. A possible explanation for the lower on-resistance for this device is partly attributed to a

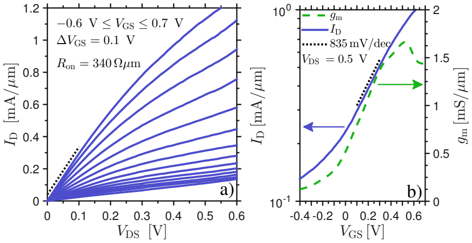

Fig. 4: a) Output and b) transfer characteristics of a nanowire MOSFET with a spacing of $500\,\mathrm{nm}$ between nanowires and $L_{\mathrm{G}} = 120\,\mathrm{nm}$. The nanowires are grounded at the bottom.

shorter gate length but also to a slightly thicker shell ($\approx 1\,\mathrm{nm}$) for the 500-nm-spaced nanowires and a higher doping-level of the overgrown shell, allowing for lower resistance in the semiconductor and lower metal-semiconductor contact resistance. The sub-threshold characteristics, Figure 4b), is, however, severely degraded. The changed characteristics is attributed to the nanowire spacing-dependent HSQ thickness during device fabrication. With a wider spacing, the film is thinner and the top metal edge is positioned lower and closer to the foot of the nanowire. This foot has a thicker shell, which is insufficiently etched during the digital shell etching. With a gate positioned in this region, a highly doped shell still remains, resulting in poor off-characteristics and partly contributing to a lower on-resistance. By optimization of the contact process scheme, the nanowire geometry and the processing conditions, it is expected that the transistor performance may be further improved.

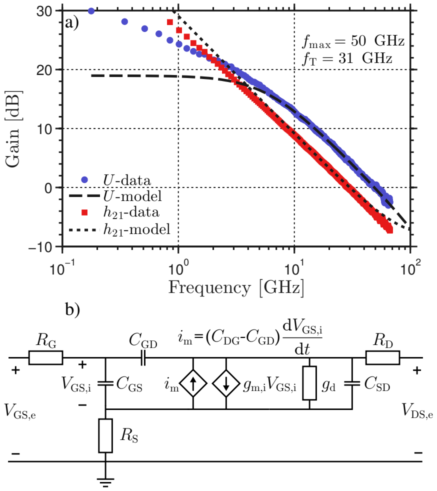

Fig. 5: a) Measured current gain and unilateral power gain as a function of frequency together with an applied small-signal model. The device is measured at $V_{\mathrm{DS}} = 0.5\,\mathrm{V}$, $V_{\mathrm{GS}} = 0.4\,\mathrm{V}$. b) Circuit diagram of the small-signal model used to characterize the measured RF data.

In order to study a possible improvement of the sub-threshold characteristics with annealing, the transistors are annealed at temperatures between $250\,°\mathrm{C}$ and $330\,°\mathrm{C}$. However, no SS improvement is observed, while instead a degradation of the top contact is measured, verifying the stability of the contact as one main limiting factor for the transistor performance.

IV. RF CHARACTERIZATION

To validate the transistor geometry, a 200-nm-spaced transistor is characterized at radio frequencies by vector network analyzer measurements of the transistor S-parameters. After de-embedding of the contacting pads, the unilateral power gain (U) and the current gain (h_{21}) are calculated and presented as a function of frequency in Figure 5a). The maximum oscillation frequency (f_{max}) and transition frequency (f_{T}) are found to be $50\,\mathrm{GHz}$ and $31\,\mathrm{GHz}$, respectively. These values are comparable to what has previously been reported for vertical nanowire MOSFETs of similar electrode configuration [13], [14]. In order to determine the limiting factors of the high-frequency performance, the small signal model from Figure 5b), is applied to the measured data, with the corresponding extracted values given in Table I. Especially noteworthy is the large gate-source capacitance (C_{GS}), originating from a large overlap area between the gate electrode and the InAs epitaxial layer, and a too thin bottom spacer layer.

TABLE I: Extracted parameter values used in the small signal model of Figure 5b)

R_{G}	R_{D}	R_{S}	$g_{\mathrm{m,i}}$	g_{d}	g_{GD}
$4\,\Omega$	$14\,\Omega$	$7\,\Omega$	$71\,\mathrm{mS}$	$5\,\mathrm{mS}$	$0.1\,\mathrm{mS}$
C_{GS}	C_{GD}	C_{DG}	C_{SD}		
$310\,\mathrm{fF}$	$15\,\mathrm{fF}$	$6\,\mathrm{fF}$	$5\,\mathrm{fF}$		

V. CONCLUSION

In this work, vertical nanowire MOSFETs fabricated using a new self-aligned gate-last process are realized. Using this process, the best combined performance of on- and off-performance for any vertical nanowire MOSFET is obtained. By analysis of the device performance, contact resistances at the top of the nanowires and parasitic capacitances between gate and source are found to be the limiting properties of the device. By improvements of these extrinsic parasitics, competitive DC- and RF-performance is expected.

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Paper II

A transmission line method for evaluation of vertical InAs nanowire contacts

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In this paper, we present a method for contact characterization to vertical nanowires using the transmission line method (TLM) on a cylindrical geometry. InAs nanowire resistors are fabricated on Si substrates using a hydrogen silsesquioxane (HSQ) spacer between the bottom and top contact. The thickness of the HSQ is defined by the dose of an electron beam lithography step and by varying the separation thickness for a group of resistors, a TLM series is fabricated. Using this method, the resistivity and specific contact resistance is determined for InAs nanowires with different doping and annealing conditions. The contacts are shown to improve with annealing at temperatures up to 300 °C for 1 min, with specific contact resistance values reaching down to below 1 Ω µm^2.

PACS numbers: 73
Keywords: Nanowires, Contacts, TLM, transmission line model, Nickel, Ni, InAs, Vertical

Extrinsic resistances degrade the performance for any electronic or optoelectronic device. For metal-oxide-semiconductor field-effect transistor (MOSFET), especially the on-current and transconductance are sensitive, which in turn reduces the energy efficiency and operational frequency of the device[1]. It has been estimated that the optimization of these extrinsic resistances might be more important than that of the intrinsic device performance[2]. For future technology nodes, vertical nanowire-based MOSFETs are of interest since they allow for longer contact regions, and therefore smaller contact resistances, without impacting the footprint area of the device compared to conventional lateral devices. They have also been show to offer good scalability and performance for the 7 nm node and beyond[3]. Available methods to characterize metal-semiconductor contacts to nanowires requires breaking the nanowires off and from these, fabricate resistors to determine the contact properties[4–6]. However, the results from these methods might not be applicable to the actual vertical nanowire devices as the contact processing techniques differ. Furthermore, the procedure is time consuming as each device is aligned manually keeping fabrication volumes small and statistical analysis an extensive task. In this paper, we propose and demonstrate a characterization method for the specific contact resistance between a semiconductor nanowire and a metal contact adopting the standard transmission line method[7] (TLM) in a vertical geometry. The proposed method is easily implemented into the process flow of any vertical nanowire devices, e.g. MOSFETs, for on-chip quality control or characterization of the extrinsic access resistances.

A schematic illustration of a vertical nanowire resistor can be seen in Fig. 1a). The resistors are fabricated on substrates consisting of a 300-nm-thick InAs epitaxial layer grown on a silicon wafer[8]. This highly doped epitaxial layer serves both as buffer layer for nanowire growth, and as low-resistance contacts to the nanowires avoiding transport across the Si/InAs heterojunction[9]. The InAs nanowires are grown from gold seed particles, de-

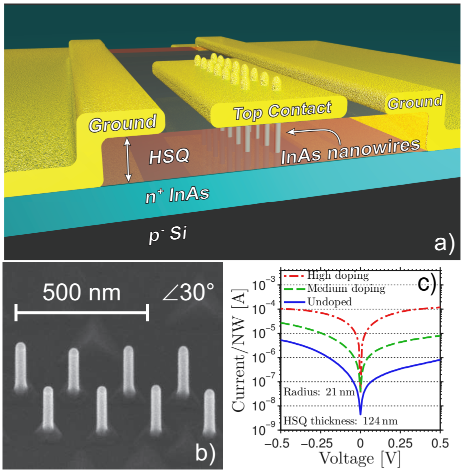

FIG. 1. a) Schematic illustration of a fabricated nanowire resistor consisting of several nanowires in parallel. b) SEM image (tilted by 30°) of a nanowire array placed in an equilateral zigzag stripe arrays. c) *I*-*V* characteristics of three devices with different doping and the same HSQ thickness (124 nm). The bias is applied at the top of the nanowire with the bottom contact set as ground.

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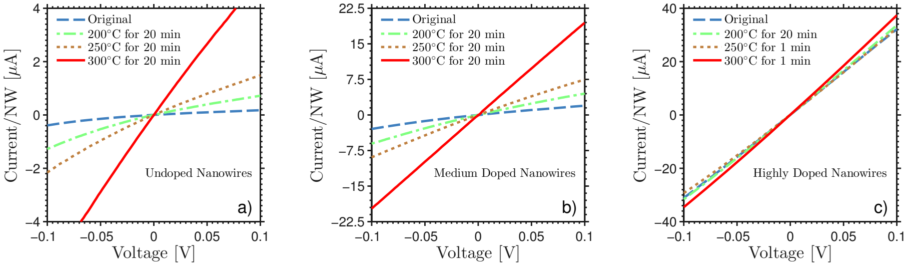

FIG. 2. The effect of annealing in N_2 of a) undoped nanowires, b) medium doped nanowires, c) highly doped nanowires for devices with an HSQ thickness of 124 nm. In all steps the resistance decreases and a more linear behavior is observed.

fined using an electron beam-defined lift-off process. The seed particles are positioned in equilateral zigzag stripe arrays with a spacing of 200 nm. Growth is performed using metalorganic vapor phase epitaxy (MOVPE) for 400 s at 420 °C with a trimethylindium (TMIn) molar fraction of 2.79 ppm and an arsine (AsH_3) molar fraction of 192 ppm. The electron beam-controlled nanowire radii ranges between 12 nm and 23 nm corresponding to lengths of 1020 nm and 200 nm, respectively. Three samples are grown with different Sn doping flows corresponding to Sn/In molar fractions of 0, 0.14 and 0.63 corresponding to carrier concentrations of $2 \times 10^{16}\,\mathrm{cm}^{-3}$, $1 \times 10^{18}\,\mathrm{cm}^{-3}$, and $6 \times 10^{18}\,\mathrm{cm}^{-3}$ respectively, as obtained from field-effect mobilities of back-gated lateral nanowire MOSFETs. A scanning electron micrograph (SEM) for one of the grown nanowire arrays can be seen in Fig. 1b). A spacer is formed using an electron beam exposed hydrogen silsesquioxane (HSQ) to transform the film into SiO_2[10]. The HSQ is developed in concentrated tetramethylammonium hydroxide (TMAH) for 60 s followed by water rinsing. The thickness of the SiO_2 is controlled by the exposure dose, which is varied to form thicknesses from 50 nm to 400 nm. After development, the HSQ is baked at 350 °C for 20 min. Prior to top metal deposition, the nanowires are etched using $HCl : H_2O$ (1:10) for 30 s. A top metal contact consisting of Ni, W, and Au (15 nm, 30 nm, 200 nm) is sputtered, with only Ni being in direct contact with the semiconductor. The metal is patterned using photolithography; the Au is etched using a KI-based wet etchant, the W is dry etched using an SF_6/Ar reactive ion etch (RIE), and finally Ni is wet etched using $CH_3COOH : H_2SO_4 : HNO_3 : H_2O$ (1:2.5:2.5:15).

The fabricated resistors are electrically characterized by two terminal *I*-*V* DC measurements, where the resistances are evaluated at 0 V. In our vertical TLM analysis, the contact separation corresponds to the HSQ thickness that is varied systematically. This thickness is measured using spectral reflectance and confirmed using both atomic force microscopy (AFM) and cross-sectional SEM.

The measured *I*-*V* characteristics for three devices with different doping levels but the same HSQ thickness are shown in Fig. 1c). From these curves it is evident that the different doping conditions used have a great impact on the resistance in the devices, as expected. The highly doped sample exhibits ohmic behavior, whereas a slight asymmetry is observed for medium and undoped nanowires. It indicates a potential barrier related to either the Ni/InAs interface or the HSQ separation layer.

Annealing the samples improves the ohmic behavior, Fig. 2a-c). The effect of annealing, as expected, is strongest for the undoped nanowires (Fig. 2a) where the current increases by more than a factor of 20 with the curve shape approaching a perfectly linear characteristic. Similar improvement is seen for the other two doping levels (Fig. 2b-c) as well, although to a lesser extent.

The total resistance is modeled as two series elements, a nanowire resistance (R_{NW}) and a distributed contact resistance (R_{C})[4]. The nanowire resistance is modeled to have a uniform resistivity in a cylindrical geometry, Eq. (1) and the contact resistance is modeled as a distributed resistive network, with its corresponding

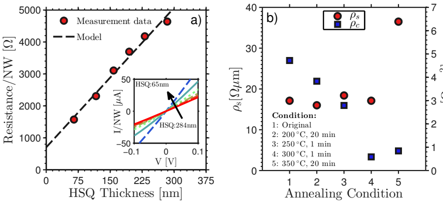

FIG. 3. a) Resistance as a function of the contact separation for highly doped nanowires with a radius of 19 nm, which have been annealed at 200 °C for 20 min. From the model ρ_s and ρ_c are found to be $16\,\Omega\,\mu\mathrm{m}$ and $3.8\,\Omega\,\mu\mathrm{m}^2$ respectively. These values correspond to a transfer length of 47 nm. The *I*-*V* characteristics of the TLM series are presented in the inset. b) Determined ρ_s and ρ_c for the same TLM series subjected to different annealing conditions.

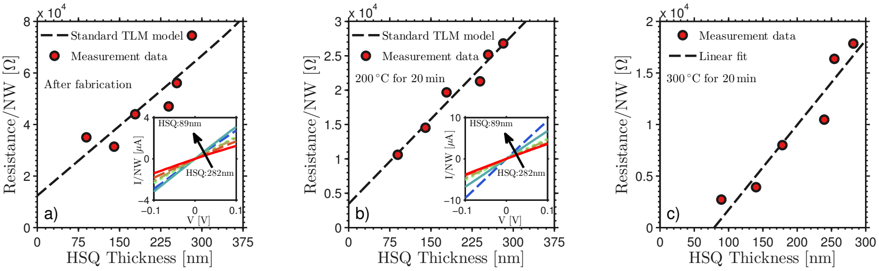

FIG. 4. Resistance as a function of the contact separation for lightly doped nanowires with a radius of 16 nm. a) The measured data directly after device fabrication. Here, a ρ_s of 138 Ω µm and a ρ_c of 84 Ω µm^2 are determined. b) Data measured after a 200 °C annealing in N$_2$. From the standard TLM model, ρ_s and ρ_c are found to be 63 Ω µm and 14 Ω µm^2 respectively. c) Data measured after 300 °C annealing. A linear slope corresponding to a resistivity of 63 Ω µm is observed with an intersection with the resistance axis at negative values.

lumped resistance can be expressed as Eq. (2). The model can be applied to the measurement data by least-square fitting of the nanowire resistivity (ρ_s) and the metal-semiconductor transfer length (L_T). From these parameters, the specific contact resistance (ρ_c) can be calculated using Eq. (3).

$$R_{\mathrm{NW}} = \frac{\rho_s L_{\mathrm{HSQ}}}{\pi r^2} \tag{1}$$

$$R_C = \frac{\rho_s L_T}{\pi r^2}\coth\left(\frac{L_{\mathrm{NW}} - L_{\mathrm{HSQ}}}{L_T}\right) = $$

$$= [L_T \ll (L_{\mathrm{NW}} - L_{\mathrm{HSQ}})] = \frac{\rho_s L_T}{\pi r^2} \tag{2}$$

$$\rho_c = \frac{2L_T^2 \rho_s}{r}. \tag{3}$$

Here, L_{HSQ} is the HSQ thickness, r is the nanowire radius, and L_{NW} is the total length of the nanowires. A uniform resistivity and current distribution in the uncontacted nanowire section is assumed. These assumptions should be valid for a highly doped nanowire with a transfer length equal to, or larger than, the nanowire radius.

The TLM series for nanowires with the highest estimated doping and a nanowire radius of 19 nm can be seen in Fig. 3a). The model reproduces the measurement data well. With a determined ρ_s of 16 Ω µm it corresponds well to what has previously been observed from two-terminal InAs nanowires[11]. The transfer length is found to be 47 nm with ρ_c calculated to 3.8 Ω µm^2. The same TLM series is subjected to different annealing conditions with the corresponding ρ_s and ρ_c shown in Fig. 3b). The nanowire resistivity is constant for all conditions. In contrast, the specific contact resistance is decreased significantly after annealing. This decrease can be attributed to in-diffusion of Ni into the nanowire crystal forming a Ni-InAs alloy[6,12,13]. This results in a local lowering of the nanowire resistivity and improvement of the metal contact. The lowest achieved ρ_c of 0.6 Ω µm^2 is comparable to what has previously been achieved with in-diffused Ni contacts to InAs planar surfaces[12]. According to ITRS, this ρ_c is the target value for MOSFETs with a physical gate length of 14 nm estimated for the year 2017[14]. The samples are also annealed at 350 °C, keeping the contact properties while the resistivity is degraded. This is similar to[12], where a sharp sheet resistance increase at 400 °C is observed for a Ni-InAs layer.

Contact improvements with annealing can also be seen for the medium doped sample. The data measured directly after fabrication, shown in Fig. 4a), exhibit a scattered behavior, originating from the non-linear I-V characteristics. TLM analysis gives a high ρ_s of 138 Ω µm and ρ_c of 84 Ω µm^2. However, after N$_2$ annealing at 200 °C, a much clearer linear dependence is observed (Fig. 4b) with a ρ_s of 62.9 Ω µm and a ρ_c of 14.2 Ω µm^2 determined. Both these values are about a factor of four higher than what is observed for the highly doped nanowires with similar radii, in good agreement with the different carrier concentrations. After annealing at even higher temperatures, the linear trend is discerned, as shown in Fig. 4c), with a slope indicating an unchanged ρ_s of

TABLE I. Summary from TLM analysis for highly and medium doped nanowires with different diameters and annealing conditions.

Doping	r [nm]	Annealing	ρ_s [Ωµm]	ρ_c [Ωµm^2]	L_T [nm]
High	19	None	17	4.7	53
High	19	300 °C, 1 min	17	0.6	18
High	16	None	24	< 2.3[a]	< 28[a]
High	16	250 °C, 1 min	20	1.2	21
Medium	19	250 °C, 20 min	52	69	118
Medium	18	250 °C, 20 min	69	37	74
Medium	16	None	140	83	68
Medium	16	200 °C, 20 min	63	14	42

[a] Value too small to be accurately determined.

62.9 Ω µm. By applying the standard TLM model, the line would intersect the resistance axis at negative values. One probable explanation is in-diffusion of Ni during this extended annealing time, forming a low-ohmic region[5,6,15] and thus reducing the effective length. To confirm this, more points would be needed at thinner HSQ thicknesses. The same findings are observed for the undoped nanowires with identical annealing conditions. A summary for the TLM analysis can be seen in Table I. Thinner nanowires generally have higher ρ_s, possibly due to larger degree of surface scattering. Annealing is shown to improve both the contacts and the resistivity. No reliable data could be determined from undoped nanowires, which suffer from less linear I-V characteristics and increased sensitivity to surface conditions

In this work, we have in summary successfully implemented a method to characterize resistivity and specific contact resistance for vertically aligned nanowires by applying a standard transmission line method in a cylindrical geometry. Using this method, sputtered Ni contacts to InAs nanowires with hydrogen silsesquioxane separation layers are studied for various doping levels. The contacts are shown to be improved with annealing at temperatures below 300 °C and specific contact resistances below 1 Ω µm^2 are demonstrated for highly doped nanowires.

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Paper III

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InAs nanowire MOSFETs in three-transistor configurations: single balanced RF down-conversion mixers

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Abstract
Integration of III–V semiconductors on Si substrates allows for the realization of high-performance, low power III–V electronics on the Si-platform. In this work, we demonstrate the implementation of single balanced down-conversion mixer circuits, fabricated using vertically aligned InAs nanowire devices on Si. A thin, highly doped InAs buffer layer has been introduced to reduce the access resistance and serve as a bottom electrode. Low-frequency voltage conversion gain is measured up to 7 dB for a supply voltage of 1.5V. Operation of these mixers extends into the GHz regime with a –3 dB cut-off frequency of 2 GHz, limited by the optical lithography system used. The circuit dc power consumption is measured at 3.9 mW.

Keywords: nanowire, InAs, mixer, MOSFET, circuit, differential

(Some figures may appear in colour only in the online journal)

1. Introduction

Mixers are a fundamental part of the RF front end and are used in order to down-convert a radio frequency (RF) input to an intermediate frequency (IF), containing the transmitted information. A large transconductance on the input stage and well-behaved transistor output characteristics are desired to get a large circuit gain. III–V semiconductors are considered as emerging channel materials in Si-based electronics [1–5]. III–V channels have been demonstrated with advantageous transport properties [6] and recent studies concerning both low-frequency and high-frequency noise suggest that noise levels are competitive with Si-technology [7, 8]. The good electrostatic control in cylindrical geometries makes III–V nanowires attractive for low power, high performance mixers and other analogue circuits [9, 10]. Furthermore, by using a vertical nanowire geometry [11–14], the dependency between the device footprint area and the gate length, L_G, is de-coupled, thus allowing for a higher degree of freedom during device optimization.

To demonstrate the use of nanowire-based InAs MOSFETs in future Si-based RF applications, an active single balanced down-conversion mixer has been implemented as it includes both a transducer stage and a mixing stage, where both conductance and frequency properties are of high importance [15]. A circuit diagram of the implemented circuit can be seen in figure 1 together with simulations of the associated sine-wave signals at the corresponding input and output nodes. The mixer input senses the RF-signal, v_{RF}, at the gate of transistor M_1. The local oscillator (LO) signal, v_{LO}, is applied to the gates of transistors M_2 and M_3, after a power split with a phase shift of 180° between the signals reaching the left and right device. The down-conversion of the RF-signal is performed by the multiplication of the input signal and the LO signals at the M_2 and M_3 stages, which are ideally alternatingly switched fully on and off in each cycle using a large-amplitude v_{LO}. The generated signals on the output are multiples of the sum and difference between the RF and LO frequencies, $f_{RF} \pm f_{LO}$. The differential output is defined as the difference between the voltages of the two IF ports, v_{IF+} and v_{IF-}. A differential implementation as selected here reduces common mode signals such as RF leakage.

For the implementation, we used InAs MOSFETs integrated on Si substrates with vertically aligned nanowire

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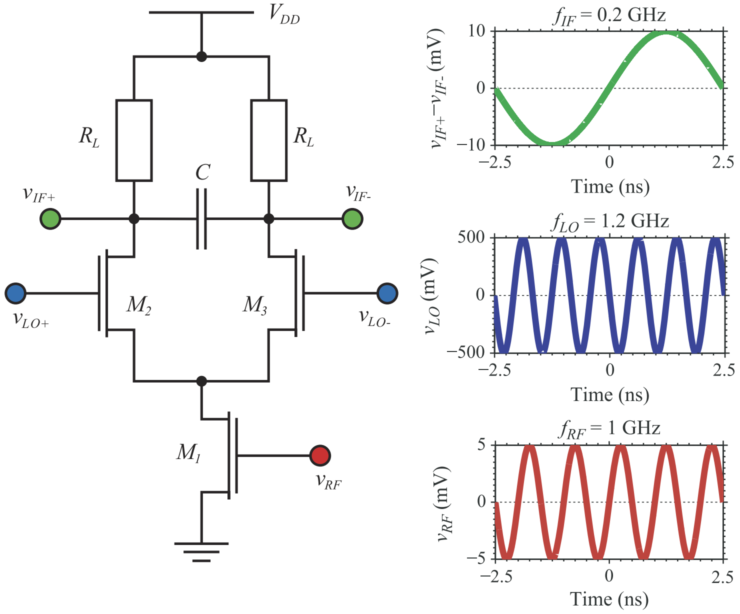

Figure 1. The circuit diagram of a single balanced down-conversion mixer with the corresponding port ac signals in the time domain. The shown signals are simulated but correspond in amplitude to the applied and measured signals. The high-order mixer products are omitted from the IF signal. Here, C is the parallel-plate capacitance, R_L is the load resistances, and V_{DD} is the supply voltage.

channels that have been demonstrated with a transconductance, g_m, normalized to the circumference of 1.36 mS μm^{-1} at a drain-source voltage, V_{DS}, of 0.5 V [12] with RF performance, showing unity transducer gain above 100 GHz [14]. Characterization of the fabricated circuits show attractive low-frequency gain in the GHz regime with a high yield of the transistor process.

2. Methods

2.1. Device fabrication

The fabricated mixers contain three nanowire-based MOSFETs as active devices, two nanowire-based resistors as load resistors, and one parallel-plate capacitor acting as a low-pass filter.

MOSFET fabrication is initiated with the placement of Au seed particles on a substrate consisting of 300 nm-thick epitaxially grown InAs layer on highly resistive Si (111)-substrate with sample sizes of 2×2 cm^2 [16]. This is accomplished using electron-beam lithography with a PMMA bi-layer photoresist followed by evaporation of 15 nm gold and lift-off. The substrate is consequently cleaved into four equally big pieces with sizes of 1×1 cm^2. The seed particles, placed in equilateral zigzag stripe arrays, are catalysts for the growth of InAs nanowires with diameters, controlled by the size of seeds, typically about 35 nm. The length of the nanowires is aimed at 600 nm to be able to fit all of the different contact layers. The nanowires are grown using metalorganic vapor phase epitaxy, with the planar InAs layer as a buffer layer. The InAs nanowires are subsequently covered by a high-κ bi-layer dielectric, consisting of 10 cycles of Al_2O_3 deposited at 250 °C and 50 cycles of HfO_2 deposited at 100 °C, using atomic layer deposition. The total dielectric thickness is 5.5 nm corresponding to an effective oxide thickness of 1.5 nm.

Aside from serving as a buffer layer for nanowire growth, the InAs epitaxial layer is also used as an n-type interconnecting layer with a sheet resistance of $6\ \Omega/\square$ and a mean carrier concentration of 5×10^{18} cm^{-3}. In order to electrically isolate different devices, the InAs layer is masked by a photoresist, and the covering high-κ is etched by buffered oxide etch (BOE), and the InAs layer is finally transformed into mesa structures by a wet etch procedure using H_3PO_4: H_2O_2: H_2O (1 : 1 : 25). For the isolation between source and gate, a 60 nm-thick Si_3N_4 film, deposited by plasma enhanced chemical vapor deposition, is used. In order to preserve the planar Si_3N_4 film, while removing the Si_3N_4 covering the nanowire sidewalls, an organic spacer is applied and thinned down by O_2-plasma, followed by Si_3N_4 dry etching using reactive ion etching (RIE) with a gas mixture of

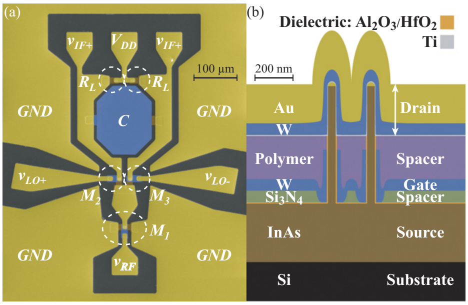

Figure 2. (a) A Scanning electron micrograph of a fabricated mixer circuit showing the location of the active and passive devices as well as the input and output ports. (b) A schematic cross-section of a fabricated vertical InAs nanowire MOSFET, showing the different metal and separation layers.

SF_6 and Ar. Sputtering of a 60 nm-thick W film is used to form the gate metal. The gates are isolated between devices by masking and etching of W using heated H_2O_2. The gate length is defined in a similar way as the first separation layer by spinning on and thinning down an organic spacer to serve as an etch mask. The gate metal on the nanowire sidewalls is etched by the same RIE etchant as was used to etch the Si_3N_4 film. The characterized devices have L_G defined to about 200 nm. For the isolation layer between gate and drain, an organic spacer is spun on, baked, and thinned down such that the top of the nanowires are sticking up while the gate metal is sufficiently below the polymer surface. Before the sputtering of the top metal, via holes are formed down to the InAs layer and to the gate metal layer, followed by etching of the high-κ dielectric at the top of the nanowires. The top metal stack consists of Ti, W, and Au with thicknesses of 5, 60, and 200 nm, respectively. After patterning of the top metal stack, the metals are etched in turn: Au is etched by a KI-based wet etch, the W is etched by the same dry etch procedure used to define the gate length, and Ti is etched by BOE.

The nanowire-based resistors are fabricated using the same fabrication techniques used for the MOSFET, albeit with all of the gate metal removed during the formation of the MOSFET gate metal pad. Parallel-plate capacitors are formed between the InAs planar layer and the gate metal layer with a dielectric film consisting of a thin high-κ dielectric and a 60 nm-thick Si_3N_4 film. Measurements show that these capacitors have a weak voltage dependence in the 1 V bias range and show a normalized capacitance of 113 nF cm^{-1}, corresponding to an effective relative permittivity of 8.26. All lithography used in the fabrication processes, except the definition of the nanowire seed particles, is performed by ultraviolet lithography with a minimum feature size of a few μm. The scanning electron micrograph in figure 2(a) shows one of the fabricated circuits and a schematic cross-section of a vertical nanowire MOSFET is shown in figure 2(b).

2.2. Measurement details

Characterization of the single balanced down-conversion mixer circuits is performed using an Agilent E8361A network analyzer as a source to the mixer input and using a Rohde and Schwarz FSU spectrum analyzer to measure the output power. A differential voltage buffer is connected between the mixer output nodes and the spectrum analyzer in order not to load the mixer with the instrument port impedance of 50 Ω. The switching of the LO devices is carried out by an Agilent 8257D signal generator. The scattering parameters are measured at the RF input of the mixer in order to determine the delivered power to the gate of transistor M_1, and thereby calculate the ac voltage at the mixer input. To determine the voltage conversion gain, G_{VC}, the measured output power of the buffer stage is recalculated to a voltage where the output of the buffer is matched to 50 Ω. The performance of the MOSFET devices is characterized in dc using a Keithley 4200 parameter analyzer. The same devices are also characterized at radio frequencies using an Agilent E8361A network analyzer.

3. Results and discussion

3.1. MOSFET dc characterization

The output and transfer characteristics for one of the individual transistors are shown in figure 3(a). The maximum transconductance, at a V_{DS} of 0.5 V, is found to be 0.27 mS μm^{-1}, which is comparable to previous implementations and limited by the series resistance, found primarily in the top part of the nanowires [12]. The performance of the individual transistors is comparable to the active devices in the mixer circuits. The transfer characteristics of one mixer RF-input device is shown in figure 3(a). The difference in the normalized transconductance (25%) may be attributed to a small deviation in the nanowire diameter.

The output characteristics for all three active devices in a mixer circuit are shown in figure 3(b). The devices exhibit good saturation behavior for low overdrive voltages, V_{GS}–V_T, but the performance deteriorates at higher biases due to parasitic resistances in the order of 1–10 k$\Omega\,\mu$m. Some mismatch in g_m, I_{DS} and subthreshold characteristics is observed between transistors M_2 and M_3. In terms of circuit performance, this mismatch could lead to increased LO to RF leakage [17] as well as reduced common-mode rejection ratio.

3.2. Mixers

The single balanced down-conversion mixers are characterized in terms of frequency behavior and linearity. To study the frequency behavior, the voltage conversion gain as a function of RF-frequency is measured. This is done for three different fabricated circuits, all with the three active devices in the mixers consisting of arrays of 500 nanowires. The results can be seen in figure 4(a). Here, the IF-frequency is kept constant at 100 kHz and V_{DD} is set to 1.5 V. The input power is kept at –34 dBm to ensure linear operation and the switching power of

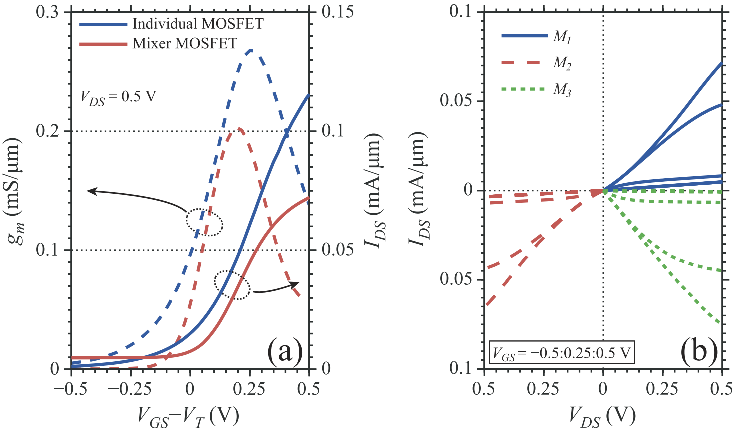

Figure 3. (a) The transfer characteristics and transconductances at a V_{DS} of 0.5 V, for two MOSFETs; one for an individual transistor and one MOSFET included in a mixer circuit. Both metrics are normalized to the number of wires and the circumference of the nanowire. (b) Output characteristics for three MOSFETs included in the same mixer circuit with V_{GS} of 0.5 V to –0.5 V with steps 0.25 V. Note that all axis limits are positive to display the transistor symmetry in the same graph.

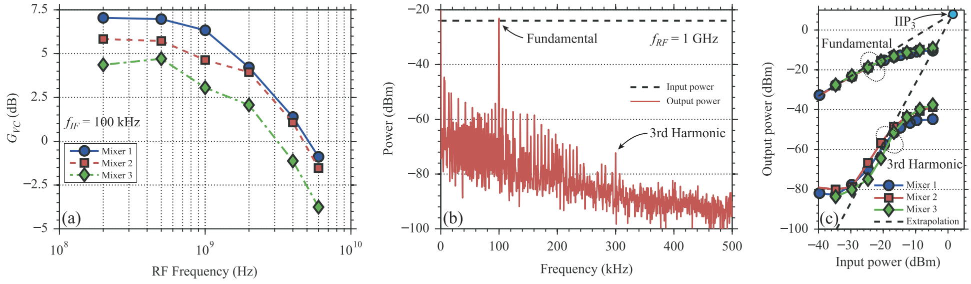

Figure 4. (a) The voltage conversion gain of a single balanced down-conversion mixer as a function of frequency for three separate circuits, at a supply voltage of 1.5 V, an RF input power of –34 dBm, and a LO switching power of –3 dBm. (b) Measured output spectrum of a mixer circuit at a constant input power. (c) The output power of the same three mixers as a function of input power at the fundamental frequency and its third-order harmonic. Also shown is the intersection between the extrapolation of power characteristics at the fundamental frequency and its third-order harmonic, from their linear regimes.

transistors M_2 and M_3 are held at –3 dBm to properly switch the devices on and off. The highest G_{VC} measured is 7 dB, with a $f_{3\ dB}$ of 2 GHz and a unity gain frequency, $f_{0\ dB}$, of 5 GHz at a dc power consumption of about 3.9 mW. The three mixer circuits show simiar cut-off frequencies but some dissimilarities in the low-frequency gains. These dissimilarities originate from process variations in the transconductance of transistor M_1 and in the load resistances.

Besides measuring the amplitude of the down conversion mixing product at the fundamental frequency peak, it is important to determine the amplitudes of the higher order harmonic peaks that are also generated during frequency mixing. A spectrum of the measured power at the differential output port for a fixed input power is displayed in figure 4(b). Seen in the figure are both the peaks corresponding to the fundamental frequency at 100 kHz and its third order harmonic at 300 kHz. A single tone test is used to determine the linearity of the output power as a function of the input power. The power level of the harmonic signals differ a factor of 3 from a third-order intermodulated signals [17].

Measured data sets of the same three mixer circuits of figure 4(a) are shown in figure 4(c). In these measurements, f_{IF} and f_{RF} are kept constant at 100 kHz and 1 GHz, respectively. Both the power at the fundamental frequency and its third-order harmonic are shown together with the extrapolations in the linear and cubic regime, respectively. The two mixing products are extrapolated to cross at the input intercept point, IIP_3, which is found to be at an input power of 1.8 dBm. Another important figure of merit is the 1 dB compression point, $P_{in,1\ dB}$, describing the highest level of input power where linear gain is achieved. It is determined that $P_{in,1\ dB}$ have a value of –21 dBm at the fundamental

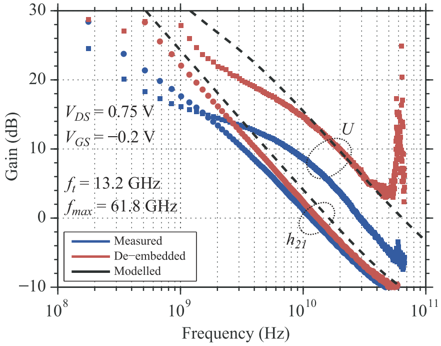

Figure 5. The current gain and unilateral power gain as a function of frequency for an individual nanowire MOSFET at a biasing of $V_{DS} = 0.75$ V and $V_{GS} = -0.2$ V. Three separate lines are shown for each quantity; the measured characteristics (blue), the de-embedded characteristics (red), and the modelled characteristics (black).

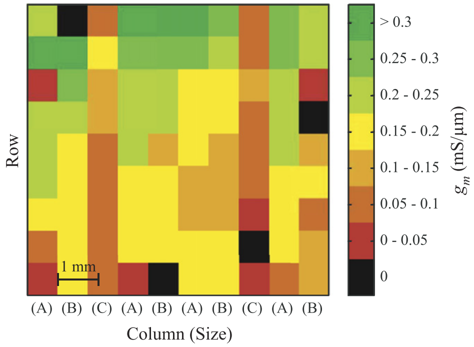

Figure 6. Transconductance variation across the sample presented as a color map. Device footprint area is varied with the columns for three different types: A, B, and C; corresponding to device areas of 12 × 12 μm^2, 8 × 8 μm^2, 5 × 5 μm^2, respectively.

frequency. The low value for $P_{\text{in},1\text{ dB}}$ is attributed to the sharp g_{m} peak of the RF transistor, originating from large series resistances in the nanowires on the drain side of each MOSFET, thus the compression is referred to the input [15].

3.3. MOSFET RF characterization

The frequency behavior of the mixer circuits can be compared to the RF characteristics of the active devices. In figure 5, the unilateral power gain, U, and the current gain h_{21}, are plotted as a function of frequency for the same individual device as shown in figure 3. The maximum oscillation frequency, $f_{\max}$, and the unity transducer gain frequency, f_{t}, is found to be 29.0 GHz and 11.5 GHz, respectively. By de-embedding the contributions of the parasitic elements from external sources, these values are instead extracted to about 61.8 GHz for $f_{\max}$ and 13.2 GHz for f_{t}, which are among the highest values we have reported [12, 14]. A small signal model [13] is fitted to the de-embedded curves and $g_{\text{m,RF}}$ is found to be 0.26 mS μm^{-1}, which is close to what is obtained from dc measurements. The high-frequency performance of the MOSFETs is in this implementation found to be limited by the parasitic overlap capacitance between gate and source,C_{GS} [12].

For the circuits, the G_{VC} roll-off occurs at lower frequencies than what is observed for the unilateral power gain of individual MOSFETs, as seen in figure 5. Here, the main roll-off occurs at about 11 GHz. Part of the discrepancy between the mixer and the MOSFET performance is attributed to increased parasitic capacitances originating from transistors M_2 and M_3, as well as some expected wiring capacitance. Another cause is inter-device current leakage through the silicon substrate, on the order of a few μA, which effectively increases the output conductance and increases the off-state current of the switching devices, thus reducing both G_{VC} and $f_{0\text{ dB}}$.

3.4. Performance variations

To evaluate the process stability, we have mapped the wafer uniformity on the transistor level to verify that a sufficiently high yield for circuit implementation may be obtained. Individual transistors as well as the active devices in each mixer have been characterized and the maximum g_{m} has been extracted. Figure 6 shows a map of g_{m} for 90 devices distributed uniformly across the 1 × 1 cm^2 sample. The fabricated overlap area between the source, gate and drain electrodes are varied across the sample with three sizes being used: 12 × 12 μm^2 (type A), 8 × 8 μm^2 (type B), 5 × 5 μm^2 (type C). It is evident that two of the columns, both of the type C, display a lower transconductance than the rest. This is explained by the smaller device footprint area on those columns where the technology is limited by the resolution of the optical lithography process used. The yield is determined for the three different device footprint areas (types A, B, and C) on the sample. For this purpose, a functioning device is defined as having a maximum g_{m} higher than 0.1 mS μm^{-1} and the yields are found to be 86%, 86% and 22% for the three device sizes (A, B, and C), respectively. It can also be observed that the top rows exhibit better performance than the lower part of the sample attribute to non-uniformities in the spin-coating of the resists used.

4. Conclusions

In this work we have successfully integrated vertically aligned InAs nanowire MOSFETs in single balanced down-conversion mixer circuits. This is achieved by the development of a high-yield and stable fabrication methodology for vertical InAs MOSFETs on a silicon substrate where nanowires serve as both active devices and resistors. The fabricated mixer circuits show a low frequency voltage conversion gain of up to 7 dB and a unity gain frequency of 5 GHz while consuming 3.9 mW of power. Similar performance is achieved for several mixer circuits. The basis for the mixer performance is improved transistor performance concerning both channel saturation and high frequency behavior compared to previously reported device characteristics.

Acknowledgments

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Paper IV

InAs nanowire MOSFET differential active mixer on Si-substrate

K.-M. Persson, M. Berg, H. Sjöland, E. Lind and
L.-E. Wernersson

An active single balanced down-conversion mixer is implemented using InAs nanowire metal oxide semiconductor field effect transistors (MOSFETs) as both active devices and passive resistive loads. Circuits with 6 dB low-frequency voltage gain and a 3 dB bandwidth of 2 GHz are measured for a DC power consumption of 3.8 mW from a 1.5 V supply. The circuits are fabricated using contacts made with 12 µm-line-width optical lithography.

Introduction: The introduction of III–V channel materials offers the possibility for faster switching speeds at reduced power consumption as compared to Si-based CMOS devices [1, 2]. To maintain electrostatic control at scaled gate lengths, the nanowire (NW) metal oxide semiconductor field effect transistor (MOSFET) is arguably the most promising candidate [3]. Vertical NW MOSFETs are predicted to have excellent high-frequency performance [2] and they can be grown on Si substrates using a thin buffer [4]. We have previously reported the performance of InAs NW MOSFETs (NW-FETs) on Si with a transconductance, g_m, of 1.36 mS/µm, at a drain–source voltage, V_{DS}, of 0.5 V [5]. To demonstrate circuit feasibility of InAs NW-FETs, we have implemented a single balanced down-conversion mixer using three gated NW devices (M_1, M_2 and M_3). Measured data show a low-frequency voltage gain, $G_{VC,low-f}$, of 6 dB, a 3 dB bandwidth (BW), $f_{RF,BW-3\,dB}$, of 2 GHz and a unity voltage gain at 5 GHz, adding further circuit capabilities for NWs [6–8].

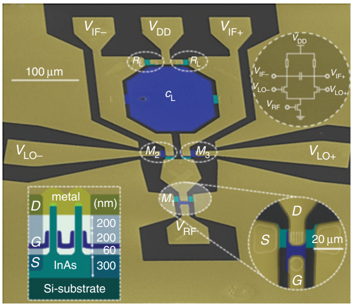

Fig. 1 *Scanning electron microscopy image of fabricated circuit, with insets of magnified image of contact pads, as well as schematics of device and circuit layout*

Supply terminal, V_{DD}, inputs, v_{RF}, v_{LO-} and v_{LO+}, and outputs, v_{IF-} and v_{IF+}, are indicated. Large blue coloured area is load capacitor, C_L

Fabrication: Mixer circuits are fabricated side-by-side on 1 × 1 cm^2 samples. N-type InAs NWs are initially grown on InAs buffer layers (300 nm thick) on 2 × 2 cm^2 Si substrates, which are cleaved after growth. The InAs buffer layer mitigates the growth [5] and is doped to a level of $N_D = 2 \times 10^{19}$ cm^{-3} (corresponding to a sheet resistance of 6 Ω/□), in order to reduce the NW-FET source access resistance. Arrays of NWs are defined using electron-beam-lithography with controlled position and size of gold catalyst particles. The NWs are grown by metal-organic vapour-phase epitaxy (MOVPE) at standard conditions [5] with an Sn doping flow of 22 sccm. For electrical isolation, source mesas are etched-out from the buffer layer after growth. The high-*k* is deposited in an Oxford Savannah atomic layer deposition (ALD) system with 10 cycles of Al_2O_3 at 250°C and 50 cycles of HfO_2 at 100°C, corresponding to an equivalent oxide thickness (EOT) of 1.5 nm. The source mesa and the sputtered W gate contact are separated by a 60 nm Si_3N_4 film, whereas the gate and drain contacts are separated with a spin-on polymer [5]. The top contact is sputtered Ti/W/Au. Excluding the placement of the NWs, all lithography is done with a contact UV aligner. The overlapping gate- and drain-contact pads are 12 × 12 µm^2 in size. A scanning electron microscopy image of a fabricated mixer circuit is shown in Fig. 1. A schematic cross-section of the NW MOSFET, with approximate layer thicknesses, is shown as an inset.

Each NW-FET device has arrays of 120–500 NWs, acting as parallel channels, with an NW diameter of about 35 nm, and with channel lengths of 200 nm. The mixer circuit is implemented with three NW-FETs (one RF input and two LO switch devices), as well as two non-gated NW arrays, acting as load resistances, R_L. A load capacitance, C_L, is fabricated using the first spacer layer (SiNx) as capacitor dielectric between the buffer layer and the gate metal layer. Measurements of reference capacitors show values of about 12 pF.

Measurement: DC characterisation is performed with a Keithley 4200 semiconductor characterisation system (SCS). The transfer characteristics of the three individual active devices in a mixer circuit, with 500 NWs per device, are shown in Fig. 2*a*. On the sample, devices typically show $g_m = 0.1–0.3$ mS/µm at $V_{DS} = 0.5$ V, which is limited by series resistance in the range 1–10 kΩ µm.

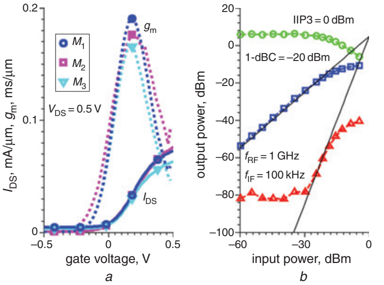

Fig. 2 *Device and circuit characterisation*

a Transfer characteristics of three active devices of mixer circuit, with RF data shown in Fig. 2*b*. Solid lines represent I_{DS}, whereas dotted lines represent g_m. Numbers are normalised to NW circumference

b Single tone test showing fundamental (squares) and third-order (triangles) harmonics against input power. Conversion power gain is shown as circles

The RF circuit characterisation is performed with an Agilent E8361A network analyser and a Rohde & Schwarz FSU spectrum analyser. As the RF input terminal is not matched to the measurement equipment, the scattering parameters of the RF input is measured in order to determine the actual input power and input voltage, used for gain calculations. The impedance at the input at 1 GHz is 460 Ω. To measure the voltage gain of the mixer, an operational voltage amplifier in unity gain configuration is connected between the circuit and the input of the spectrum analyser. The measurement (single tone test) of the intermediate frequency (IF) output power as a function of the delivered RF input power is shown in Fig. 2*b*. The overdrive voltage bias, V_{OD}, of M_1 is set to 0.18 V, whereas V_{OD} is set to 0.5 V for M_2 and M_3. In all the circuit measurements, a DC power consumption of 3.8 mW is drawn from a 1.5 V supply. The LO switching power is set constant at −3 dBm. In Fig. 3, the output power is plotted against RF frequency, for an IF of 100 kHz. Several circuits show similar performance concerning both gain and BW.

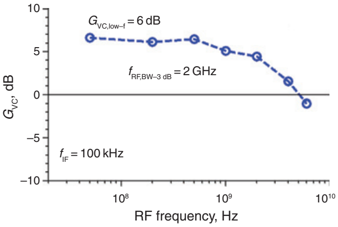

Fig. 3 *Voltage conversion gain against input frequency*

3 dB BW corresponds to 2 GHz

Performance analysis: To validate the measured circuit performance, we use the analytical expressions for the active down-conversion mixer where the voltage gain is ideally given by

$$G_{\mathrm{VC}} = \frac{2}{\pi} g_{\mathrm{m,RF}} R_{\mathrm{L}} \tag{1}$$

In (1), $g_{\mathrm{m,RF}}$ is the transconductance of the input stage. From DC measurements, $g_{\mathrm{m,RF}}$ equals 11 mS at the bias point. However, the transconductance has been shown to be frequency dependent for MOSFETs [9]. Using (1), the small-signal R_{L} is extracted to be >300 Ω, which is in line with the measured circuit DC node potentials (corresponds to >0.4 V over the load resistors) considering the slight nonlinear characteristics of the NW resistors. Here we assume that losses to non-idealities of the loads and switches are negligible. In actuality, there is leakage of a few µA between mesa structures (through the Si-substrate) and a mismatch between the switching circuit branches measured to be within 10%. The determined value of R_{L} corresponds to 1.3 times the on-resistance of the active devices.

The 1 dB compression point (1-dBC) is limited by the narrow $g_{\mathrm{m,RF}}$-peak shown in Fig. 2*a*. The g_{m} reduction is originating from the large device drain series resistance, gradually bringing the device out of saturation as the gate potential is increased beyond the point of the $g_{\mathrm{m,RF}}$-peak. The RF-BW limitation is highly dependent on the parasitic capacitances from the large contact pads, a limitation linked to the optical lithography system used. Normalising to the NW circumference, the parasitic gate capacitance is about 3.3 fF/µm. This limitation is also observed in analysis of the RF performance of individual NW-FETs [5].

Conclusion: We have demonstrated a down-conversion mixer operating in the GHz range using vertical InAs NW MOSFETs.

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Paper V

Extrinsic and Intrinsic Performance of Vertical InAs Nanowire MOSFETs on Si Substrates

Karl-Magnus Persson, *Member, IEEE*, Martin Berg, Mattias B. Borg, *Member, IEEE*, Jun Wu, Sofia Johansson, Johannes Svensson, Kristofer Jansson, Erik Lind, and Lars-Erik Wernersson

***Abstract*—This paper presents dc and RF characterization as well as modeling of vertical InAs nanowire (NW) MOSFETs with $L_G = 200$ nm and Al_2O_3/HfO_2 high-κ dielectric. Measurements at $V_{DS} = 0.5$ V show that high transconductance ($g_m = 1.37$ mS/μm), high drive current ($I_{DS} = 1.34$ mA/μm), and low ON-resistance ($R_{ON} = 287$ $\Omega\mu$m) can be realized using vertical InAs NWs on Si substrates. By measuring the $1/f$-noise, the gate area normalized gate voltage noise spectral density, $S_{VG} \cdot L_G \cdot W_G$, is determined to be lowered by one order of magnitude compared with similar devices with a high-κ film consisting of HfO_2 only. In addition, with a virtual source model we are able to determine the intrinsic transport properties. These devices ($L_G = 200$ nm) show a high injection velocity ($v_{inj} = 1.7 \times 10^7$ cm/s) with a performance degradation for array FETs predominantly due to an increase in series resistance.**

***Index Terms*—InAs, MOSFET, nanowire (NW), RF.**

I. INTRODUCTION

STRIVING toward ultrascaled devices, the transistor architecture and the material properties need consideration. The nanowire (NW) geometry offers advantageous electrostatic scaling [1] and the use of a high-κ gate dielectric allows reduced equivalent oxide thickness (EOT) without large gate leakage currents. InAs has a high injection velocity, v_{inj}, and allows simple fabrication of low resistance contacts [2], [3]. High current densities have been demonstrated for thin InAs transistor channels [4].

In this paper, we demonstrate dc characterization, modeling, and RF characterization of FETs consisting of arrays of vertical NWs (a-FETs) [5]–[7]. Our data for a-FETs show a threefold improvement on earlier data and we achieve transconductance values above 1 mS/μm for individual NWs. This is attributed to an improved bi-layer gate dielectric using Al_2O_3/HfO_2, as well as more reliable processing with a thin Si_3N_4 film, reducing the source series resistance [8]. From dc modeling, we identify the main limiting factors in the transistor layout.

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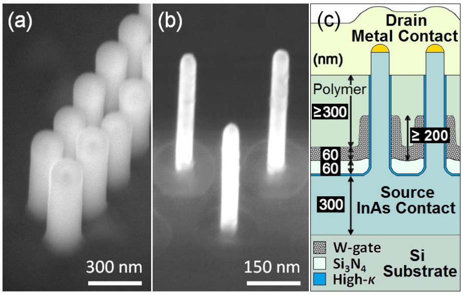

Fig. 1. SEM images at 30° tilt angle of NW array (a) after PECVD of Si_3N_4 and (b) after side removal etch. (c) Schematic cross section of the NW FET device. A 60-nm-thick Si_3N_4 film separates the InAs source contact layer from the gate metal while a spin-on resist (≥300 nm) separates the gate and drain metals.

II. DEVICE FABRICATION

Devices are fabricated on Si substrates cut from a 4-in Si wafer covered by a 300-nm-thick InAs contact layer (ICL). The Si is highly resistive and the InAs layer is grown without intentional doping ($n = 3 \times 10^{18}$ cm^{-3}) demonstrating a sheet resistance of 36 $\Omega/\square$. Definition of size and position of gold seed particles is made with electron-beam-lithography and growth of InAs NWs is performed in an metal-organic-vapor-phase-epitaxy growth chamber at 420 °C and with a Sn dopant flow corresponding to a doping level of $\sim 1 \cdot 10^{18}$ cm^{-3} [9]. For a-FETs, NWs are placed in zigzag rows to reduce the parasitic capacitance within the array [10], with 300-nm spacing between each NW [Fig. 1(a) and (b)]. Devices are fabricated with 1, 52, 96, and 192 NWs and with two NW diameters; $D_{NW} = 45$ nm and $D_{NW} = 28$ nm [8]. In addition to the difference in size of catalytic gold particles, the rest of the growth conditions are identical. The dielectric is deposited in a Cambridge Savannah ALD process with 10 cycles of Al_2O_3 at 250 °C and 60 cycles of HfO_2 at 100 °C, with a total thickness of 7 nm translating to an estimated EOT of 1.8 nm. The $D_{NW} = 28$ nm have a thinner HfO_2 layer, yielding an estimated EOT = 1.3 nm. Subsequent to the ALD, the 2 × 2-cm^2 pieces are cleaved into four samples and each sample is thereafter processed individually. Devices are isolated by etching out source-mesas from the ICL in a wet-etch procedure. A 60-nm-thick source-to-gate spacer layer is fabricated in a process where a

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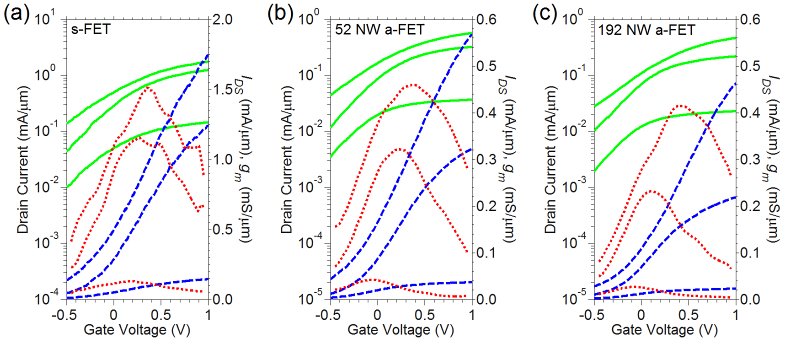

Fig. 2. DC transfer characteristics for $V_{\mathrm{DS}} = 0.05$, 0.5, and 1.0 V, showing I_{DS} on a logarithmic scale (green solid line), I_{DS} on a linear scale (blue dashed line), and g_m on a linear scale (red dotted line). (a) s-FET. (b) 52 NW a-FET. (c) 192 NW a-FET.

plasma-enhanced-chemical-vapor-deposited (PECVD) Si_3N_4-film [Fig. 1(a)] is conformaly formed on the NWs. The film is then selectively removed on the sides of the wires, while keeping the lateral film intact by protecting it with a polymer etch mask in a SF_6 dry-etch process [Fig. 1(b)]. The sputtered W-gate is defined to 200-nm length by the thickness of an etched down polymer etch mask, using a SF_6 dry-etch process similar as with the nitride. The gate-drain top spacer is fabricated with a spin-coated polymer resist, which is etched-back to ~300 nm. The top contact metal consist of 250-nm sputtered Ti/W/Au. A schematic cross section of a device is shown in Fig. 1(c). The ICL acts as source, and the top metal as the drain contact.

III. MEASUREMENTS AND SMALL-SIGNAL MODEL

DC characterization is performed with a Keithley 4200-SCS. For the $D_{\mathrm{NW}} = 45$-nm devices, transfer characteristics of a single NW FET (s-FET) and two a-FETs (52 and 192 NWs, respectively) are shown in Fig. 2(a)–(c), respectively. The peak transconductance is reduced for a-FETs as compared with the s-FETs, and the data are presented in Table I. Plots of output characteristics are shown in Fig. 3(a) and (b) for an s-FET and an a-FET (52 NWs), respectively. In Fig. 3(c), g_m versus V_{GS} for three s-FETs is shown. At $V_{\mathrm{DS}} = 0.5$ V, the best device show $g_m = 1.37$ mS/μm. The s-FET device referred to as NW1 is the same in Fig. 3(a) and (c). In Fig. 3(d), transconductance for several devices have been plotted against the ON-resistance (R_{ON}) to correlate the transconductance with the access resistance. All our performance measures are normalized to circumference [$I_{\mathrm{DS,norm}} = I_{\mathrm{DS}}/(n \cdot \pi \cdot D_{\mathrm{NW}})$], where n is the number of NWs. For the $D_{\mathrm{NW}} = 45$-nm NWs, the uniform doping coupled with the large diameter causes a substantial band bending inside the NWs, which limits the off performance. This is strongly dependent on the NW doping and radius, as the Fermi level movement is restricted toward the valence band due to the increasing D_{it} toward the valence band of InAs [11]. In Table I, we have as a reference included data for a 28-nm-diameter a-FET that shows a substantially improved subthreshold swing (SS). The fact that the thinner NWs show better off-state performance and lower DIBL is attributed to increased electrostatic control due to its smaller diameter and the thinner EOT. In contrast, a difference in conduction related to confinement effects is only expected for sub-15-nm NWs, as concluded from a simulation study of the band structure as a function of NW diameter scaling [12]. A further interesting point of reference is that the reported data for InAs NW FETs with $D_{\mathrm{NW}} = 40$ nm and $L_G = 35$ nm show SS = 130 mV/decade, a value that is significantly lower than the reported values here. This dissimilarity can be attributed to the three times higher doping used in this paper, preventing full depletion of the channel [13].

TABLE I

PEAK VALUES LISTED FOR 45-nm S-FETS AND 45- AND 28-nm a-FETS WITH 52, 96, AND 192 NWS, RESPECTIVELY. ALL OUR MEASURES ARE NORMALIZED TO NW CIRCUMFERENCE. TRANSCONDUCTANCE CHARACTERISTICS OF THE TABLED S-FETS[a] ARE SHOWN IN FIG. 3(c). AS REFERENCE, DATA FOR A XOI FET[b] [14], A RADIAL NW FET[c] [15], A LATERAL NW FET[d] [4], AND A TOP DOWN GAA FET[e] [16] ARE ADDED. ALL VALUES GIVEN FOR $V_{\mathrm{GS}} - V_T \leq V_{\mathrm{DS}} = 0.5$ V, WHICH IS ALSO HERE CHOSEN AS THE DEFINITION FOR I_{ON}. SOME VALUES ARE ESTIMATES MADE BY THE AUTHORS*

Diameter / # of NWs	L_g (nm)	EOT (nm)	R_{SD} (Ωμm)	g_m (mS/μm)	I_{ON} (mA/μm)	SS (mV/dec)	DIBL (mV/V)
28 nm / 96	~300	1.3	~3000	0.15	0.06	140	110
45 nm / 192	~300	1.8	1630	0.23	0.13	540	240
45 nm / 52	~300	1.8	1240	0.32	0.17	480	320
45 nm / 1 (NW3)[a]	~200	1.8	310	1.09	0.59	420	260
45 nm / 1 (NW1)[a]	~200	1.8	210	1.19	0.67	500	320
45 nm / 1 (NW2)[a]	~200	1.8	190	1.37	0.75	800	600
13 nm / N/A[b]	230	2.4	170	1.72	0.9	180	-
25 nm / 1[c]	170	-	-	1.07	0.5*	260	-
15 nm / 1[d]	100	1.3	150	1.23	0.6	140	60
20x30 nm / 1[e]	20	1.2	~500*	1.65	0.54	88	7

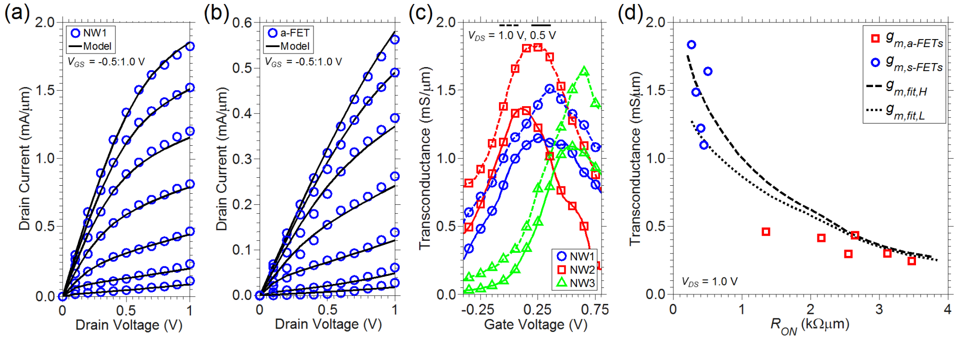

Fig. 3. $I_{\rm DS}$ versus $V_{\rm DS}$ (data normalized to circumference) for (a) s-FET and (b) 52 NW a-FET. (c) g_m normalized to circumference versus $V_{\rm DS}$ for s-FETs. (d) Measured $g_{m,\text{peak}}$ normalized to circumference for a-FETs (red squares) and s-FETs (blue circles) plotted against measured RON at $V_{\rm DS} = 1.0$ V. The black dashed line, $g_{m,\text{fit},H}$, is simulated using the VS model for $v_{\rm inj} = 1.7 \cdot 107$ cm/s and $L_G = 200$ nm. The black dotted line, $g_{m,\text{fit},L}$, is simulated using the VS model for $v_{\rm inj} = 1.2 \cdot 10^7$ cm/s and $L_G = 300$ nm.

Comparing V_T for our $D_{\rm NW} = 45$-nm s-FETs and a-FETs, devices shows similar values (typically between -0.4 and -0.2 V) and there is no relation between V_T and peak transconductance, $g_{m,\text{peak}}$. Quantifying $g_{m,\text{peak}}$ widths, the values for s-FETs and a-FETs do not differ, suggesting there is no significant spread in V_T within arrays that would cause a degraded maximum g_m. For reference, we have benchmarked our data with other high performance InAs and InGaAs NW FETs; a 13-nm planar XOI FET, $L_G = 230$ nm [14], a 25-nm diameter InAs/InP radial NW FET [Ω-gate, $I_{\rm DS,norm} = I_{\rm DS}/(n \cdot 0.75\pi \cdot D_{\rm NW})$], $L_G = 170$ nm [15], a 15 nm in diameter lateral NW, $L_G = 100$ [4], and a top–down rectangular GGA FET (20 nm × 30 nm), $L_G = 20$ nm [16].

Low frequency noise (LFN) characterization is made with a Stanford SR830 lock-in amplifier in series with a Stanford SR570 LNA. The current noise spectral density, $S_{\rm ID}$, is measured for $V_{\rm DS} = 50$ mV and $f = 10$ Hz. A common measure of comparison is the deduced gate voltage noise spectral density, $S_{\rm VG} = S_{\rm ID}/g_m^2$, normalized to the gate area ($S_{\rm VG} \cdot L_G \cdot W_G$). Data for two s-FETs and two a-FETs are plotted in Fig. 4. The lowest levels for all the measured devices are determined to range in the interval $S_{\rm VG} \cdot L_G \cdot W_G =$ 310–410 μm$^2\mu$V^2/Hz. Another common measure of comparison is the $S_{\rm ID}$ normalized to the drain current, $S_{\rm ID}/I_{\rm DS}^2$. The lowest measured levels are $S_{\rm ID}/I_{\rm DS}^2 = 0.9 \times 10^{-10}$–$1.5 \times 10^{-10}$ Hz^{-1} and $S_{\rm ID}/I_{\rm DS}^2 = 0.9 \times 10^{-8}$– 2.0×10^{-8} Hz^{-1}, for two 52-NW a-FETs and two s-FETs, respectively. The measurements indicate that when accounting for the difference in total gate width, the extracted $S_{\rm VG}$ for s-FETs and a-FETs show undeviating values. Further, comparing the $1/f$-noise to similar devices but fabricated with a high-κ of HfO_2 only [15], the new devices improved the noise performance about one order of magnitude in terms of $S_{\rm VG} \cdot L_G \cdot W_G$ 5700 μm^2 μV^2/Hz and even greater for $S_{\rm ID}/I_{\rm DS}^2 = 7.3 \times 10^{-7}$ Hz^{-1}. The decrease in LFN can be related to the introduction of an Al_2O_3 film, which more efficiently can reduce the amount of suboxides [11]. For comparison, the ITRS roadmap states that for the year 2015, multigate MOSFET devices for mm-wave applications should comply with $S_{\rm VG} \cdot L_G \cdot W_G =$ 10.3 μm$^2\mu$V^2/Hz [17]. Hence, further work is required to reach the target goals within the roadmap.

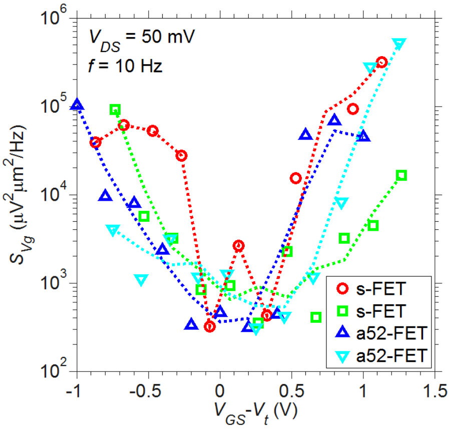

Fig. 4. $S_{\rm VG}$ plotted versus $V_{\rm GS} - V_T$ for four different devices, two s-FETs, and two 52 NW a-FETs. The data were measured at $V_{\rm DS} = 50$ mV and $f = 10$ Hz and is normalized to total gate area, $L_G \cdot W_G$. The dotted lines are added to indicate the voltage dependence.

The RF characterization is performed using an Aglient E8361A network analyzer from 60 MHz to 40 GHz at a RF power of -27 dBm [5]. For measurements, a-FETs with 192 NWs was chosen on the premises of having a higher absolute g_m and a scanning electron microscopy (SEM) image of the InAs mesa structure of one such device is shown in Fig. 5(a). The highlighted areas show the location where contact vias and pads will be formed in later stages. The deduced

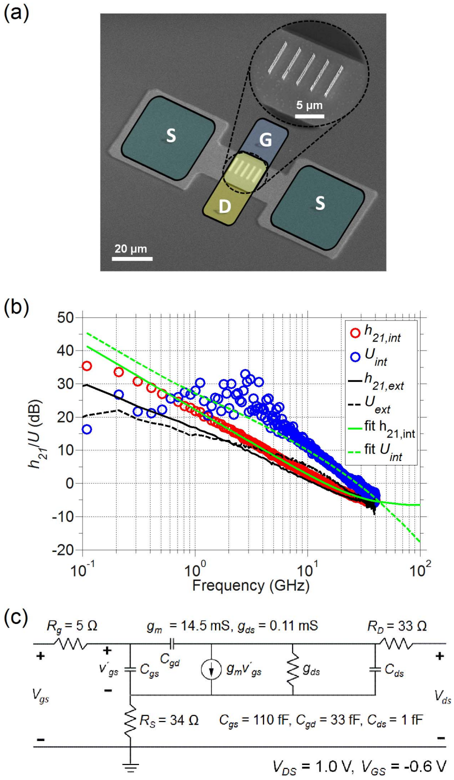

Fig. 5. (a) SEM image with highlighted areas for the source via contacts, S, the gate pad, G, and the drain pad, D, and where the intrinsic region corresponds to the quadratic area in the center, also shown at higher magnification. (b) Graph is shown intrinsic and extrinsic current gain, $h_{21,\text{int}}$ and $h_{21,\text{ext}}$, respectively, and intrinsic and extrinsic unilateral power gain, U_{int} and U_{ext}, respectively, for a 192 NW a-FET device. In addition, fitting of a small-signal model to the intrinsic data is added (fit $h_{21,\text{int}}$ and fit U_{int}). (c) Extracted small-signal parameters for the measured device at $V_{\text{DS}} = 1.0$ V and $V_{\text{GS}} = 0.6$ V.

current gain, h_{21}, and unilateral power gain, U, for the best device is shown in Fig. 5(b), for which $f_t = 14.6$ GHz and $f_{\max} = 30.0$ GHz at $V_{\text{DS}} = 1.0$ V, and $V_{\text{GS}} = -0.45$ V and -0.60 V, respectively. The RF data are fitted to a standard MOSFET small-signal model [5] where the parasitic elements are included in Fig. 5(c). For simplicity, impact ionization was not accounted for as it turned out to have negligible effect in fitting to the measured data. Statistics over four devices show f_t in an interval of 9.7–17.4 GHz and $f_{\max}$ of 20.3–30.0 GHz, at $V_{\text{DS}} = 1.0$ V.

IV. DC DEVICE MODELING

To describe the transistor characteristics of the $D_{\text{NW}} = 45$-nm devices, a virtual source (VS) model is fitted to the measured dc data [18]. The model is based on a channel charge equation and also provides a coherent intrinsic gate capacitance [19]. Modeled devices are chosen on the premises of low R_{ON} in combination with less pronounced impact ionization, thus being able to neglect the later. Since a direct measurement of the NW contact and channel resistivity is difficult, we do a simultaneous fit of the VS-model parameters with estimates of the source/drain resistance. For a s-FET (referred as NW1), assuming a NW resistivity of 1.0×10^{-3} Ωcm [20] and a first spacer layer thickness of 67 nm (60-nm Si_3N_4 + 7 nm high-κ), we obtain $R_S = 65$ Ωμm. The metal-ICL contact resistance is measured to be in the order of 2 Ω and for simplicity it is counted as a constituent of the ICL. For the s-FET, the 18 Ω series resistance contribution from the ICL, corresponding to 2.5 Ωμm, can be ignored. Fitting the data in Fig. 3(a) gives $R_D = 141$ Ωμm, equivalent to 300 nm resist top spacer thickness [translating to 160-nm nongated resistive NW segment length, see Fig. 1(c)] and in agreement with the experimental implementation. At a gate length of $L_G = 200$ nm, we obtain values of mobility, $\mu_{\text{LOW-FIELD}} = 1300$ cm^2/V s and $v_{\text{inj}} = 1.7 \times 10^7$ cm/s. While the rather low mobility can be expected for a highly doped surface channel, the injection velocity is in the same range as reported for an InAs HEMT of similar gate length [2] ($v_{\text{inj}} \sim 2 \times 10^7$ cm/s).

To analyze a-FETs, the fitted model for the s-FET is expanded and fitted to an a-FET with 52 NWs. The significant increase in R_{ON} for a-FETs compared with s-FETs can in part be explained by the undoped ICL that adds 18 Ω source series resistance, see Fig. 6. To obtain a good fit, however, it is needed to reduce v_{inj} by ~30% and also increase the resistivity of the NWs by a factor of around four, and this fitting is shown in Fig. 3(b). The decrease in v_{inj} can be explained by longer channels for a-FETs as compared with the s-FET (as well as thicker spacer layers) due to the defining polymer resist, used for the etch-back of the gate that tends to become thicker around arrays. The steep increase in series resistance can, however, not be explained simply by a thicker gate-drain separation. Instead, it must be considered that the doping incorporation of the surfactant Sn is higher for single NWs as compared with NWs grown in arrays due to the limited collection area for the a-FETs during the vapor–liquid–solid growth. The radial band bending inefficiency for the 45-nm-diameter NW FETs, as described earlier, can effectively be modeled as a parasitic parallel conduction. For the measured s-FET in Fig. 3(a), it is in the order of 0.25 mS/μm. For a-FETs, this value is ~4–6 times lower; however, the transfer characteristics are not significantly improved compared with s-FETs as the transconductance is reduced by a similar factor due to series resistance. The variance in characteristics between devices with equal number of NWs is thought to be related to diameter variation (NWs in arrays typically vary between 40–45 nm) in combination with variations of separation layer thicknesses over the sample. To compare the effect of the reduced v_{inj} with the effect of external resistances, we plot calculated values for the extrinsic transconductance, $g_{m,\text{ext}}$, as a function of R_{ON}, in Fig. 3(d) using the VS model. In the plot there

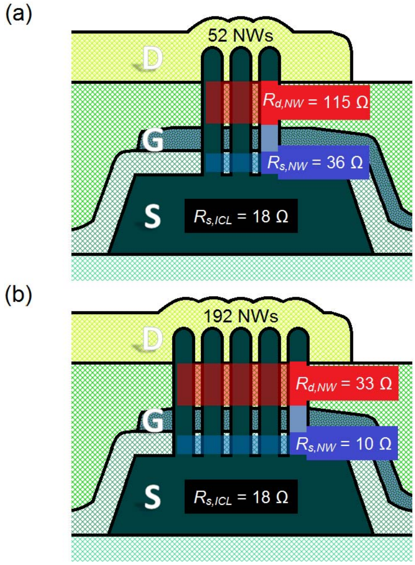

Fig. 6. Schematic illustration of the distribution of the parasitic series resistance extracted from dc measurements and VS modeling where the subscripts $R_{\text{S,ICL}}$ and $R_{\text{S,NW}}/R_{\text{D,NW}}$ are the series resistances associated with the ICL and the NW, respectively. Values are shown for (a) 52-NW a-FET and (b) 192-NW a-FET.

are two lines representing two values of v_{inj} (the fitted s-FET and a-FET) corresponding to $L_G = 200$ nm ($g_{m,\text{fit},H}$) and $L_G = 300$ nm ($g_{m,\text{fit},H}$), respectively. Comparing the simulated data with the experimentally measured $g_{m,\text{ext}}$, a good fit can be obtained. This indicates that the external resistances are the major source for device performance degradation of a-FETs as compared with s-FETs. This can essentially be described using the conventional formula relating the extrinsic and intrinsic transconductance $g_{m,\text{ext}} = g_{m,\text{int}}/(1 + g_{m,\text{int}} \cdot R_S + g_{d,\text{int}} \cdot (R_S + R_D))$ [21]. Here, g_d is the output conductance. From the average experimental data for the s-FETs shown in Fig. 3(c), we deduce a value for the intrinsic transconductance, $g_{mi} = 2.4$ mS/μm. For the a-FETs, this value range between 0.5–0.7 mS/μm.

The total parallel resistance contributions from the un-gated segments of the NWs are shown in Fig. 6(a) and (b) for a 52-NW a-FET and a 192-NW a-FET, respectively. Comparing the normalized series resistance contributions attributed to the un-gated NW segments (omitting the ICL), $R_S = 265$ Ωμm and $R_D = 845$ Ωμm for the 52-NW a-FET, and $R_S = 270$ Ωμm and $R_D = 900$ Ωμm for the 192-NW a-FET. These values are quite close as expected (2% and 6% in difference for R_S and R_D, respectively). For a 52-NW a-FET, the ICL (18 Ω) adds another 12% to the total series resistance while for a 192-NW a-FET, the series resistance contribution from the ICL adds another 42%. This explains why a 52-NW a-FET has better normalized dc performance than a 192-NW a-FET.

V. RF DEVICE MODELING

Performing electrostatic simulations of the capacitances of the de-embedded structure of 12 × 12 μm^2 [5], that is the overlapping source-gate and gate-drain areas, as shown in Fig. 5(a) with the overlapping rectangles, the parasitic capacitances $C_{\text{gs,p}}$ and $C_{\text{gd,p}}$ are determined to 131 fF and 16 fF, respectively. The substantially larger $C_{\text{GS,p}}$ originates from the thinner source spacer layer and higher permittivity of the Si_3N_4 as compared with the drain spacer. Considering the low density of states for InAs, the high frequency intrinsic gate capacitance, $C_{\text{gg,i}}$, for 192 NWs is simulated to be in the interval of 6–23 fF for $V_{\text{GS}}–V_T$ varying between −0.5 and 0.5 V, at $V_{\text{DS}} = 1$ V. Considering the low measurement gate bias and assuming that the $C_{\text{gg,i}}$ contribution lies in the middle of the given range, the simulated number ($C_{\text{gg,tot}} = 5.95$ fF/μm) is 13% larger than the number extracted from the measurement ($C_{\text{gg,tot}} = 5.27$ fF/μm). Actual pad size difference compared with the patterned area as well as uncertainty in the spacer layer thicknesses and dielectric constants are likely the reasons for the deviation between measured and calculated capacitances. The extracted $g_{m,\text{int}}$ of 0.53 mS/μm corresponds to a $g_{m,\text{ext}}$ of 0.36 mS/μm, which can be related to the maximum $g_{m,\text{ext}}$ measured at dc for the same device ($g_{m,\text{ext}} = 0.30$ mS/μm, 20% lower). The low V_{GS} in the measurement for maximum f_t and $f_{\max}$ suggest a shift in V_T as compared with dc ($V_T = -0.45$ V for $V_{\text{DS}} = 1$ V). Both the shift in V_T and the increase in g_m can be related to slow traps that are not responding at higher frequencies, thus explaining the lowering of the V_T and a frequency dependent g_m [22]. Comparing the series resistances from the RF model extraction with those from the VS model fitting of the dc measurements, they are found to be fairly similar. The RF extraction gives $R_S = 34$ Ω and $R_D = 33$ Ω while the dc measurements translates into $R_S = 28$ Ω and $R_D = 33$ Ω.

VI. DISCUSSION

Based on the data presented in this paper we draw some general conclusions regarding III–V NWs and their implementation; although high intrinsic performance, that is high transconductance and drive currents, has been demonstrated in various forms of III–V NWs [4], [14]–[16], it is clear that the implementation of RF-compatible devices still is a challenge. Analysis of planar III–V MOSFETs [23] show that the control of the access resistance is one of the key parameters to increase the transconductance and to obtain attractive RF-properties. The method used in the implementation presented here, that is uniform doping of the transistor channel, needs further refinement beyond diameter scaling in order to avoid increase in the access resistance. Increased doping control may be one alternative to reduce the source/drain resistance [9]. Alternatively, the access regions may be regrown, although at the cost of parasitic capacitance [10]. A heterobarrier may also be included into the channel to increase the carrier control [24]. It appears that a combination of these appraoches may be required to fully exploit the potential of the high III–V injection velocity for RF-compatible MOSFETs in either vertical or lateral geometry.

VII. CONCLUSION

The performance of s-FET has been evaluated ($g_{m,\text{ext}} = 1.37$ mS/μm). Based on a VS model we are able to accurately model and determine intrinsic transport properties including $v_{\text{inj}} = 1.7 \times 10^7$ cm/s. The performance is degraded by series resistance for devices consisting of arrays of NWs. The introduction of a thin Al_2O_3 film combined with an outer HfO_2 film may be responsible for the measured reduction in $1/f$-noise compared with similar devices fabricated with HfO_2 only.

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Paper VI

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High quality InAs and GaSb thin layers grown on Si (1 1 1)

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ABSTRACT

We have investigated growth of thin epitaxial layers of InAs on Si (1 1 1) substrates by metalorganic vapor phase epitaxy (MOVPE) and successfully grown GaSb layers on InAs. Furthermore, we have studied the effect of growth temperature and material flow on the nucleation stage and also nucleated GaSb nanowires on the underlying GaSb layer. The InAs layers are grown by a standard two-step growth approach. The main parameter under investigation is the effect of incorporating more nucleation layers into the growth process. The addition of more nucleation layers clearly correlates with the surface morphology and quality of the resulting InAs layer. Morphological and structural characterizations prove that a perfect quality InAs layer is achieved by incorporating 4 nucleation layers. Deposited layers with 250 nm thickness and 0.4 nm atomic step roughness have a mobility of 2400 cm^2/Vs and a carrier concentration of 2.7×10^{18} cm^{-3}. Moreover, we have utilized the InAs film to grow a GaSb layer and observed atomic step roughness for a thin film of ~300 nm. Finally we demonstrate the growth of GaSb nanowires on the GaSb layer.

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1. Introduction

InAs is an attractive material for optical and high-speed devices due to its high electron mobility and narrow direct band gap [1,2]. However, integration of InAs on Si has remained a challenge over the last 30 years [3,4]. The large lattice mismatch of 11.6% between InAs and Si substrates creates dislocations and can cause strain to the epitaxial layer. Also, epitaxial growth of polar material on non-polar materials causes the formation of antiphase domains (APD) [5]. In the case of Si (1 1 1) substrates, it can also result in stacking defects in the InAs layer. The last main challenge is the different thermal expansion coefficients, which comes from dissimilar behavior of InAs and Si in response to temperature changes [5].

Previously, we have reported MOVPE growth of thick InAs layers on Si (1 1 1) substrates [6,7]. However, even for samples of 2 μm thickness, holes remained on the surface. The hole formation originates from incomplete surface coverage of one nucleation layer growth approach. In this paper, for the first time, we report step-flow like growth of InAs on Si (1 1 1). The major improvement is achieved by optimizing the growth conditions and by introducing more nucleation layers into the growth process. The InAs buffer layers are grown using a standard two-step growth approach by MOVPE. First, a nucleation layer is grown at low temperature and high V/III ratio with a thickness of ~15 nm. The low temperature growth limits the surface diffusion length of the precursors and results in deposition of a high density of Stranski–Krastanov islands. After the nucleation step, the temperature is ramped up and the nucleation layer is annealed for 6 min. This annealing step helps Ostwald ripening and improves the InAs surface coverage [6]. In the case of multiple nucleation layers, the same nucleation and annealing steps are repeated. Then, a second layer growth is followed at the same high temperature for 45 min with a low V/III ratio favoring adatom mobility and step-flow. Fig. 1a shows a schematic structure of the InAs layer with four nucleation layers. Furthermore, we have used our mirror-like InAs samples as a substrate for GaSb layer growth. Heteroepitaxial growth of GaSb/InAs is an interesting structure since the conduction band of the InAs layer has a negative energy offset to the valence band of GaSb layer. This type II band alignment is used in some device applications such as infrared detectors [8]. We have studied the GaSb layer growth while keeping the same temperature as InAs layer growth and we have investigated the effect of lowering the TMSb molar fraction on the surface morphology of the samples. We have also grown GaSb nanowires on the GaSb layer, which are suitable candidates for high-speed electronic devices [9].

2. Experimental detail

Highly resistive Si (1 1 1) was used as substrates. Prior to the growth, the Si substrate was cleaned by a standard RCA cleaning

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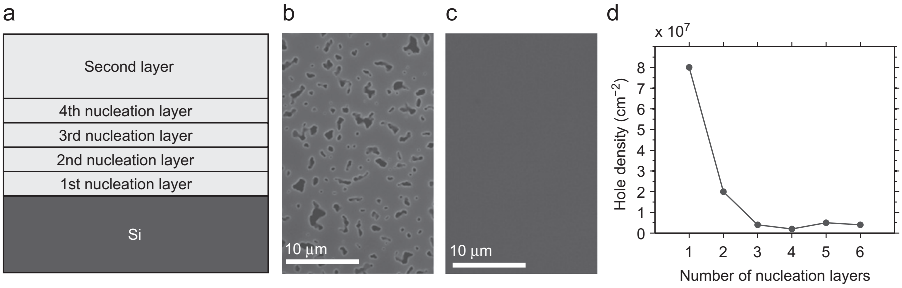

Fig. 1. (a) Schematic structure of the obtained InAs layer with four nucleation layers. SEM top surface of InAs samples with (b) one nucleation layer (c) four nucleation layers. (d) Evaluation of the surface hole density that decreases drastically when inserting more number of nucleation layers.

method [10]. The RCA cleaning procedure is known to remove possible contaminations on the surface, including carbon, and it subsequently forms a very thin oxide layer on the surface. The last cleaning step was etching of this oxide by dipping the substrates in HF solution (10%). This produces an H-terminated surface and protects the surface against oxidation during the loading time inside the reactor. Growth was performed in a horizontal MOVPE reactor (Aixtron 200/4). Trimethylindium (TMIn), Trimethylgallium (TMGa), Triethylgallium (TEGa), Arsine (AsH_3), and Trimethylantimony (TMSb) were used as precursors with hydrogen as a carrier gas with a total flow of 13 l/min and a reactor pressure of 100 mbar.

After being loaded inside the reactor, the samples were annealed for 5 min at 700 °C under AsH_3 flow to transform the surface from H-terminated to As-terminated. The growth of the nucleation layer was performed at a low temperature of 350 °C for 10 min followed by ramping up to 600 °C, where the nucleation layer was annealed for 6 min and a second layer growth continued at the same high temperature. The TMIn molar fraction was constant during the deposition at 1.88×10^{-5}. The AsH_3 molar fraction was 3.46×10^{-3} during the growth of the nucleation layer and was decreased one order of magnitude for the growth of the second layer. Intentional doping of the samples was performed by introducing TESn with molar fraction of 2.33×10^{-7} during the second layer growth.

For heteroepitaxial growth of GaSb on InAs, the TEGa molar fraction was set to 1.1×10^{-4} and the TMSb molar fraction was varied from 2.17×10^{-4} to 1.08×10^{-4}. The GaSb layers were grown at the temperature of 600 °C for 10 min [11].

GaSb nanowires were grown from aerosol deposited gold seed particles. The Au nanoparticles were deposited with density of 1 μm^{-2} and 40 nm diameter, where the nanowire diameter is determined by the Au nanoparticle diameter. GaSb nanowires were grown with TMGa and TMSb at different temperatures ranging from 400 to 530 °C. TMGa and TMSb molar fractions were increased starting from 7.09×10^{-6} and 2.28×10^{-5}, respectively. However, the V/III ratio was constant (3.2) [12].

The surface morphology of the InAs layer was evaluated by scanning electron microscopy (SEM), FEI Nova NanoLab 600. D3100 Nanoscope IIIa atomic force microscopy (AFM) was used to determine the atomic roughness and dislocation structure of our samples. The quality, composition, and strain of the samples were determined by high resolution X-ray diffraction (HR-XRD) measurements using a Bruker-AXS D8 system with a CuKα X-ray source. Finally, carrier mobility and concentration in the grown layers were measured by Van-der-Pauw technique for a square geometry on samples with thermally evaporated Ti/Au ohmic contacts. Hall measurements were carried out with magnetic field of 0.1 T at room temperature as well as at 77 K.

3. Result and discussion

3.1. *InAs on Si (1 1 1)*

3.1.1. *Structural characterization*

Deposition of InAs on Si using one nucleation step results in layers with holes remaining on the surface [6]. To investigate the effect of incorporating more nucleation layers, we have grown a set of six samples with one to six nucleation layers. Inserting additional nucleation layers results in a thickness variation from 220 to 320 nm. SEM inspection of the samples clearly indicates that there is a major improvement in the surface morphology and reduction in holes as we increase from one (Fig. 1b) to two nucleation layers. From the four nucleation layered samples, the hole formation is suppressed down to 4×10^6 cm^{-2} (Fig. 1c). For the cases of five and six nucleation layers, the surface structure looks the same as the four nucleation layered sample (Fig. 1c). As demonstrated in Fig. 1d, the density of holes on the surface decreases significantly with incorporating more nucleation layers.

In an optimum two-step growth, the role of the nucleation layer is to form high-density islands covering the substrate. In our case, the growth of one nucleation layer does not favor the aforementioned conditions and does not provide a homogeneous surface template for further growth. Indeed, additional nucleation layers are needed to provide complete surface coverage and eliminate hole formation.

We have analyzed the InAs surface morphology by AFM characterization. We observed that surface root mean square roughness (RMS) of a sample with one nucleation layer in flat region (areas without holes) is 1.5 nm. The RMS value decreases to 0.7 nm for the sample with 2 nucleation layers. Starting from three nucleation layers, the RMS value is reduced to 0.4 with 0.1 nm error in the measurement. Fig. 2 shows a derivative of an AFM image obtained for the six nucleation layered sample. It is worth mentioning that our Si substrate is quite rough (RMS ~0.3 nm) and polishing traces originating from the Si substrate surface are visible in the AFM image. Also, the AFM data suggests that the InAs grows in triangular nuclei shape and extends in step-flow like growth mode. As shown in Fig. 2, steps are flowing downward relative to the AFM image and step height corresponds to InAs lattice constant height [13]. It should be mentioned that there are a few reports on step-flow growth of InAs on GaAs (0 0 1) which has a lattice mismatch of ~7% [14]. However, we are unaware of any experimental result on successful step-flow growth of InAs on Si (1 1 1), which has a larger lattice mismatch (11.6%). We believe that this is the first comprehensive report and the result of this study could be applied in a variety of device applications.

XRD characterization of the samples demonstrates the high quality of the InAs layer by the clear presence of Pendellösung

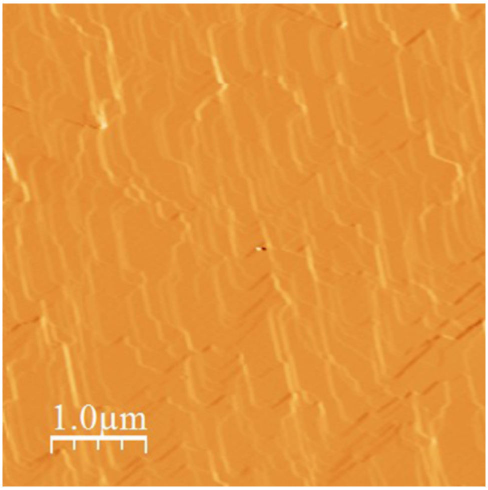

Fig. 2. 5 × 5 μm^2 derivative AFM image of sample with six nucleation layers. The image confirms a step-flow like growth mode, where the atomic step roughness corresponds to InAs lattice constant.

fringes on both sides of the InAs peak. High resolution 2θ/ω-scans of six samples with one–six nucleation layers are shown in Fig. 3. The XRD data shows that as the number of nucleation layers increases, more Pendellösung fringes on either side of the InAs peak are distinguished and the spacing between the fringes decreases. This indicates that the introduction of more nucleation layers results in an improvement in the film quality. FWHM values from the InAs rocking curves are shown in Fig. 3b and it clearly shows a decrease in the FWHM data as more nucleation layers are incorporated and the thickness increases. This decrease of FWHM values could be related to an improvement in film quality and a reduction of the dislocation density. Finally, a simulation analysis shows that incorporating four nucleation layers results in a relaxation of 99.5% in the InAs layer.

3.1.2. Electrical characterization

Results from Hall characterization of our samples are presented in Fig. 4. The data shows a carrier density of 3×10^{18} cm^{-3} and a mobility between 2000 and 3000 cm^2/Vs. The carrier concentrations (n-type) are higher than the intrinsic bulk value for InAs of 8.75×10^{14} cm^{-3} [15] and the electron mobilities are lower compared to typical bulk values of around 40,000 cm^2/(Vs). Compared to previously presented data on similar samples from other groups [16–18] the mobilities are in the range of what can be expected for these thicknesses, but the carrier concentrations are 1–2 orders of magnitude higher in our case [19,20]. The details show that inserting additional nucleation layers increases the mobility as shown in Fig. 4a; for more than two layers, a sharp increase in mobility can be acquired. Also, a change of growth parameters directly affects the electrical characteristics of the samples. As previously stated, lowering the AsH$_3$ flow and raising the growth temperature results in higher mobility films [6].

The effects of temperature on electron mobility and carrier concentration are shown in Fig. 4b. The comparably weak temperature dependence has been previously reported and could be attributed to the small thickness of the epitaxial layers [18].

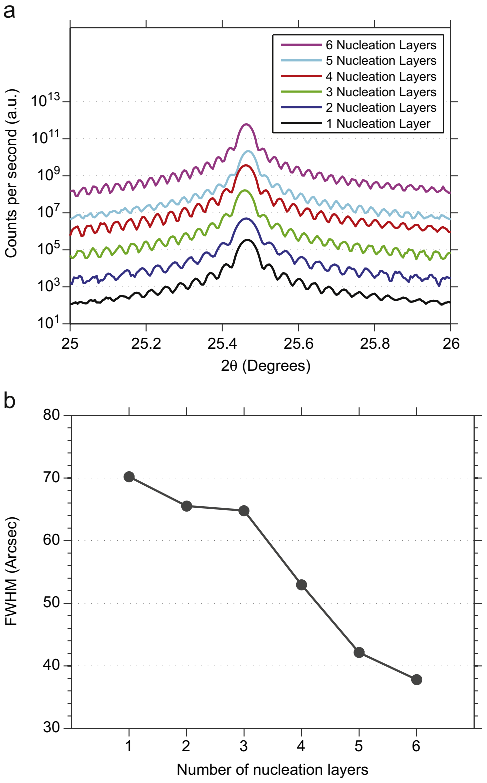

Fig. 3. (a) High resolution 2θ/ω-scans of samples with different number of nucleation layers, respectively. Starting from 2 nucleation layers, the XRD data is shifted upward for clarity. (b) FWHM values from the InAs rocking curve for one–six nucleation layers. The FWHM decreases with increasing number nucleation layers due to film quality improvement and also the increase in film thickness.

Apart from these studies, intentional Sn doping has been incorporated on some InAs films. We have found that it is thereby possible to increase the carrier concentration by at least an order of magnitude. This, however, comes at the cost of a reduced mobility, probably due to increased impurity scattering.

3.2. GaSb on InAs (1 1 1)

We have grown GaSb layers on an InAs deposited with four nucleation layers, shown in Fig. 5b. Depending on the switching sequence of the source materials, different interface structures can be preferentially grown, such as GaAs- and InSb-like. We have investigated GaSb growth with an InSb-like interface type, which is reported to give superior electrical characteristics compared to a GaAs-like interface type [21]. The switching sequence is done in the following order: As off, 3 s pause, In off and simultaneously Sb on, 3 s pause, Ga on, as shown in Fig. 5a.

As reported by other groups as well [22,23], we find that the morphology of the GaSb layer is directly related to the growth temperature and the V/III ratio. We have studied the effect of lowering the V/III ratio on the surface morphology using the same temperature for the InAs layer growth by means of AFM measurement. The study has been performed by keeping the TEGa molar fraction constant and lowering the TMSb molar fraction. Fig. 5c and d show AFM images of the GaSb layer grown on the four nucleation layered InAs buffer layer with TMSb molar fraction of (c) 2.17×10^{-4} and (d) 1.08×10^{-4}. It can be seen that the surfaces of both samples are decorated by clockwise and anti-clockwise hillocks. We attribute the presence of these spiral hillocks to screw dislocations, which arise from the step edges on the InAs surface. The density of spiral hillocks induced by InAs screw dislocations in Fig. 5d is $\sim 8\times10^{6}$ cm^{-2}. Considering the thickness of our GaSb layer (~300 nm), this dislocation density is quite low, which further confirms the high quality of the InAs layer [24].

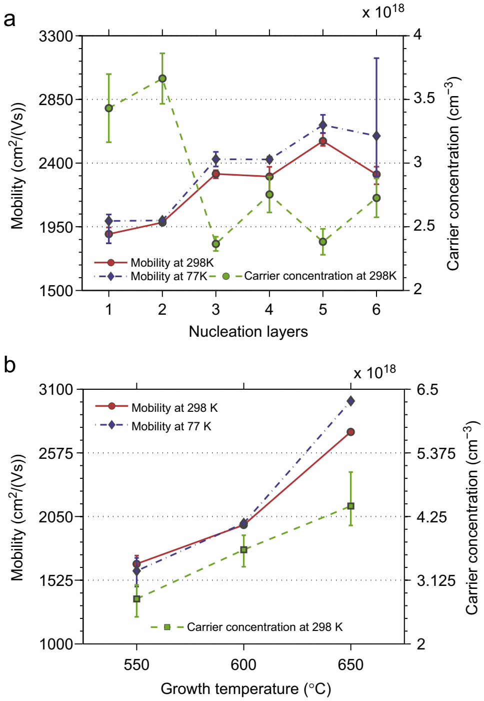

Fig. 4. Mobility and carrier concentration as a function of (a) number of nucleation layers (b) growth temperature. Inserting more nucleation layers and raising the growth temperature increases the mobility of the InAs thin film. The error bars indicate the range between the highest and lowest values in the data set.

For all investigated growth conditions, the formation of different steps is easily distinguishable and the step height corresponds to the GaSb lattice constant. It should be noted that lowering the TMSb flow decreases both size and height of the hillocks on the surface and results in a smoother surface. Moreover, the RMS value is reduced from 3 to 1.5 nm. The power spectral density with respect to the spatial frequency of the surface roughness revealed that the roughness amplitude of the surface decreased considerably with lowering TMSb flow, which is consistent with the RMS value of roughness.

The results from XRD characterization of these samples are shown in Fig. 6a where the first peak from the left corresponds to the GaSb layer. $2\theta/\omega$-spectra of both samples show exactly the same peak position and intensity indicating similar thickness. Our simulation analysis revealed that the GaSb layer is 99.5% relaxed, which explains the small shift in the GaSb peak position. It should be noted that there is no incorporation of In from the underlying InAs layer inside the GaSb film. Finally, the FWHM decreases slightly for the sample with lower TMSb flow.

3.3. *GaSb nanowire growth*

Finally, to demonstrate the use of these GaSb (1 1 1) films as virtual substrates, we have also investigated epitaxial growth of GaSb nanowires on the obtained GaSb film using Au aerosol nanoparticles [25,26]. We have studied the effects of growth temperature and material flow on the nucleation stage and demonstrated the growth of GaSb nanowires on the underlying GaSb layer. To the best of our knowledge, GaSb nanowire growth on a GaSb (1 1 1) substrate has not been previously achieved. We have observed that increasing the TMGa and TMSb molar fractions and lowering the temperature helps the nanowire nucleation, attributed to reduced surface diffusion of the precursors. No nanowire growth was observed for temperatures above 470 °C. SEM inspections of our samples indicate that 420 °C is the optimized temperature for nucleation and that an increased material flow assists the nucleation of more nanowires. However, a higher material flow facilitates radial growth of the nanowires and results in increased nanowire diameter compared to the Au particle. Fig. 6b shows a SEM image of GaSb nanowires grown at 420 °C with a respective TMGa and TMSb molar fractions of 2.13×10^{-5} and 6.84×10^{-5}. It is worth noting that even under our optimum growth conditions, the investigated nanowire growth yield is about 50%. We would like to emphasize that optimization of GaSb nanowire growth would be beyond the scope of this study.

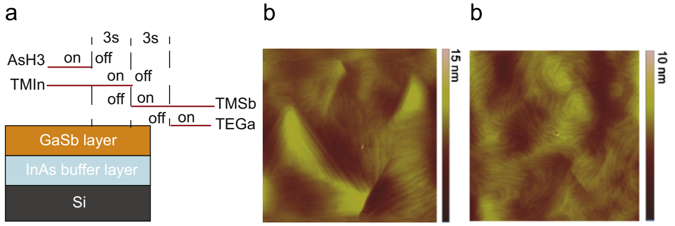

Fig. 5. (a) Switching sequence of material flow used to form an InSb-like interface structure. (b) Schematic structure of GaSb layer grown on the InAs buffer layer. 5×5 μm^2 AFM scan of GaSb layer grown on our InAs buffer layer with TMSb molar fraction of (c) 2.17×10^{-4} and (d) 1.08×10^{-4}. The spiral size and height decreases substantially by lowering the TMSb molar fraction.

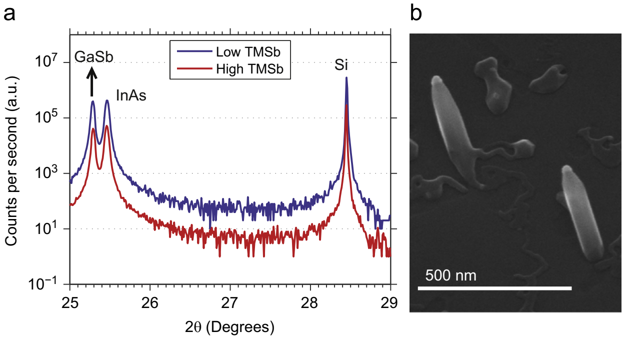

Fig. 6. (a) High resolution $2\theta/\omega$-scan of the respective samples. The blue signal corresponds to the lower TMSb molar fraction (1.08×10^{-4}). It is shifted upward for clarity. (b) SEM image of epitaxially grown GaSb nanowires on the GaSb layer. GaSb nanowires are grown at 420 °C with respective TMGa and TMSb molar fractions of 2.13×10^{-5} and 6.84×10^{-5} (for interpretation of the references to color in this figure legend, the reader is referred to the web version of this article).

4. Summary

This paper reports on successful growth of InAs thin layers on Si (1 1 1) substrates. We have investigated the influence of incorporating additional nucleation layers on the surface morphology and film quality. We have characterized different samples with one–six nucleation layers. It is observed that by inserting additional nucleation layers in the growth process, the surface morphology and quality of the InAs improve significantly. Our systematic study revealed that using four nucleation layers results in the formation of high quality InAs thin layers. We have also presented the successful growth of GaSb thin films on our obtained InAs layers, which offers new possibilities for realization of GaSb (1 1 1) substrates to be used in Si based electronic devices. Finally, we have demonstrated an elegant way to grow GaSb nanowires on the GaSb (1 1 1) substrates. This technology demonstrates the possibility to integrate high performance III/V nanowires transistors [27,28] on Si substrate.

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Paper VII

A High-Frequency Transconductance Method for Characterization of High-κ Border Traps in III-V MOSFETs

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***Abstract*—A novel method that reveals the spatial distribution of border traps in III-V metal–oxide–semiconductor field-effect transistors (MOSFETs) is presented. The increase in transconductance with frequency is explored in a very wide frequency range (1 Hz–70 GHz) and a distributed RC network is used to model the oxide and trap capacitances. An evaluation of vertical InAs nanowire MOSFETs and surface-channel InGaAs MOSFETs with Al_2O_3/HfO_2 high-κ gate dielectric shows a deep border-trap density of about 10^{20} $cm^{-3}eV^{-1}$ and a near-interfacial trap density of about 10^{21} $cm^{-3}eV^{-1}$. The latter causes an almost steplike increase in transconductance at 1–10 GHz. This demonstrates the importance of high-frequency characterization of high-κ dielectrics in III-V MOSFETs.**

***Index Terms*—Al_2O_3, border traps, frequency, HfO_2, high-k, InAs, InGaAs, interface traps, metal–oxide–semiconductor field-effect transistor (MOSFET), nanowire (NW), transconductance.**

I. INTRODUCTION

III-V SEMICONDUCTORS, such as InAs and InGaAs, are attractive as channel material in metal–oxide–semiconductor field-effect transistors (MOSFETs) [1], [2] due to their high electron mobilities and injection velocities [3]. The use of atomic layer deposition (ALD) high-κ dielectric in the gate stack has gained a lot of attention as it enables the scaling of the equivalent oxide thickness below 1 nm while maintaining low gate leakage currents [4]. It is, however, recognized that large densities of traps in the gate oxide and at the oxide–semiconductor interface may severely degrade the performance of III-V MOSFETs. To facilitate optimized high-κ integration and accurate device modeling, it is not only the interface trap densities D_{it} that need to be characterized but also the number of border traps N_{bt} and their spatial distribution.

The charge pumping method [5] used for characterizing N_{bt} in Si CMOS is often not applicable for III-V MOSFETs or nanowire (NW) FETs as no body contact is available. Commonly, N_{bt} is instead deduced indirectly by the conductance $(G–V)$ or capacitance $(C–V)$ [6] methods by measurements on capacitor test structures, which follow a somewhat different processing scheme. Furthermore, it is often only the interface traps that are considered when using these methods. Recently, Sun *et al.* reported on a method with frequency-dependent transconductance $g_m(\omega)$ measurements in the 10^1–10^4-Hz frequency range for the characterization of very deep border traps [7]. By extending the frequency range of the transconductance measurements to much higher frequencies, e.g., 10^{10} Hz, the entire border-trap-depth profile may be characterized, including the region adjoining the oxide–semiconductor interface. Furthermore, radio-frequency (RF) measurements can be used to reveal the intrinsic transconductance g_{mi} as no traps respond at sufficiently high frequencies.

This paper reports on a method for characterizing the distribution of border traps in III-V MOSFETs using frequency-dependent g_m measurements in the 10^0–$7 \cdot 10^{10}$-Hz frequency range. To deduce the $N_{\mathrm{bt}}(x_m)$ depth profile, a transistor model is used where the oxide capacitance C_{ox} is replaced by a distributed RC network. Measurements are performed in the 10^0–10^5-Hz frequency range by a lock-in amplifier and in the 10^5–$7 \cdot 10^{10}$-Hz frequency range by network analyzers. The experimental results are reported for two different device geometries: vertical InAs NW wrap-gate MOSFETs and planar InGaAs MOSFETs. In the latter, a high cutoff frequency $(f_t = 100\ \mathrm{GHz})$ allows for an extension of the characterization method to very high frequencies. A significant increase in g_m is obtained for frequencies above 1 GHz, implying a large number of traps very close to the oxide–semiconductor interface. The model that we propose does not distinguish border traps very close to the semiconductor–oxide interface from interface traps with similar capture cross section. Hence, one interpretation of these results is that the depth profile includes both border and interface traps.

II. DUTs

Fig. 1 schematically shows the two device geometries evaluated in this work: a surface channel $In_{0.53}Ga_{0.47}As$ MOSFET on an InP substrate and a vertical InAs NW wrap-gate MOSFET on a Si substrate. For the planar device, a 10-nm undoped $In_{0.53}Ga_{0.47}As$ layer was grown by molecular beam epitaxy on a p-type $(5 \cdot 10^{16}\ cm^{-3})$ $In_{0.52}Al_{0.48}As$ buffer layer

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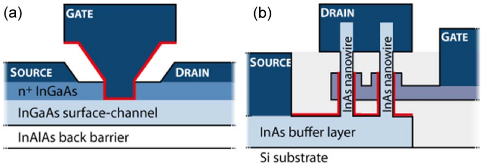

Fig. 1. Cross-sectional schematics of (a) a surface-channel InGaAs MOSFET and (b) a vertical InAs NW MOSFET.

with n-type delta doping of $4 \cdot 10^{12}$ cm^{-3}. ALD was used for depositing a gate dielectric of 0.5-nm Al_2O_3 and 6.5-nm HfO_2 where Al_2O_3 is deposited at 300 °C using TMA and water as precursors and HfO_2 was deposited at 100 °C using TDMA-Hf and water as precursors. Prior to the ALD deposition, the sample was treated with a 21% $(NH_4)S_x$ solution for 20 min at room temperature. Moreover, the device has a gate length of $L_g = 200$ nm and a gate width of $z = 16\ \mu$m. Low access resistance was realized by source/drain regrowth and a self-aligned gate-last process. More details on the device fabrication are found elsewhere [8].

In the vertical NW devices, Sn-doped NWs with 45-nm diameters were grown from Au seed particles by metal–organic vapor phase epitaxy on a 250-nm-thick InAs layer. From the InAs layer, isolated mesa source contacts were formed by etching. Furthermore, the NW FETs have a 0.5-/6.5-nm Al_2O_3/HfO_2 gate dielectric, which was deposited by ALD after NW growth using the same precursor as for the surface-channel MOSFETs. Wrap gates with a gate length of about $L_g = 250$ nm were formed on arrays of vertical NWs by the back-etching of a sputtered W film, and drain contacts were formed at the upper part of the NWs. The array of NWs in each device consists of nominally 192 NWs. A detailed description of the device fabrication may be found elsewhere [9], [10].

The Al_2O_3/HfO_2 gate dielectric used in both devices was chosen as previous studies have shown that a thin Al_2O_3 interface layer gives less interface traps compared with HfO_2 [4]. However, HfO_2 is preferred for the bulk part of the oxide due to its higher permittivity ($\kappa(HfO_2) = 25$, $\kappa(Al_2O_3) = 9$) [11].

III. MEASUREMENT SETUPS

Two different setups were used depending on which part of the frequency range was considered. For low frequencies (1 Hz–100 kHz), g_m was directly measured as the ac source i_s over the ac gate voltage v_g. The setup consisted of a lock-in amplifier with a current amplifier at the input and a resistive bias network at the output. The device under test (DUT) was also dc biased as shown in Fig. 2(a). By connecting the source to the current amplifier, i_s is the input of the lock-in amplifier divided by the multiplication factor of the current amplifier. The resistive network in Fig. 2(a) with three equally large resistances was used for superimposing v_g on a dc gate voltage V_G. Furthermore, the DUTs were measured by on-chip probing, and the dc gate and drain voltages V_G and V_D were applied by a Keithley voltage source.

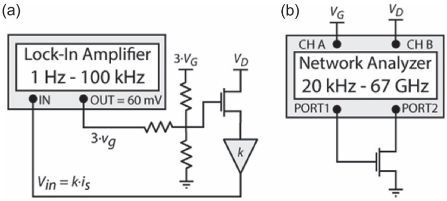

Fig. 2. Schematics of the measurement setups used in (a) the low-frequency range and (b) high-frequency range.

For high frequencies (20 kHz–60 GHz), g_m was deduced from the admittance (y) parameters (as further described in Section IV). For this, scattering (s) parameters were measured by a network analyzer, where V_D and V_G were applied through a bias tee internal to the network analyzer, as shown in Fig. 2(b). Two different network analyzers were used: an R&S ZVC PNA (20 kHz–8 GHz) and an Agilent PNA (40 MHz–67 GHz). The measurements were calibrated off-chip using load–reflect–reflect–match calibration, and the impedance of the probing pads was subtracted from the y parameters using dedicated on-chip de-embedding short and open structures. Both DUTs described in Section II use 50-Ω coplanar pad layouts.

IV. TRANSISTOR BORDER-TRAP MODEL

The spatial distribution of border traps was evaluated from the border-trap capacitance ΔC_{bt} and the time constant of trapping $\tau(x)$ [7], [12]. The latter increases exponentially with tunneling depth x [see (1)] and provides the upper frequency limit for which a trap at depth x is able to respond [12]

$$\tau(x) = \tau_0 e^{x/\lambda}. \tag{1}$$

Here, x is defined as zero at the semiconductor–oxide interface [see Fig. 3(a)]. $\tau_0 = (n\sigma_0 v_{\mathrm{th}})^{-1}$ is the trap time constant at the interface, where n is the carrier density at the semiconductor surface, σ_0 is the cross-sectional area of a trap, and v_{th} is the thermal velocity. $\lambda = \hbar/\sqrt{8m_{\mathrm{ox}}^* \cdot (E_C^{\mathrm{ox}} - E)}$ is the attenuation coefficient of the electron wave function where m_{ox}^* is the effective mass in the oxide and E_C^{ox} is the conduction band edge in the oxide.

The border-trap capacitance ΔC_{bt} reflects the amount of border traps in a slice of the oxide with thickness Δx

$$\Delta C_{\mathrm{bt}} = q^2 \cdot N_{\mathrm{bt}}(x) \cdot \Delta x. \tag{2}$$

Here, $N_{\mathrm{bt}}(x)$ is the density of border traps at depth x. In terms of circuit modeling, the incremental capacitance ΔC_{bt} may be connected in series with an incremental conductance ΔG_{bt}, the value of which is tuned to give the correct time constant $\tau(x)$

$$\tau(x) = \Delta C_{\mathrm{bt}}(x)/\Delta G_{\mathrm{bt}}(x). \tag{3}$$

To describe the distribution of traps at different depths in the oxide, the oxide is divided into incremental steps ΔC_{ox} corresponding to the slices of the oxide with the width Δx. At each depth, an RC leg that express $\tau(x)$ at that particular oxide depth [12] is connected [see Fig. 3(b)].

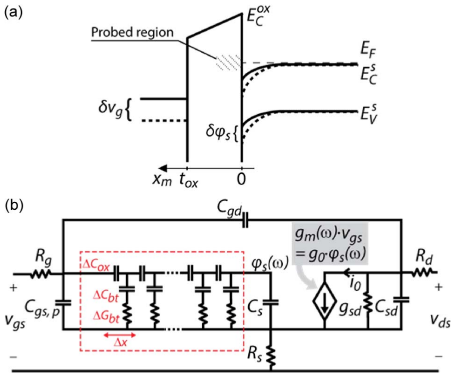

Fig. 3. (a) Illustration of the probed regions induced by an ac gate voltage. (b) Distributed RC network representation of the (marked in pink) gate dielectric inserted in a standard FET small-signal model. For a FET without traps, this RC network reduces to C_{ox}. Each leg of the RC network represents a slice of C_{ox} at a certain depth x_m with the width Δx and the capacitance ΔC_{ox}.

Using the expressions in (2) and (3), the change in voltage and current caused over one incremental step Δx may be expressed in the continuous limit by the following differential equations:

$$\begin{cases} \frac{\partial v}{\partial x} &= -\frac{i(x)}{j\omega\varepsilon_{\text{ox}}} \\ \frac{\partial i}{\partial x} &= -\frac{v(x)\cdot j\omega q^2 N_{\text{bt}}(x)}{1+j\omega\tau(x)}. \end{cases} \tag{4}$$

The approach for deriving the aforementioned equations is the same as for standard transmission line models. The equations were then used to deduce the y parameters of the distributed RC network. The y parameters of the complete transistor small-signal model were obtained by inserting the y parameters of the distributed RC network in a standard FET model, as shown in Fig. 3. To extract the various small-signal parameters, the source and drain resistances (extracted from dc measurements) were first subtracted from the y parameters. The values for gate resistance R_g, gate–drain capacitance C_{gd}, and parasitic gate–source capacitance $C_{\text{gs},p}$ were deduced from the y parameters of the DUT under the assumption that the input conductance is much smaller than 1 and that $\omega^2 \cdot R_g \cdot C_\Sigma^2 \ll 1$ [13]. Here, $C_\Sigma = C_{\text{gd}} + C_{\text{gs},p} + C_{\text{gs}}$ is the total input gate capacitance.

According to the small-signal model, $g_m(\omega)$ can be deduced from the y parameters of the DUT as the real part of y_{21} with a small modification for high frequencies [13]

$$\text{Re}(y_{21}) = \text{Re}\left(g_m(\omega)\right) - \omega^2 R_g C_{\text{gd}} C_\Sigma. \tag{5}$$

The effects of border traps on the transconductance can thus be captured from $\text{Re}(y_{21})$ as long as $\omega^2 \cdot R_g \cdot C_{\text{gd}} \cdot C_\Sigma \ll g_m$ and $\text{Im}(g_m) \ll \text{Re}(g_m)$. The imaginary part of g_m is due to the phase lag from the distributed RC network and was found to be small compared with the real part for all samples and measurement frequencies used in this work.

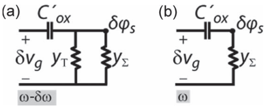

Fig. 4. Admittance models of the oxide at ω–$\delta\omega$ in (a) and at ω in (b).

To find the intrinsic high-frequency transconductance g_{mi}, we considered the voltage drop over the oxide, i.e., how well δv_{gs} translates into a surface potential $\delta\varphi_s$ [see Fig. 3(a)]. For most frequencies, the relationship between δv_{gs} and $\delta\varphi_s$ is complicated as charge is induced not only in the channel but also in the traps. This is also the origin of the frequency dependence of the extrinsic transconductance $g_m(\omega)$. However, for sufficiently high frequencies, no charge traps respond due to the time constant of the trap capturing process. At these frequencies, the distributed RC network reduces to the ordinary trapless C_{ox} and the expression for g_{mi} simplifies to

$$g_{\text{mi}} = \left.\frac{\partial i_0}{\partial v_{\text{gs}}}\right|_{\omega\to\infty} = v_{\text{inj}} \cdot z \cdot C_s \frac{C_{\text{ox}}}{C_{\text{ox}} + C_s} = g_0 \cdot \frac{C_{\text{ox}}}{C_{\text{ox}} + C_s}. \tag{6}$$

This expression also relates g_0 to $g_m(\omega)$, as shown in Fig. 3(b). v_{inj} is the injection velocity, z is the gate width, and C_s is the semiconductor (or quantum) capacitance of the channel.

An analytical expression is deduced for simple calculations of $N_{\text{bt}}(x_m)$. Here, it is assumed that, for an incremental change in frequency between ω and $\omega - \delta\omega$, all traps at a thickness δx around a point x_m charge and discharge during one cycle [7]. Equation (1) gives the following expressions for δx and x_m:

$$\delta x = -\lambda\delta\ln(\omega) \tag{7}$$

$$x_m = \lambda\ln(\omega_0/\omega). \tag{8}$$

The admittance models of the oxide at the two frequencies ω and ω–$\delta\omega$ are shown in Fig. 4. The part of the oxide located beyond x_m can be treated as an ordinary capacitance, i.e., $C'_{\text{ox}} = C_{\text{ox}}/((1 - x_m)/t_{\text{ox}})$, as no traps respond in this part of the oxide at this frequency. The admittance at a distance x_m into the oxide within the thickness δx and is given by

$$y_T = \frac{j\omega q^2 N_{\text{bt}}(x_m)\delta x}{1 + j\omega\tau(x_m)}. \tag{9}$$

The admittance corresponding to the remainder of the oxide and semiconductor capacitance is described by y_Σ. This admittance also gives a relationship between the frequency-dependent transconductance $g_m(\omega)$ and the intrinsic transconductance g_{mi}

$$\begin{aligned} g_m(\omega) &= \frac{j\omega C'_{\text{ox}}}{(y_\Sigma + j\omega C'_{\text{ox}})} \cdot \frac{C_{\text{ox}} + C_s}{C_{\text{ox}}} \cdot g_{\text{mi}} \\ &= \frac{j\omega C'_{\text{ox}}}{(y_\Sigma + j\omega C'_{\text{ox}})} \cdot g_0. \end{aligned} \tag{10}$$

To account for the derivative of $g_m(\omega)$ in the expression for $N_{\text{bt}}(x_m)$, the variation in φ_s at the frequencies ω and ω–$\delta\omega$ is considered. From Fig. 4, we obtain

$$\delta\varphi_s^{\omega} = \frac{j\omega C'_{\mathrm{ox}}}{y_\Sigma + j\omega C'_{\mathrm{ox}}}\delta v_g \tag{11}$$

$$\begin{aligned}\delta\varphi_s^{\omega-\delta\omega} &= \frac{j\omega C'_{\mathrm{ox}}}{y_\Sigma + y_T + j\omega C'_{\mathrm{ox}}}\delta v_g \\ &\approx j\omega C'_{\mathrm{ox}}\delta v_g\left(\frac{1}{j\omega C'_{\mathrm{ox}} + y_\Sigma}\right. \\ &\qquad \left. - \frac{j\omega q^2 N_{\mathrm{bt}}\delta x}{(1+j\omega\tau)\left(j\omega C'_{\mathrm{ox}} + y_\Sigma\right)^2}\right).\end{aligned} \tag{12}$$

In (12), a first-order Taylor expansion in δx is assumed. The change in channel potential with frequency is subsequently given by

$$\delta(\delta\varphi_s) = \delta\varphi_s^{\omega-\delta w} - \delta\varphi_s^{\omega}. \tag{13}$$

Using (7) and (11)–(13), we obtain

$$\frac{\delta g_m(\omega)}{\delta\ln(\omega)} = \frac{\delta(\delta\varphi_s)g_0}{\delta\ln(\omega)\delta v_g} = \frac{j\omega C'_{\mathrm{ox}} j\omega q^2 N_{\mathrm{bt}}\lambda g_0 g_m^2(\omega)}{(1+j\omega\tau)\left(j\omega C'_{\mathrm{ox}}\right)^2 g_0^2}. \tag{14}$$

Solving for $N_{\mathrm{bt}}(x_m)$ and taking the real part, we finally obtain the approximate analytical expression

$$N_{\mathrm{bt}}(x_m) \approx \frac{(C_s + C_{\mathrm{ox}})\cdot g_{\mathrm{mi}}}{q^2\lambda\cdot\left(1-\frac{x_m}{t_{\mathrm{ox}}}\right)\cdot g_m^2(\omega)}\cdot\frac{\partial g_m(\omega)}{\partial\ln(\omega)}. \tag{15}$$

Note that, for a III-V quantum-well FET, $C_s \approx (q^2\cdot m^*)/(\pi\cdot\hbar^2)$. The analytical expression in (15) is particularly suitable for materials, such as InAs, where C_s is comparable to or smaller than C_{ox}. For these materials, the variation in surface potential with gate voltage is larger, resulting in larger $\delta g_m(\omega)/\delta ln(\omega)$. Note also that, for very deep border traps, the oxide band bending is more pronounced and is likely to be responsible for $\delta g_m(\omega)/\delta ln(\omega)$ rather than $\delta\varphi_s$. Furthermore, (15) requires knowledge of g_{mi}, which is found using RF measurements at high enough frequencies where no traps respond.

V. RESULTS AND DISCUSSION

The transfer characteristics for an InGaAs surface-channel MOSFET are shown in Fig. 5. Here, the transconductance is deduced both from dc and RF measurements (20 GHz). The curves have similar shape and show a peak transconductance close to $V_G = 0.1$ V; however, g_m is about three times higher at RF.

Also, it should be noted that all measurements on the surface-channel MOSFET presented in this work were conducted about six months after device fabrication. During this time, the peak dc transconductance has degraded by a factor of three and the threshold voltage has shifted more than 0.5 V, indicating the creation of excess defects in the oxide. Aging is particularly pronounced for these devices as no passivation is used and the gate oxide is directly exposed to air, which could cause damages such as an increased number of traps in the oxide.

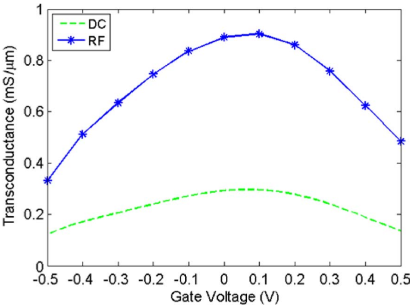

Fig. 5. Transconductance as a function of gate voltage for two different measurements on an InGaAs surface-channel MOSFET is plotted. The green dotted line shows the g_m deduced from dc measurements, and the blue starred line shows the g_m deduced from RF measurements. A drain voltage of $V_D = 0.55$ V was used. The threshold voltage is $V_t = -0.5$ V.

Fig. 6 shows the frequency dependence of g_m for the vertical InAs NW MOSFET and InGaAs surface-channel MOSFET measured in the 1 Hz–67 GHz-frequency range. For low frequencies (below 100 MHz), g_m increases at a rate of about 0.009 mS/μm per decade and 0.006 mS/μm per decade for the NW and surface-channel devices, respectively, which result in roughly a doubling of g_m from dc up to 100 MHz. These high rates in the two DUTs distinctly indicate high densities of deep border traps in both devices.

In the frequency interval between 1 and 10 GHz, a dramatic increase in g_m is seen for the surface-channel device with an increase of roughly 0.30 mS/μm per decade. The largest effect is seen for the bias conditions that give the highest g_m; still, the same trend was observed for all measured gate voltages (−0.5–0.5 V) and for low drain voltage ($V_D = 50$ mV). This steep slope in the $g_m(\omega)$ graph implies that the trap profile is dominated by traps very close to the oxide–semiconductor interface. For frequencies above 10 GHz, a plateau is observed, which corresponds to an intrinsic transconductance of about $g_{\mathrm{mi}} = 0.66$ mS/μm. Similar transconductance behavior has been observed also in other MOSFETs on the same chip, in MOSFETs on other chips, and using two different network analyzers. For the NW MOSFET, the moderate f_t of a few gigahertz and the large parasitic capacitances unfortunately veil any similar effects as described in (5). The deduced $g_m(\omega)$ is only valid up to about 1 GHz for the NW device. It should be noted that when calculating $N_{\mathrm{bt}}(x_m)$, the intrinsic transconductance is set to $g_{\mathrm{mi}} = 0.16$ mS/μm for the NW device, which is an underestimation if the slope of $g_m(\omega)$ at high frequencies is similar to the surface-channel MOSFET. However, the accuracy is still sufficient to give a good indication of $N_{\mathrm{bt}}(x_m)$ also for the NW MOSFET.

Fig. 7 shows the quantitative border-trap-depth profiles of the vertical InAs NW MOSFET and the InGaAs surface-channel MOSFET, which are deduced from the measured $g_m(\omega)$ using (15) with $\lambda = 1.1\cdot 10^{-8}$ cm. For the InGaAs surface-channel device, N_{bt} is dominated by a large peak situated within a few angstroms from the oxide–semiconductor interface. The magnitude of the peak provides a large density of near-interfacial traps of $N_{\mathrm{bt}}(x_m) = 10^{21}$ cm^{-3}eV^{-1}. It is possible that the interface between the Al_2O_3 and HfO_2 in the gate dielectric, located at

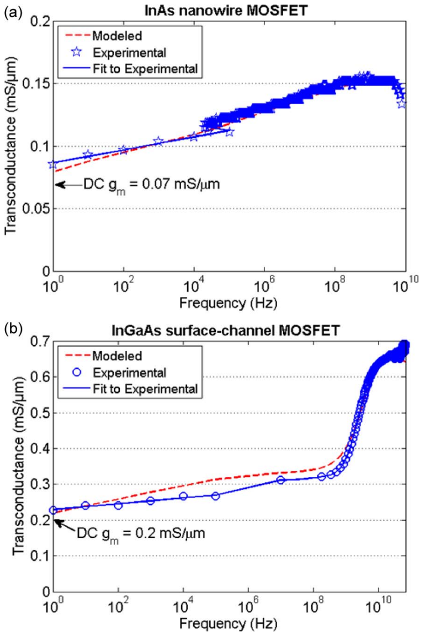

Fig. 6. Transconductance as a function of frequency for (a) a vertical InAs NW MOSFET at dc $V_D = 0.55$ V and dc $V_G = -0.4$ V and (b) an InGaAs surface-channel MOSFET at dc $V_D = 0.55$ V and dc $V_G = -0.3$ V. Here, g_m is represented by $\mathrm{Re}(y_{21})$ for the de-embedded s parameters in the case of measurements from the network analyzers. The measured g_m is shown by blue stars; a fit to the measured data is shown by a dashed blue line; and the g_m of the model using (15) is shown by a solid red line. For comparison, the dc g_m is also shown in the two graphs. The threshold voltage is $V_t = -0.5$ V for both MOSFETs.

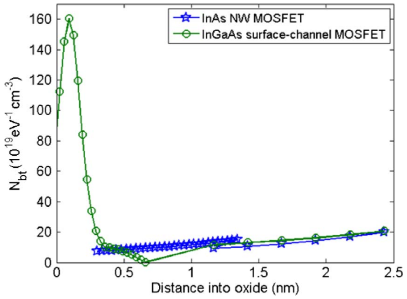

Fig. 7. Number of border traps at different oxide depths deduced from the $g_m(\omega)$ in Fig. 6 for (blue curve) a vertical InAs NW MOSFET and (green curve) a surface-channel InGaAs MOSFET.

about 0.5-nm depth, contributes to the increased $N_{\mathrm{bt}}(x_m)$ [14]. In addition, it could even be argued that this is why a peak is observed. However, preliminary evaluation of MOSFETs with pure $\mathrm{HfO_2}$ gate dielectric have shown similar $g_m(\omega)$ behavior, indicating that the $\mathrm{Al_2O_3/HfO_2}$ interface is not the culprit.

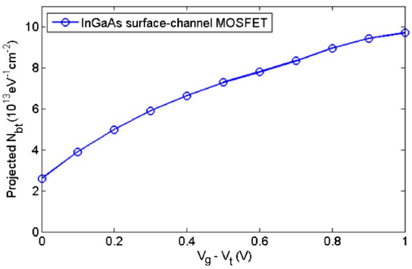

Fig. 8. Voltage dependence of the projected number of border traps is presented. Here, the peak in $N_{\mathrm{bt}}(x_m)$ is integrated for frequencies down to 40 MHz; however, the deep border traps are neglected. $V_t = -0.5$ V is subtracted from V_G.

Another possibility is that the peak is partially or fully caused by interface traps. As the capture/emission mechanism suggested for trapping inside the semiconductor conduction band is also associated with a characteristic frequency $\omega_{0,\mathrm{it}}$ and as all interface traps are located at the interface, the $g_m(\omega)$ dependence is expected to show an abrupt increase at $\omega_{0,\mathrm{it}}$. This means that Fig. 6(b) could be interpreted as the $g_m(\omega)$ dependence of the interface traps superimposed on the $g_m(\omega)$ dependence of the border traps. However, it is a delicate issue to judiciously distinguish between different trapping mechanisms. In addition, it may not be possible to describe the interface between InGaAs and $\mathrm{Al_2O_3}$ as atomically abrupt, but instead, it is associated with a more complex transition region. Furthermore, the x-axis is dependent on τ_0 for which a large variation is found in the reported values [12]. A value of $\tau_0 = 4 \cdot 10^{-11}$ s was chosen as it corresponds well to the frequency where g_m ceases to increase and gives the smallest error when comparing modeled and measured g_m's. It should be noted that the uncertainty of τ_0 limits the spatial resolution of this method.

A smaller density of *deep* border traps of about $N_{\mathrm{bt}}(x_m) = 10^{20}\ \mathrm{cm^{-3} \cdot eV^{-1}}$ are observed for both DUTs. The similar values for the two DUTs suggest that the density of deep border traps is not greatly affected by the device geometry or choice of semiconductor. These values are also similar to what has been observed from C–V measurements on InGaAs/$\mathrm{Al_2O_3}$ capacitors ($N_{\mathrm{bt}} \sim 4.5 \cdot 10^{19}\ \mathrm{eV^{-1}cm^{-3}}$) [12]. Moreover, $N_{\mathrm{bt}}(x_m)$ appears to increase somewhat with depth; however, we suggest that this is due to measurement errors.

A projected density of traps of $N_{\mathrm{bt,int}} = 5 \cdot 10^{13}\ \mathrm{cm^{-2} \cdot eV^{-1}}$ is calculated for the surface-channel MOSFET by integrating over the measured depths. Fig. 8 shows the total N_{bt} calculated from measurements at different gate voltages. Here, it is observed that the total N_{bt} increases with increasing voltage. In the presented voltage interval, e.g., $V_G = -0.5$ V to $V_G = 0.5$ V, the Fermi level is understood to be above the conduction band edge as the device is in its ON-state. Hence, Fig. 8 shows that the total N_{bt} increases as the Fermi level is moved up in the conduction band, which is consistent with the extractions of the density of interface traps for InGaAs C–V structures [15].

To verify the model, the analytically extracted border-trap density is used as input to the full device model in Fig. 3(b), giving a modeled extrinsic g_m as shown in Fig. 6. The analytically extracted border-trap density is thus seen to give a good reproduction of the measured g_m.

VI. CONCLUSION

We have reported a novel method for the characterization of border traps in III-V MOSFETs. The method combines $g_m(\omega)$ measurements with y parameter modeling of the oxide and trap capacitances using a distributed RC network. From this, an analytical expression has been deduced, giving the density of border traps as a function of oxide depth. The method has been demonstrated for an InGaAs surface-channel MOSFET and a vertical InAs NW MOSFET. For both DUTs, $g_m(\omega)$ was steadily increased throughout the 1 Hz–100 MHz frequency range. For the surface-channel MOSFET, a steep increase in $g_m(\omega)$ was observed at about 1–10 GHz. For even higher frequencies, a plateau was observed corresponding to the intrinsic transconductance. The method hence revealed that the spatial distribution of border traps is dominated by trap states very close to the oxide–semiconductor interface with $N_{\mathrm{bt}} = 10^{21}$ cm$^{-3} \cdot$ eV^{-1}, whereas the density of deep border traps is about $N_{\mathrm{bt}} = 10^{20}$ cm$^{-3} \cdot$ eV^{-1}. The high N_{bt} is reasonable when considering the performance degradation of III-V MOSFETs compared with other III-V FETs, such as HEMTs and buried-channel MOSFETs, and it further emphasizes the importance of optimizing the high-κ integration in III-V MOSFETs.

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