III-V MOSFETs for High-Frequency and Digital Applications

Zota, Cezar

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III-V MOSFETs for High-Frequency and Digital Applications

Doctoral Thesis

Cezar Bogdan Zota

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Cezar Bogdan Zota
Department of Electrical and Information Technology
Lund University
Ole Römers väg 3, 223 63 Lund, Sweden

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Abstract

III-V compound semiconductors are used in, among many other things, high-frequency electronics. They are also considered as a replacement for silicon in CMOS technology. Yet, a III-V transistor outperforming state-of-the-art silicon devices in VLSI-relevant metrics has not yet decisively been demonstrated. In this work, the limits of III-V FET performance, for both RF and VLSI applications, are explored experimentally.

MOSFETs using selectively grown lateral InGaAs nanowires as the channel are demonstrated. The performance of devices using this technology includes among the highest reported transconductance for any transistor of 3.3 mS/µm, among the lowest subthreshold slope of a III-V FET at sub-100 nm gate length of 66 mV/decade, as well as the highest reported on-current (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) of 650 µA/µm, for any transistor, thus outperforming current industrial silicon MOSFETs. RF-compatible devices exhibit extrapolated f_t and f_{max} of 275 GHz and 400 GHz, respectively, the highest combined values for a III-V MOSFET. Junctionless InGaAs transistors where also fabricated, demonstrating a simplified process scheme and record performance for junctionless devices, with g_m = 1.6 mS/µm and SS = 76 mV/decade.

Several techniques for characterization of these kinds of devices have also been developed. Low-temperature measurement of single nanowire transistors revealed the presence of quantized conductance, among the first reports for a high-performance device. From the quantized conductance, the electron mean free path was determined in the range of 140 to 180 nm, indicating excellent material quality and device operation deep in the ballistic regime. Furthermore, it was shown that subband quantization significantly impacts device performance through threshold voltage variability.

Oxide characterization was performed through hysteresis measurements, leading to a general method of determining trap distributions of specific surfaces in a multi-gate FET. Finally, noise characterization in terms of 1/f and RF noise was performed on single nanowire devices and RF-compatible devices, respectively, showing low input gate voltage noise and promising RF noise performance.

Populärvetenskaplig Sammanfattning

Bara sedan de senaste 50 åren har datorerna förändrat våra liv och vårt samhälle i grunden. De har skapat den digitala eran och informationsåldern. Allt detta började 1947, då Shockley, Bardeen och Brattain, tre forskare vid Bell Labs i USA uppfann transistorn, för vilken de senare vann Nobelpriset i fysik. Transistorn föddes ur ett behov av att förstärka elektriska signaler, något som man tidigare hade gjort främst med elektronrör. Dessa hade många användningsområden, till exempel för radio och telefoni, men begränsades av hög effektförbrukning och av att de lätt gick sönder. Den första transistorn bestod av en halvledarkristall, germanium, med tre metallkontakter, och den visade sig inte bara fungera som utmärkt förstärkare av elektriska signaler, utan också lösa de problem som hörde till elektronrören.

Elektronikindustrin tog fart på riktigt först med uppfinnandet av den integrerade kretsen, på slutet av 50-talet, av forskare på Texas Instrument. Där man tidigare satte ihop elektriska kretsar för hand med pincetter, kunde man med den integrerade kretsen tillverka alla kretselementen direkt på halvledarkristallen. Detta underlättade tillverkningen enormt, och tillät en kontinuerlig utveckling, med mindre, snabbare och energisnålare kretsar– en utveckling som fortsätter ännu idag, och bygger främst på halvedaren kisel.

Dagens teknologi har emellertid blivit så komplex, och de minsta beståndsdelarna av transistorn har blivit så små, att en vidare utveckling snart förespås bli svår. Ett av problemen är att energiförbrukningen per area i en processor, som består av flera miljarder transistorer på en yta av någon kvadratcentimer, har blivit exceptionellt hög– snart lika hög som i en kärnreaktor. Detta gör chippet svårt att kyla, och kan leda till att det slutar fungera.

Där den tidigare utvecklingen främst byggt på att göra transistorn mindre, har forskare på senare år börjat se till andra typer av förbättringar. En sådan möjlig förbättring är användandet av III-V sammansatta halvledare, till exempel indium-gallium-arsenid, även kallad InGaAs. Elektroner i InGaAs har en högre hastighet än i kisel, vid samma spänning. Genom att sänka drivspänningen till ett chip byggt med InGaAs, kan det fungera lika bra som ett byggt med kisel, men förbruka mindre energi. Denna avhandling omfattar design och tillverkning av InGaAs-transistorer som visas slå kisel-transistorer i viktiga prestandamått, och representerar de bäst presterande transistorerna för lågenergiapplikationer som någonsin tillverkats.

Acknowledgments

This thesis is dedicated to my mother for her unwaivering support and endless kindness. Time flies, but some things remain the same, and I am thankful for that.

I would like to express my gratitude to my supervisor Erik. We have shared many things over these last few years, have had many ideas, some excellent, some merely good, and the rest forgotten. But personally, I will never forget my time here, and I hope our friendship will last through the years.

Lars-Erik, you have been a role model to me, in arts both technical and not. The many things I have learned from you, I will value for life.

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Also, my colleagues at the department of Solid State Physics and friends in the lab, Tim, Peter, Bekmurat, David, Robert, Erik, Malin, Simon, Neimantas, Vishal, to name a few.

My sincere gratitude is also dedicated professor Takagi-sensei and professor Takenaka-sensei, under whose supervision I began my journey into science. Sang-Hyeon, Noguchi, Chang, Sang-Hoon and all my colleagues from Tokyo University, have my sincerest gratitude and friendship.

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And, of course, my friends and family, my girlfriend and our dog. Sniff, from your love of playing with rocks, we all have much to learn.

Cezar Bogdan Zota
Lund, June 2017

Contents

List of Papers

This thesis is based on the work presented in the following papers, referred to by their roman numerals. They are organized here into three groups: *low-power digital applications*, *high-frequency applications* and *device and material characterization*.

LOW-POWER DIGITAL APPLICATIONS

Paper I: C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "InGaAs Tri-gate MOSFETs With Record On-current," *2016 IEEE Int. Electron Devices Meeting (IEDM)*, pp. 3.2.1–3.2.4, Dec. 2016.

▶ *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper II: C. B. Zota, L.-E. Wernersson and E. Lind, "High-Performance Lateral Nanowire InGaAs MOSFETs With Improved On-Current", *IEEE Electron Device Letters*, vol. 37, no. 10, pp. 1264–1267, Oct. 2016.

▶ *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper III: C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "InGaAs Nanowire MOSFETs With $I_{ON} = 555$ uA/um at $I_{OFF} = 100$ nA/um and $V_{DD} = 0.5$" *Symposium on Very Large Scale Integrated Circuits and Technology (VLSI)*, Jun. 2016.

▶ *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper IV: C. B. Zota, L.-E. Wernersson and E. Lind, "Single Suspended InGaAs Nanowire MOSFETs," *2015 IEEE Int. Electron Devices Meeting (IEDM)*, pp. 31.2.1–31.2.4, Dec. 2015.

▶ *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper V: C. B. Zota, L.-E. Wernersson and E. Lind, "$In_{0.53}Ga_{0.47}As$ Multiple-Gate Field-Effect Transistors With Selectively Regrown Channels," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 342–344, Mar. 2014.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

HIGH-FREQUENCY APPLICATIONS

Paper VI: C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "High-Frequency InGaAs Tri-Gate MOSFETs With f_{max} of 400 GHz," *Electronics Letters*, vol. 55, no. 22, pp. 1869–1871, Sept. 2016.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper VII: C. B. Zota, G. Roll, L.-E. Wernersson and E. Lind, "Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4078–4083, Dec. 2014.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper VIII: C. B. Zota, L.-E. Wernersson and E. Lind, "$In_{0.63}Ga_{0.37}As$ FinFETs using selectively regrown nanowires with peak transconductance of 2.85 mS/μm at $V_{ds} = 0.5$ V," *72nd Annual Device Research Conference (DRC)*, pp. 209–210, Jun. 2014.

► This paper won the 72nd DRC best student paper award.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

DEVICE AND MATERIAL CHARACTERIZATION

Paper IX: C. B. Zota, D. Lindgren, L.-E. Wernersson and E. Lind, "Quantized Conduction and High Mobility in Selectively Grown $In_xGa_{x-1}As$ Nanowires," *ACS Nano*, vol. 9, no. 10, pp. 9892–9897, 2015.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper X: C. B. Zota and E. Lind, "Size-Effects in Indium Gallium Arsenide Nanowire Field-Effect Transistors," *Applied Physics Letters*, vol. 108, no. 6, p. 063505, 2016.

► *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper XI: S. Netsu, M. Hellenbrand, C. B. Zota, Y. Miyamoto and E. Lind, "A Method for Determining Trap Distributions of Specific Channel Surfaces in InGaAs Tri-gate MOSFETs," *IEEE Journal of the Electron Device Society*, in review, 2017.

▶ *I performed the device fabrication and helped to write the paper.*

Paper XII: C. Möhle, C. B. Zota, M. Hellenbrand and E. Lind, "1/f and RTS Noise in InGaAs Nanowire MOSFETs," *Microelectronics Journal*, accepted for publication, 2017.

▶ *I performed the device fabrication and helped to write the paper.*

EXTRANEOUS PAPERS

The following papers are not included in the thesis, but summarise related work which I have contributed to.

Paper XIII: C. B. Zota, M. Borg, L.-E. Wernersson and E. Lind, "Record Performance for Junctionless Transistors in InGaAs MOSFETs" *Symposium on Very Large Scale Integrated Circuits and Technology (VLSI)*, Jun. 2017.

▶ *I designed, fabricated and measured the devices, as well as wrote the paper.*

Paper XIV: C. B. Zota, L.-E. Wernersson and E. Lind, "High transconductance, f_t and f_{max} in $In_{0.63}Ga_{0.37}As$ FinFETs using a novel fin formation technique," *26th International Conference on Indium Phosphide and Related Materials (IPRM)*, May 2014.

▶ Invited paper, presented at the conference by the author of this thesis.

▶ *I designed, fabricated and measured the devices; wrote the paper.*

Paper XV: C. B. Zota, S.-H. Kim, M. Yokoyama, M. Takenaka and S. Takagi, "Characterization of Ni-GaSb alloys formed by direct reaction of Ni with GaSb," *Applied Physics Express*, vol. 5, no. 7, pp. 071201, 2012.

Paper XVI: C. B. Zota, S.-H. Kim, Y. Asakura, M. Takenaka and S. Takagi, "Self-aligned metal S/D GaSb p-MOSFETs using Ni-GaSb alloys," *70th Annual Device Research Conference (DRC)*, pp. 71–72, Jun. 2012.

Paper XVII: C. B. Zota, L.-E. Wernersson and E. Lind, "Self-aligned metal S/D GaSb p-MOSFETs using Ni-GaSb alloys," *GigaHertz 2014*, Gothenburg, Sweden, Mar. 2014.

Paper XVIII: C. B. Zota, L.-E. Wernersson and E. Lind, "Conductance quantization in Quasi-ballistic InGaAs nanowire MOSFETs," *73rd Annual Device Research Conference (DRC)*, pp. 257–258, Jun. 2015.

Paper XIX: F. Lindelöw, C. B. Zota, L.-E. Wernersson and E. Lind, "High transconductance InGaAs Nanowire MOSFETs," *GigaHertz 2016*, Linkoping, Sweden, Mar. 2016.

Paper XX: F. Lindelöw, C. B. Zota and E. Lind, "Hall effect measurements on lateral InGaAs nanowire transistors," *Nanowire Week 2017*, accepted for poster presentation, 2017.

Paper XXI: F. Lindelöw, C. B. Zota, L.-E. Wernersson and E. Lind, "Gated Hall Effect Measurements on Selectively grown InGaAs Nanowires," *Nanotechnology*, accepted for publication, 2017.

Paper XXII: C. Möhle, C. B. Zota, M. Hellenbrand and E. Lind, "1/f and RTS Noise in InGaAs Nanowire MOSFETs," *Conference on Insulating Films on Semiconductors (INFOS)*, Jun., 2017.

Paper XXIII: C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "High-Performance Field-Effect Transistors Using Selectively Grown Lateral InGaAs Nanowires," *Nanowire Week 2017*, Jun., 2017.

Paper XXIV: L. Ohlsson, F. Lindelöw, C. B. Zota, M. Ohlrogge, T. Merkle, L.-E. Wernersson and E. Lind, "First InGaAs Lateral Nanowire MOSFET RF Noise Measurements and Model," *75rd Annual Device Research Conference (DRC)*, Jun., 2017.

Abbreviations and Symbols

ABBREVIATIONS

$(NH_4)_2S$ diammonium sulphide

AC alternating current
Al aluminum
Al_2O_3 aluminum oxide
ALD atomic layer deposition

CMOS complementary metal-oxide-semiconductor
CPU central processing unit

DOS density of states
DUT device under test

EOT effective oxide thickness

FET field-effect transistor

GAA gate-all-around
GaAs gallium arsenide
GaSb gallium antimonide

H_2O_2 hydrogen peroxide
H_3PO_4 phosphoric acid
HCl hydrochloric acid
HEMT high-electron-mobility transistor
HF hydrofluoric acid
HfO_2 Hafnium oxide
HSQ hydrogen silsesquixane

In indium
InAlAs indium aluminum arsenide
InAs indium arsenide
InGaAs indium gallium arsenide

InP indium phosphide
ITRS international technology roadmap for semiconductors

La_2O_3 lanthanum oxide

Mo molybdenum
MOCVD metal organic chemical vapor deposition
MOSCAP metal-oxide-semiconductor capacitor
MOSFET metal-oxide-semiconductor field-effect transistor

NH_4OH ammonium hydroxide
Ni nickel

Pd palladium
PDA post-deposition annealing
PMMA poly(methyl methacrylate)

QCL quantum capacitance limit

RF radio-frequency

S. I. semi-insulating
S/D source and drain
Si silicon
SiO_2 silicon dioxide
Sn tin
SPL single pixel line
SRAM static random access memory
SS inverse subthreshold slope

TESn tetraethyltin
Ti titanium
TiN titanium nitride

VLS vapour-liquid-solid
VLSI very-large-scale integration

W tungsten

Y_2O_3 yttrium oxide

ZrO_2 Zirconium oxide

GREEK SYMBOLS

$\varepsilon(0)$ top of the barrier energy
λ mean free path
μ carrier mobility
σ surface energy
β adhesion energy
ρ_C specific contact resistivity
κ dielectric constant

LATIN SYMBOLS

C_{it} capacitance due to interface traps
C_L load capacitance
C_{OX} oxide capacitance
C_Q quantum capacitance

D diffusion constant
D_{it} density of interface traps

E_F Fermi level
E_G band gap

f_{max} maximum oscillation frequency
f_t cut-off frequency

G Gibb's free energy
g_d output conductance
g_m transconductance

I_{OFF} off-state current
I_{ON} on-state current

k wave vector

L_G gate length

M number of conducting subbands
m^* effective electron mass

N_D donor doping concentration

$\boldsymbol{n_{1D}}$ 1-D carrier density under bias
$\boldsymbol{n_0}$ carrier density under zero bias

$\boldsymbol{Q}$ channel charge

$\boldsymbol{R_g}$ gate resistance
$\boldsymbol{R_{ON}}$ on-resistance

$\boldsymbol{T}$ ballistic transmission
$\boldsymbol{T_L}$ crystal lattice temperature

$\boldsymbol{V_{DD}}$ drive bias
$\boldsymbol{V_T}$ threshold voltage

1

Background

1.1 EARLY HISTORY OF THE TRANSISTOR

During the last century, humanity has experienced a tremendous advancement of computational power. An important step in this advancement was made in 1907 by Lee De Forest, with his invention of the triode. The triode is an amplifiying vacuum tube, consisting of an anode, a cathode and a control grid inside a vacuum sealed glass container. This is a transconductance device: A voltage signal applied to the control grid results in an amplified current signal at the anode. Five years later, De Forest sold his triode patent to AT&T, who intended to use it for amplification of long-distance telephone communication signals. These devices, however, proved unreliable and consuming much power, and in the 1930's, it was recognized that a better amplifier was needed.

Meanwhile, semiconductor diodes made of high-purity germanium were developed at Bell labs during the war, for use in radar applications. Using this newly gained expertise in semiconductors, William Shockley secured funding for the work on a semiconductor amplifier. John Bardeen and Walter Brattain were also recruited to his team at the AT&T Laboratories, where they began work on what would be the point-contact transistor, demonstrated in December of 1947 (Figure 1.1). This device consisted of two closely spaced gold contacts on one side of a germanium crystal which was placed on a metal plate. A small current applied to one of the gold contacts amplified the current flowing from the other gold contact to the metal plate. This was the first experimental demonstration of what was termed a transistor - a contraction of transresistance, for which the three where jointly awarded the Nobel Prize in Physics in 1956.

Commercialization of transistors began in the 1950's, after the invention of the bipolar junction transistor by Shockley. Applications at the time included hearing aids and transistor radios. The first transistor-based commercial computer was the IBM 7070, introduced in 1958 by IBM. By that time, transistors had become common in various electrical products. Circuits where manufactured by hand using tweezers to connect the various components. In 1958, Jack Kilby at Texas Instruments built the first integrated circuit – all the circuit components where made directly on the same semiconductor crystal, this allowed smaller and easier

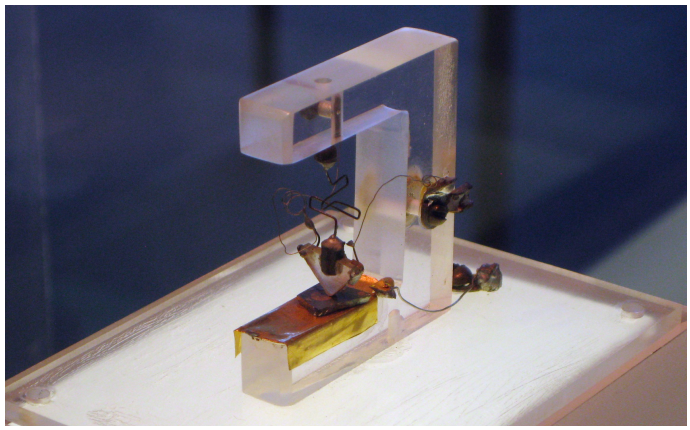

Figure 1.1: The first transistor fabricated used a germanium crystal substrate on a metal plate, and two gold contacts, one on each side of the triangular wedge, which is pushed onto the crystal by the spring. (Photo by Jacopo Werther.)

to produce circuits. Kilby was awarded the Nobel Prize in Physics in 2000 for this invention.

Independently, Robert Noyce of Fairchild Semiconductor invented a similar circuit in 1959. In 1968, he and colleague Gordon Moore started Intel (a contraction of Integrated Electronics), initially manufacturing bipolar static random access memory (SRAM), and in 1969 the first commercial metal-oxide-semiconductor field-effect transistor (MOSFET) SRAM based on silicon. Gordon Moore summarized the pursuit of the integrated circuit industry in the title of his paper from 1965, "Cramming more components onto integrated circuits", and in the prediction later called Moore's law, from the same paper: The number of transistors in an integrated circuit approximately doubles every year (later revised to two years) [1]. A fortuitous circumstance was that this pursuit was accompanied by both vast technological possibilities and huge economical incentives. These factors drove the increase of transistor count in a central processing unit (CPU) from thousands in the 1970's to billions in 2017, and gave rise to the digital era.

1.2 TRANSISTOR SCALING

The prevailing rule guiding the improvement of transistor performance through most of its history was Dennard scaling [2]. Dennard observed in 1974 that the drive bias and current of a transistor should be kept proportional to its dimensions. Thus,

as the transistor dimensions are scaled down, so is its power consumption reduced. This rule of thumb keeps the power density of the chip constant. At the same time, due to the reduced transistor area, leading to a reduction of the capacitance, the performance of the transistor improved, allowing operation at higher frequencies [3].

What Dennard scaling did not account for was the off-state leakage current, which does not scale with device dimensions. This can be understood in terms of the inverse subthreshold slope, the parameter describing the voltage required to switch the transistor between on and off states. In a MOSFET device, the inverse subthreshold slope can be no smaller than 60 mV per decade of current at room temperature, and so the drive voltage cannot be reduced much below about 0.5 V [4].

For this reason, Dennard scaling could not be maintained, and in the beginning of the 21st century, transistor scaling entered a power-constrained regime, meaning that the power density of about 100 Wcm^{-2}, could not be further increased without placing unacceptable requirements on chip cooling and packaging [5]. As a result, CPU clock frequency has remained at around 4 GHz since 2006.

In addition to scaling, many other performance enhancing technologies have been implemented in silicon complementary metal-oxide-semiconductor (CMOS). For instance, high-κ gate oxides, FinFET architecture and strained channels. The FinFET architecture, i.e. the use of a non-planar high-aspect ratio channel, allowed for, in part, reduced leakage currents at scaled gate length and, in part, increased drive current per chip area, due to the vertical elements of the channel [6]. Strained channels included the use of SiGe and improved the carrier mobility, meaning that the supply voltage could be reduced while still obtaining a sufficiently large drive current [7]. For a similar reason, i.e. due to their high carrier mobilities, III-V compound semiconductors were envisioned as a replacement for the silicon channel [8].

1.3 III-V COMPOUND SEMICONDUCTORS

III-V electronics already constitute a multi-billion dollar industry, with a plethora of applications, such as lasers, LEDs, wireless networks, radar and smart phones, to name a few [9]. These applications make use of the favorable optical properties of III-V, as well as their high electron mobility in high-frequency applications [10]. Figure 1.2 shows experimental electron mobility versus nanowire diameter for various material systems, as reported in the literature. At scaled nanowire dimensions, an order of magnitude higher electron mobility is observed in indium gallium arsenide (InGaAs), as compared to silicon. For use in CMOS technology, however, III-V

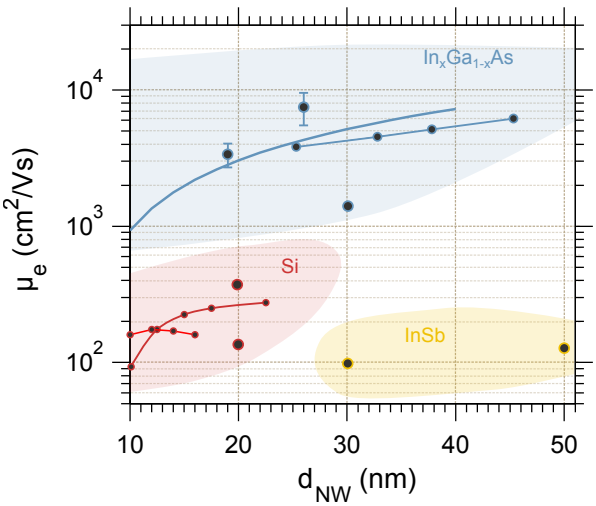

Figure 1.2: Experimental values for the electron mobility versus nanowire diameter in non-planar channels reported in literature as well as in Paper IX. For non-symmetrical channel structures, an effective diameter, giving the same cross-sectional channel area, was used.

FETs must also meet a number of other performance marks to enable low enough power consumption in scaled technology nodes.

One of these performance marks is an inverse subthreshold slope of close to 60 mV per decade of current at room temperature. The gate oxide is a key component of the transistor to enable this. Silicon has a native oxide, silicon dioxide (SiO_2), which forms an interface to the semiconductor relatively free of defects. This allows the gate potential to effectively modulate the potential of the channel, strongly improving the inverse subthreshold slope. On the other hand, III-Vs, and InGaAs in particular, form a variety of poor quality native oxides which are unsuitable for device operation [11]. However, since 2003, when aluminum oxide (Al_2O_3) was discovered to be an excellent gate oxide on the InGaAs system, progress has been very strong, and state-of-the-art gate stacks now exhibit defect densities approaching those of silicon FETs [12, 13].

Nevertheless, III-V FETs decisively outperforming industrial silicon FETs for CMOS applications have not been reported, in part due to the gate oxide problem, in part due to other key issues, such as the formation of low-resistance ohmic contacts, and establishing a proper scheme for the formation of a non-planar III-V channel [14].

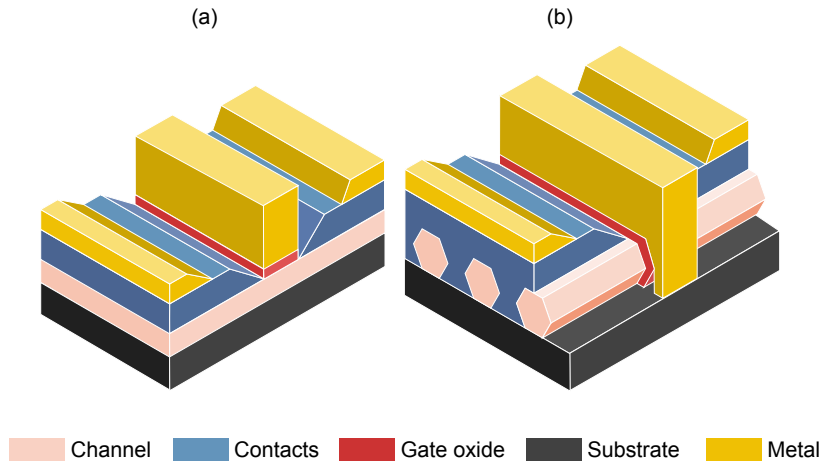

Figure 1.3: Schematic illustration of (a) planar and (b) non-planar device structures. Here, the non-planar device employs lateral nanowires as the channel, with an omega gate configuration.

1.4 DIGITAL APPLICATIONS

Digital transistor applications, or very-large-scale integration (VLSI) compatibility, requires highly scaled devices, with small footprints and low power consumption. The use of a non-planar channel, i.e. a channel architecture where gate covers the channel in three dimensions, allows for enhanced scalability (Figure 1.3). In contrast, a planar device has a channel which is 2-dimensional. The non-planar device, as compared to the planar device at similar dimensions, more strongly suppresses the influence of the source and drain fields on the channel potential [15]. This enables a lower subthreshold slope at a given gate length, or further scaled gate length while keeping the subthreshold slope constant.

III-V MOSFETs for digital applications have recently been studied extensively. Different material choices, device architectures and channel geometries have been examined. Planar indium arsenide (InAs) FETs with a 2.5 nm thick channel layer and a gate length (L_G) of 25 nm, were reported by Lee *et al.*, demonstrating a very high on-current of 500 µA/µm (at $V_{DD} = 0.5$ V and $I_{OFF} = 100$ nA/µm) [16,17]. Lin *et al.* also reported planar III-V FETs, using a 9 nm thick InGaAs/InAs channel, demonstrating a very high transconductance of 3.45 mS/µm [18]. Kim *et al.* reported planar InAs FETs utilizing a Silicide-like nickel (Ni)-alloy self-aligned contact formation scheme [19].

Techniques for integration of III-V channels on silicon substrate include the use

of a metamorphic buffer layer, as reported by Huang *et al.* [20] and wafer bonding, as reported by Kim *et al.* [21] and Deshpande *et al.* [22].

For non-planar geometries, Kim *et al.* demonstrated InGaAs tri-gate FETs with channel width and height of 20 nm, exhibiting on-current of 410 µA/µm (at $V_{DD} = 0.5V$ and $I_{OFF} = 100$ nA/µm). Radosavljevic *et al.* also reported tri-gate InGaAs FETs, demonstrating good electrostatic control and relatively high-quality oxide interface [23,24]. Gu *et al.* demonstrated gate-all-around InGaAs FETs with strong electrostatic control [25]. Waldron *et al.* also demonstrated gate-all-around InGaAs devices fabricated on Si substrate with excellent performance [26]. In all these reports, the non-planar channels were formed by etching using a mask to define the channel. There are also reports of non-planar III-V FETs with channels not defined by etching, for instance by Schmid *et al.* using templated-assisted selective epitaxy, allowing for integration on Si substrate as well as implementation of heterostructure systems [27, 28].

Vertical transistors are a class of non-planar transistors, which are characterized by that the carriers in the channel travel vertically from source to drain. State-of-the-art vertical transistors utilizing vapour-liquid-solid (VLS) catalyst-based growth to form the nanowire channel, have been reported by, for instance, Berg *et al.*, demonstrating InAs channel with excellent performance, as well as by Svensson *et al.*, demonstrating cointegration with gallium antimonide (GaSb) p-channel FETs and CMOS circuits [29, 30].

1.5 HIGH-FREQUENCY APPLICATIONS

III-V materials have successfully been used in commercial high-frequency applications, for instance in high electron mobility transistors (HEMTs). These devices differ from MOSFETs by using a semiconductor gate barrier layer, rather than a gate oxide, as the gate insulator. The barrier layer, usually indium aluminum arsenide (InAlAs) or indium phosphide (InP), allows for a high-quality semiconductor-semiconductor interface at the channel surface, and avoids the issue of detrimental gate oxide interface defects [10]. HEMTs also typically use delta-doping, a thin highly doped layer which is placed just outside the channel. The delta-doping allows for increased carrier concentration in the channel, without degraded mobility due to ionized dopant scattering. These characteristics allow HEMTs to reach field-effect mobility values of 10 000 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and above [31].

$In_{0.70}Ga_{0.30}As$ HEMTs with maximum oscillation frequency of above 1 THz, and cut-off frequency of approaching 700 GHz have been demonstrated [10, 32]. These

devices show a transconductance of 1.75 mS/µm at a gate length of 50 nm and barrier thickness of 4 nm. To further improve the transconductance, and thus the high-frequency performance, increasing the gate capacitance would be beneficial. However, due to their relatively small band gap, semiconductor gate barriers cannot be scaled much further without a significant increase of the gate leakage current. For this reason, MOSFETs, which allow for aggressive gate oxide scaling, may be useful in high-frequency applications.

III-V MOSFETs are relevant for two classes of high-frequency applications. The first class is as a replacement technology for HEMTs, that is in applications requiring low noise at high gain and frequency, for instance millimetre wave wireless communication. These kinds of devices will aim to minimize parasitic effects and maximize high-frequency performance at the cost of increased device dimensions and the use of expensive substrates such as InP.

The second class is as a replacement for silicon CMOS. Silicon CMOS has several drawbacks compared to III-V technologies in high-frequency applications, such as lower carrier mobility and smaller band gap (than e.g. InP and GaAs) [33]. However, key high-frequency figures of merits have improved substantially for silicon CMOS in the last decade, with the cut-off frequency approaching 400 GHz. Importantly, silicon CMOS allows for cointegration of high-frequency functionality with digital logic for on-chip performance tuning and signal processing. III-V MOSFETs aiming for these kinds of applications must demonstrate a highly scaleable device structure, preferably integrated on silicon substrates, as well as exhibit strong performance in logic-relevant metrics.

1.6 MOTIVATION

This thesis aims to explore the potential of III-V MOSFETs both as replacements for silicon FETs in CMOS applications, and as amplifiers operating at high frequencies. This will be done through design and fabrication of InGaAs MOSFETs, as well as characterization of oxide and channel material quality through various means. In particular, selective area growth techniques will be used to form the nanowire channel used in these devices.

Chapter 2 concerns the theory of 1D ballistic FETs. This theory accurately describes the operation and properties of highly scaled FET for both digital and high-frequency applications. The I-V characteristics of such devices will be derived in detail, taking into account quasi-ballistic transport, multiple subbands, parasitic resistances, oxide scaling and the influence of oxide defects.

Chapter 3 describes MOSFETs suitable for high-frequency operation as well as high-frequency characterization of such devices, including small-signal modeling and performance metrics. Particular features of 1D quasi-ballistic devices will also be highlighted.

Chapter 4 covers the design and fabrication of InGaAs MOSFETs. This includes the selective area growth process, as well as characterization of the nanowires used as the channel in the devices of this work. Several schemes of contact formation are examined, including both regrown contacts and silicide-like processes. Various gate oxide choices are considered, as well as metallization options for both source, drain and gate. Finally, different schemes of T-gate formation are considered.

2

Transistor Theory

2.1 BENCHMARKING MOSFETS FOR DIGITAL APPLICATIONS

Digital applications, i.e. CMOS logic, impose strict requirements on device architecture and performance. A primary metric is the drive current delivered by the transistor in the on-state, I_{ON}. The on-state is defined as the bias point $V_{DS} = V_{DD}$, $V_{GS} = V_{OFF} + V_{DD}$, where V_{OFF} is V_{GS} such that $I_{DS} = I_{OFF}$. I_{OFF} typically takes one of three values: 1, 10 or 100 nA/µm, corresponding respectively to low-power, general purpose and high performance applications, as defined by the international technology roadmap for semiconductors (ITRS). For III-V MOSFETs, $V_{DD} = 0.5$ V is often intended.

A large I_{ON} is desireable in CMOS in order to reduce the propagation delay of the CMOS inverter, which is described as

$$t_p = \frac{C_L V_{DD}}{2 I_{ON}} \tag{2.1}$$

where C_L is the load capacitance. A small propagation delay allows for logic operation at higher clock frequencies [3].

I_{ON} is determined by the inverse subthreshold swing, SS, and the transconductance, g_m, as shown in Figure 2.1a. The SS is the V_{GS} change required for the change of one decade of current below threshold. Similarly, g_m is number of amperes delivered per volt of V_{GS} above threshold. Together they determine the required V_{GS} change for a full swing from I_{OFF} to I_{ON}.

A path to achieve small SS and large g_m is to implement a non-planar channel, such as a FinFET, Tri-gate FET or nanowire FET in a short-L_G device structure. This kind of device will exhibit 1D transport characteristics if the channel is small enough, and operate in the quasi-ballistic regime, if L_G is short enough. Thus, an ideal MOSFET for digital applications can be described by the theory of ballistic 1D MOSFETs, developed by Lundstrom and others [34, 35].

2.2 THEORY OF BALLISTIC 1D MOSFETS

The $I-V$ characteristics of a ballistic and quasi-balistic 1D MOSFET at $T_L = 0$ K will now be derived [36]. A ballistic MOSFET can be understood as two electron

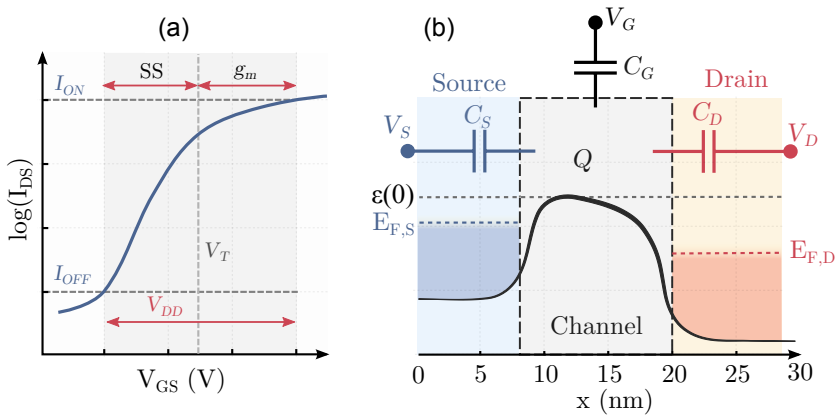

Figure 2.1: (a) A schematic figure of the subthreshold characteristics of a MOSFET. The drive bias V_{DD} determines the swing from on-state to off-state, thus I_{OFF} and I_{ON}. The subthreshold slope sets the current swing per voltage below the threshold voltage, while the transconductance does so above threshold. (b) Band diagram of conduction band of a MOSFET in the top of the barrier model. The transistor is here modeled as a system consisting of three capacitors modulating the channel charge Q.

reservoirs separated by an energy barrier. The Fermi level of one side, the source, is $E_{F,S}$, and the Fermi level of the other, the drain, is $E_{F,D} = E_{F,S} - qV_{DS}$ under an applied bias, V_{DS}. Carriers from each side will be injected into the other, forming two oppositely directed currents, I^+ and I^-. The total current is $I_{DS} = I^+ - I^-$.

$$I^+ = \frac{2q^2}{h}\frac{\Psi}{q}\Theta(\Psi) \tag{2.2}$$

$$I^- = \frac{2q^2}{h}\frac{\Psi - qV_{DS}}{q}\Theta(\Psi - qV_{DS}) \tag{2.3}$$

where $\Psi = E_F - \varepsilon(0)$, the difference between the source Fermi energy and the energy at the top of the barrier. The bias-dependencies of I_{DS} can be determined from the top-of-the-barrier model, illustrated in Figure 2.1b.

In the top-of-the-barrier model, the transistor is modeled as a three-capacitor system with three terminals, V_G, V_S and V_D. $\varepsilon(0)$ is then determined from the solution of the Poisson equation representing this system, including a bias-induced charge, Q, corresponding to the mobile charge in the channel, at their common terminal.

$$-\varepsilon(0) = \frac{C_G}{C_\Sigma}qV_G + \frac{C_D}{C_\Sigma}qV_D + \frac{C_S}{C_\Sigma}qV_S - q\frac{Q}{C_\Sigma} \tag{2.4}$$

where $Q = q(n_{1D} - n_0)$, n_{1D} is the total 1-D carrier density under bias, and n_0 is the carrier density under zero bias. C_Σ is a parallel coupling of the capacitors, $C_S + C_D + C_G$. n_{1D} is understood as the total directed moments in both directions, $n^+ + n^-$, at the top of barrier energy. From a ballistic transport model, they are evaluated as [36]

$$n^+ = \frac{\sqrt{2m^*\Psi}}{\pi\hbar}\Theta(\Psi) \tag{2.5}$$

$$n^- = \frac{\sqrt{2m^*(\Psi - qV_{DS})}}{\pi\hbar}\Theta(\Psi - qV_{DS}) \tag{2.6}$$

The V_{GS} and V_{DS} dependence of I_{DS} can be determined by solving equations (2.4), (2.5) and (2.6) self-consistently, but simple equations can be obtained for I_{DS} by observing three regions of operation.

Region 1: $\varepsilon(0) > E_{F,S}$, as shown in Figure 2.2a. There are no states in the channel below $E_{F,S}$, thus both I_{DS} and $n_{1D} = 0$. If we assume perfect electrostatic gate control, $C_S/C_\Sigma = 0$, $C_D/C_\Sigma = 0$ and $C_G/C_\Sigma = 1$, then (2.4) simplifies to

$$\varepsilon(0) = -qV_{GS} \tag{2.7}$$

A current will begin to flow when $E_{F,S}$ lines up with $\varepsilon(0)$, thus we may define the threshold voltage as $V_T \equiv V_{GS} = E_{F,S}/q$.

Region 2: $E_{F,D} < \varepsilon(0) < E_{F,S}$, as shown in Figure 2.2b. Here, the bottom of the barrier is below $E_{F,S}$, but above $E_{F,D}$. The channel states are therefore occupied only by carriers travelling in the positive direction, $I^- = 0$ and $n^- = 0$, while I^+ and n^+ follow equations (2.2) and (2.5), respectively, with the step function $\Theta(\Psi) = 1$. I_{DS} is obtained from equations (2.2), (2.4) and (2.5) as

$$I_{DS} = \frac{2q}{h}\left[-\frac{\sqrt{2m^*}q^2}{hC_{OX}} + \sqrt{\frac{2m^*q^4}{h^2C_{OX}^2} + q(V_{GS} - V_T)}\right]^2 \tag{2.8}$$

I_{DS} is therefore independent of V_{DS} in this region. This is also clear from the band structure. There are no occupied states below $E_{F,D}$, therefore, as V_{DS} is increased, the number of occupied states in the channel remains constant. Similarly, the V_{GS}-dependence is understood qualitatively as follows: As V_{GS} increases, the number of positive states below E_{FS} increases, thus I_{DS} increases.

Region 3: $\varepsilon(0) < E_{F,D}$, as shown in Figure 2.2c. Here, the bottom of the barrier is below both $E_{F,S}$ and $E_{F,D}$.

$$I_{DS} = I^+ - I^- = \frac{2q^2}{h}\frac{\Psi}{q} - \frac{2q^2}{h}\frac{\Psi - qV_{DS}}{q} = \frac{2q^2}{h}V_{DS} \tag{2.9}$$

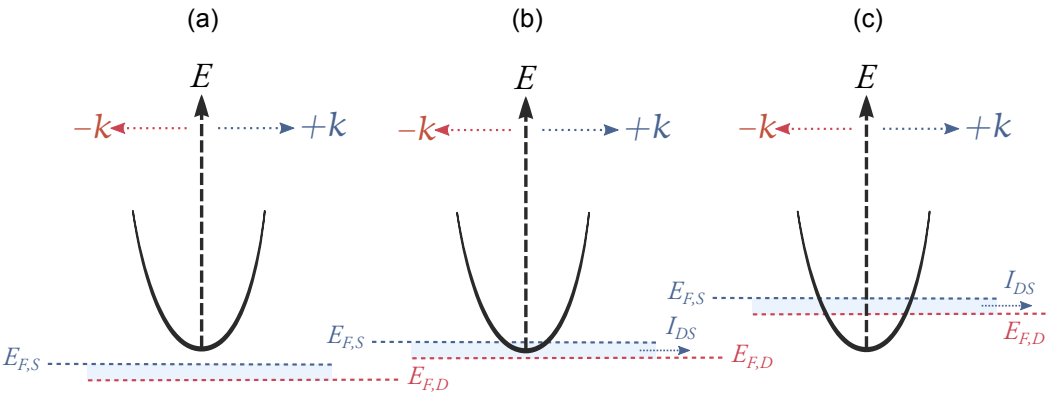

Figure 2.2: Schematic illustration of the conduction band edge in a 1D channel, i.e. the energy of lowest quantized subband, indicating three regions of behavior of the current versus the applied biases. (a) In region 1, the drain current is zero. (b) In region 2, the current is dependent on V_{GS}, but independent of V_{DS}. (c) In region 3, the current is dependent on V_{DS}, but independent of V_{GS}.

Thus, I_{DS} becomes independent of V_{GS}. This simply follows from that lowering $\varepsilon(0)$ does not change the number of carriers in the channel, while lowering $E_{F,D}$ lowers I^-, therefore increases I_{DS}. From the band diagram, it is also clear that as V_{DS} is increased, the system will eventually re-enter region 2 by satisfying its condition $E_{F,D} < \varepsilon(0) < E_{F,S}$. This will happen when $\varepsilon(0) = E_{F,D} = E_{F,S} - qV_{DS,sat}$. $V_{DS,sat}$ is the saturation voltage, the value of V_{DS} which constitutes the boundary between region 2 and region 3. If $V_{DS} < V_{DS,sat}$, then equation (2.8) is true and I_{DS} is independent of V_{DS}. If $V_{DS} > V_{DS,sat}$, then equation (2.9) is true and I_{DS} is independent of V_{GS}.

The band diagram also shows that $V_{DS,sat}$ must depend on V_{GS}. The exact expression for $V_{DS,sat}$ when $V_{DS} > V_{DS,sat}$ can be obtained by

$$qV_{DS,sat} = E_{F,S} - \varepsilon(0) = \left[-\frac{\sqrt{2m^*}q^2}{hC_{OX}} + \sqrt{\frac{2m^*q^4}{h^2C_{OX}^2} + q(V_{GS} - V_T)} \right]^2 \tag{2.10}$$

Figure Figure 2.3 shows a calculation of I_{DS} using equations (2.8) and (2.9), with $m^* = 0.04$ and $C_{OX} = 1.3 \cdot 10^{-9}$ F/m, with $V_{DS} = 10$ to 50 mV. According to equation (2.9), the saturation current is $V_{DS}2q^2/h$, and therefore the conductance I_{DS}/V_{DS} is constant at a value of $2q^2/h$, which is called the quantum conductance.

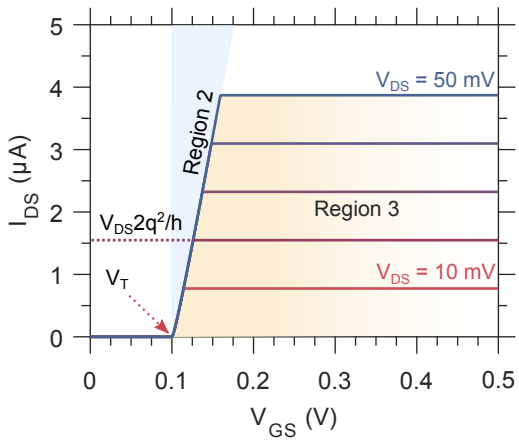

Figure 2.3: Ideal transfer characteristics of a 1D ballistic MOSFET with a single occupied subband, at different values of V_{DS}. Regions 2 and 3, correlating with those in Figure 2.2, are indicated. Region 1 is below V_T but is not indicated.

2.2.1 BALLISTIC TRANSCONDUCTANCE

The transconductance $g_m = dI_{DS}/dV_{GS}$ is zero in regions 1 and 3. In region 2, it is obtained by derivating equation (2.8). Equation (2.8) can be simplified by identifying the quantum capacitance

$$C_Q = -q^2 \frac{\partial n_{1D}}{\partial \varepsilon(0)} = \frac{\sqrt{2m^*}q^2/\pi\hbar}{-(\sqrt{2m^*}q^2/hC_{OX}) + \sqrt{(2m^*q^4/h^2C_{OX}^2) + q(V_{GS} - V_T)}} \quad (2.11)$$

which gives

$$I_{DS} = \frac{2q^2}{h} \frac{C_{OX}}{C_{OX} + C_Q}(V_{GS} - V_T) \quad (2.12)$$

g_m can now be examined in the quantum capacitance limit (QCL), $C_{OX} \gg C_Q$,

$$g_m = \frac{2q^2}{h} \quad (2.13)$$

and in the classical limit ($C_{OX} \ll C_Q$)

$$g_m = \frac{h}{2m^*q} C_{OX}^2 (V_{GS} - V_T) \quad (2.14)$$

As seen in (2.14), in the classical limit, g_m has a dependence on the effective mass. In MOSFETs operating in the drift-diffusion regime, g_m is indirectly dependent on

the effective mass, through the mobility, which is typically higher for lower effective mass. In a fully ballistic device, the dependence instead comes from the density of states. However, truly ballistic transistors are not currently achievable. It is therefore useful to model quasi-ballistic devices, i.e. devices with small amounts of scattering in the channel [37, 38].

2.2.2 QUASI-BALLISTIC DEVICES

Consider again equation (2.9), where I_{DS} is described by a forward, and a backward current as [39]

$$I_{DS} = I^+ - I^- \tag{2.15}$$

Assume now that $I^+ = I_B^+$ is the ballistic foward current, and that a portion T of I^- scatters in the opposite direction. I^- is then constituted by a component from the scattered ballistic forward current, $(1-T)I_B^+$, and a component from the non-scattered ballistic backward current, TI_B^-

$$I^- = TI_B^- + (1-T)I_B^+ \tag{2.16}$$

Inserting equation (2.16) into equation (2.15) gives

$$I_{DS} = T(I_B^+ - I_B^-) = TI_B \tag{2.17}$$

When scattering is present in the channel, the ballistic current I_B is thus reduced by a factor T, called the transmission.

To determine an expression for T, consider a channel with the length L (corresponding to the gate length of a quasi-ballistic device), and the current fluxes $J_{DS}(x) = J^+(x) - J^-(x)$. It is clear that the forward flux at $x = L$ is reduced by scattering by a factor T compared to the forward flux at $x = 0$ and that $J^-(L) = 0$

$$J_{DS}(L) = J^+(L) = TJ^+(0) \tag{2.18}$$

The probability of a scattering event at an arbitrary distance x into the channel is x/λ, where λ is the mean free path, the average distance traveled between scattering events. Therefore, the forward flux at x is the difference between the forward flux at $x = 0$ and the portion of scattered total flux at x

$$J(x)^+ = J^+(0) - J_{DS}(x)\frac{x}{\lambda} \tag{2.19}$$

Inserting equation (2.19) into equation (2.18) gives

$$T = \frac{J^+(L)}{J^+(0)} = \frac{1}{1 + L/\lambda} = \frac{\lambda}{\lambda + L} \tag{2.20}$$

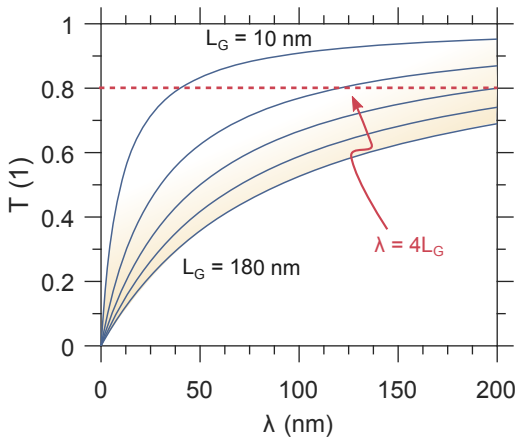

Figure 2.4: The transmission coefficient versus the mean free path at different gate lengths. The required mean free path to obtain 0.8 transmission follows the simple relationship $\lambda = 4L_G$ and is indicated.

The current in a quasi-ballistic device then becomes

$$I_{DS} = \frac{\lambda}{\lambda + L_G} \frac{2q^2}{h} \frac{C_{OX}}{C_{OX} + C_Q} (V_{GS} - V_T) \tag{2.21}$$

Figure 2.4 shows T versus λ for $L_G = 10$ to 180 nm. A transmission of 0.8 may be a reasonable target for high-performance III-V MOSFETs, this gives the simple formula

$$\lambda_{T=0.8} = 4L_G \tag{2.22}$$

An expression for λ in terms of material parameters can be obtained for non-degenerate conditions by considering Fick's law of diffusion

$$J_{DS} = -D\frac{dn}{dx} = -\frac{\lambda v_T}{2} \tag{2.23}$$

where v_T is the thermal velocity and D is the diffusion constant, which relates to the electron mobility μ through the Einstein relation

$$D = \frac{k_B T_L \mu}{q} = \frac{\lambda v_T}{2} \tag{2.24}$$

where T_L is the lattice temperature. Thus, high mobility correlates with long mean free path.

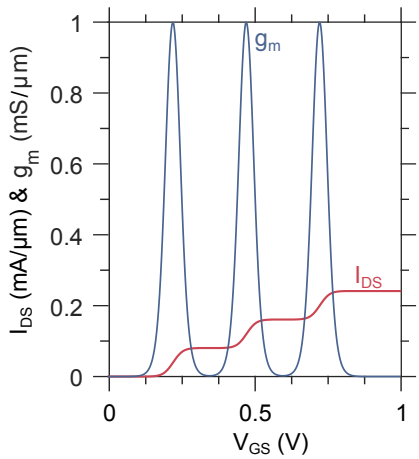

Figure 2.5: Simulated transfer characteristics of a device with three equidistant sub-bands.

2.2.3 MULTIPLE SUB-BANDS

With M number of sub-bands below $E_{F,S}$, the total current in region 3 becomes [36]

$$I_{DS} = \sum_{n}^{M} I_{DS,n} = MT\frac{2q^2}{h}V_{DS} \tag{2.25}$$

The transfer and output characteristics of a device with multiple subbands are shown in Figure 2.5 and Figure 2.6, respectively. The linear region exhibits multiple slopes, or values of R_{ON} according to $MT\frac{2q^2}{h}$, where M now indicates the number of sub-bands below $E_{F,D}$, which depends on both V_{GS} and V_{DS}. At high V_{GS} and low V_{DS}, a minimum value of R_{ON} is obtained, the ballistic on-resistance 12.9 kΩ/M. The measured R_{ON} of a quasi-ballistic device, with access resistance R_{DS} can then be described as

$$R_{ON} = \frac{h}{2q^2MT} + R_{DS} = \frac{h}{2q^2M}(1+\frac{L_G}{\lambda}) + R_{DS} = L_G\frac{h\lambda}{2q^2M} + \frac{h}{2q^2M} + R_{DS} \tag{2.26}$$

M can be determined from the linear function $R_{ON}(L_G)$, by estimating and subtracting R_{DS} from the y-axis intercept. With knowledge of M, λ can subsequently be calculated from the slope.

A first order approximation of the energy separation E between sub-bands is

provided by a simple symmetric quantum well model

$$E = \frac{k^2\hbar^2}{2m^*} \tag{2.27}$$

where k is the wave vector. Clearly, a small m^* results in a large energy separation.

2.2.4 NON-PARABOLICITY

The effective mass approximation used here is valid only for low energies. At high energies, the dispersion relationship is no longer parabolic, but approaches a material-dependent linear slope. Using k · p theory, this can be modeled as [40, 41]

$$E(1+\alpha E) = \frac{k^2\hbar^2}{2m^*} \tag{2.28}$$

where α determines the degree of non-parabolicity and can be approximated as [41]

$$\alpha \approx \frac{1}{E_G}(1-\frac{m^*}{m_0})^2 \tag{2.29}$$

Thus, the effective mass in a non-parabolic model increases at higher energies.

2.2.5 THE DENSITY OF STATES BOTTLENECK

In a 2D, i.e. quantum well FET, the current is

$$I_{DS,2D} \propto \left(\frac{C_{OX}}{C_{OX}+C_Q}\right)^{3/2}\sqrt{m^*} \tag{2.30}$$

where the 2D quantum capacitance is

$$C_Q = \frac{q^2 m^*}{\pi\hbar^2} \tag{2.31}$$

The optimization of $I_{DS,2D}$ with respect to m^* gives an optimum at $C_Q = 2C_{OX}$, which means that a lower m^* is beneficiary only up to a certain degree. For large m^*, $I_{DS,2D}$ is limited by low carrier velocity, while for small m^* it is limited by a low density of states (DOS). This effect is called the DOS bottleneck [42].

For a 1D channel, the optimization of I_{DS} with respect to m^*, i.e. using equations (2.11) and (2.21), implies no limit to the increase of I_{DS} with the reduction of m^*. Nevertheless, a DOS bottleneck-like effect is present in the fact that $E \propto 1/m^*$ as shown in equation (2.27). Essentially, at a fixed V_{GS}, a reduction of m^* will reduce

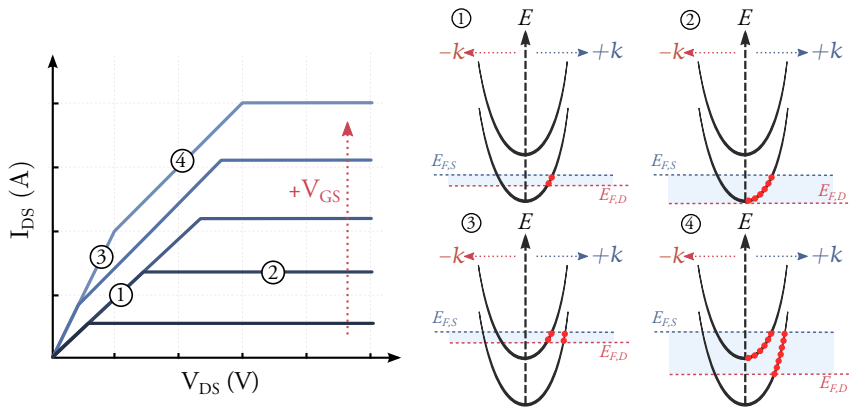

Figure 2.6: Ideal output characteristics of a 1D ballistic MOSFET with up to two occupied subband, at different values of V_{GS}. The numbers and the corresponding schematic figures indicate the band alignment at the various biasing conditions. The red dots in the band diagram denote k-states that contribute to the drain current.

the number of sub-bands below $E_{F,S}$ and thus the current according to equation (2.25). These considerations are valid for nanowires with radii of approximately above 10 nm, in which $M > 1$ under normal bias conditions. When $M = 1$, E does not influence I_{DS}, and so this effect is not present.

2.2.6 INTERFACE TRAPS

The influence of charging of interface traps on the electrostatics of the device can be modeled by including the trapped charges n_{trap} in the total total bias-induced charge Q in equation (2.4)

$$-\delta\varepsilon(0) = q\delta V_G - q^2 \frac{n_{1D} - n_0 + \delta n_{trap}}{C_{OX}} \tag{2.32}$$

The trapped charges are described as $\delta n_{trap} = D_{it}\delta\varepsilon(0)$, where D_{it} is the density of interface traps.

$$-\delta\varepsilon(0) = q\delta V_G - q^2 \frac{n_{1D} - n_0}{C_{OX}} - \frac{q}{C_{OX}} D_{it}\delta\varepsilon(0) \tag{2.33}$$

Calculating the current as before, now gives

$$I_{DS} = T\frac{2q^2}{h}\frac{C_{OX}}{C_{OX} + C_Q + q^2 D_{it}}(V_{GS} - V_T) \tag{2.34}$$

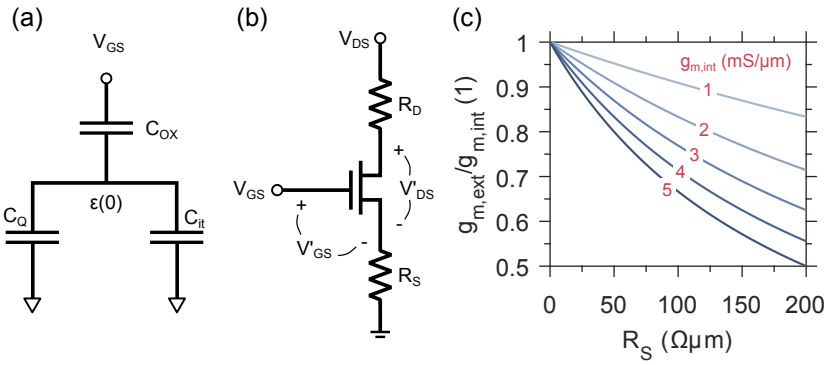

Figure 2.7: (a) A capacitative model of the channel in a MOSFET, assuming ideal electrostatics. The quantum capacitance, and the capacitance due to interface charge have a similar detrimental effect on device performance. (b) Circuit of a MOSFET including extrinsic resistance, source and drain access resistance. (c) Calculated degradation of the transconductance at increasing values of source resistance for different values of intrinsic transconductance. This effect is most severe in devices with large intrinsic transconductance.

The influence of trap charging can thus be described through the addition of a capacitor C_{it} in parallel with C_Q according to Figure 2.7(a), which degrades I_{DS}.

2.3 DEVICE CHARACTERISTICS

2.3.1 EXTRINSIC TRANSCONDUCTANCE

So far, the intrinsic tranconductance g_m, or $g_{m,int}$ has been derived, which does not include the effects of parasitic source and drain resistances, $R_{DS} = R_D + R_S$. The measured transconductance is the extrinsic transconductance, $g_{m,ext}$. The relationship between $g_{m,ext}$ and $g_{m,int}$, assuming symetric resistances $R_D = R_S$, was derived by Chou *et al.* as follows [43]. Define $g_{m,int}$ and the intrinsic output conductance $g_{d,int}$ as

$$g_{m,int} = \frac{\delta I_{DS}}{\delta V'_{GS}} \tag{2.35}$$

$$g_{d,int} = \frac{\delta I_{DS}}{\delta V'_{DS}} \tag{2.36}$$

According to Figure 2.7(b), a change in the drain current can then be described as

$$\delta I_{DS} = g_{m,int}\delta V'_{GS} + g_{d,int}\delta V'_{DS} \tag{2.37}$$

with

$$V'_{DS} = V_{DS} - (R_D + R_S)I_{DS} = V_{DS} - R_{DS}I_{DS} \tag{2.38}$$

$$V'_{GS} = V_{GS} - R_S I_{DS} \tag{2.39}$$

Transconductance is measured at constant V_{DS}, i.e. $\delta V_{DS} = 0$. The differentials of the intrinsic voltages are then

$$\delta V'_{DS} = -R_{DS}\delta I_{DS} \tag{2.40}$$

$$\delta V'_{GS} = \delta V_{GS} - R_S \delta I_{DS} \tag{2.41}$$

Combining (2.37) with (2.40) and (2.41) gives

$$\delta I_{DS} = g_{m,int}(\delta V_{GS} - R_S\delta I_{DS}) - g_{d,int}R_{DS}\delta I_{DS} \tag{2.42}$$

Solving (2.42) for $g_{m,int}$ and using $g_{m,ext} = \delta \mathrm{I}_{DS}/\delta \mathrm{V}_{GS}$ gives

$$g_{m,int} = \frac{\delta I_{DS}(1 + g_{d,int}R_{DS})}{\delta V_{GS} - R_S\delta I_{DS}} = \frac{g_{m,ext}(1 + g_{d,int}R_{DS})}{1 - R_S g_{m,ext}} \tag{2.43}$$

This means that a large output conductance will cause a drop in the measured transconductance, which is a well-known short-channel effect. For a long-channel device, with $g_d << g_m$, (2.43) simplifies to

$$g_{m,int} = \frac{g_{m,ext}}{1 - R_S g_{m,ext}} \Leftrightarrow g_{m,ext} = \frac{g_{m,int}}{1 + R_S g_{m,int}} \tag{2.44}$$

Figure 2.7(c), shows the reduction of $g_{m,ext}$ as a function of R_S and $g_{m,int}$. High $g_{m,int}$ devices are more severely degraded by access resistance, but e.g. at $R_S = 50\ \Omega\,\mu\mathrm{m}$ and $g_{m,int} = 3$ mS/µm, similar to the values reported in this work, the degradation is only about 10%.

2.3.2 OXIDE CAPACITANCE

As shown in equation (2.34), increasing the oxide capacitance by gate oxide scaling offers an improvement of I_{DS} and g_m, but the gain is limited by the quantum capacitance [44]. In a 1D gate-all-around (GAA) cylindrical geometry, the oxide capacitance is calculated from

$$C_{OX} = \frac{2\pi\epsilon_r\epsilon_0}{\ln(\frac{t_{OX}+r}{r})} \tag{2.45}$$

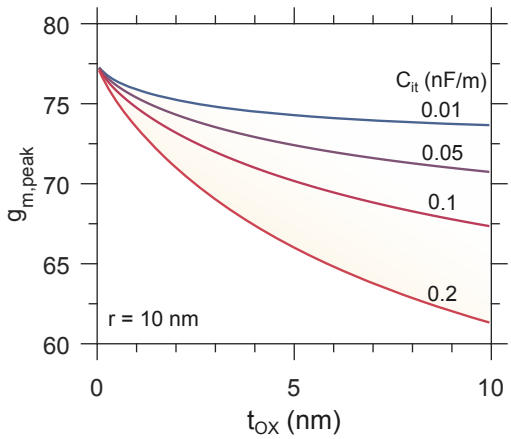

Figure 2.8: Peak transconductance versus gate oxide thickness in gate-all-around geometry and with nanowire radius of 10 nm, at different levels of interface trap-induced capacitance. It is clear that gate oxide scaling effectively counteracts the detrimental effects of interface traps, but for already low interface trap densities, oxide scaling provides only a minor enhancement of transconductance.

where t_{OX} is the gate oxide thickness, and r is the radius of the 1D channel. Figure 2.8 shows peak g_m versus t_{ox} at different values of C_{it}. At low values of C_{it}, t_{OX} scaling offers minimal improvement to g_m. As shown, with regards to g_m, t_{ox} scaling is primarily a means to compensate for the effects of interface traps.

In a rectangular gate-all-around geometry, the oxide capacitance instead is approximated as [45]

$$C_{OX} \approx \frac{2\epsilon_r\epsilon_0(W+H)}{t_{OX}} + 2.232\epsilon_r\epsilon_0 \tag{2.46}$$

where W and H are the width and height of the channel, respectively, and the condition $t_{OX} \ll W, H$ is true. Similarly, if the rectangular channel is gated on three sides (tri-gate), the oxide capacitance can be approximated as

$$C_{OX} \approx \frac{\epsilon_r\epsilon_0(W+2H)}{t_{OX}} + 1.116\epsilon_r\epsilon_0 \tag{2.47}$$

Figure 2.9 shows a comparison of the oxide capacitance for the three geometries, calculated using channel dimensions with the same circumference, and $\epsilon_r = 20$. In the gate-all-around geometry, cylindrical and rectangular channels have approximately equivalent oxide capacitance.

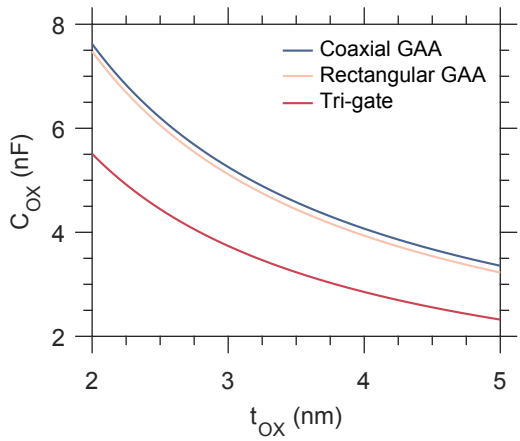

Figure 2.9: Oxide capacitance for three different geometries: Cylindrical gate-all-around, rectangular gate-all-around and tri-gate. Here, 20 nm is used for the rectangular channels, and a radius of 12.7 nm is used for the cylindrical, which give the same channel circumference for all three cases, and the same gated circumference for the first two cases.

2.3.3 NATURAL LENGTH SCALE

As L_G is scaled down in order to increase the transmission $T = \frac{\lambda}{\lambda + L_G}$ and reduce the size of the transistor, the oxide thickness and channel dimensions must also be reduced in order to avoid short channel effects [40, 46–48]. In particular, short-channel effects are caused by the source/drain potential influencing the channel potential. The length at which the source/drain influences the channel is described in terms of the natural length scale of the transistor, λ_n [48]. To avoid degradation of the subthreshold slope, the DIBL, as well as the transconductance through increased output conductance,

$$L_G \geq 5\lambda_n \tag{2.48}$$

should be maintained [46].

For gate-all-around cylindrical geometry and assuming extremely scaled nanowires, $t_{OX} \gg r$, λ_n, can be approximated as

$$\lambda_n \approx \pi \frac{t_{OX} + r}{2.4} \tag{2.49}$$

For an ultra-thin-body planar FET with the channel thickness t_c, this expression instead becomes [48]

$$\lambda_n \approx \pi (t_{OX} + \frac{\epsilon_r}{\epsilon_c} t_c) \tag{2.50}$$

where ϵ_c is the relative permeability of the channel material. Using the condition in equation (2.48), the required dimensions become $L_G \geq 6.5(t_{OX} + r)$ and $L_G \geq 16(t_{OX} + t_c)$ (assuming $\epsilon_r \approx \epsilon_c$), for gate-all-around and planar geometry, respectively [40]. Gate-all-around geometry therefore allows approximately 2.5 times thicker oxide and channel thickness, as compared to planar geometry, at a fixed L_G. Any other non-planar geometry, such as FinFETs and Tri-gates, will have a natural length scale in between those described by equations (2.50) and (2.49). This is the primary motivation for the use of non-planar geometries.

3

RF-Transistors

The response of transistors under an AC input bias is examined here. First, S-parameter measurements are described, followed by small-signal modeling of the devices presented in this work. Finally, key high-frequency performance metrics are analyzed.

3.1 HIGH-FREQUENCY CHARACTERIZATION

High frequency properties regard the response of the current through a device under test (DUT) to an input AC signal. The circuit that describes the electrical response of the DUT is called the small-signal model. The components of the small-signal model are determined by measurements of the matrix of the transfer function S for electromagnetic power waves, called the scattering parameters. As the MOSFET has two ports, i.e. where V_{GS} and V_{DS} are applied, the transfer function becomes

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.1}$$

where a_1 and a_2 are incident power waves at port one and two. Similarly, b_1 and b_2 are reflected power waves. Figure 3.1a shows a schematic figure of the S-parameter measurement, and Figure 3.1b shows the measurement setup. The related transfer function Y, the admittance matrix, describing $I \rightarrow V$ can be analytically derived from S, and from it, the elements of the small-signal model can be derived.

The S-parameters, rather than the Y-parameters, are measured because when measuring AC signals, a termination for the signal at the measurement station must be supplied in order to suppress reflection back to the DUT. For Y-parameters, the ports carry electrical current in and out of the DUT. For current signals, short-circuit and open-circuit terminations are necessary, but these are difficult to provide in a high-frequency setting. For S-parameters, termination by impedance matching is sufficient, and this is supplied by the 50 Ω impedance of the measurement system, following calibration, as seen from the DUT.

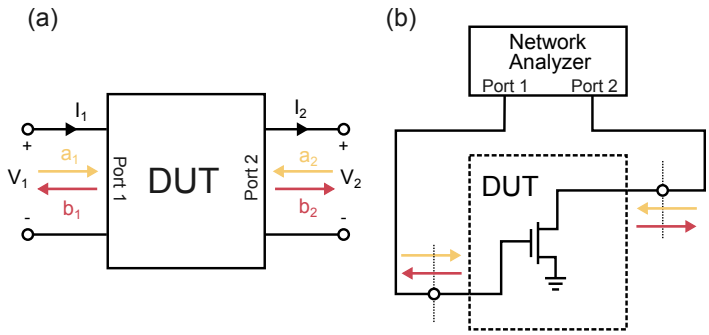

Figure 3.1: (a) Schematic figure of a two-port S-parameter measurement, with the incoming and reflected power waves a and b, respectively, as well as the associated currents and voltages of the system. (b) The S-parameter measurement setup, using a network analyzer.

3.2 THE SMALL-SIGNAL MODEL

The small-signal model is a circuit representing the small-signal, i.e. the RF-signal, response of the DUT. It aims to capture the gain provided by the transistor at arbitrary frequencies. A hybrid-π small signal model is typically used to model MOSFETs (Figure 3.2). The measured Y-parameter response of the transistor can be described in terms of the elements of the small-signal model [49]:

$$Y_{11} = \frac{I_1}{V_1}\bigg|_{V_2=0} = \frac{\omega^2(C_{gs}+C_{gd})^2 R_g + j\omega(C_{gs}+C_{gd})}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \tag{3.2}$$

$$Y_{12} = \frac{I_1}{V_2}\bigg|_{V_1=0} = \frac{-\omega^2 C_{gd}(C_{gs}+C_{gd})R_g - j\omega C_{gd}}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \tag{3.3}$$

$$Y_{21} = \frac{I_2}{V_1}\bigg|_{V_2=0} = \frac{g_m - j\omega g_m R_g(C_{gs}+C_{gd})}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \tag{3.4}$$

$$Y_{22} = \frac{I_2}{V_2}\bigg|_{V_1=0} = g_{ds} + j\omega C_{sd} + j\omega C_{gd} + \frac{\omega^2 g_m R_g^2 C_{gd}(C_{gs}+C_{gd}) + j\omega g_m R_g C_{gd}}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \tag{3.5}$$

Here, $C_{dg}, R_D, R_S = 0$ is assumed. The elements of the the hybrid-π small signal model are determined from the measured S-parameters, transformed to Y-parameters, by first setting $R_S = R_D = 0$. To do this, R_S and R_D are first estimated,

then subtracted from the measured impedence parameters Z [49]. The small-signal model elements are then calculated as follows [50]:

$$g_m = \mathrm{Re}[Y_{21}]|_{\omega^2=0} \tag{3.6}$$

$$g_d = \mathrm{Re}[Y_{22}]|_{\omega^2=0} \tag{3.7}$$

$$R_g = \frac{\mathrm{Re}[Y_{21}]}{(\mathrm{Im}(Y_{11}))^2} \tag{3.8}$$

$$C_{gd} = \frac{-\mathrm{Im}[Y_{12}]}{\omega} \tag{3.9}$$

$$C_{dg} = \frac{-\mathrm{Im}[Y_{21}]}{\omega} - g_m R_g (C_{gs} + C_{gd}) \tag{3.10}$$

$$C_{gs} = \frac{\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}]}{\omega} \tag{3.11}$$

$$C_{sd} = \frac{\mathrm{Im}[Y_{22}]}{\omega} - C_{gd} - g_m R_g C_{gd} + \omega^2 C_{gd} C_{dg} (C_{gd} + C_{gs}) R_g^2 \tag{3.12}$$

Subsequently, the modeled Y-parameters are determined from above equations. Finally, R_S and R_D are added to the modeled Z-parameters, which now give the response of the DUT at arbitrary frequencies. This allows predicting high-frequency metrics such as the cut-off frequency f_t and the maximum oscillation frequency f_{max} while measuring response at relatively low frequencies, e.g. up to 67 GHz.

Impact ionization becomes important at high V_{DS}. This effect is modeled by the inclusion of the two current sources I_{i1} and I_{i2}, that reflect the voltage dependencies of the impact ionization generation rate [51]

$$I_{i1} = \frac{g_{i1} V_{dg}}{1 + j\tau_1 \omega} \tag{3.13}$$

$$I_{i2} = \frac{g_{i2} V'_{gs}}{1 + j\tau_2 \omega} \tag{3.14}$$

I_{i1} describes carrier generation from a strong drain electric field, i.e. the dependence on the carrier energy. I_{i2} describes the dependence on the number of carriers, i.e. the drain current. Impact ionization occurrs during a finite time, and therefore exhibits a frequency-dependence. In particular, at high frequencies, impact ionization is unable to follow the signal, and is therefore suppressed. $j\tau\omega$ in the above expressions captures this effect, with τ being an associated time constant.

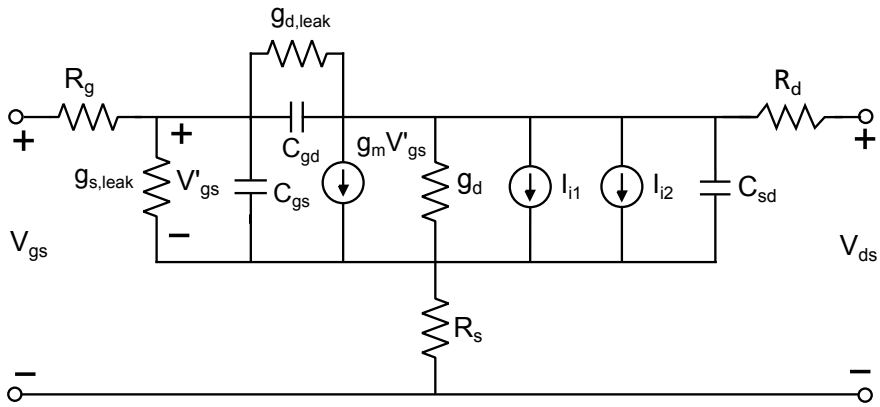

Figure 3.2: A small-signal model accurately describing the frequency response of devices measured and characterized in this work.

3.3 HIGH-FREQUENCY PERFORMANCE

The cut-off, or transition, frequency f_T is a common figure of merit for high-frequency transistors. f_T is the frequency at which the transistor delivers unity current gain. The current gain is described in terms of the h-parameter h_{21}

$$h_{21} = \frac{i_2}{i_1}|_{V_1=0} = \frac{Y_{21}}{Y_{11}} \tag{3.15}$$

f_T is then obtained either from extrapolating $|h_{21}|^2$ linearly at high frequencies with a slope of -20 dB/decade, or from a small-signal model with a good fit to the measured S-parameters. Assuming $R_S = R_D = 0\ \Omega$,h_{21} in terms of the small-signal elements is

$$|h_{21}| = \frac{\sqrt{g_m^2 - \omega^2 C_{gd}^2}}{\omega(C_{gs} + C_{gd})} \tag{3.16}$$

which for $\omega \gg g_m/C_{gd}$ simplifies to

$$|h_{21}| \approx \frac{g_m}{\omega(C_{gs} + C_{gd})} \tag{3.17}$$

and gives f_T at unity

$$\omega_T = 2\pi f_T \approx \frac{g_m}{C_{gs} + C_{gd}} \Leftrightarrow f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3.18}$$

In a traditional transistor, i.e. one operating in the drift-diffusion regime, with minimal parasitic gate capacitance operating in the classical limit, $C_{gs} + C_{gd} \approx \frac{2}{3} W L_G C_{OX}$, equation (3.18) simplifies to

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{\mu C_{OX} \frac{W}{L_G}(V_{GS} - V_T)}{2\pi \frac{2}{3} L_G W C_{OX}} = \frac{3\mu(V_{GS} - V_T)}{4\pi L_G^2} \tag{3.19}$$

where μ is the carrier mobility and W the channel width. While C_{OX} increases g_m, it also adds a delay due to charging of the capacitance, and so the overall C_{OX} dependence cancels out. The quadratic dependence on L_G is due to a simultaneous increase of g_m and reduction of C_{OX}. However, parasitic capacitances may often dominate the gate capacitance, which strongly affects these scaling characteristics.

A quasi-ballistic device can be analyzed by using the ballistic expression for g_m. In the classical limit, equation (3.18) becomes

$$f_T \approx \frac{\frac{hTC_{OX}^2}{2m^* q}(V_{GS} - V_T)}{2\pi \frac{2}{3} C_{OX} L_G} = \frac{3hTC_{OX}}{8\pi m^* q L_G}(V_{GS} - V_T) \tag{3.20}$$

Here, the dependence on C_{OX} does not cancel out, but C_{OX} can be increased in order to improve f_T, which relates to a reduction of an intrinsic delay in the channel.

For very large C_{OX} the device enters the quantum capacitance limit, $C_{gs} + C_{gd} \approx \frac{2}{3} W L_G C_Q$, and equation (3.18) becomes

$$f_T \approx \frac{q^2 T}{\pi h \frac{2}{3} L_G C_Q} = \frac{3T}{4\pi L_G} \sqrt{\frac{q(V_{GS} - V_T)}{2m^*}} \tag{3.21}$$

A reduced m^* gives a smaller density of states, and thus a lower C_Q, while g_m is independent of m^*. This explains the overall dependence of f_T on m^* in this regime.

With $R_S, R_D > 0\ \Omega$, the expression for f_T is obtained by adding the resistances to the Z-parameters, which gives

$$\frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} + \frac{C_{gs} + C_{gd}}{g_m}(R_S + R_D) g_d + (R_S + R_D) C_{gd} \tag{3.22}$$

The maximum oscillation frequency, f_{max}, is another figure of merit for high-frequency applications, and is defined as the frequency at which the power gain is unity. |U| is the power gain of a unilateral transistor, i.e. one whose reverse transmission parameter, for instance h_{12}, is zero. It represents the maximum unilateral power gain achievable by the transistor, and is obtained by the addition of

a lossless feedback network. It has the benefit of being independent of the transistor configuration, e.g. common-source and common-gate configurations. It is expressed in Z-parameters as [49]

$$U = \frac{|Z_{21} - Z_{12}|^2}{4[\mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12})\,\mathrm{Re}(Z_{21})]} \tag{3.23}$$

One of the significances of U is that the device is passive when $U < 1$ and active when $U > 1$. The frequency associated with this transition is f_{max} [49]

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{gd}\left[1 + \frac{2\pi f_T}{C_{gd}}\right]\Psi}} \tag{3.24}$$

where Ψ is

$$\Psi = (R_D + R_S)\frac{(C_{gs} + C_{gd})^2 g_d^2}{g_m^2} + (R_D + R_S)\frac{(C_{gs} + C_{gd})C_{gd} g_d}{g_m} + \frac{(C_{gs} + C_{gd})^2 g_d}{g_m^2} \tag{3.25}$$

4

Transistor Design & Fabrication

In this chapter, key steps of the MOSFET fabrication process will be described. Important design and process considerations will be highlighted. A detailed description of the device fabrication process, shown in Figure 4.12, is found in Appendix A.

4.1 SELECTIVE AREA NANOWIRE GROWTH

Selective area MOCVD growth is a method whereby growth on certain areas of the substrate is blocked by a pre-defined mask. This method has been used to fabricate, for instance, lasers and diodes. Compared to vapor-liquid-solid (VLS) growth, this method has the benefit of being catalyst-free and facilitating the formation of non-vertical nanowire structures, such as lateral nanowires and steps. Compared to a scheme of etching out lateral nanowires using an etch mask, selective growth allows the formation of similar structure without any potentially damaging etching steps.

Figure 4.1 shows a schematic figure of the selective area lateral nanowire formation process by use of an hydrogen silsesquixane (HSQ) growth mask. First, the HSQ mask is patterned by electron beam lithography on InP:Fe (S. I.) substrate. Subsequently, an InGaAs film is grown in the MOCVD reactor. Finally, the HSQ mask is stripped. Figure 4.2a shows a cross-sectional image of nanowires with {111}B facets grown this way.

The growth dynamics of selective area growth is understood as follows. Growth precursors reach the surfaces from the vapor phase supply, where pyrolysis occurs. Material is then transported by diffusion along the growth mask and into the non-covered areas, where epitaxial growth occurs. As shown in Figure 4.2b, growth proceeds along three interfaces: Nucleation from a supply on the (i) top and (ii) side surfaces of a crystal, and (iii) self-nucleation [52]. Nucleation of a crystal is associated with a change of Gibb's free energy, ΔG, from vapor phase to crystalline nucleus. The energetically favored growth interface is that for which ΔG is the smallest. Generally,

$$\Delta G = -n\Delta\mu + Ph\sigma + A(2\sigma - \beta) \tag{4.1}$$

where n is the number of atoms added to the crystal, $\Delta\mu$ is the change of chemical potential related to the nucleation interface, σ is the surface (or step) energy of a nuclei with the perimeter P, height h and area A. β is the adhesion energy which

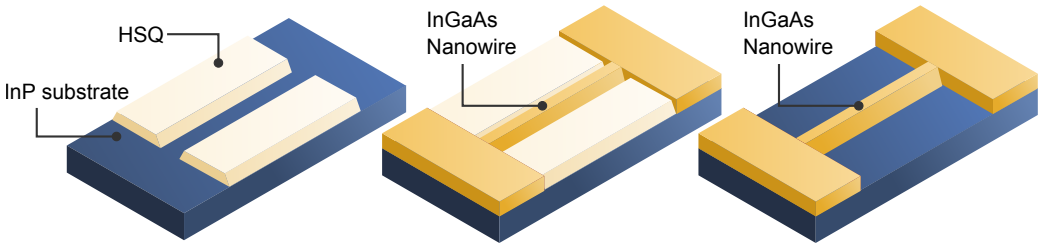

Figure 4.1: Schematic illustrations of lateral selective nanowire growth. First, an HSQ growth mask is patterned on the InP substrate. Subsequently, the InGaAs layer is grown by MOCVD. A nanowire is formed in between the HSQ-covered areas. Finally, the HSQ mask is stripped.

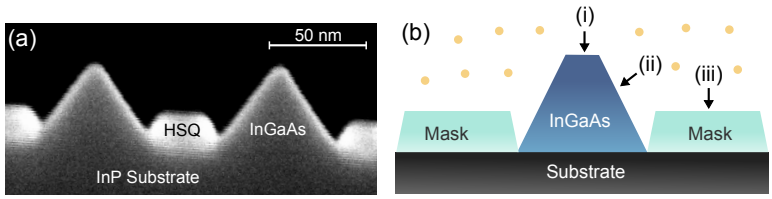

Figure 4.2: (a) A cross-sectional SEM image of a selectively grown InGaAs nanowire, as well as the HSQ growth mask. (b) Illustration of the three different growth surfaces, (i)-(iii), present in the selective growth of a crystal.

accounts for interactions between the crystal and nucleation surface. Furthermore, Dupré's equation relates β with σ and the interfacial energy σ_i [53]

$$\sigma_i = \sigma_o + \sigma_n - \beta \tag{4.2}$$

σ_i is the energy of the interface between original surface, with the surface energy σ_o, and the new surface, with the surface energy σ_n. For the formation of a nucleus from vapor on a crystal, that is interfaces (i) and (ii), the interfacial energy σ_i is approximately zero, because the bonding is similar to that of bulk, and $\sigma_o = \sigma_n = \sigma$, since the crystal surface does not change after nucleation. From equation (4.2), it follows that $\beta = 2\sigma$. Inserting this into equation (4.5) gives

$$\Delta G_i = -n\Delta\mu + Ph\sigma_i \tag{4.3}$$

$$\Delta G_{ii} = -n\Delta\mu + Ph\sigma_{ii} \tag{4.4}$$

for the two surfaces, top and side facets, associated with interfaces (i) and (ii). The difference between σ for different surfaces determines the shape of the nucleus and

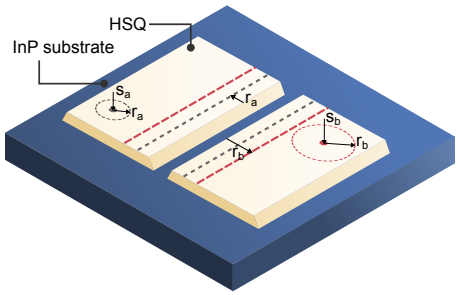

Figure 4.3: Illustration of selective growth of a binary semiconductor, indicating that the differences in sticking coefficient s and mean free path r for the two precursor results in different collection regions (red and black dashed traces) around the opening of the mask. This may cause a mask-induced enrichment effect, whereby the composition of the selectively grown patterns differ from the rest of the film.

as such the facet structure of the lateral nanowire. The surface with the lowest σ, in this case the top surface associated with (i), will be the preferred nucleation surface, thus the side surface associated with (ii) will be the dominating facet.

In the case of (iii), growth on the mask, there is approximately no interaction between the nucleus and the mask surface, $\beta \approx 0$. This is called self-nucleation because the Gibb's free energy is not reduced by interactions with a surface. Equation (4.5) gives

$$\Delta G_{iii} = -n\Delta\mu_{iii} + Ph\sigma_{iii} + 2A\sigma_{iii} \tag{4.5}$$

where μ_{iii} denotes the chemical potential difference of the nucleus-mask interface. Generally, ΔG_{iii} will be much higher than ΔG_i and ΔG_{ii} due to the addition of the third term, and so growth on the mask is suppressed.

4.1.1 MASK-INDUCED ENRICHMENT

In this work, we have shown that the indium molar fraction of a lateral InGaAs nanowire formed by selective area growth is different from that of the film layer, i.e. the material far away from the growth mask (Paper IX). This mask-induced enrichment has been observed previously on larger-scale selectively grown structures [54]. Figure 4.3 shows a schematic figure of the selective area growth of an arbitrary tertiary system $a_x b_{1-x} c$, with the sticking coefficient s and the mean free path r associated with the precursors a and b. r is the average path traveled by a precursor on the surface before it desorbs back into the vapor, and s is the probability that a precursor adsorbs to the surface. Due to the absence of growth on the mask, there

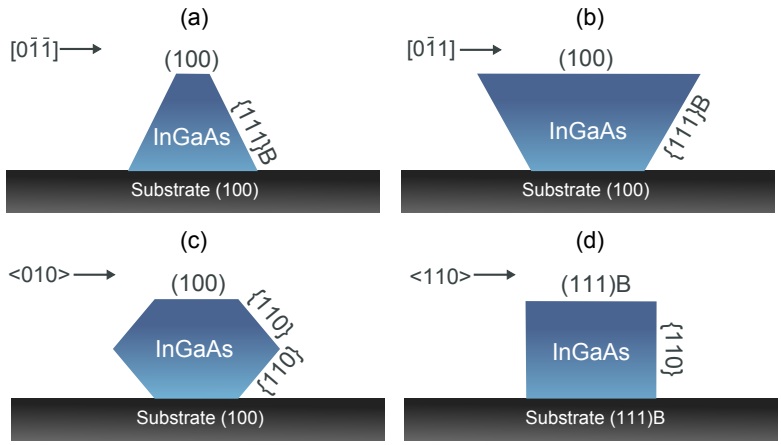

Figure 4.4: Schematic figure of four theoretically predicted single facet nanowire crystal shapes, with associated crystal directions and substrate orientations.

is a precursor-dependent collection area around the mask opening, determined by r. In addition to the vapour phase composition of the precursors, x of the selectively grown crystal is also dependent on r_a/r_b and s_a/s_b. Since both r and s are surface dependent, a difference in x for the film layer and the selectively grown crystal can arise.

4.1.2 NANOWIRE FACETS

The facet structure of the nanowire is determined by the substrate and nanowire orientations. Four predicted single facet crystal shapes are shown in Figure 4.4. Nanowires oriented as shown in Figure 4.4c have mostly been used in this work. As seen in Figure 1 in Paper IX, the experimental nanowire shape in this direction exhibits smaller or no bottom facets. This can be explained by that the growth of these facets is blocked by the HSQ mask. A change of the substrate orientation to (111)B can theoretically allow for nanowires with vertical sidewalls. A similar crystal shape was demonstrated by Akabori *et al.* for vertical InGaAs nanowires on InP (111)B [55].

4.2 CONTACT REGROWTH

In MOSFETs utilizing pn-junctions, or heterogenous doping junctions, at source and drain, doped regions must be formed on each side of the channel. In this work,

a n^+-n_i-n^+ structure is often used. In silicon technology, the doped regions are often formed by ion implantation. Ion implantation requires activation temperatures above 700 °C, which makes it unsuitable in a III-V FET process, due to its lower thermal budget [9].

Another key concern of III-V contacts is the relatively low doping saturation concentration, i.e. the maximum doping concentration. For InGaAs, n-type doping concentration, N_D, of $5 \cdot 10^{19}$ cm^{-3} is typically obtained. High doping concentration in the contacts is important since the contact resistance is approximately inversely proportional to N_D [56].

The development of in-situ doped selective MOCVD growth of raised source and drain contacts was a breakthrough for III-V FETs [57]. This technology allows for a thermal budget of below 600 °C and offers a highly controlled process, with respect to doping depth and concentration. Selective contact regrowth on Si was first demonstrated already in 1984 by Wong et al., but a high-performance III-V FET utilizing this technology was first demonstrated by Egard *et al.*, utilizing HSQ as a growth mask [57,58]. A similar process has been employed in the present work, where a so-called dummy gate, an HSQ line, is patterned across the channel by EBL (Figure 4.5a) to define the gate length in the subsequent growth step.

A further benefit of this technology is its self-aligned nature. Self-aligned, in this case, means that the highly doped regions are defined at the same time as the channel. There is no additional alignment and patterning step required to define a gate length of the device. This is a key requirement for device designs suitable at scaled gate-length, $L_G < 30$ nm, where typical alignment accuracy would interfere with the definition of such a small dimension.

4.2.1 SILICIDE-LIKE FORMATION

An alternative self-aligned contact formation scheme typically used in Si technology is Silicide, which entails the use of a blanket deposition of a metal layer (commonly Ni) in the device region [59]. During the subsequent annealing step, the gate stack shields the channel region, while the metal alloys to form contacts on each side of the gate. FETs with excellent performance utilizing a Silicide-like process has been developed by Kim *et al.* for various III-V systems, in particular utilizing Ni as the alloying metal [21].

A drawback of a Silicide-like process is that it does not readily facilitate a gate-last process. The standard process requires an alloying annealing step in the range of 300-400 °C post gate-stack deposition, which may present a risk of degrading the III-V interface or oxide quality. This issue could in principle be resolved by the

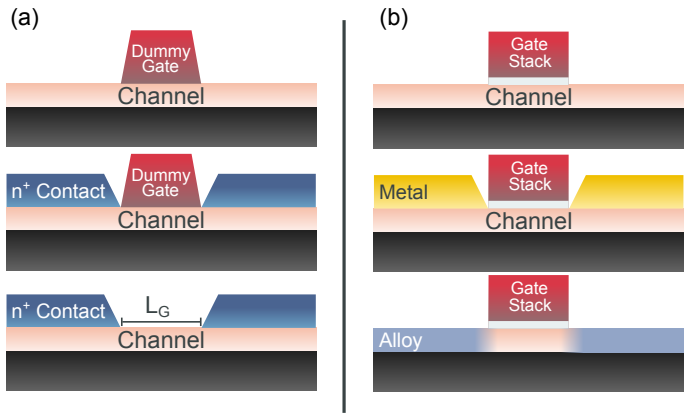

Figure 4.5: Schematic figure of two contact formation schemes. (a) Selectively grown contacts using a dummy gate to define the gate length. Allowing some overlap of the gate stack on contact regions, this process is self-aligned. (b) Silicide-like contact formation, using the gate stack to define the contacts in a self-aligned manner.

use of a dummy gate, but there is currently no experimental demonstration of this for III-V:s. During the alloying of Ni and InGaAs, there is also an effect of the Ni spreading and alloying underneath the gate [21]. Though this effect has been used to form sub-20 nm gate lengths, ultimately it may present a challenge in controlling the dimensions of the device. In contrast, selectively regrown raised contacts readily enable a gate-last process, as well as allow for sub-20 nm gate lengths with excellent control.

4.2.2 MOCVD CONTACT GROWTH

Regrown InGaAs contacts are commonly, as in this work, doped *in situ* by supplying a gas flow of tetraethyltin (TESn) during the growth of the layer [60]. The overall growth process for the n^+ $In_{0.63}Ga_{0.37}As$ contacts utilized in the present work is as follows: (i) Surface annealing under AsH_3 over pressure at 590 °C for 10 minutes. (ii) Lower reactor temperature to 500 °C. (iii) Grow the n^+ $In_{0.63}Ga_{0.37}As$ layer.

The flow of TESn to obtain peak doping concentration is a calibrated value, which is determined by a growth series of layers on which Hall measurements are performed to determine N_D [61]. Enough points in the series are needed in order to determine the peak of the TESn flow versus N_D relationship. N_D is reduced at excessive flows of TESn due to the formation of Sn islands in the material. Maximizing N_D is important in order to reduce the contact resistivity and the sheet resistance of the

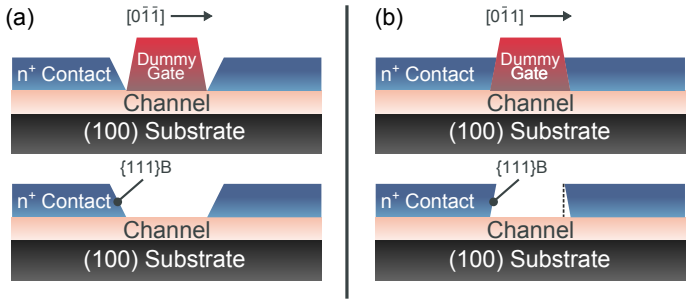

Figure 4.6: Illustrations of the contact facets in the (a) [0-1-1] and (b) [01-1] directions. In the first case, the contact facets have an outward slope. In the latter case, the contact facets have an inward slope, which may induce an ungated region under the ridge of the contact, if gate metallization is performed by evaporation.

contact layer.

The composition of the contact layer is chosen in relation to, in part, the thickness of the layer, in part, the composition of the channel material. Generally, higher molar fraction of In, up to InAs, provides lower contact resistivity due to surface Fermi level pinning in the conduction band [62]. Nittono et al. showed that higher In molar fraction up to 0.7 reduced the specific contact resistivity ρ_C, attributed to a reduction of the Schottky barrier height [63]. The InGaAs contact layer composition was therefore chosen as the highest possible In molar fraction, at a given thickness, without relaxation of the layer due to lattice mismatch to the channel and substrate. In this work, an In molar fraction of 0.63 was chosen, together with a contact thickness of 40 nm. To a certain limit, a thicker contact layer may provide a reduction of the contact resistivity and the sheet resistance, but a thick layer may interfere with the overall design of the device. Graded InGaAs-to-InAs contact layers have also been demonstrated, showing similar contact resistivity as for single InAs layers [64].

The facets, i.e. the facet surface chemistry and the facet angle, of the contact layer near the dummy gate is determined by the orientation of the dummy gate along the substrate surface. Figure 4.6 shows a schematic of two obtainable contacts facets, from the [0-1-1] and [0-11] directions, defined according to the figure. Both facets are {111}B types, but the facet angles are approximately +55° and -55°, respectively. The latter will typically interact with the dummy gate, since the contrast of the HSQ is high, forming an uneven edge, in addition to the overhanging part of the contact (dashed traces) which is not properly covered by metal through a standard

lift-off procedure.

4.3 MESA DEFINITION

In this work, a wet etch mesa definition process utilizing an HSQ etch mask was developed. 6% HSQ baked at 200 °C is utilized in this case, which exhibits good adhesion to the InGaAs surface, and allows for sharp definition of the mesa edges with very minor underetching. A H_3PO_4:H_2O_2:H_2O (1:1:25) solution is used to etch the InGaAs layers, with an etch rate of approximately 2 nm/s. Subsequently, the mesa is raised by an InP etch using HCl (1:1), with an etch rate of approximately 4 nm/s. This latter etch step is highly sensitive to the temperature of the solution, which is raised by self-heating at mixture.

The InGaAs mesa etch is isotropic, but the InP etch is anistropic. HCl (1:1) will etch (100) and (110) fast, and (111)B slowly. Etch rates of 0.1 nm/min, 1.4 nm/min and <0.01 nm/min have been reported for the three surfaces [65]. This anisotropicity is important for the formation of free-floating, i.e. suspended nanowires, where nanowires oriented along <110> can be more readily released from the substrate [66].

4.4 SOURCE AND DRAIN METALLIZATION

There are several candidates as the optimal contact metal to InGaAs, including Mo, Ti and Ni. The InGaAs surface rapidly oxidizes when exposed to air. For that reason, an *ex situ* pre-deposition oxide cleaning procedure is often employed, such as NH_4OH, diluted HCl and ammonium sulphide [67]. However, due to the high rate of the oxidation, it is uncertain to what extent this facilitates a true semiconductor-metal interface. *In situ* plasma cleaning is promising for that reason, with reports showing that the surface oxide can be removed without degradation of the surface quality [68].

Ti has been investigated as a contact metal due to its strong adhesion to InGaAs, as well as for providing oxygen gettering, i.e. oxygen scavenging, and for its relatively low melting temperature, allowing for deposition by thermal evaporation. On the other hand, Ti contacts are thermally unstable above 375 °C [63], which may affect high-current device operation as well. Specific contact resistivity of $\rho_C = 7\ \Omega\,\mu m^2$ has been demonstrated for Ti/InGaAs contacts, as well as $\rho_C = 8\ \Omega\,\mu m^2$ in this work using *ex situ* HCl surface cleaning [20].

The refractory metal Mo has also been investigated as a contact metal to InGaAs. Mo/InGaAs contacts have been shown to exhibit very low $\rho_C < 1\ \Omega\,\mu m^2$ and very

weak diffusion into the semiconductor, together with high temperature stability [64, 69].

Ni contacts have been investigated for instance due to their use in Silicide-like contact formation schemes [21]. For these contacts, $\rho_C = 5\,\Omega\,\mu m^2$ was demonstrated for the Ni-InGaAs/InGaAs alloy interface. Additional contact resistance arose in the Metal/Ni-InGaAs interface due to oxidation of the alloy. Ni/InAs contacts with very low $\rho_C < 1\,\Omega\,\mu m^2$ have been reported in vertical nanowires [70].

Theoretical calculations support both Ti and Mo in forming $\rho_C < 1\,\Omega\,\mu m^2$ contacts to InGaAs [71], with the metal work function playing only a minor role [56], therefore the metal choice should instead be motivated by e.g. thermal stability, oxidizing properties and process compatibility.

4.5 GATE OXIDE DEPOSITION

A number of different high-κ oxides have been evaluated as the gate oxide on InGaAs channels. Reactivity with Si, the formation of a silicide or an interfacial SiO_2 layer, originally limited the choice of high-κ oxides to ZrO_2, HfO_2, Al_2O_3, Y_2O_3 and La_2O_3 [72]. The contenders have remained mostly the same for InGaAs, with the Al_2O_3/HfO_2 bilayer and HfO_2 and ZrO_2 single layers receiving the most attention. Generelly, high-κ oxides exhibit dielectric constants ranging from 10 for Al_2O_3, to approximately 25 for HfO_2 and La_2O_3. A figure of merit for the resulting gate oxide is the equivalent oxide thickness

$$\mathrm{EOT} = d\frac{\kappa_{SiO_2}}{\kappa} \tag{4.6}$$

where κ is the dielectric constant of the gate oxide. A low value of EOT is only attractive if it is accompanied by a low gate leakage. However, EOT does not capture all of the effects of the gate oxide on device performance, such as the gate capacitance and the influence on carrier mobility.

Additional requirements include a band gap, E_G, of approximately 5 eV, thermal stability within the thermal budget of the device process, and band offset of above 1 eV to the substrate [13]. There is a relationship between κ and E_G, such that a high κ correlates with a small E_G [73]. This is qualitatively explained by that the dielectric constant relates to the polarizability of the oxide, and a high dielectric constant implies strong polarizability, which in turn implies weaker bonding and smaller E_G.

Finally, the high-κ oxide must form a high-quality interface to the semiconductor channel. High-quality here means the absence of interface and oxide defect states.

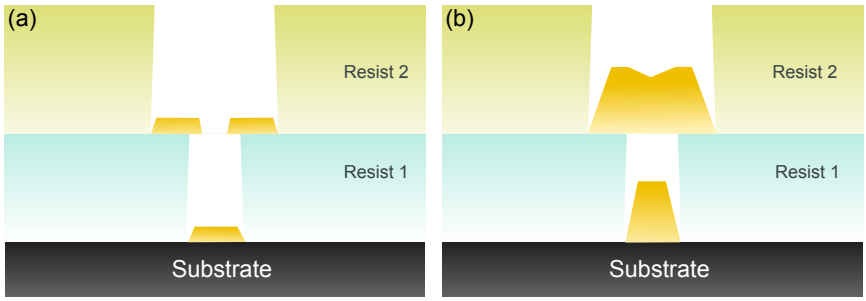

Figure 4.7: (a) Illustration of the bridging effect during thermal evaporation of metals, whereby lateral deposition forms a bridge across the opening. If the the aspect ratio of the opening versus the thickness of the resist 1 is high, the bridge may completely block further evaporation, causing a disconnect of metal and collapse of the structure.

The charging and de-charging of defect states during device operation, as shown in Chapter 2, can be described as a parasitic capacitance element, degrading the performance of the device in both off and on states. Defect states deep in the oxide are called border traps, and degrade the transconductance of the transistor [74]. Moreover, defects may cause a reduction of the carrier mobility, through increased coulomb scattering by the charged defect state.

Several ways of improving the III-V/oxide interface have been explored. Pre-deposition cleaning procedures include the treatment of the III-V surface with sulphur, e.g. using $(NH_4)_2S$ solution, immediately prior to oxide deposition, and has been shown to reduce the interface defect density [75]. Other methods include the use of an interfacial layer, engineering of the deposition conditions and parameters, in particular the deposition temperature, as well as PDA treatments [76]. A promising approach is *in situ* surface pre-cleaning using N_2 and H_2 plasma [77]. For Al_2O_3/HfO_2 bilayers, *in situ* pre-treatment with several pulses of trimethylaluminum is commonly used.

4.6 GATE METALLIZATION

Several choices for the gate metal in high-performance III-V FETs have been reported, such as Mo, TiN, Ni, Pd, W , Al and Ti [18, 78–80]. III-V MOS studies tend to focus on high-κ deposition rather than metallization, therefore there are few conclusive results indicating the better metal. Burek et al. showed that electron beam deposition of Ni caused a significant increase of D_{it} as compared to thermally

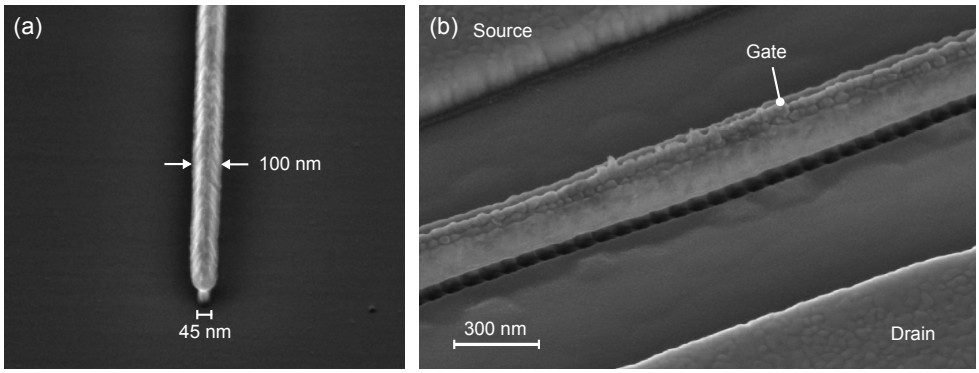

Figure 4.8: SEM images of a fabricated T-gate using the fabrication flow depicted in Figure 4.11. (a) Bottom and middle metal layers after the first patterning and lift-off step, with characteristic dimensions. (b) Completed T-gate with all three segments. The nanowires are visible underneath the sides of the gate.

evaporated Ni, which was attributed to damage caused to the III-V surface by energetic species such as electrons and ions generated during deposition [81]. Pt was found to behave similarly to Ni and produce interfaces with similar D_{it}. It was also found that a forming gas PDA at 400 °C for 50 min could heal the damage and restore D_{it} to equal levels. However, these results where on MOSCAP structures, and may not transfer to MOSFETs, in particular in a gate-last process, where the S/D contacts could be damaged.

Similar results where reported by Chen *et al.*, who studied the damage caused by thermal and electron beam evaporation, as well as sputtering on buried InGaAs quantum wells through photoluminescence [82]. It was found that shallow wells were more damaged and that electron beam evaporation caused the greatest damage, followed by sputtering and thermal evaporation at similarly low levels. Several studies report a direct relation between deposition-induced damage and the concentration of free carriers in the III-V material, i.e. N_D, e.g. by deterioration of I-V characteristics [82, 83].

4.6.1 T-GATE FORMATION

For RF-compatible devices, a T-gate is fabricated in order to reduce the gate resistance. Several T-gate fabrication schemes have been explored in this work. The first scheme employs air spacers and a low-sensitivity/high-sensitivity bilayer resist stacks and several metallization steps, and is shown in figure Figure 4.11. An

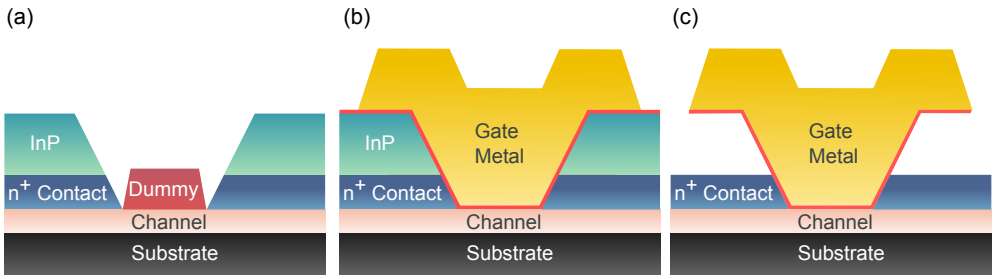

Figure 4.9: Process flow for the T-gate formation scheme using a sacrifical InP layer.

80 nm PMMA A2/180 nm MMA EL9 bilayer with a single pixel line (SPL) dose is used to define the bottom part of the gate, which determines the gate length. The middle part of the gate is defined by backscattering from the single pixel line dose. The metal thickness in the first metallization step is approximately 120 nm. The width of the bottom part is $L_G < 50$ nm, and the width of the middle part is approximately 100 nm (Figure 4.8a). The air spacers are defined as the distance S between the bottom part of the gate and the source and drain contacts, as indicated in Figure 4.11a.

Subsequently, an 80 nm PMMA A2/380 nm MMA EL9 bilayer is used to define the top part of the gate. Since the height of the bottom and middle parts is greater than the thickness of the PMMA A2, the gate is only weakly covered by resist, and the resist thus acts as a spacer layer for the metallization of the top part. The remaining resist on the gate can be removed by a SPL dose on top of the gate and/or dry etching. Finally, the top part is metallized using 150 nm metal (Figure 4.8b). The purpose of this scheme is to reduce forward scattering in the definition of L_G, as well as to decrease the aspect ratio of the bottom part of the gate, to lessen the effect of bridging.

Optimizations of the T-gate dimensions include shorter gate length, taller bottom part, narrower middle part, and wider top part. Reduction of the gate length is challenged by forward scattering through the resist stack, which degrades the single pixel line resolution. Forward scattering can be reduced by minimizing the total thickness of the bi-layer resist stack. A shorter gate length also increases the risk of bridging, which is the formation of a bridge from one side of the opening to the other, shielding evaporation into the opening and causing a disconnect between the foot and the head of the T-gate (Figure 4.7).

A second T-gate fabrication scheme, which was used in Papers VI to VIII, is shown in Figure 4.9. This process yields a self-aligned T-gate, but no air spacers.

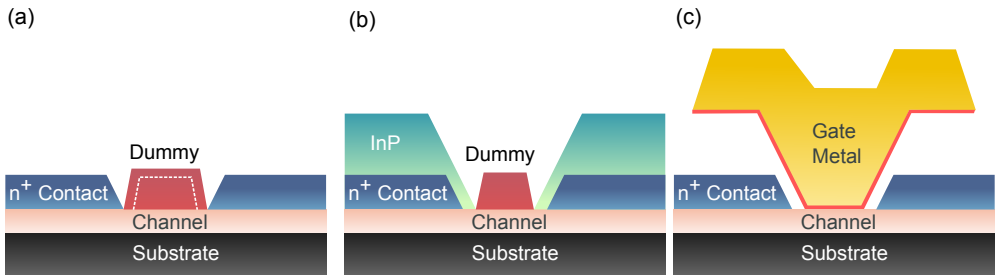

Figure 4.10: Process flow for the T-gate formation scheme using an etched dummy and sacrifical InP layer to form air spacers.

Here, a sacrificial InP layer is grown on top of the InGaAs contact layer, in the same MOCVD growth step. After gate stack deposition, the InP layer is etched by HCl, which leaves a T-gate. The overlap between the bottom of the T-gate and the source and drain contacts, however, causes an increase of the parasitic capacitances.

A variation of this process is shown in Figure 4.10. After growth of the InGaAs contact layer, the HSQ dummy layer is etched by strongly diluted HF. The width of the dummy gate is reduced by approximately 30 nm. Subsequently, the InP sacrificial layer is grown, which finally yields a self-aligned T-gate with air spacers. The main challenge of this process is the etching of the InP in the narrow region between the gate and the source and drain contacts.

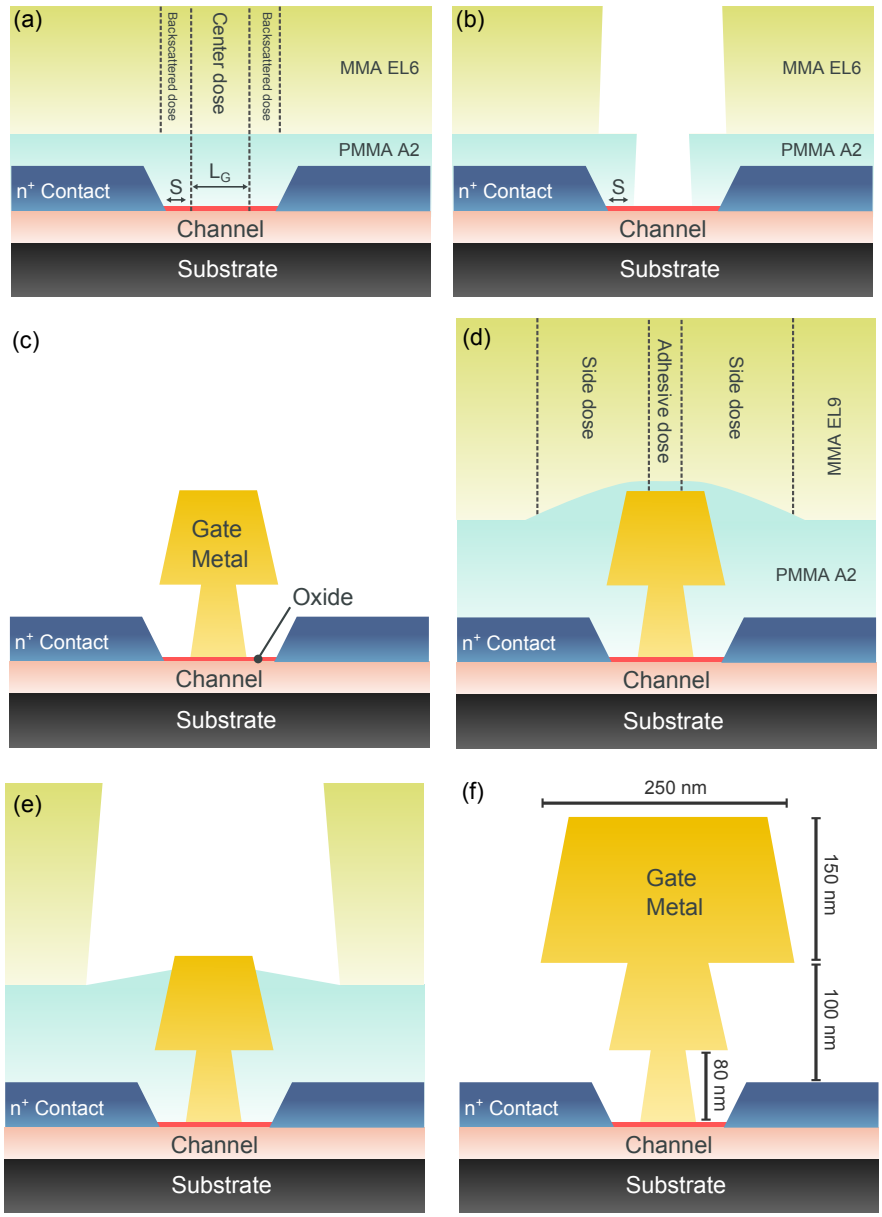

Figure 4.11: Schematic figure of a T-gate formation scheme using multiple lithography and metallization steps. (a)-(c) First, the bottom and middle segments are patterned and metallized (d)-(f) Secondly, the top segment is patterned by use of a resist spacer layer, which is etched during the lift-off of the metal.

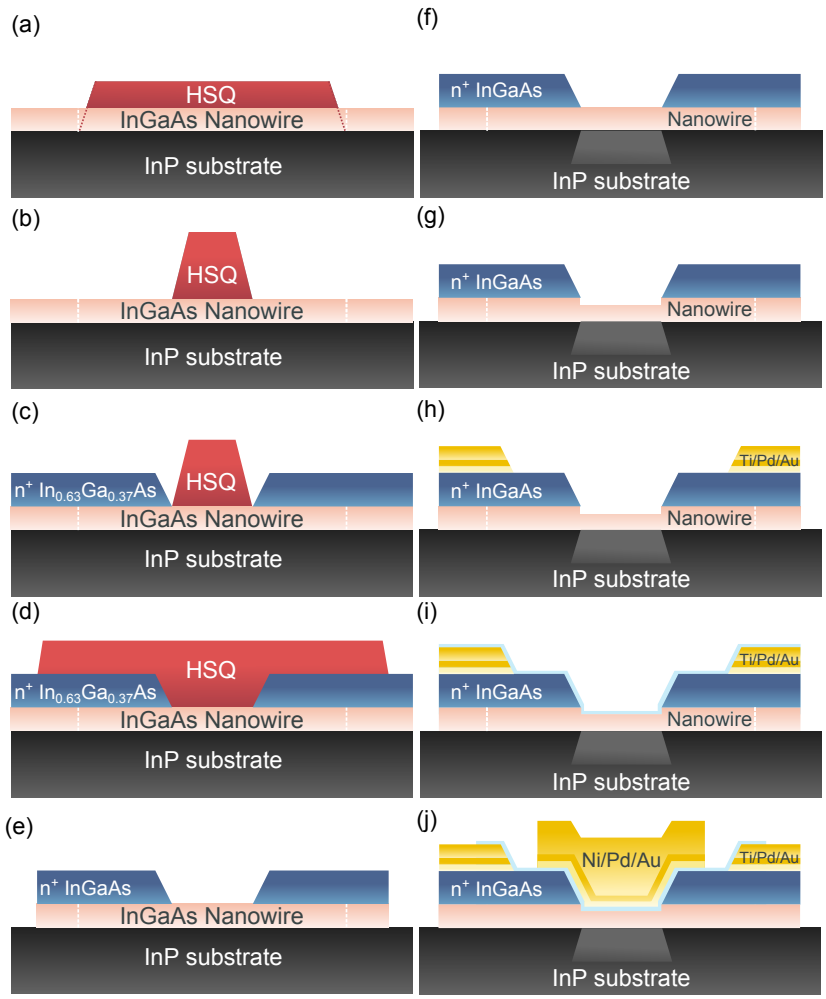

Figure 4.12: Schematic figures of the device process utilized in the work of Paper I. (a) The InGaAs nanowire channel is formed by selective area growth, as previously described. (b) An HSQ dummy gate is patterned across the nanowires, which defines the gate length of the device. (c) The highly doped InGaAs contacts are grown. (d) The dummy gate is stripped, an HSQ etch mask is patterned on the device area. (e) Mesa etch is performed using the HSQ etch mask to define the mesa. (f) A partial etch of the InP in the channel region is performed, as well as (g) digital etching of the nanowires. (h) Source and drain metal is patterned and deposited by thermal evaporation and lift-off. (i) Gate oxide is deposited by atomic layer deposition. (j) Gate metallization is performed by lift-off.

5

Summary and Conclusions

During the time of this doctoral research, I have authored and co-authored several peer-reviewed publications. Here I will summarize a selection of these works, provide context and highlight their main contributions to the research field. Papers I-V detail the development of VLSI-compatible, low-power, III-V FETs in reverse chronological order. Figure Figure 5.1 summarizes the performance of devices presented in these papers over time. Papers VI-VIII relate to III-V FETs optimized for RF-performance. Papers IX to XII detail work in characterizing these kinds of devices, including noise, oxide and low-temperature characterization. A list of key results and changes in the device design and fabrication process follows.

5.1 SUMMARY OF PAPERS

VLSI-COMPATIBLE FETS

Paper V: $In_{0.53}Ga_{0.47}As$ Multiple-Gate Field-Effect Transistors With Selectively Regrown Channels

C. Zota, L.-E. Wernersson and E. Lind, IEEE Electron Device Letters 35(3), 2014

The first InGaAs FET utilizing selectively grown lateral nanowires is demonstrated [84]. The design employs a self-aligned contact regrowth scheme, developed by others in the group [57], and is RF-compatible, with a T-gate and 200 parallel nanowires split over two gates. Peak g_m is 1.7 mS/µm, and SS is 185 mV/decade at L_G = 32 nm.

Paper IV: Single Suspended InGaAs Nanowire MOSFETs

C. Zota, L.-E. Wernersson and E. Lind, IEEE International Electron Device Meeting (IEDM), 2015

InGaAs FETs with the, at the time, highest reported g_m = 3.3 mS/µm for FETs in any material system are reported [85]. The increase of g_m follows primarily from a series of optimizations of the Ohmic contacts, where the Indium molar fraction of the contact layer was increased from 0.53 to 0.63, and the doping concentration was recalibrated to its peak value. Due to

these changes, the total contact resistance was reduced from about 120 to 25 Ω µm. These devices are the first of a new generation of devices, which specifically target VLSI applications, by employing a single nanowire as the channel and a truly gate last process, in exchange for the loss of RF compatibility.

Paper III: InGaAs Nanowire MOSFETs With I_{ON} = 555 uA/um at I_{OFF}= 100 nA/um and V_{DD} = 0.5 V

C. Zota, F. Lindelow, L.-E. Wernersson and E. Lind, IEEE Symposium on VLSI Technology (VLSI), 2016

A record on-current (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) of 555 µA/µm is reported [86]. This can be compared with the on-current of about 150 µA/µm in the devices of paper IV. The large improvement is due to a significant lowering of the subthreshold slope to 80 mV/decade in these devices, as well as a lowering of the voltage of peak g_m. The suspended nanowire scheme in paper IV is abandoned due to its complexity and negative impact on the yield. Key optimizations in this work relate to the gate oxide and nanowire dimensions.

Paper II: High-Performance Lateral Nanowire InGaAs MOSFETs With Improved On-Current

C. Zota, L.-E. Wernersson and E. Lind, IEEE Electron Device Letters 37(10), 2016

This work presents a improvement of the on-current to 565 µA/µm, and a study of the scaling behavior of these devices versus nanowire width and gate length [87]. The ultimate limit of III-V FETs is explored through simulations of, and comparisons with, ideal performance.

Paper I: InGaAs Tri-Gate MOSFETs With Record On-Current

C. Zota, F. Lindelow, L.-E. Wernersson and E. Lind, IEEE International Electron Device Meeting (IEDM), 2016

An on-current (at I_{OFF} = 100 nA//µm and V_{DD} = 0.5 V) of 650 µA/µm is reported, which, to this date, represents the record value of all transistors [88]. Key changes include: (i) Implementation of a "pillar etch", selective etching of the InP at the sides, but not underneath, the nanowire, ideally improving the electrostatics of the device. (ii) Optimization of the number and the location in the process order of digital etches. (iii) Scaling down of the effective oxide thickness (EOT). (iv) Optimization of the gate oxide passivation process. (v) Further increased Indium

molar fraction in the nanowire layer to above 0.8.

RF-COMPATIBLE FETS

Paper VIII: $In_{0.63}Ga_{0.37}As$ FinFETs Using Selectively Regrown Nanowires With Peak Transconductance of 2.85 mS/um at V_{DS} = 0.5 V

C. Zota, L.-E. Wernersson and E. Lind, Device Research Conference (DRC), 2014

A device with $f_t = 281$ GHz and $f_{max} = 365$ GHz at $V_{DS} = 1$ V is demonstrated [89]. This f_t represents the highest reported value for a non-planar III-V FET, and is close to the top value reported even for planar III-V FETs. Compared to the previous work in paper V, which exhibited $f_t = 210$ and $f_{max} = 250$ GHz, the main improvement comes from the increased intrinsic transconductance, which is increased from about 2.8 to well over 3 mS/µm in this work.

Paper VII: Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs

(C. Zota, G. Roll, Lars-Erik Wernersson and Erik Lind, IEEE Transactions on Electron Devices 61(12), 2014

Devices similar to those in paper VIII are here studied in detail. S-parameter modelling is performed to determine a small-signal model [90]. The small-signal includes both impact ionization and border traps, and shows a good fit to measurement data. The parasitic gate-to-source and gate-to-drain capacitances are determined and analyzed. Several schemes to enhance performance are suggested based on the analysis.

Paper VI: High-Frequency InGaAs Tri-Gate MOSFETs With f_{max} of 400 GHz

C. Zota, F. Lindelow, L.-E. Wernersson and E. Lind, Electronics Letters 52(22), 2016

A record combined $f_t = 275$ GHz and $f_{max} = 400$ GHz for III-V MOSFETs at a reduced V_{DS} of 0.5 V is reported [91]. The f_{max} in this work is also the record value for all III-V MOSFETs. This improvement is achieved by in part a reduction of L_G to 20 nm, and in part an optimization of the T-gate structure.

DEVICE CHARACTERIZATION

Paper IX: Quantized Conduction and High Mobility in Selectively Grown $In_xGa_{1-x}As$ Nanowires

(C. Zota, D. Lindgren, Lars-Erik Wernersson and Erik Lind, ACS Nano 9(10), 9892, 2015)

Quantized conductance was reported for single nanowire devices similar to those presented in Paper 1. A mean free path of approximately 180 nm was determined from the transmission at 10 K, as well as an effective electron mobility of approximately 3300 cm^2/Vs [92]. In addition, the nanowires where optically characterized through photoluminescence and Raman spectroscopy measurements. A mask-induced indium enrichment effect was observed, which increased the indium molar fraction in the nanowires from 0.63 to 0.85, as compared to a reference planar film.

Paper X: Size-Effects in Indium Gallium Arsenide Nanowire Field-Effect Transistors

(C. Zota and E. Lind, Applied Physics Letters 108, 063505, 2016)

This work presents further low-temperature studies, investigating quantized conductance as a function of nanowire dimensions [93]. The nanowire size dependence of the quantization is modeled and found to be well explained by an asymmetric effective mass quantum well model. More importantly, a threshold voltage increase for smaller nanowires is observed, and established to be caused by quantization of the first subband. This effect becomes severe at widths of below 15 nm and causes a degradation of the threshold voltage variability, since a small variation in the width, will cause a large shift in the threshold voltage.

Paper XI: A Method for Determining Trap Distributions of Specific Channel Surfaces in InGaAs Tri-gate MOSFETs

(S. Netsu, M. Hellenbrand, C. Zota, Y. Miyamoto and E. Lind, Journal of the Electron Device Society, 2017)

A method for calculating the interface trap distributions on each surface of a multi-gate device is presented. This is done by measuring the hysteresis of I-V characteristics on devices with different channel dimensions, and modeling the hysteresis as a function of the total trap distribution, which is a linear combination of the distributions of each channel surface. The method is applied to InGaAs

nanowire devices similar to those in Paper I, and it is found that the (100) surfaces exhibit almost an order of magnitude lower minimum trap density compared to the {110} side walls, which may be explained by the specific surface chemistries.

Paper XII: 1/f and RTS Noise In InGaAs Nanowire MOSFETs

(C. Mohle, C. Zota, M. Hellenbrand and E. Lind, Microelectronics Journal, 2017)

Low-frequency noise measurements are performed on devices similar to those in Paper I. 1/f noise measurements show among the lowest reported minimum input gate voltage noise for III-V FETs, indicating the feasability of a high-quality high-κ gate oxide on InGaAs. Number fluctation rather than mobility fluctuation is also shown to be the dominant noise source. Random telegraph signal measurements indicate trap response from deep in the oxide, with large current fluctuation amplitude.

5.2 FUTURE WORK

Potential improvements to the present work will be highlighted here, categorized as improvements to the off-state and on-state, as well as additional improvements specifically to RF-performance.

5.2.1 OFF-STATE IMPROVEMENTS

1. Reduction of the overall dimensions of the nanowire: In this work, a strong improvement of off-state performance is been observed as the nanowire width is scaled down to below 30 nm (Paper I). Further scaling to 10 nm may offer additional enhancements.

2. Implementation of an electrostatically stronger channel structure, i.e. gate-all-around, or fins: Low-aspect ratio nanowires have mainly been explored in this work, but symmetrical nanowires and gate design offers optimal electrostatic control. High-aspect ratio fins present a compromise between process complexity and electrostatic control.

3. Improvement the interface and oxide quality, reduction of D_{it}, for instance, utilizing plasma-enhanced atomic layer deposition (ALD) processes [13].

4. Reduction of the EOT to below 7 Å: While the devices of the present work are expected to operate quite close to the quantum capacitance limit, the trend shown in Paper I indicates that further enhancement of SS due to EOT scaling is possible.

5.2.2 ON-STATE IMPROVEMENTS

1. Scaling of L_G to below 20 nm: A transmission of approximately 70% at LG $\approx$ 70 nm has been demonstrated in this work (Paper X). Assuming similar λ, the transmission can be improved to approximately 90%, i.e. a 25% improvement of I_{ON}, by reducing L_G to < 20 nm.

2. Improvement of the electron mean free path in the nanowire. This can be done by reducing the background doping in the nanowires, improving the line edge roughness of the nanowires and increasing the indium molar fraction in the nanowires.

3. Reduction of EOT to below 7 Å. EOT scaling may also improve g_m, as shown in Chapter 2. In particular by counteracting the degradation due to D_{it}.

For instance, Hashemi *et al.* demonstrated SiGe MOSFETs with excellent performance in part enabled by the EOT of 7 Å [94].

4. Reduction of the overall parasitic resistances, e.g. by reduction of the contact resistance. The devices of the present work typically exhibit $R_C \approx 25\ \Omega\,\mu m$, with on-resistance typically $R_{ON} < 200\ \Omega\,\mu m$. Implementation of contacts, for instance Mo, with $\rho_C < 1\ \Omega\,\mu m^2$ could thus offer a significant improvement to g_m.

5. Implementation of a high-aspect ratio channel, i.e. fins. Selective growth of high-aspect ratio InGaAs is theoretically possible, for instance using (111)B substrates with careful engineering of fin directions and dimensions, as well as control of growth facets. This allows for increased current density per chip area.

5.2.3 RF-PERFORMANCE IMPROVEMENTS

1. Implementation of a self-aligned spacer formation scheme, for instance by use of SiN spacers. This will improve the yield of the process, as well as allow for more reliable impedance matching in low noise amplifiers.

2. Overall optimization of nanowire layout, in particular the nanowire dimensions and the spacing between nanowire, which should be minimized.

3. Optimization of the T-gate design in terms of shape and dimensions, according to what was discussed in Chapter 4.

5.3 CONCLUSIONS

This work has explored the limits of III-V transistor performance. Figure 5.1 shows a summary of some of the performance improvements achieved here. Several records where achieved, such as the highest on-current for any transistor, best performing junctionless transistor and highest combined f_t/f_{max} for a III-V MOSFET. These devices where characterized through various techniques, such as noise measurements at low and high frequencies, oxide characterization, Hall measurements and low-temperature investigation of electron scattering in the channel, indicating excellent oxide properties as well as channel material quality. The overall emerging picture here is of a technology with real potential for many different applications.

For digital applications, III-V transistors often solicit the comparison to silicon CMOS technology, and the question of the feasability of its replacement by III-V technology. In Paper I, the first, or one of the first, experimental III-V transistors outperforming state-of-the-art silicon devices in VLSI-relevant performance metrics is demonstrated. A complete answer to the industrial viability of III-V transistors in CMOS, however, is a function of not only transistor performance, but also of economical incentives and is such outside the scope of this work.

On the other hand, recent times have shown that the potential of technology is not easily predicted. As power consumption of digital circuits was reduced by various performance enhancing schemes on circuit and device level, completely new applications where enabled, which were from the onset not easily predictable. As such, the performance of III-V transistors should be evaluated, ultimately, not only in the realm of density scaling, incremental reduction of power consumption, but also in the realm of actual applications.

To use a concrete example, if the reduction of power consumption of a particular circuit is reduced by a certain percentage, this improves various aspects of the circuits use incrementally. But what if the power consumption becomes low enough that the circuit may be fully powered by a co-integrated energy harvesting scheme? Completely new applications will emerge, and the gain can no longer be called incremental. In this sense, the pay-off of performance enhancement is not as linear as it may seem. A few milliwatts could open entirely new doors.

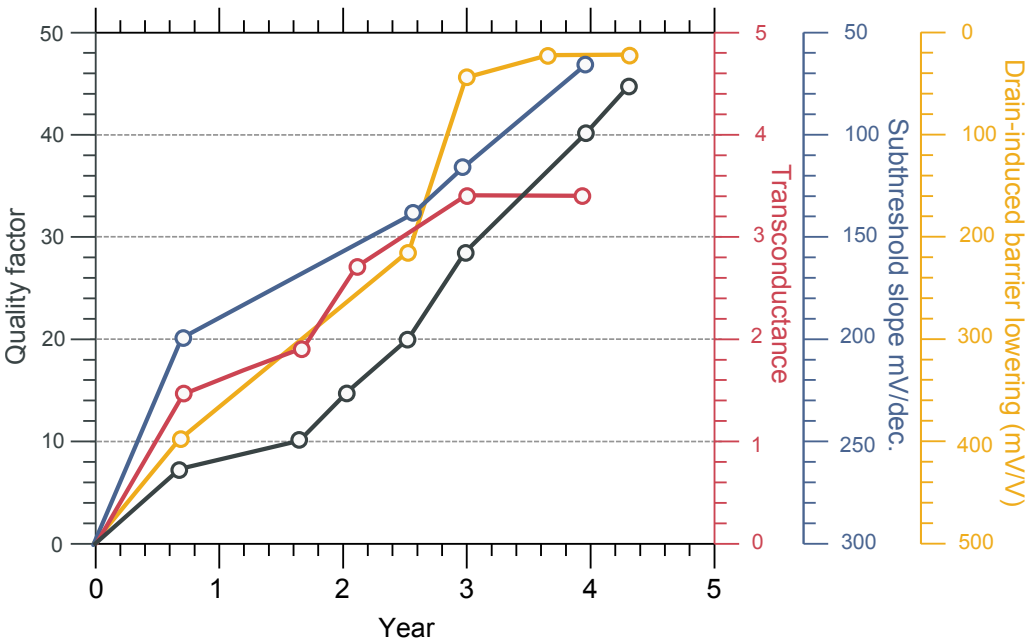

Figure 5.1: The performance of the transistors developed in this work over the duration of the project. The transconductance, the drain-induced barrier-lowering, the subthreshold slope and the quality factor, defined as the transconductance over the subthreshold slope, in particular, are shown.

A

Appendix A

A.1 DEVICE FABRICATION

The following process was developed for the fabrication of the single-nanowire MOSFETs characterized in paper I.

A.1.1 SINGLE NANOWIRE MOSFETS

1. **Sample preparation**
   Cut (100) InP:Fe (S.I.) into appropriately sized pieces.

2. **Organic cleaning (degreasing)**
   2 min in 60 °C acetone on hot-plate.
   1 min in ultra-sonic bath at medium power.
   2 min in 60 °C acetone on hot-plate.
   2 min in 60 °C iso-2-propanol on hot-plate.

3. **Ozone cleaning**
   10 min with 500 sccm O_2 flow in ozone cleaner.
   ▶ This step is assumed to improve HSQ adhesion to InP. The purpose is to provide a properly oxidized surface.

4. **Demoisturizing bake**
   5 min on 200 °C hot-plate.

5. **Resist dilution**
   1:3 HSQ:MIBK (1.5%), MIBK is methyl isobuthyl ketone, diluted just prior to application in a pre-cleaned dry and cold plastic bottle.

6. **Resist application**
   Spin-on at 3000 RPM, 1500 RPM/s for 1 min.
   Bake at 200 °C on hot-plate for 2 min.
   ▶ 1.5% HSQ under these conditions gives patterns that are 20-25 nm tall depending on EBL dose.
   ▶ Baking temperature is one of the most important factors for adhesion of HSQ on InP, where a higher baking temperature generally improves adhesion.

7. **EBL 1: Nanowire patterning**

   Expose at the maximum resolution settings (typically the lowest current) of the EBL system. Here was used 50 kV acceleration voltage, 2 nm step size, 240 pA current and a base dose of 500 $\mu C/cm^2$ for very large features.

8. **Development and surface cleaning**

   90 s in tetra-methyl ammonium hydroxide (25%).

   2 min in H_2O, rinsed twice.

   2 min in iso-2-propanol, rinsed twice, then blow-dry with N_2.

   10 s in hydrochloric acid (1:5).

   1 min in H_2O, then blow-dry with N_2.

   ▶ The purpose of the iso-2-propanol rinse is to enable more gentle blow-drying of the sample. After the hydrochloric acid cleaning step, the surface becomes hydrophobic, thus blow-drying trivial.

9. **MOCVD 1: Nanowire growth**

   Growth of 13 nm $In_{0.63}Ga_{0.37}As$ at 500 °C, with surface cleaning at 690 °C in Ph_3 over-pressure. Here, an Aixtron 200/4 MOCVD system was used.

10. **HSQ removal and surface cleaning**

    2.5 min in 10:1 buffered oxide etch solution.

    1 min in H_2O.

    2 min in acetone.

    1 min in iso-2-propanol.

11. **Digital etching**

    7 min with 500 sccm O_2 flow in ozone cleaner.

    10 s in hydrochloric acid (1:10).

    1 min in H_2O.

    Repeat once for a total of two cycles.

    ▶ Each cycle etches approximately 1.4 nm from the height and 4 nm from the width.

12. **Resist application**

    Bake at 200 °C on hot-plate for 2 min.

    Spin-on 6% HSQ at 3000 RPM, 1500 RPM/s for 1 min.

    Bake at 200 °C on hot-plate for 2 min.

13. **EBL 2: Dummy gate patterning**
    Expose at the maximum resolution settings. A 30 nm wide dummy gate will require approximately 3000 µC/cm^2.

14. **Development and surface cleaning**
    2 min in tetra-methyl ammonium hydroxide (25%).
    2 min in H_2O, rinsed twice.
    2 min in iso-2-propanol, rinsed twice, then blow-dry with N_2.

15. **MOCVD 2: Raised contacts growth**
    Growth of 30 nm $In_{0.63}Ga_{0.37}As$ doped with Sn at 500 °C, with surface cleaning at 590 °C.

16. **HSQ removal and surface cleaning**
    3 min in 10:1 buffered oxide etch solution.
    1 min in H_2O.
    2 min in acetone.
    1 min in iso-2-propanol.

17. **Resist application**
    Bake at 200 °C on hot-plate for 2 min.
    Spin-on 6% HSQ at 3000 RPM, 1500 RPM/s for 1 min.
    Bake at 200 °C on hot-plate for 2 min 15 s.

18. **EBL 3: Mesa etch mask**
    A 1 by 10 µm^2 mesa pattern will require approximately 1000 µC/cm^2.

19. **Development and surface cleaning**
    2 min in tetra-methyl ammonium hydroxide (25%).
    2 min in H_2O, rinsed twice.
    2 min in iso-2-propanol, rinsed twice, then blow-dry with N_2.

20. **Mesa etch**
    40 s in H_3PO_4:H_2O_2:H_2O 1:1:25.
    1 min in H_2O.
    5 s in hydrochloric acid (1:1).
    1 min in H_2O.
    3 min in 10:1 buffered oxide etch solution.

1 min in H_2O.

▶ The first etching step etches the InGaAs, the second etches approximately 10 to 20 nm of substrate InP, the third etches the HSQ. A color change indicates complete etching of the InGaAs layer.

21. **Pillar etch and digital etching**

    8 min with 500 sccm O_2 flow in ozone cleaner.

    8 s in hydrochloric acid (1:1).

    1 min in H_2O.

    8 min with 500 sccm O_2 flow in ozone cleaner.

    10 s in hydrochloric acid (1:5).

    1 min in H_2O.

    ▶ The first etching step etches approximately 20 to 30 nm of substrate InP in the channel, forming a "pillar" on which the nanowire rests, due to etching anisotropy. In total this step constitues two cycles of digital etching for a total of four intentional cycles. Additional unintentional cycles are expected from etching the HSQ by buffered oxide etch solution.

22. **Resist application**

    Bake at 200 °C on hot-plate for 2 min.

    Spin-on PMMA 950 A8 at 4500 RPM, 1500 RPM/s for 50 s. The resist layer thickness is 900 nm.

    Bake at 180 °C on hot-plate for 2 min 15 s.

23. **EBL 4: Source and drain contacts and pads**

    A very large pattern will require approximately 325 µC/cm^2, using the EBL settings described here.

24. **Development and surface cleaning**

    90 s in 1:3 methyl isobutyl ketone and iso-2-propanol.

    30 s in iso-2-propanol.

25. **Metallization 1: Source and drain**

    35 s at 5 mbar O_2 pressure in oxygen plasma etcher.

    Thermal evaporation of 140/160/2000 Å Ti/Pd/Au, using rotating sample.

    2 h in acetone.

    1 min in iso-2-propanol.

    38 s at 5 mbar O_2 pressure in oxygen plasma etcher.

26. **Surface passivation and gate oxide deposition**
    8 min with 500 sccm O_2 flow in ozone cleaner.
    20 min $(NH_4)_2S$:H_2O (1:1).
    7 s in H_2O, stirred.
    Atomic layer deposition: 5 cycles of TMAl, 5 cycles of Al_2O_3 at 300 °C, 35 cycles of HfO_2 at 125 °C.

27. **Resist application**
    Bake at 200 °C on hot-plate for 2 min.
    Spin-on PMMA 950 A8 at 4500 RPM, 1500 RPM/s for 50 s. The resist layer thickness is 900 nm.
    Bake at 180 °C on hot-plate for 2 min 15 s.

28. **EBL 5: Gate metal and pad**
    A 300 nm wide gate pattern will require approximately 740 $\mu C/cm^2$, using the EBL settings described here.

29. **Development and surface cleaning**
    90 s in 1:3 methyl isobutyl ketone and iso-2-propanol.
    30 s in iso-2-propanol.

30. **Metallization 2: Gate**
    35 s at 5 mbar O_2 pressure in oxygen plasma etcher.
    Thermal evaporation of 450/50/1400 Å Ni/Pd/Au, using rotating sample.
    2 h in acetone.
    1 min in iso-2-propanol.
    38 s at 5 mbar O_2 pressure in oxygen plasma etcher.

A.1.2 RF-COMPATIBLE MOSFETS

For RF-compability, the following changes to the process are made:

- 200 parallel nanowires are formed, split over two gate fingers.
- RF-pads are patterned, adapted to the pitch of the RF-probes.
- A T-gate is used, which is patterned at a separation from the source and drain regions in the channel.

A description of the T-gate formation process follows.

1. **Resist application**
   Bake at 200 °C on hot-plate for 2 min.
   Spin-on PMMA 950 A2 at 3500 RPM, 1500 RPM/s for 45 s. The resist layer thickness is approximately 90 nm.
   Bake at 180 °C on hot-plate for 2 min.
   Spin-on Copolymer MMA EL6 at 2000 RPM, 1500 RPM/s for 45 s. The resist layer thickness is approximately 180 nm.
   Bake at 150 °C on hot-plate for 90 s.

2. **EBL 5: Bottom and middle gate metal**
   A single pixel line gate pattern (45 nm wide) will require approximately 4000 pC/cm, using the EBL settings described here. This gives a middle gate width of approximately 100 nm.

3. **Development and surface cleaning**
   90 s in 1:3 methyl isobutyl ketone and iso-2-propanol.
   30 s in iso-2-propanol.

4. **Metallization 2: Bottom and middle gate**
   7 s at 5 mbar O_2 pressure in oxygen plasma etcher.
   Thermal evaporation of 50/50/780 Å Ti/Pd/Au, using rotating sample. Centralization of the sample relative the metal source is important to avoid bridging and self-shadowing.
   30 min in acetone at 60 °C on hot-plate.
   1 min in iso-2-propanol.
   20 s at 5 mbar O_2 pressure in oxygen plasma etcher.

5. **Resist application**
   Bake at 200 °C on hot-plate for 2 min.
   Spin-on PMMA 950 A8 at 4500 RPM, 1500 RPM/s for 50 s. The resist layer thickness is 900 nm.
   Bake at 180 °C on hot-plate for 2 min 15 s.

6. **EBL 6: Gate pad**

7. **Development and surface cleaning**
   90 s in 1:3 methyl isobutyl ketone and iso-2-propanol.
   30 s in iso-2-propanol.

8. **Metallization 3: Gate pad**
   35 s at 5 mbar O_2 pressure in oxygen plasma etcher.
   Thermal evaporation of 50/100/1200 Å Ti/Pd/Au, using rotating sample.
   2 h in acetone.
   1 min in iso-2-propanol.
   38 s at 5 mbar O_2 pressure in oxygen plasma etcher.

9. **Resist application**
   Bake at 200 °C on hot-plate for 2 min.
   Spin-on PMMA 950 A2 at 3000 RPM, 1500 RPM/s for 45 s. The resist layer thickness is approximately 100 nm.
   Bake at 180 °C on hot-plate for 2 min.
   Spin-on Copolymer MMA EL9 at 4500 RPM, 1500 RPM/s for 45 s. The resist layer thickness is approximately 380 nm.
   Bake at 150 °C on hot-plate for 90 s.

10. **EBL 7: Top gate metal**
    A 200 nm wide line will require approximately 150 µC/cm^2, using the EBL settings described here. This will primarily expose the top resist layer.

11. **Development and surface cleaning**
    90 s in 1:3 methyl isobutyl ketone and iso-2-propanol.
    30 s in iso-2-propanol.

12. **Metallization 4: Top gate metal**
    18 s at 5 mbar O_2 pressure in oxygen plasma etcher.
    Thermal evaporation of 50/50/1200 Å Ti/Pd/Au, using rotating sample. Centralization of the sample relative the metal source is important to avoid self-shadowing.
    30 min in acetone at 60 °C on hot-plate.
    1 min in iso-2-propanol.
    20 s at 5 mbar O_2 pressure in oxygen plasma etcher.

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Papers

Paper I

Paper I

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "InGaAs Tri-gate MOSFETs With Record On-current," *2016 IEEE Int. Electron Devices Meeting (IEDM)*, pp. 3.2.1–3.2.4, Dec. 2016.

InGaAs Tri-gate MOSFETs with Record On-Current

Cezar B. Zota, Fredrik Lindelow, Lars-Erik Wernersson and Erik Lind
Department of Electrical and Information Technology, Lund University, Lund, Sweden
E-mail: cezar.zota@eit.lth.se. Phone: +46462228062

***Abstract*—**We demonstrate InGaAs tri-gate MOSFETs with an on-current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, enabled by an inverse subthreshold slope of SS = 66 mV/decade and transconductance of g_m = 3 mS/μm, a Q-factor of 45. This is the highest reported I_{ON} for both Si-based and III-V MOSFETs. These results continue to push III-V MOSFET experimental performance towards its theoretical limit. We find an improvement in SS from 81 to 75 mV/dec. as the effective oxide thickness (EOT) is scaled down from 1.4 to 1 nm, as well as improvements in SS, g_d and DIBL from reducing the nanowire width. We also find that electron mobility remains constant as the width is scaled to 18 nm.

I. Introduction

An important path for reducing the power density in CMOS technology has been to lower the supply voltage V_{DD}. To maintain sufficient drive current, innovations are required, such as strained channels, novel channel materials and 3D device architectures [1]-[14]. For this purpose, high indium $In_xGa_{1-x}As$ is an attractive channel material due to its excellent electron transport properties, i.e. high electron mobility μ_e and long mean free path λ [6]. While the relatively low DOS of indium-rich $In_xGa_{1-x}As$ is predicted to limit I_{DS} in highly scaled devices, compared to competing technologies such as Si and Ge, this may be offset by the gain from the long λ and high μ_e of $In_xGa_{1-x}As$ [15]. Since this technology likely will be implemented in a 3D channel architecture, such as FinFETs or NWFETs, a further question concerns the dependence of λ on the channel dimensions, i.e. the influence of surface roughness on device performance.

In this work, we demonstrate tri-gate MOSFETs utilizing an $In_{0.85}Ga_{0.15}As$ nanowire (NW) as the channel. By gate oxide scaling, improvements of the surface passivation process and optimization of device dimensions, we achieve a drive current of I_{ON} = 650 μA/μm at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm. This is a record value for both III-V and Si MOSFETs. We also show that, as the NW width, W_{NW}, is scaled down, electrostatic properties significantly improve, while g_m and λ do not degrade. These results continue to push the limits, as well as explore the potential, of III-V FETs.

II. Device Fabrication

The process flow and schematic images of the device are shown in Fig. 1(a)-(f). The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask, as described elsewhere [4]. Each device consists of a single NW. The composition of the NW is $In_{0.85}Ga_{0.15}As$, as determined by optical characterization [15]. Fig. 1(g) shows an SEM image of an NW with W_{NW} = 90 nm, with the {110} sidewall facets denoted [15]. The inset of Fig. 1(h) shows a schematic figure of the NW cross-section. 30 nm highly doped $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) is subsequently grown by MOCVD as the contact layer, utilizing HSQ as a dummy gate [Fig. 1(h)]. After mesa isolation, the InP in the channel is etched by HCl (10%) in order to form a ~30 nm tall plateau, with the purpose of improving the gate coverage along the bottom of the sides of the NW. 4 cycles of surface oxidation by ozone and diluted HCl etching (digital etching) are performed to reduce the dimensions of the NW. The final height of the NW is H_{NW} = 8 nm, as determined from AFM. Subsequently, Ti/Pd/Au contact metal is evaporated and patterned by lift-off. Surface passivation, by ozone cleaning and $(NH4)_2S$ (10%) for 20 min, is followed by deposition of Al_2O_3/HfO_2 gate oxide (5/35 cycles and EOT ≈ 1 nm, unless otherwise stated). A 12 hour post-deposition anneal step at 100 °C in N_2 atmosphere is performed in-situ. Thermal evaporation and patterning by lift-off of 30/10/150 nm Ni/Pd/Au as the gate metal complete the process [Fig. 1(i)].

III. Results

Fig. 2 shows transfer characteristics of a tri-gate MOSFET with L_G = 75 nm and W_{NW} = 25 nm. All normalization is done to the total gated NW periphery, i.e. the three sides of the tri-gate. Peak transconductance is $g_m \approx 3.0$ mS/μm at V_{DS} = 0.5 V. Subthreshold characteristics of the same device are shown in Fig 3. At V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm, I_{ON} = 650 μA/μm. The gate current is I_G < 1 nA/μm. Minimum inverse subthreshold slope SS reaches 66 mV/decade (Fig. 4) at V_{DS} = 0.5 V, and 61 mV/decade at V_{DS} = 0.05 V. The drain-induced barrier-lowering (DIBL) is 65 mV/V, measured at I_{DS} = 1 μA/μm. The on-resistance of this device is R_{ON} = 175 Ω·μm at V_{GS} = 1 V. Output characteristics for W_{NW} = 90 and W_{NW} = 25 nm devices with L_G = 75 nm are shown in Fig. 5 and 6, respectively. The output conductance of these devices is g_d = 0.45 and 0.25 mS/μm (voltage gain is 5.5 and 10) at $V_{GS} - V_T = V_{DS}$ = 0.5 V.

Minimum SS versus L_G is shown for W_{NW} = 25 nm and W_{NW} = 90 nm devices at V_{DS} = 0.05 and 0.5 V (Fig. 7). The reduced W_{NW} offers improved resilience against short channel effects (SCEs), but at L_G = 25 nm, SS is degraded (110 mV/decade) even at W_{NW} = 25 nm. Minimum SS versus W_{NW} is shown in Fig. 8 for L_G = 75 nm devices at V_{DS} = 0.5 V. Average minimum SS improves from approximately 95 mV/dec. for W_{NW} > 90 nm to SS < 70 mV/dec. for W_{NW} < 30 nm due to enhanced electrostatic control. The lowest SS of a device at this bias is 64 mV/dec. The theoretical values

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indicate *SS* obtained from a solution of Laplace's equation modeling the full 3D structure of the nanowire using COMSOL. To improve performance at short L_G, W_{NW} must be further reduced. Scaling of H_{NW} will improve *SS* but reduce the aspect ratio (AR), which is undesirable. Moreover, the implementation of a wider band gap back-barrier, such as InAlAs or a BOX layer, is also expected to improve resilience to SCEs. Fig. 9 shows median (crosses) and mean (squares) minimum *SS* for four samples with L_G = 75 nm and W_{NW} = 25-30 nm at both V_{DS} = 0.05 and 0.5 V (~40 devices each). Sample D has 5/50 cycles Al_2O_3/HfO_2. Sample C has 5/45 cycles Al_2O_3/HfO_2. Sample B and A have 5/35 cycles Al_2O_3/HfO_2. In addition, samples D, C and B where passivated with $(NH_4)_2S$ (10%) produced by Merck, while sample A was passivated with $(NH_4)_2S$ (10%) produced by Sigma-Aldrich. Fig. 10 shows mean minimum *SS* of samples D to B versus EOT (1 cycle = 1.1 Å, κ = 18 and 9 for HfO_2 and Al_2O_3). These results indicate an improvement both from oxide scaling (average *SS* improves from 81 to 75 mV/dec. for EOT from ~1.4 nm to ~1 nm), and from optimization of the surface passivation parameters (mean *SS* improves from 75 to 70 mV/dec. for sample B to A). The trend indicates that *SS* may be further improved by scaling of the EOT. We do not observe a clear trend of g_m versus EOT.

Fig. 11 shows g_d versus W_{NW} at V_{DS} = 0.5 V and $V_{GS} - V_T$ = 0.5 V for L_G = 75 nm devices. Average g_d is reduced from 0.5 mS/µm at W_{NW} = 90 nm to ~0.2 mS/µm at W_{NW} = 25 nm. The DIBL measured at 1 µA/µm is shown in Fig. 12. It is similarly reduced from 170 mV/V at W_{NW} = 90 nm, to 38 mV/V at W_{NW} = 25 nm. The threshold voltage (V_T) defined at I_{DS} = 1 µA/µm increases in narrow NWs (Fig. 13). The trend approximately follows calculated values from an effective mass quantum wire model, indicating that the V_T increase is due to quantum confinement.

Fig. 14 shows g_m versus W_{NW}. The highest g_m observed in these devices is ~3.3 mS/µm (SS_{sat} = 90 mV/dec.) at V_{DS} = 0.5 V and L_G = 50 nm. g_m increases as W_{NW} is scaled down to approximately 35 nm from planar architecture (W_{NW} = 1 µm). This may be explained by that narrow NWs are more Indium-rich, due to interactions with the HSQ mask during MOCVD growth, which may improve mobility as well as change the D_{it} distribution [15]. This shows that the improvement of g_d with W_{NW}, is in fact due to improved electrostatics. The inset of Fig. 15 shows average values of g_m versus L_G for W_{NW} = 25 nm. Dashed traces show an analytical quasi-ballistic model with λ = 140 nm fitted to the measured data.

I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm is shown in Fig. 15 versus both W_{NW} and L_G (inset). I_{ON} increases from 200 to 650 µA/µm as W_{NW} goes from 1 um (planar) to 25 nm, due to the simultaneous improvements of *SS* (100 to 66 mV/dec.) and g_m (1.1 to 3 mS/µm). I_{ON} peaks at L_G = 75 nm, which is explained by the degraded *SS* (Fig. 7) and that g_m only improves slightly (Fig. 14) for shorter L_G.

These devices exhibit quantized conductance at 10 K due to subband splitting in a 1D channel (inset of Fig. 16). From the conductance steps, the transmission is obtained. The device in Fig. 3 shows a transmission of T = 0.67, which indicates quasi-ballistic transport. Fig. 16 shows electron mobility μ_e and λ for NWs with W_{NW} = 18 – 32 nm calculated from quantized conductance. To obtain μ_e, we use the Einstein relation and a correction factor of 1.6 to account for degeneracy [15]. We note that this method is not strongly influenced by D_{it}. No dependency versus W_{NW} is observed, which correlates with g_m versus W_{NW} with W_{NW} < 35 nm, explained by small surface scattering. Since g_m is temperature-independent, the same is true for μ_e.

A benchmark of the I_{ON} (at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm) for state-of-the-art III-V planar and non-planar MOSFETs is shown in Fig. 17. The value of 650 µA/µm presented in this work is the record value of both categories. The same is true for the quality factor Q = g_m/SS, which is 45 in this work (Fig. 18). Fig. 19 compares I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/µm for various technologies. $I_{DS,surface}$ is I_{ON} normalized to the gated channel periphery, while $I_{DS,chip}$ is normalized to the chip surface width including the specified pitch size. $I_{ON,chip}$ in our devices is lower than that of 14 nm FinFET (570 compared to 650 µA/µm for a pitch of 42 nm), which demonstrates the importance of high AR in 3D channels, but we observe a two-fold increase in $I_{ON,surface}$ over 14 nm FinFET technology, which is due primarily to the high μ_e of $In_xGa_{1-x}As$ [16].

IV. Conclusion

We have demonstrated $In_xGa_{1-x}As$ tri-gate MOSFETs with a record on-current of 650 µA/µm at V_{DD} = 0.5 V and I_{ON} = 100 nA/µm, *SS* = 66 mV/decade and g_m = 3.0 mS/µm. From data versus NW width, we observed improvements in *SS*, DIBL and g_d for scaled down NWs. Furthermore, we observed improvements both from oxide scaling the surface passivation process. From low-temperature measurements we obtain μ_e and λ, which remain high, 2750 cm^2/Vs and 150 nm, respectively, even in scaled NWs.

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V. References

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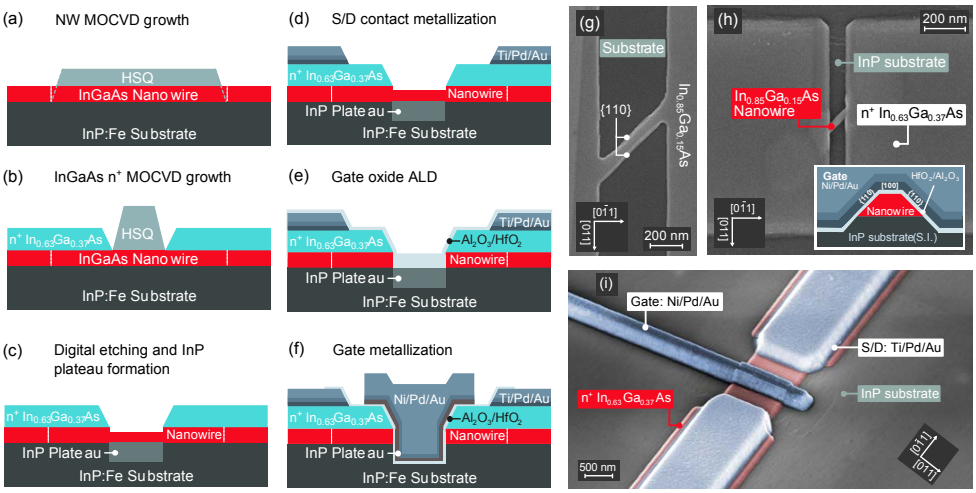

Fig. 1: Schematic figures SEM images of the device fabrication process. (a) NW formation utilizes selective area MOCVD growth with an EBL-defined HSQ hard mask. (b) Contacts are defined using an HSQ dummy gate and MOCVD regrowth of n^+ $In_{0.63}Ga_{0.37}As$. (c) NW is scaled down using "digital etching". (d) S/D metal is deposited by evaporation and lift-off. (e) A bilayer of Al_2O_3/HfO_2 is used as the gate oxide. (f) Ni/Pd/Au is evaporated as the gate metal. (g) SEM image of a 90 nm wide NW with the {110} side facets denoted. (h) The device after contact regrowth. Inset shows a schematic cross-section of the NW in the finished device. (i) False-color SEM image of the finished device. The NW is located at the center of the 1 µm wide mesa.

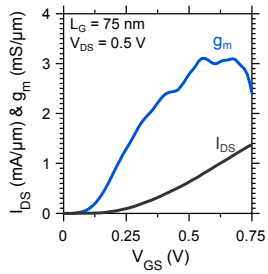

Fig. 2. Transfer characteristics for a device with W_{NW} = 25 nm.

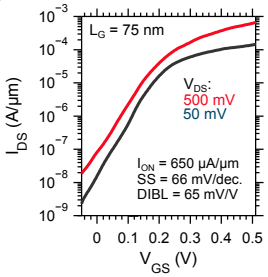

Fig. 3: Subthreshold characteristics for the same device as in Fig. 2.

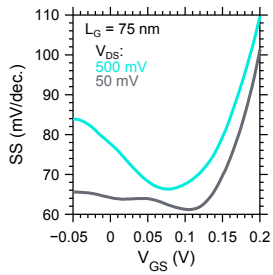

Fig. 4: Subthreshold slope versus V_{GS} for the same device as in Fig. 2.

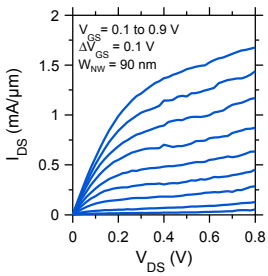

Fig. 5: Output characteristics for a device with L_G = 75 nm and W_{NW} = 90 nm.

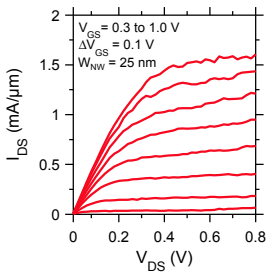

Fig. 6: Output characteristics for a device with L_G = 75 nm and W_{NW} = 25 nm.

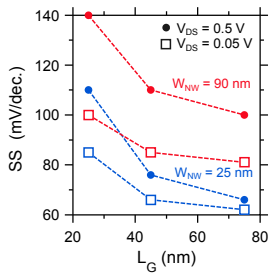

Fig. 7: Subthreshold slope for devices with different W_{NW} and L_G.

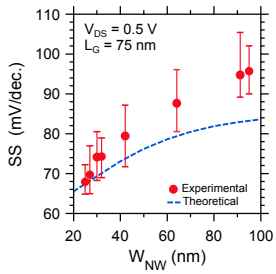

Fig. 8: Subthreshold slope versus W_{NW} at V_{DS} = 0.5 V and L_G = 75 nm.

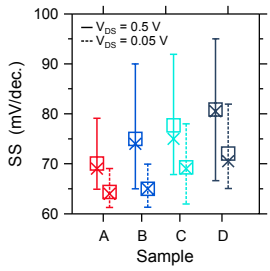

Fig. 9: Mean (squares) and median (crosses) *SS* for different samples.

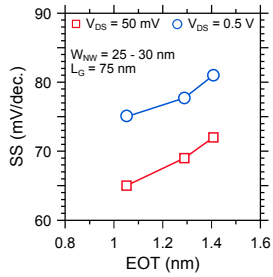

Fig. 10: Average subthreshold slope (each point is ~40 devices) versus EOT.

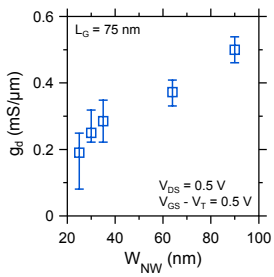

Fig. 11: Output conductance versus W_{NW}, measured at $V_{DS} = V_{GS} - V_T = 0.5$ V.

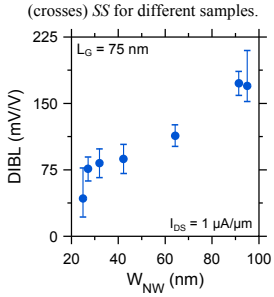

Fig. 12: DIBL versus W_{NW} measured at I_{DS} = 1 μA/μm.

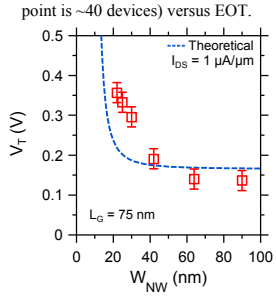

Fig. 13: Threshold voltage versus W_{NW}. Dashed traces show a QW model.

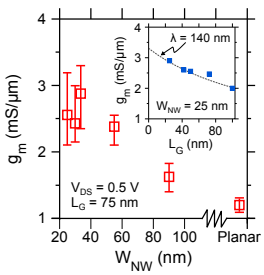

Fig. 14: Peak g_m versus W_{NW} and (inset) L_G, all measured at V_{DS} = 0.5 V.

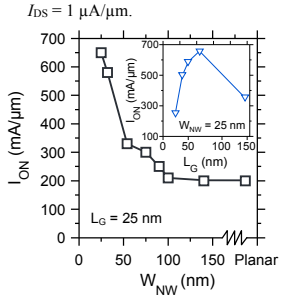

Fig. 15: I_{ON} versus W_{NW} and L_G at I_{OFF} = 100 nA/μm.

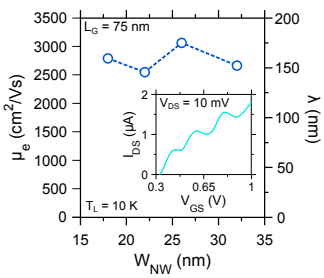

Fig. 16: μ_e and λ, measured from quantized current (inset), versus W_{NW}.

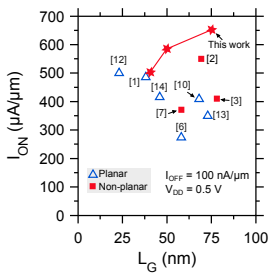

Fig. 17: Benchmark of I_{ON} at V_{DD} = 0.5 V and I_{OFF} = 100 nA/μm.

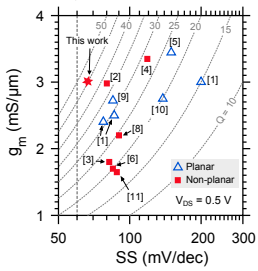

Fig. 18: Benchmark of the quality factor g_m/SS at V_{DS} = 0.5 V.

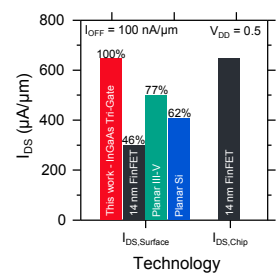

Fig. 19: Benchmark of various technologies.

Paper II

Paper II

C. B. Zota, L.-E. Wernersson and E. Lind, "High-Performance Lateral Nanowire InGaAs MOSFETs With Improved On-Current," *IEEE Electron Device Letters*, vol. 37, no. 10, pp. 1264–1267, Oct. 2016.

High-Performance Lateral Nanowire InGaAs MOSFETs With Improved On-Current

Cezar B. Zota, Lars-Erik Wernersson, and Erik Lind, *Member, IEEE*

***Abstract*— We report on $In_{0.85}Ga_{0.15}As$ MOSFETs utilizing selectively grown lateral nanowires as the channel. These devices exhibit ON-current of $I_{ON} = 565\ \mu A/\mu m$ at $I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V, which is higher than all other reported values for III–V FETs. This is enabled by a transconductance of 2.9 mS/μm and a minimum SS_{sat} of 77 mV/decade. A ballistic top-of-the-barrier model is used to model these devices and to predict their ultimate performance, which is approximately twice that of the fabricated devices.**

***Index Terms*— MOSFET, III-V, InGaAs, nanowire.**

I. Introduction

INDIUM-RICH III-Vs have been considered as a replacement for silicon as the channel in CMOS technology [1]. This is due to their excellent electron transport properties, such as high mobility, which enables increased transconductance g_m at a given L_G and may allow a reduction of the supply voltage V_{DD} to 0.5 V. For instance, there have recently been several reports on $In_xGa_{1-x}As$ MOSFETs with g_m of above 3 mS/μm [2], [3]. However, to achieve high I_{ON} at a specified I_{OFF} and V_{DD}= 0.5 V, which is a primary metric for CMOS applications, the subthreshold slope must be near the thermal limit of 60 mV/decade. This is a challenge in III-V technology due to e.g. the high-k oxide interface quality. Moreover, the narrow band gap of $In_xGa_{1-x}As$ causes, for instance, band-to-band-tunneling in the off-state which makes reaching lower I_{OFF} such as 1 and 10 nA/μm (low-power and general purpose limits, respectively) difficult. For this reason, 3D channel architectures, such as various implementations of FinFETs and Tri-gate devices, are promising to improve electrostatic integrity at scaled down gate-lengths [4].

In this work, we report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs with a tri-gate architecture and a record I_{ON} of 565 μA/μm at $I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V, together with a combination of $g_m = 2.9$ mS/μm and minimum SS of 77 mV/decade. Compared to our previous work, we have here optimized the nanowire dimensions, as well as examined the influence of gate length scaling [5]. We also explore the ultimate potential of these devices by comparing with a modeled fully ballistic device.

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The authors are with the Department of Electrical and Information Technology, Lund University, 221 00 Lund, Sweden (e-mail: cezar.zota@eit.lth.se).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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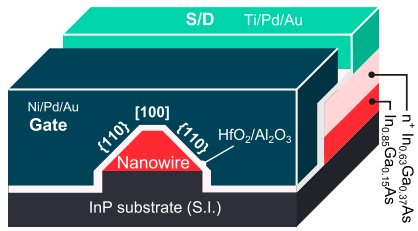

Fig. 1. Schematic figure of the fabricated device. The crystal facet are deduced from facet angels and the NW orientation.

II. Device Fabrication

Lateral $In_{0.85}Ga_{0.15}As$ nanowires (NWs) are formed on semi-insulating InP:Fe (100) by selective area growth using hydrogen silsequioxane (HSQ) as a hard mask, as described elsewhere [6]. The composition of the NWs is determined by optical characterization [7]. The direction of the NW is ⟨010⟩. The main focus of this work is on devices consisting of a single NW with width, W_{NW}, and height of 28 and 8 nm, respectively, and with gate length, L_G, of 75 nm. To explore the scaling properties, devices with $L_G = 50 - 150$ nm, and $W_{NW} = 28 - 140$ nm are also fabricated. A 30 nm highly doped $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) raised contact layer is regrown using an HSQ dummy gate hard mask. The direction of the dummy gate is ⟨110⟩. Subsequently, the InP in the channel is etched down by HCl solution. This is to ensure proper gating of the lower edge of the nanowire. The dimensions of the nanowire are reduced by 4 cycles of Ozone oxidation and diluted HCl oxide etch. 50 nm Ti/Pd/Au source/drain metal is deposited by thermal evaporation. Prior to ALD deposition of Al_2O_3/HfO_2 (10/40Å, EOT ≈ 1.5 nm) at 300/100°C, sulphur passivation in $(NH_4)_2S$ (10%) is performed for 20 min. Following, an in-situ post-deposition annealing step is performed at 100°C for 12 hours in N_2 atmosphere, which is found to improve the subthreshold slope. Finally, 150 nm Ni/Pd/Au is patterned and thermally evaporated as the gate-metal and gate pad using lift-off. Since the gate was defined in the contact regrowth step, gate metallization is self-aligned. Fig. 1 shows a schematic image of the fabricated device, and the facets of the NW, which have 45° facet angles, as we have

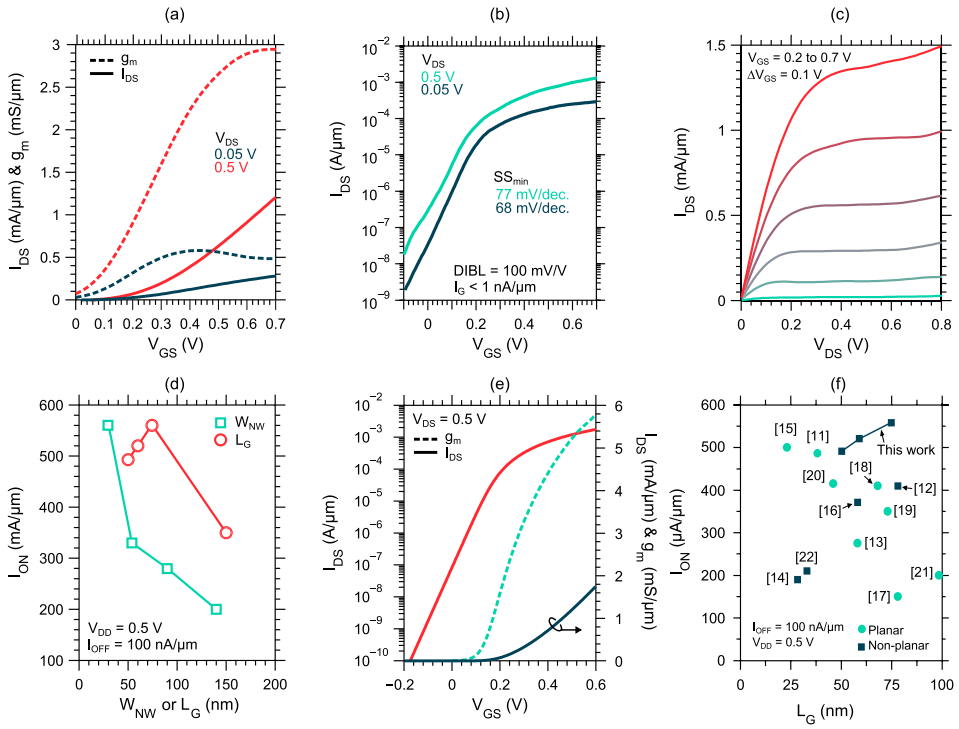

Fig. 2. (a) Transfer, (b) subthreshold and (c) output characteristics of the same L_G = 75 nm device. (d) I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 versus W_{NW} (squares) and L_G (circles). Squares have a fixed L_G = 75, and circles have a fixed W_{NW} = 28 nm. (e) Transfer and subthreshold performance of a fully ballistic ideal device using a top-of-the-barrier model. (f) A benchmark of I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V for state-of-the-art III-V planar and non-planar MOSFETs.

previously shown [7]. The distance between S/D contact metal and the gate is 700 nm. The width of the contacts is 1 μm.

III. Results

Fig. 2(a)-(b) show transfer and subthreshold characteristics for a device with L_G = 75 nm. The data is normalized to the gated perimeter according to the shape in Fig. 1. The peak transconductance is g_m = 2.9 mS/μm at V_{DS} = 0.5 V. Minimum inverse subthreshold slope (SS_{sat}) is 77 mV/decade, and the drain-induced barrier lowering (DIBL), measured at I_{DS} = 1 μA/μm, is 100 mV/V. The gate-leakage current I_G is below 1 nA/μm. At V_{DS} = 50 mV, minimum SS is 68 mV/decade. The on-current, measured as I_{DS} at a fixed voltage swing of 0.5 V from I_{OFF} = 100 nA/μm and V_{DS} = 0.5 V, is I_{ON} = 565 μA/μm. The output characteristics of an L_G = 75 nm device is shown in Fig. 2(c). The on-resistance is R_{ON} = 180 $\Omega\mu$ m, and the contact resistance is approximately R_C = 20 $\Omega\mu$ m, as determined from transmission line measurements.

Fig. 2(d) shows I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 versus both the width of the nanowires, W_{NW} (with L_G = 75 nm for all devices) and L_G (with W_{NW} = 28 nm for all devices). I_{ON} significantly improves as W_{NW} is scaled down from 140 nm to 28 nm, which is primarily due to an improvement of SS, from > 100 mV/decade to approximately 80 mV/decade, as an effect of improved electrostatic control. The optimal I_{ON} is found at L_G = 75 nm for these devices. At shorter L_G, short-channel effects begin to degrade performance through a degradation of the subthreshold slope. This can be offset by, e.g. further scaling of the NW. The peak transconductance is weakly increasing with the reduction of gate length.

The ideal device performance was calculated using a fully ballistic top-of-the-barrier model and is shown in Fig. 2(e). The gate length is assumed long enough to suppress any short channel effects. For the evaluation of device density of states, a 2-band non parabolic quantum wire model was used [8]. Quantum well band bending was approximately taken into account through a first order perturbation scheme.

The nanowire was modeled as a 28 × 8 nm rectangular wire (which is more voluminous than the fabricated NWs, due to their 45° facet angles), with a bulk effective

TABLE I
COMPARISON OF THEORETICAL PERFORMANCE WITH RECORD FABRICATED III-V DEVICES

Metric	Experimental	Theoretical
I_{ON} (I_{OFF} = 100 nA/μm)	565 μA/μm	1200 μA/μm
I_{ON} (I_{OFF} = 10 nA/μm)	360 μA/μm [5]	930 μA/μm
I_{ON} (I_{OFF} = 1 nA/μm)	---	670 μA/μm
$g_{m,peak}$ (V_{DS} = 0.5 V)	2.9 mS/μm	6 mS/μm
SS_{min} (V_{DS} = 0.05 V)	68 mV/dec.	60 mV/dec.
SS_{min} (V_{DS} = 0.5V)	77 mV/dec.	60 mV/dec.

mass $m^* = 0.027m_0$ and a bulk bandgap of $E_g = 0.44$ eV, roughly corresponding to $In_{0.9}Ga_{0.1}As$. The oxide capacitance was calculated from the tri-gate configuration, with $t_{ox} = 4.7$ nm and $\varepsilon_{r,ox} = 15.9$ [9]. Extrinsic resistances are 0 Ω.

Ideal nanowire device performance is compared to that of fabricated III-V MOSFETs with record I_{ON} in table 1. Currently, $I_{OFF} = 1$ nA/μm has not been demonstrated experimentally in non-planar InGaAs MOSFETs. The g_m and SS values are those reported in this work. Ideal g_m and I_{ON} (at 100 nA/μm) are 6 mS/μm and 1200 μA/μm, respectively. The difference of about a factor 2 compared to our devices is explained mainly by quasi-ballistic transport, e. g. a transmission less than 1, as well as non-ideal electrostatics partly due to traps (D_{it}), in the fabricated devices [10]. We have previously shown that the transmission, T, in devices similar to those reported here is approximately 70% [7]. Therefore, to improve device performance, device dimensions, W_{NW} and L_G must be optimized, EOT must be reduced and the oxide interface quality improved. T is inversely proportional to L_G, and W_{NW} also influences T since smaller W_{NW} typically correlates to lower mobility and mean free path.

Finally, we benchmark our results with state-of-the art III-V planar and non-planar MOSFETs [Fig. 1(f)] [11]–[22]. The I_{ON} (at 100 nA/μm) of 565 μA/μm reported in this work is the record value for both planar and non-planar devices.

IV. CONCLUSION

We have reported $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs with record I_{ON} at 100 nA/μm. This was enabled by a transconductance of 2.9 mS/ μm and minimum SS of 77 mV/decade. We also compared record III-V MOSFET performance to an ideal fully ballistic device using a top-of-the-barrier model. Fabricated device performance was found to have reached approximately half of that of the ideal device.

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Paper III

Paper III

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "InGaAs Nanowire MOSFETs With I_{ON} = 555 uA/um at I_{OFF} = 100 nA/um and V_{DD} = 0.5," *Symposium on Very Large Scale Integrated Circuits and Technology (VLSI)*, Jun. 2016.

InGaAs Nanowire MOSFETs with I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V

Cezar B. Zota, Fredrik Lindelöw, Lars-Erik Wernersson and Erik Lind
Department of Electrical and Information Technology, Lund University, Box 118, Lund, Sweden
E-mail: cezar.zota@eit.lth.se. Phone: +46462228062

Abstract

We report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs (NWFETs) with record performance in several key VLSI metrics. These devices exhibit I_{ON} = 555 µA/µm (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), I_{ON} = 365 µA/µm (at I_{OFF} = 10 nA/µm and V_{DD} = 0.5 V) and a quality factor Q ≡ g_m/SS of 40, all of which are the highest reported for a III-V as well as silicon transistor. Furthermore, a highly scalable, self-aligned gate-last fabrication process is utilized, with a single nanowire as the channel. The devices use a 45° angle between the nanowire and the contacts, which allows for up to a 1.4 times longer gate length at a given pitch.

Introduction

$In_xGa_{x-1}As$ MOSFETs are expected to deliver high on-currents at a reduced V_{DD} of 0.5 V, making them suitable for VLSI applications [1]-[17]. This is due to their high mobility, which enables increased transconductance g_m at a given L_G. For instance, we have recently demonstrated $In_{0.85}Ga_{0.15}As$ NWFETs with g_m = 3.3 mS/µm, surpassing that of all other III-V and silicon transistors, including HEMTs [4]. However, to achieve high I_{ON} at a specified I_{OFF} and V_{DD} = 0.5 V comparable to state-of-the-art silicon technology, the subthreshold slope must be near 60 mV/decade. This is challenging in III-V technology due to the oxide interface quality and narrow band gap, causing e.g. band-to-band-tunneling in the off-state. Recently, planar InAs MOSFETs with I_{ON} matching or surpassing that of silicon technology were reported [12]. In this work, we report on NWFETs with a new record of I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V.

Device Fabrication

Fig. 1 shows a schematic of the fabricated device, and the process flow [17]. The nanowires are formed by selective area growth, using hydrogen silsesquioxane (HSQ) as the MOCVD growth mask. The composition of the nanowire layer is $In_{0.63}Ga_{0.37}As$, while the nanowire is $In_{0.85}Ga_{0.15}As$, as determined by optical characterization. Fig. 2(a)-(c) demonstrate the scalability of the selective growth process. A high-density nanowire-cluster with nanowire spacing of <10 nm is shown in fig. 2c. In this work, we characterize single-nanowire devices. The highly doped $In_{0.63}Ga_{0.37}As$ (N_D = 5 × 10^{19} cm^{-3}) contact layer is formed from a subsequent MOCVD growth step using HSQ as a dummy gate [Fig. 2(d)]. A 45° angle between the nanowire and the contacts is chosen in order to obtain optimal crystal facets. At a given pitch, this will also improve electrostatic control by allowing a longer gate length. After mesa isolation, Ti/Pd/Au is patterned and evaporated as the contact metal. The InP in the channel region is etched by HCl (1:1), in order for the metal to properly cover the sides of the nanowire. Several cycles of surface oxidation by ozone and diluted HCl etching is performed in order to reduce the dimensions of the nanowire. Surface passivation, by $(NH4)_2S$ (1:1) for 20 min, is followed by deposition of Al_2O_3/HfO_2 (EOT ≈ 1.5 nm) by ALD at 300/100ºC. Subsequently, an in-situ 12 hour post-deposition annealing step at 100°C in N_2 atmosphere is performed. Ni/Pd/Au gate metal patterning and evaporation completes the process.

Results

Fig. 3(a)-(c) show subthreshold, transfer and output characteristics of an L_G = 70 nm NWFET with nanowire width and height W_{NW}/H_{NW} = 25/7 nm. The peak transconductance is $g_{m,peak}$ = 2.85 mS/µm at V_{DS} = 0.5 V. The subthreshold characteristics for the same device are shown in Fig. 4. The subthreshold slope (SS) is 80 mV/decade at both V_{DS} = 0.5 V and 50 mV. The drain-induced barrier-lowering (DIBL) is 43 mV/V at I_{DS} = 1 µA/µm. The device exhibits I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, which is the highest reported value for a MOSFET. The quality factor Q ≡ g_m/SS is 35 for this device. The on-resistance is R_{ON} = 177 Ωµm. The specific contact resistivity is ρ_C = 7×10^{-8} Ωcm^{-2} and the sheet resistance of the n^+ $In_{0.63}Ga_{0.37}As$ contact layer is R_{Sh} = 70 Ω/□, both obtained from TLM measurements.

Fig. 4 shows transfer characteristics for another L_G = 70 nm device with $g_{m,peak}$ = 2.65 mS/µm at V_{DS} = 0.5 V. The average SS over one, two and three decades is 65, 69 and 73 mV/decade, respectively, all at V_{DS} = 0.5 V. This device shows I_{ON} = 535 µA/µm at I_{OFF} = 100 nA/µm and I_{ON} = 365 µA/µm at I_{OFF} = 10 nA/µm, V_{DD} = 0.5 V. This is the highest reported I_{ON} at I_{OFF} = 10 nA/µm. DIBL is 56 mV/V at I_{DS} = 1 µA/µm. The quality factor Q ≡ g_m/SS is 40 for this device, which is the highest reported Q-factor for a MOSFET. The difference in SS between these devices may in part be explained by the discrete nature of traps in the small channel area (2 × 10^{-3} µm^2).

The hysteresis (Fig. 5) is ΔV_T = 60 mV for V_{GS} = 0.2-1.0 V, indicating high-quality oxide and oxide interface. I_{OFF} versus I_{ON} for several devices with L_G = 70 nm and W_{NW}/H_{NW} = 25/7 nm is shown in Fig. 6, measured at a swing of V_{DD} = 0.5 V. Fig. 7 shows SS versus L_G. Error bars show the standard deviation. SS and DIBL versus nanowire width W_{NW} is shown in Fig. 8 (H_{NW} = 7 nm), with data points offset for clarity. Improved electrostatic control from use of smaller nanowires can clearly be observed. The trend indicates that SS can be further reduced by additionally scaling down W_{NW}. Fig. 9 and 10 show benchmarks of I_{ON} and Q for various planar and non-planar MOSFETs.

Conclusions

We have demonstrated highly scalable nanowire MOSFETs with record high performance in several key VLSI metrics. We have shown a device with g_m = 2.85 mS/µm, SS = 80 mV/decade and I_{ON} = 555 µA/µm at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V. We have also shown a device with g_m = 2.65 mS/µm and SS = 65 mV/decade, which gives a quality factor Q = 40.

Acknowledgements

This work was supported in part by the Swedish Research Council, in part by the Knut and Alice Wallenberg Foundation, in part by the Swedish Foundation for Strategic Research, and in part by the European Union H2020 program INSIGHT (Grant Agreement No. 688784).

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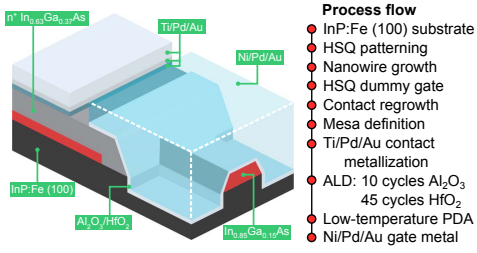

Fig. 1. Schematic of the final device, as well as the device fabrication process flow.

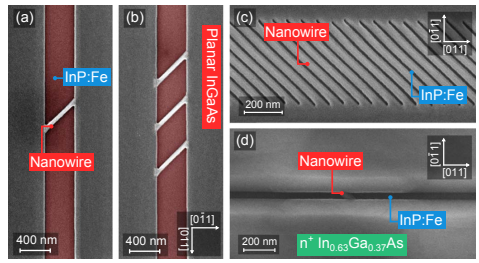

Fig. 2. (a-c) False-color SEM images showing the scalability of the NW fabrication process. (d) The device after contact regrowth.

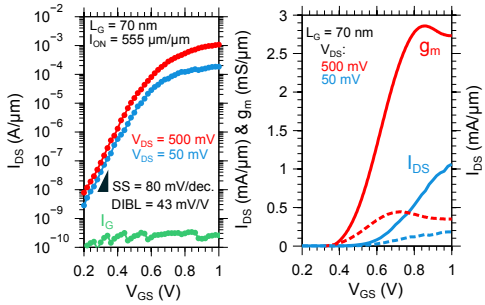

Fig. 3. (a) Subthreshold, (b) transfer and (c) output characteristics of the same L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device. I_{ON} = 555 μA/μm at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

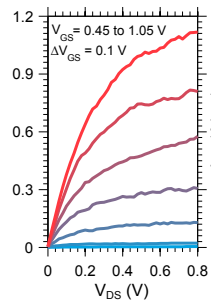

Fig. 4. I_{DS}-V_{GS} for an L_G = 70 nm, W_{NW}/H_{NW} = 25/7 nm device.

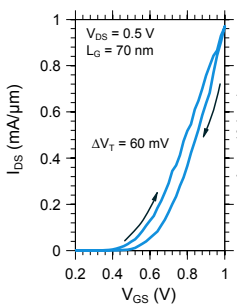

Fig. 5. Hysteresis measurement of an L_G = 70 nm device.

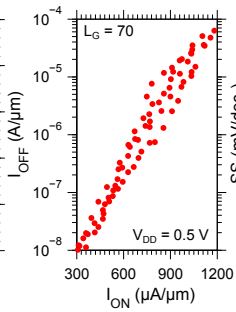

Fig. 6. I_{OFF} versus I_{OFF} for L_G = 70 nm devices.

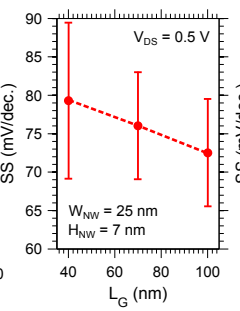

Fig. 7. SS versus L_G for W_{NW} = 25 nm devices.

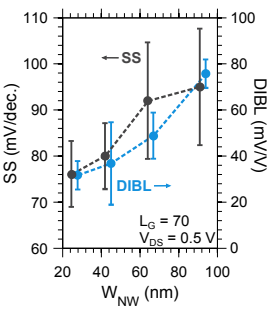

Fig. 8. SS and DIBL versus W_{NW} with L_G = 70 nm and H_{NW} = 7 nm.

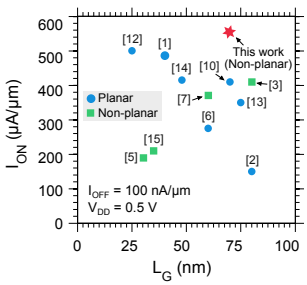

Fig. 9. Benchmark of I_{ON} at I_{OFF} = 100 nA/μm and V_{DD} = 0.5 V.

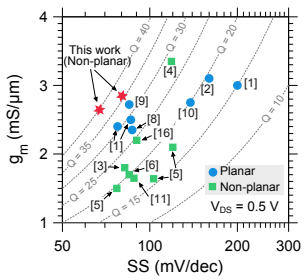

Fig. 10. Benchmark of Q = g_m/SS at V_{DS} = 0.5 V for various planar and non-planar III-V FETs.

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Paper IV

Paper IV

C. B. Zota, L.-E. Wernersson and E. Lind, "Single Suspended InGaAs Nanowire MOSFETs," *2015 IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2015.

Single Suspended InGaAs Nanowire MOSFETs

Cezar B. Zota, Lars-Erik Wernersson and Erik Lind
Department of Electrical and Information Technology, Lund University, Box 118, Lund, Sweden
E-mail: Cezar.Zota@eit.lth.se. Phone: +46 46 222 80 62

I. Abstract

We report on $In_{0.85}Ga_{0.15}As$ NWFETs utilizing a single suspended (above the substrate) selectively grown nanowire as the channel. These devices exhibit g_m = 3.3 mS/μm and subthreshold slope SS = 118 mV/dec, both at V_{DS} = 0.5 V and L_G = 60 nm. This is the highest reported value of g_m for all MOSFETs and HEMTs, as well as a strong combination of on and off performance, with Q = g_m/SS = 28, the highest for non-planar III-V MOSFETs.

II. Introduction

Indium-rich $In_{1-x}Ga_xAs$ nanowires are promising candidates as the channel in future CMOS technology for both high-performance and low-power applications. This is due to the high electron mobility and injection velocity offered by $In_{1-x}Ga_xAs$, as well as the strong electrostatic control enabled by multiple-gate architectures, such as FinFETs and nanowire MOSFETs (NWFETs) [1]–[5]. A key issue is the nanowire formation scheme. Since surface scattering is strongly nanowire diameter-dependent, high-quality nanowire surfaces are important in order to maintain high I_{DS} as the diameter is scaled down. Several nanowire formation methods have been reported. In particular, vapor-liquid-solid growth, utilizing a metal particle catalyst, as well as etched-out nanowires have been widely studied. Electron mobility for diameters less than 30 nm is typically 2000-5000 cm^2/Vs, more than an order of magnitude lower than bulk mobility [6]. However, in deeply scaled, i.e. ballistic or quasi-ballistic devices, the interpretation of mobility and its relation to I_{DS} is not straightforward. Rather, I_{DS} is proportional to the mean free path λ. In fact, $In_{1-x}Ga_xAs$ is promising also for its long λ, shown in nanowires to be approximately an order of magnitude longer than that of Si [6]. At a given L_G, this results in transport closer to the ballistic limit.

NWFETs are also of interest in high-frequency applications, where the MOS-structure allows for scaling beyond the capabilities of traditional HEMT technology, and strong electrostatics can improve high-frequency metrics such as the voltage gain (A_V) as well as f_t and f_{max}.

In this work, we demonstrate high-performance quasi-ballistic NWFETs utilizing a single selectively grown $In_{0.85}Ga_{0.15}As$ nanowire suspended above the substrate, as the channel. We also determine the mean free path, and electron mobility of the nanowires, utilizing both room-temperature and low-temperature methods.

III. Device Fabrication

Fig. 1(a) shows a schematic illustration of the nanowire formation process. The $In_{1-x}Ga_xAs$ composition of the nanowire is different from the nominal composition due to growth interactions with the HSQ mask. From optical characterizations, it is determined to be $In_{0.85}Ga_{0.15}As$.

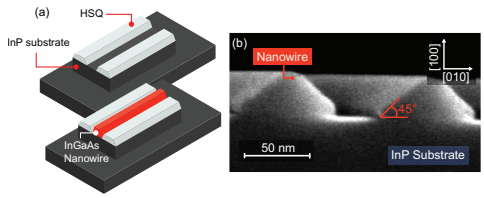

Fig. 1. (a) Schematic of the selective nanowire growth process. Areas of HSQ are patterned on semi-insulating InP:Fe. In the narrow space between HSQ areas, an $In_{0.85}Ga_{0.15}As$ nanowire is formed during MOCVD growth. (b) Cross-sectional SEM image of wider reference nanowires oriented along [001], which is the same direction as in the fabricated devices.

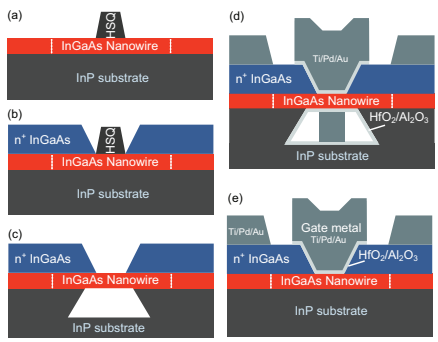

Fig. 2. (a) An HSQ dummy gate is patterned across the nanowire. (b) n^+ $In_{0.63}Ga_{0.37}As$ contacts are regrown by MOCVD. (c) The InP underneath the nanowire is etched by HCl solution. Due to anisotropic etch rates, there is only very little etching underneath the contacts. (d) Final device in the suspended and (e) on-substrate configuration.

Fig. 2(a)-(e) illustrates the device fabrication. An HSQ dummy-gate is patterned across the nanowire, which after MOCVD regrowth of n^+ $In_{0.63}Ga_{0.37}As$ ($N_D = 5{\cdot}10^{19}$ cm^{-3}) defines the gate-length L_G of the device. The HSQ is removed by buffered oxide etch [Fig. 3(b)]. The orientations of the nanowire and the dummy gate are chosen as shown in Fig. 3 in order to obtain optimal crystal facets. The nanowires are suspended by selective etching of the InP:Fe substrate by $HCl:H_2O$. We also fabricate devices which have not suspended nanowires (on-substrate). The dimensions of the nanowire are scaled down by several cycles of ozone

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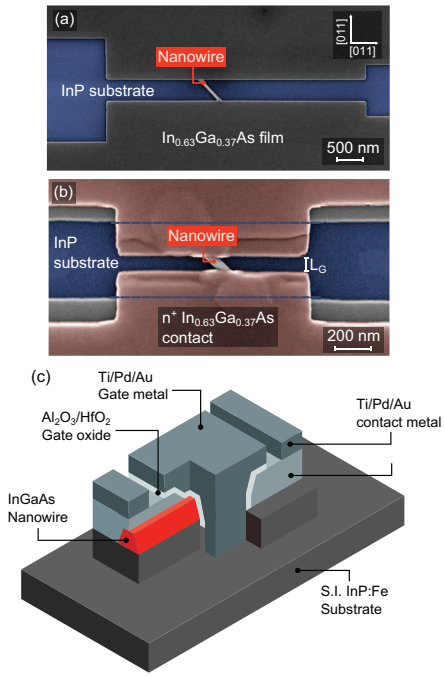

Fig. 3. (a) False-color SEM image of the device after nanowire regrowth [corresponding to Fig 1(a)]. The 45° tilt of the nanowire facilitates optimal directions for the subsequent InP etching, as well as optimal facets for the regrown contact layer. (b) False-color SEM image of the device after contact regrowth [corresponding to Fig. 2(c)]. (c) Schematic of the final device in the suspended configuration.

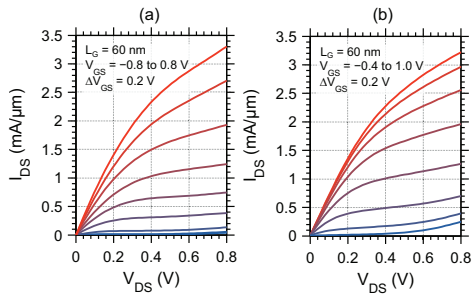

Fig. 4. Output characteristics of L_G = 60 nm NWFETs in the (a) suspended and (b) on-substrate configurations. Both configurations exhibit similar R_{ON} and peak g_m.

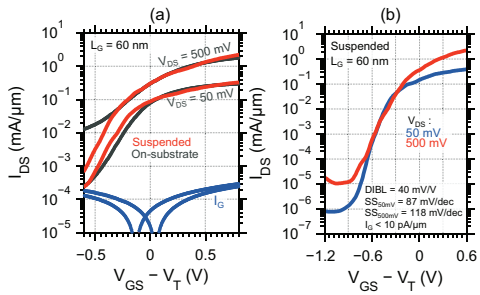

Fig. 5. (a) Subthreshold characteristics of L_G = 60 nm NWFETs in the (red) suspended and (gray) on-substrate configurations. (b) Subthreshold characteristics of suspended L_G = 60 nm NWFET with optimized gate and pad-to-pad leakage currents, which improves I_{off} and DIBL.

oxidation and diluted HCl etching. The final dimensions of the nanowire are W/H = 45/12 nm. Ti/Pd/Au source and drain metal contacts are deposited by lift-off.

After $(NH_4)_2S$ surface treatment, the gate oxide (10 cycles Al_2O_3 and 60 cycles HfO_2, EOT ≈ 1.8 nm) is deposited by ALD. The Ni/Pd/Au gate metal is subsequently deposited and patterned by lift-off, which finalizes the process. Fig. 3(c) shows a schematic of the final device.

IV. Results and Discussion

The measurement data is normalized to the gated circumference of the nanowire, which has the shape seen in Fig. 1(b), i.e. defined by [110] sidewalls at 45° angles. Fig. 4(a) and (b) show output characteristics of devices in suspended and on-substrate configurations, respectively. They exhibit similar peak g_m and on-current. Fig. 5(a) shows a comparison of subthreshold characteristics for the same devices. The threshold voltage V_T is defined from linear extrapolation at maximum g_m. On-substrate nanowires exhibit minimum SS = 316 mV/dec and DIBL = 440 mV/V, while suspended nanowires exhibit SS = 140 mV/dec and DIBL = 200 mV/V, all at V_{DS} = 0.5 V. This shows the detrimental effect of the relatively small 300 meV band offset between $In_{0.85}Ga_{0.15}As$ and the InP substrate. The reduction of DIBL is due to in part a reduction of the substrate leakage current, in part due to a reduced influence of the drain potential on the channel.

Fig. 5(b) shows subthreshold characteristics of an optimized (reduced gate and pad-to-pad leakages) suspended NWFET with L_G = 60 nm, which exhibits DIBL < 40 mV/V, minimum SS = 118 mV/dec at V_{DS} = 0.5 V and SS = 87 mV/dec at V_{DS} = 0.05 V. Transfer characteristics are shown in Fig. 6 for the same device as in Fig. 5(b). Devices with L_G = 60 nm exhibit I_{DS} = 2.9 mA/μm, corresponding to 160 μm/nanowire, at V_{DS} = 0.5 V and $V_{GS} - V_T$ = 1.0 V. The peak transconductance is g_m = 3.3 mS/μm at V_{DS} = 0.5 V, and Q = g_m/SS is 28. The g_m-peak is relatively wide, with g_m > 2.5 mS/μm over a range of ~1 V.

Peak transconductance versus L_G is shown in Fig. 7. In

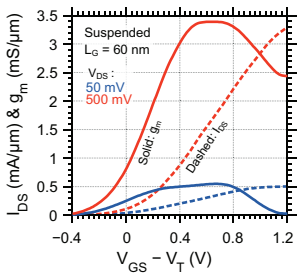

Fig. 6. Transfer characteristics of the same L_G = 60 nm suspended NWFET as in Fig. 4(b) at V_{DS} = 0.5 V.

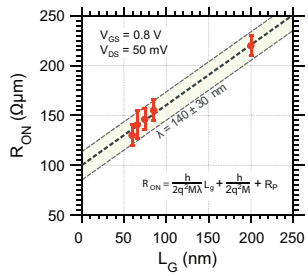

Fig. 8. R_{ON} versus L_G for suspended NWFETs. Dashed traces show a fit of R_{ON} from which λ is calculated.

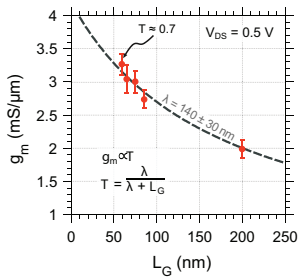

Fig. 7. Peak g_m versus L_G for suspended NWFETs at V_{DS} = 0.5 V. Dashed traces show a fit of the transmission T to the data.

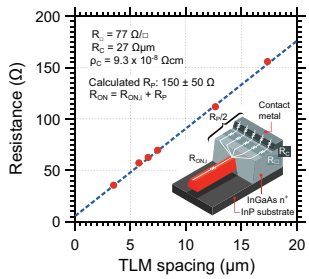

Fig. 9. Contact resistance R_C and sheet resistance $R_\square$ as determined from on-sample TLM measurements. Inset shows a schematic of the parasitic spreading access resistance R_P.

a ballistic device, g_m is proportional to the transmission $T = \lambda/(L_G + \lambda)$ [7]. Dashed traces show a fit of T with λ = 140 ± 30 nm to the measurement data, which gives the effective electron mobility $\mu_{eff} = q\lambda v_T/2k_BT_L$ = 7000 ± 1500 cm^2/Vs from the Einstein relation. μ_{eff} can alternatively be calculated from R_{ON} versus L_G shown in Fig. 8. In a ballistic FET, $R_{ON} = (G_0M)^{-1}(\lambda^{-1}L_G + 1) + R_P$, where $G_0 = 2e^2/h$ is the quantum conductance, M is the number of conducting sub-bands and R_P is the parasitic spreading access resistance. Fitting this equation to the measurement data and subtracting our calculated R_P, we again obtain λ_{eff} = 7000 ± 1500 cm^2/Vs. This is among the highest reported values for $In_{1-x}Ga_xAs$ nanowires of similar dimensions [6].

The on-resistance is R_{ON} = 130 Ωμm at L_G = 60 nm, which is 2450 Ω/nanowire. The contact resistance is R_C = 25 Ωμm, the sheet resistance of the n$^+$ $In_{0.63}Ga_{0.37}As$ contact layer is $R_\square$ = 70 Ω/□, both calculated from TLM measurements (Fig. 9). The total spreading access resistance R_P, depends on R_C, $R_\square$ and the geometry of the contacts, as shown in Fig. 9, and was calculated as R_P = 150 ± 50 Ω by COMSOL 3D simulation.

Fig. 10 compares g_d of suspended and on-substrate NWFETs. At low V_{GS}, the reduced DIBL causes a reduction of g_d by a factor two. In the high-V_{GS} regime, g_d converges, which may indicate non-linear access resistance. Fig. 10 also shows an improvement of the peak voltage gain $A_V = g_m/g_d$ from 5 to 12.5 for the suspended configuration while g_m still is > 2 mS/μm, which is mainly due to the reduced g_d. This value is larger than for reported high-performance HEMTs by a factor two [8]. Fig. 11 shows a benchmark of g_m and SS for various planar and non-planar III-V MOSFETs.

Due to the discrete 1D subband band structure of the nanowire, the conductance $G = I_{DS}/V_{DS}$ displays steps at low temperature, T_L = 10 K. Fig. 12 shows the conductance at various V_{DS} for an L_G = 60 nm suspended NWFET. The steps are visible mostly at low V_{DS}. The first three steps are at approximately $0.7G_0$, $1.4G_0$ and $2.1G_0$, which gives the transmission T = 0.7 at L_G = 60 nm. Since the transmission at L_G = 60 nm from g_m-L_G and R_{ON}-L_G in Fig. 7 and 8 is also approximately 0.7, this is a sign that the conductance steps are indeed due to quantized sub-bands, rather than defect states. Since we obtain similar transmission at 10 K and room-temperature, this indicates that transport is surface roughness, rather than phonon, scattering limited [6].

Utilizing a semi-classical compact model with 2-band non-parabolic band structure, self-consistent corrections and empirical short-channel modeling, we have calculated the device performance in the ballistic limit, using the same EOT and device dimensions as for the fabricated devices. The inset

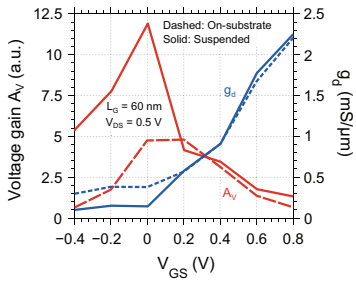

Fig. 10. Voltage gain A_V and output conductance gd versus V_{GS} for suspended (solid traces) and on-substrate (dashed traces) NWFETs at V_{DS} = 0.5 V and L_G = 60 nm.

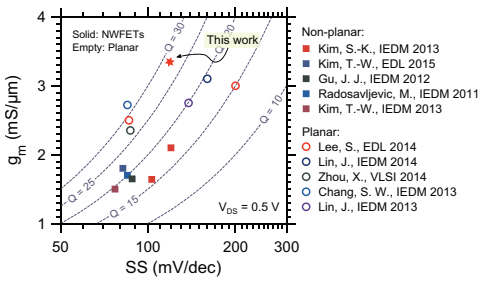

Fig. 11. Benchmark of $Q = g_m/SS$ at V_{DS} = 0.5 V for various planar and non-planar III-V MOSFETs. We compare with a suspended NWFET with L_G = 60 nm.

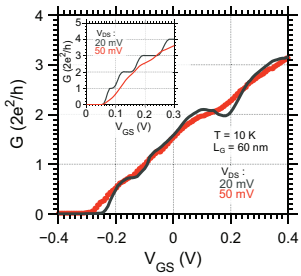

Fig. 12. Low-temperature conductance G = I_{DS}/V_{DS} for a suspended NWFET with L_G = 60 nm. Inset shows simulated conductance at 10 K for a fully ballistic device.

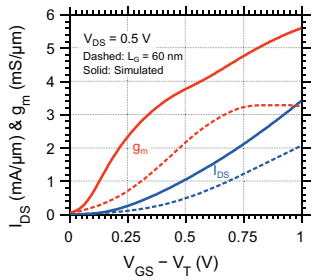

Fig. 13. Simulated transfer characteristics of a fully ballistic device. Dashed traces show a measured L_G = 60 nm NWFET.

of Fig. 12 shows low temperature conductance simulations, clearly showing the expected conductance quantization at low V_{DS}. Fig. 13 shows the calculated ballistic current and transconductance at V_{DS} = 0.5 V, indicating a peak g_m = 5.6 mS/μm. The deviations between the modeled and measured data can be explained through oxide traps and scattering.

V. Conclusion

In conclusion, we have demonstrated NWFETs with record-high g_m = 3.3 mS/μm, SS = 118 mV/dec at V_{DS} = 0.5 V and DIBL = 40 mV/V, enabled by a long mean- free path 140 ± 30 nm and high effective electron mobility λ_{eff} = 7000 ± 1500 cm^2/Vs as well as low parasitic resistances. This shows the potential of selectively regrown $In_{1-x}Ga_xAs$ nanowires for both high-frequency and digital applications.

VI. Acknowledgements

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Paper V

Paper V

C. B. Zota, L.-E. Wernersson and E. Lind, "$In_{0.53}Ga_{0.47}As$ Multiple-Gate Field-Effect Transistors With Selectively Regrown Channels," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 342–344, Mar. 2014.

$In_{0.53}Ga_{0.47}As$ Multiple-Gate Field-Effect Transistors With Selectively Regrown Channels

Cezar B. Zota, Lars-Erik Wernersson, and Erik Lind

***Abstract*— We report on $In_{0.53}Ga_{0.47}As$ n-channel multiple-gate field-effect transistors (MuGFETs or FinFETs) with a novel method of selectively regrown lateral (parallel to substrate) nanowires as channels. The device exhibits a minimum subthreshold slope of 85 mV/decade and drain-induced barrier lowering of 88 mV/V at $V_{DS} = 0.05$ V and $L_G = 200$ nm. At $V_{DS} = 0.5$ V, $g_{m,max} = 1.67$ mS/μm is achieved ($L_G = 32$ nm). The extrapolated cutoff frequency f_T of 210 GHz and the maximum oscillation frequency f_{max} of 250 GHz are the highest of any reported III–V multiple-gate MOSFET.**

***Index Terms*— FinFET, InGaAs, MOSFET, selective regrowth, MuGFET, III–V, trigate.**

I. Introduction

IN OVERCOMING the challenges facing Si CMOS technology, InGaAs metal-oxide semiconductor field-effect transistors (MOSFETs) are an attractive option due to their large carrier mobilities and injection velocity [1]–[3]. Their susceptibility to short-channel effects (SCE), owing to high permittivity and narrow band-gap, makes 3D conductive channels, i.e. multiple-gate structures, promising architectures. These device structures allow improved scalability through increased electrostatic control over the channel [4]. We demonstrate here a process of $In_{0.53}Ga_{0.47}As$ fin formation (selective area regrowth) and device implementation which is free from etching steps. Compared to etch-defined fins, which have commonly been employed, this process allows the fins to be defined by crystal planes rather than pattern transfer from a mask, and inflicts minimum damage to the channel sidewalls [5], [6]. Preservation of the channel surface is of high priority, since surface scattering is a limiting factor of effective InGaAs mobility [7]. Moreover, buried channels are not readily implemented in FinFET structures. Selectively regrown channels may therefore be an important step in advancing InGaAs MOSFET technology.

II. Device Fabrication

Arrays of thin stripes of hydrogen silesquioxane (HSQ) were patterened on epi-ready semi-insulating InP:Fe (100) substrate, using an electron beam lithography (EBL) system [Fig. 1(a)]. The width of the stripes was 35 nm, with 35 nm spacing, and they were aligned to [001]. After curing the HSQ at 350°C, 3 nm InP and 15.5 nm $In_{0.53}Ga_{0.47}As$ (N.I.D.) was grown using metal-organic vapor phase epitaxy (MOVPE). The growth temperature was 500°C, and the ratio of group III to group V precursors (III/V ratio) was 94. $In_{0.53}Ga_{0.47}As$ fins parallel to the substrate surface were formed between the HSQ stripes, which acted as a regrowth mask [Fig. 1(b)]. No growth was observed on the HSQ itself. The fins were approximately 5 nm wider than the spacing of the HSQ stripes due to mask overgrowth. The HSQ was removed using a buffered oxide etch (BOE) [Fig. 1(c)], after which a dummy gate HSQ line was patterned across the fins, as seen in Fig. 1(d). In this manner, gate lengths of 32 nm - 200 nm were defined.

In the second regrowth step, a 25 nm $In_{0.53}Ga_{0.47}As$/15 nm $In_{0.63}Ga_{0.37}As$ ($N_D = 6 \times 10^{19}$ cm^{-3}) contact layer and a 90 nm InP sacrificial support layer was grown (following here

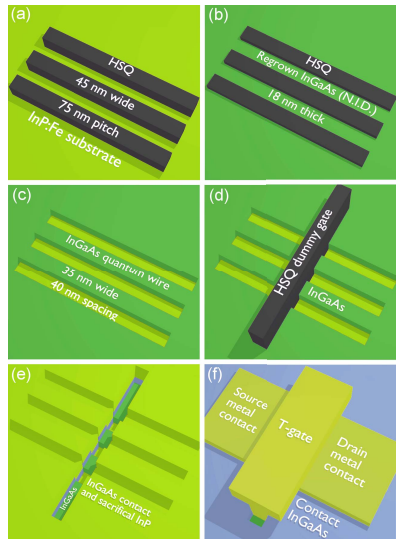

Fig. 1. (a)–(f) Schematic illustrations of the fabrication process flow described in this letter. In the fabricated devices, the fins were rotated instead 45° relative the gate.

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The authors are with the Department of Electrical Engineering, Lund University, Lund SE-221 00, Sweden (e-mail: cezar.zota@eit.lth.se).

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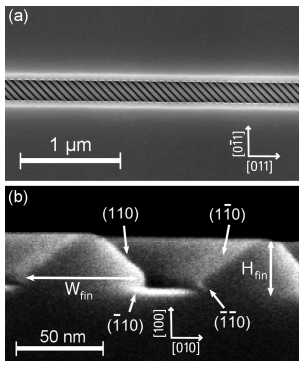

Fig. 2. (a) SEM image of a device after the second regrowth step. Shown are the fins constituting the channel, as seen through the gate-opening in the sacrificial InP and highly doped InGaAs contact layers. (b) Cross-sectional SEM image of a $W_{fin} = 60$ nm fin, with crystal planes denoted.

and onwards [3]). The HSQ was removed by BOE [Fig. 1(e)] and the samples were treated in 10% $(NH_4)_2S$ for 20 min. Fig. 2(a) shows a scanning electron microscope (SEM) image of fins through the opening left by the dummy gate after the second regrowth. A 45° rotation of the fins relative the gate was chosen in order to enable a dummy gate and fins aligned to [011] and [001] respectively, which obtains optimal facets for device fabrication, i.e. avoids mask overgrowth. The gate oxide was deposited by atomic layer deposition (ALD) of 5 cycles Al_2O_3 at 300°C and 55 cycles HfO_2 at 100°C (approximately 0.5 nm and 5.5 nm, respectively). The T-gate was defined using an EBL lift-off process and 10 nm/290 nm thermally evaporated Pd/Au. The oxide not covered by gate metal was removed by BOE to expose the support InP, which was then selectively etched away by HCl. Source and drain metal contacts were deposited using thermal evaporation of Ti/Pd/Au at a tilt of 30°, which allowed the metal to extend in under the gate [Fig. 1(f)]. Transistor isolation was done in a self-aligned manner using the T-gate and source and drain contacts as etch masks, and H_3PO_4:H_2O_2:H_2O to wet etch the channel and contact InGaAs layers. Measurements were performed to ensure there were no significant leakage paths from the pads to the channel. Deposition of Au measurement pads completed the process.

III. Results and Discussion

Fig. 2(b) shows a cross-sectional SEM image of reference 60 nm wide $In_{0.53}Ga_{0.47}As$ fins. The 45° angle between side-walls and substrate reveal that fins are defined by crystallographic {110} planes rather than pattern transfer from the HSQ. The shape of these fins are less electrostatically efficient than fins with steeper side-walls. But the InP substrate can be etched and the fins made free-floating for a gate-all-around structure, in which case a hexagonal shape may be better suited.

Output characteristics and transconductance of $L_g = 48$ and 32 nm devices are reported in Fig. 3. The drain current

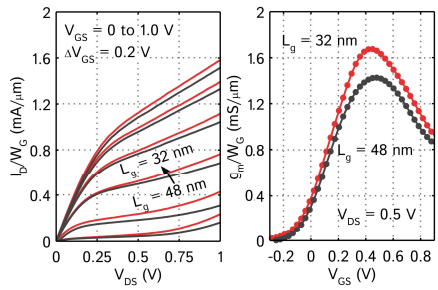

Fig. 3. (a) Output characteristics and (b) transconductances of devices with $L_g = 48$ nm and $L_g = 32$ nm.

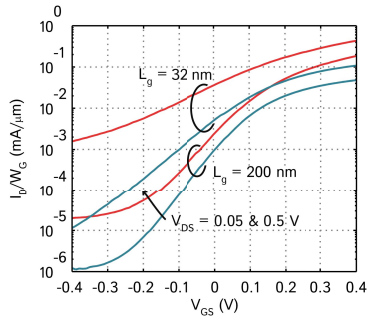

Fig. 4. Subthreshold characteristics of devices with $L_g = 200$ nm and $L_g = 32$ nm. $W_{fin} = 40$ nm.

I_D is normalized by the total gated fin circumference, 5.3 μm, (53 nm for a single fin with $W_{fin} = 40$ nm and $H_{fin} = 15.5$ nm, 100 fins in parallel) as determined from SEM images and atomic force microscopy measurements. The total gate width including fin spacing is 7.1 μm. The current contribution from the parasitic InP transistors between the fins is approximately 0.1 $nA/\mu m$ from reference devices, indicating low leakage currents. The $L_g = 48$ nm device exhibits a maximum transconductance $g_{m,max} = 1.4$ mS/μm at $V_{DS} = 0.5$ V. The $L_g = 32$ nm device shows $g_{m,max} = 1.67$ mS/μm and $I_{D,max} = 1.11$ mA/μm at $V_{DS} = 0.5$ V. The on-resistance (R_{on}) of $L_g = 32$ nm devices is 270 $\Omega\mu$m. The threshold voltage is $V_T = 0.09$ V from linear extrapolation at $g_{m,max}$. This is the highest reported g_m calculated from I_{DS} for any III-V multiple-gate MOSFET (see benchmark in [6]). We attribute these good values to the selectively regrown channel and contacts, as well as the gate-last process.

Subthreshold characteristics of $L_g = 200$ nm and $L_g = 32$ nm devices are shown in Fig. 4. For the $L_g = 200$ nm device, a minimum subthreshold swing (SS) of 85 mV/dec and drain-induced barrier lowering (DIBL) of 88 mV/V is observed at $V_{DS} = 0.05$ V, and SS = 103 mV/dec at $V_{DS} = 0.5$ V, along with $I_{on}/I_{off} = 1.5 \times 10^3$, calculated within a 0.5 V

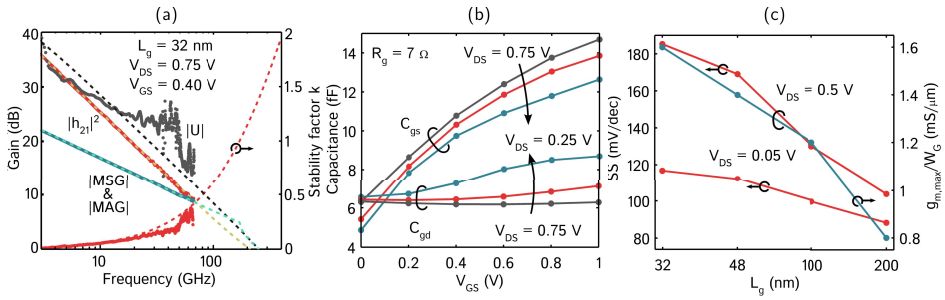

Fig. 5. (a) Measured and modeled (dashed traces) RF gains (f_T = 210 GHz and f_{max} = 250 GHz from model), and stability factor k, and (b) extracted gate-capacitances to source (C_{gs}) and to drain (C_{gd}) for the same L_g = 32 nm device. (c) Scaling metrics, SS and maximum g_m as function of L_g.

window from a fixed $I_{off} = 100$ nA/μm at $V_{DS} = 0.5$ V. The $L_g = 32$ nm device shows SS = 185 mV/dec at $V_{DS} = 0.5$ V.

Radio-frequency (RF) measurements where performed using a vector network analyzer (VNA) at 40 MHz – 67 GHz. The measured current gain (h_{21}), unilateral power gain (U) and maximum stable/available gain (MSG and MAG), as well as the stability factor k are shown in Fig. 5(a) for an $L_g = 32$ nm device. The $g_{m,RF} \approx 2.5$ mS/μm extracted from these measurements is the intrinsic g_m, i.e. without source and drain resistances. The gate resistance R_g was extracted to 7 Ω. Dashed traces show the modeled values from the best fit to a standard hybrid-π model. The maximum f_T of 210 GHz and f_{max} of 250 GHz extrapolated from the hybrid-π model are the highest of any reported III-V multiple-gate MOSFET, though below the records for planar III-V MOSFETs [8]–[10]. These good high-frequency properties are due to suppressed parasitic gate capacitances by the T-gate, as seen in Fig. 5(b) for the same device. The gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitances are nearly independent of L_g at $V_{gs} = 0$ V. The capacitance-axis-intercept in Fig. 5(b) thus gives an estimate of the parasitic capacitances between gate and source, and gate and drain, which each are around 6 fF.

Fig. 5(c) shows as summary of evaluated devices for SS and $g_{m,max}$ as functions of L_g. Scaling down L_g improves $g_{m,max}$, but degrades SS. There are several causes of the latter, such as SCE, back-barrier leakage and impact ionization. Back-barrier leakage is likely severe in these devices, due to the small conduction band offset of around 200 meV between the fins and the InP substrate. Back-barrier leakage can be removed by completely etching the InP substrate under the fins, or be suppressed by using an InAlAs back-barrier. In the case of SCE, to which there is an expected susceptibility, electrostatic control over the channel can be regained by reducing H_{fin} and W_{fin} in order to reduce the natural length of the device, as well as bring the aspect ratio AR = W_{fin}/H_{fin} closer to unity [11]. This has been shown to result in the lowest SS for a given H_{fin} [12].

IV. Conclusion

We have demonstrated $In_{0.53}Ga_{0.47}As$ FinFETs with selectively regrown fins as channel. The device exhibits good logic, as well as high-frequency performance with SS = 85 mV/dec, DIBL = 88 mV/V (at $V_{DS} = 0.05$ V and $L_G = 200$ nm), $g_{m,max} = 1.67$ mS/μm (at $V_{DS} = 0.5$ V and $L_G = 32$ nm), extrapolated $f_T = 210$ GHz and $f_{max} = 250$ GHz ($L_G = 32$ nm). This etch-free and readily scalable process shows promise in post-10 nm CMOS logic and high-frequency applications.

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Paper VI

Paper VI

C. B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "High-Frequency InGaAs Tri-Gate MOSFETs With f_{max} of 400 GHz," *Electronics Letters*, vol. 55, no. 22, pp. 1869–1871, Sept. 2016.

High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz

C.B. Zota✉, F. Lindelöw, L.-E. Wernersson and E. Lind

Extremely scaled down tri-gate RF metal-oxide-semiconductor field-effect transistors (MOSFETs) utilising lateral nanowires as the channel, with gate length and nanowire width both of 20 nm are reported. These devices exhibit simultaneous extrapolated f_t and f_{max} of 275 and 400 GHz at $V_{DS} = 0.5$ V, which is the largest combined f_t and f_{max}, as well as the largest f_{max} reported for all III–V MOSFETs.

Introduction: Tri-gate (or non-planar) metal-oxide-semiconductor field-effect transistors (MOSFETs) for RF applications are motivated by that the use of a high-k oxide, rather than a semiconductor barrier (as in high electron mobility transistors (HEMTs)) allows for higher gate capacitance in the MOSFET [1, 2]. Furthermore, the tri-gate architecture improves short-channel effects, allowing for shorter gate length, L_G, without degradation of performance due to short-channel effects. Both these points enable higher ideal transconductance, g_m, in MOSFETs compared with HEMTs, assuming similar electron mobility. In fact, state-of-the-art III–V MOSFET devices exhibit g_m larger than that of record HEMTs, although they presently do not allow RF-compatible device designs [3–5].

In this Letter, we present RF-compatible tri-gate $In_{0.85}Ga_{0.15}As$ MOSFETs utilising lateral nanowires (NWs) as the channel. Compared with our previous work, we have here further scaled down device dimensions, L_G and NW width, W_{NW} [6]. This enables higher g_m at $V_{DS} = 0.5$ V, which significantly improves f_t/f_{max} from 220/305 to 275/400 GHz. The combined f_t and f_{max}, as well as the f_{max} of these devices represent the highest reported values for all III–V MOSFETs.

Fabrication: The device fabrication process is similar to what has been described elsewhere [7]. The device channel consists of 200 lateral $In_{0.85}Ga_{0.15}As$ NWs, formed by selective area MOCVD growth on (100) InP:Fe (S.I.) substrate, split over two gate fingers. The NW width is 20 nm, and the height is 11 nm. The S/D highly doped regions are formed by a second MOCVD growth step of 40 nm n^+ $In_{0.63}Ga_{0.37}As$/100 nm InP with in-situ Sn doping ($N_D = 5 \times 10^{19}$ cm^{-3}) in the doped layer (Fig. 1*a*). Subsequently, 1 nm/5 nm Al_2O_3/HfO_2 is deposited by atomic layer deposition and Ti/Pd/Au by thermal evaporation, forming the gate stack. The regrown 100 nm InP is selectively etched by an HCl solution leaving a T-gate. S/D and pad metallisation of Ti/Pd/Au completes the process (Fig. 1*b*).

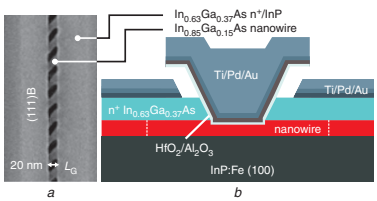

Fig. 1 *Device fabrication and device materials and design*
a SEM image of device after contact regrowth, L_G is defined as distance between n^+ contacts. (111)B denotes crystal facet of contact layer
b Schematic figure of fabricated device

Results: Fig. 2*a* shows transfer characteristics of a device with $L_G = 20$ nm measured at DC with a Keithley 4200 semiconductor characterisation system. All data are normalised to the total gated periphery of the NWs (7 μm). At $V_{DS} = 0.5$ V, peak g_m is 2.1 mS/μm. Fig. 2*b* shows the scaling behaviour of peak g_m and on-resistance R_{on} versus L_G. R_{on} reaches 220 Ω μm at $L_G = 20$ nm. The total access resistance is estimated to 130 Ω μm from transmission line measurements.

RF measurements were performed at 40 MHz to 67 GHz with an Agilent E8361A vector network analyser. On-chip pad de-embedding as well as off-chip two-port load-reflect-reflect-match calibration was performed. The total pad capacitances were ~20 fF.

A small-signal model was determined from the measured *S*-parameters, with a good fit to the measurement data [8]. Fig. 3 shows measured and modelled (dashed traces) unilateral power gain $|U|$, current gain $|h_{21}|^2$ and maximum available/stable gain (|MAG| and |MSG|) for a device with $L_G = 20$ nm. Extrapolated cut-off frequency f_t is 275 GHz and maximum oscillation frequency f_{max} is 400 GHz.

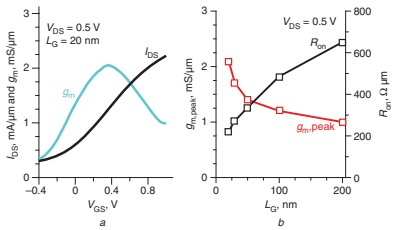

Fig. 2 *Device characteristics at DC*
a Transfer characteristics of a $L_G = 20$ nm device
b Scaling behaviour of peak g_m and R_{on} versus L_G

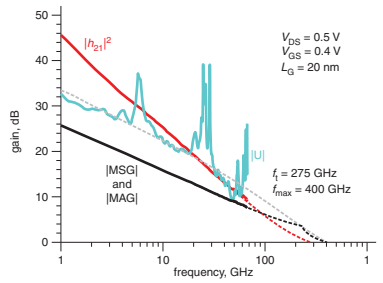

Fig. 3 *Measured and modelled (dashed traces) gain of $L_G = 20$ nm device at $V_{DS} = 0.5$ V*

The small-signal model, which is similar to that in [6], includes both the effect of border traps in the oxide, and impact ionisation. Border traps are modelled using the distributed border trap model in [9]. Border traps introduce a frequency dependency to g_m and g_d, as well as a frequency-dependent oxide loss, and explain the −10 dB slope of $|U|$ versus f [10]. Fig. 4*a* shows $g_{m,peak}$ for an $L_G = 20$ nm device extracted from the small-signal model at DC and 67 GHz (RF). $g_{m,peak}$ increases by ~13% in the latter case, to a maximum of 2.9 mS/μm at $V_{DS} = 1.25$ V, which is attributable to that trap responses are partially disabled at high frequency.

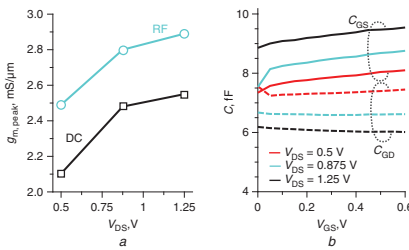

Fig. 4 *Peak g_m and capacitances*
a Peak g_m measured at both 40 MHz (DC) and 67 GHz (RF), for an $L_G = 20$ nm device
b Gate-to-source, C_{GS}, and gate-to-drain, C_{GD}, capacitances measured at different V_{DS}

The effective gate resistance is ~5 Ω, and the source and drain resistances are ~2 Ω. The gate-to-source and gate-to-drain capacitances, C_{GS}

and C_{GD}, are shown in Fig. 4*b*. At $V_{DS} = 0.5$ V, the total gate capacitance $C_{GS} + C_{GD}$ is 15 fF at peak g_m. This includes both the parasitic capacitance from the source and drain gate overlaps, and the intrinsic gate capacitance. The latter is estimated as $C_{gg,int} = (2/3)WLC_{ox}/(C_q + C_{ox})$, with the quantum capacitance $C_q = q^2m^*/\pi\hbar^2$, which is ~2 fF with $m^* = 0.04m_0$. Thus, RF performance is primarily limited by the parasitic overlap capacitance, which can be lowered by implementation of source and drain spacers.

Fig. 5 shows a benchmark of f_t, f_{max} and the geometric mean $\sqrt{f_t \times f_{max}}$ (dashed traces) for state-of-the-art III–V MOSFETs [11–18]. The geometric mean is 330 GHz for these devices, which is the highest reported value for a III–V MOSFET. Squares show planar devices, and triangles show non-planar devices.

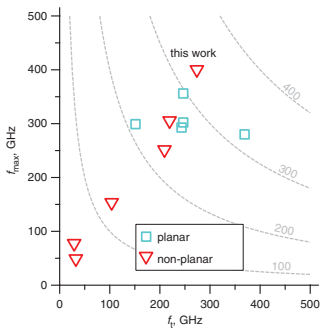

Fig. 5 *Benchmark of RF performance for III–V MOSFETs*
Squares show planar devices, triangles show non-planar devices. V_{DS} and L_G vary between devices, but are 0.5 V and 20 nm, respectively, for this work. Dashed traces show geometric mean

Conclusion: We have demonstrated $L_G = 20$ nm $In_{0.85}Ga_{0.15}As$ tri-gate MOSFETs with high-frequency performance, $f_t = 275$ GHz and $f_{max} = 400$ GHz, recorded at $V_{DS} = 0.5$ V.

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One or more of the Figures in this Letter are available in colour online.

C.B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind (*Department of Electrical and Information Technology, Lund University, Box 118 S-221 00, Lund, Sweden*)

✉ E-mail: cezar.zota@eit.lth.se

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Paper VII

Paper VII

C. B. Zota, G. Roll, L.-E. Wernersson and E. Lind, "Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4078–4083, Dec. 2014.

Radio-Frequency Characterization of Selectively Regrown InGaAs Lateral Nanowire MOSFETs

Cezar B. Zota, Guntrade Roll, Lars-Erik Wernersson, and Erik Lind

***Abstract*— We demonstrate InGaAs multigate MOSFETs, so-called FinFETs. The lateral nanowires constituting the channel in these devices have been formed using selective area regrowth, where the surfaces of the nanowires are crystallographic planes. $L_g = 32$ nm devices exhibit peak transconductance of 1.8 mS/μm at $V_{ds} = 0.5$ V. We also report on RF characterization of these devices. A small-signal hybrid-π model is developed, which includes both the effect of impact ionization and border traps and shows good fit to measurement data. Simultaneously extracted f_t and f_{max} are 280 and 312 GHz, respectively, which are the highest reported values of any III–V multiple-gate MOSFET.**

***Index Terms*— III–V, FinFET, InGaAs, MOSFET, MuGFET, RF, selective regrowth, trigate.**

I. Introduction

INDIUM-RICH $In_xGa_{1-x}As$ is a promising candidate for the channel material in MOSFETs for very large-scale integration applications, due its high electron mobility and injection velocity [1]. Devices with deeply scaled gate lengths, however, are susceptible to short-channel effects, such as high subthreshold swing and drain-induced barrier-lowering (DIBL). This originates, in part, from an increased influence of the drain potential on the surface potential. The use of multiple-gate device architectures, such as FinFETs, offers a way to increase the resilience against these effects, by improving the coupling between the gate voltage and the surface potential [2], [3]. Besides challenges for III–V FinFETs in device fabrication and high-k integration, very little is known about their high-frequency properties. Their comparably large channel surface may affect the dynamic transport properties and it is essential to verify the device characteristics also at RFs.

To date, reported $In_xGa_{1-x}As$ FinFETs utilize nanowires that have been defined by etching using an etch mask [4]–[9]. We have recently demonstrated $In_{0.53}Ga_{0.47}As$ FinFETs employing selectively regrown nanowires as the channel [10]. These nanowires are defined by crystallographic planes, rather than etch-defined surfaces. We report here on improvements to these devices, by increasing the indium content in the nanowires to $In_{0.63}Ga_{0.37}As$, scaling down nanowire dimensions and employing so-called digital etches. This enables record values of simultaneously extracted f_t and f_{max} for III–V multiple-gate MOSFETs, 280 and 312 GHz, respectively. We also report on a hybrid-π small-signal model for these devices, including both the influence of border traps in the oxide and impact ionization, which shows a good fit to measurement data.

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The authors are with the Department of Electrical Engineering, Lund University, Lund 221 00, Sweden (e-mail: cezar.zota@eit.lth.se; guntrade.roll@eit.lth.se; lars-erik.wernersson@eit.lth.se; erik.lind@eit.lth.se).

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II. Device Fabrication

Device fabrication proceeds from a semi-insulating InP:Fe (100) substrate. The selective area regrowth process used in the nanowire formation is illustrated in Fig. 1(a) and (b). First, lines of hydrogen silsesquioxane (HSQ) are patterned using an electron beam lithography system [Fig. 1(a)]. The width of the lines is 30 nm, and the spacing between two lines is 40 nm. After electron beam exposure, HSQ partially becomes SiO_2 [11]. The exposed HSQ is able to sustain the high temperatures required for metal–organic chemical vapor deposition (MOCVD) growth of InGaAs. Thus, it acts as a growth mask in the subsequent selective area growth MOCVD step, where $In_{0.63}Ga_{0.37}As$ growth occurs on all areas not covered by HSQ. The spacing between the HSQ lines defines the width of the lateral, i.e., parallel to the surface, nanowires [Fig. 1(b)]. The thickness of the grown layer determines the height of the nanowires.

Fig. 1(c) shows a top-view scanning electron microscopy (SEM) image of such nanowires, with width $W_{NW} = 40$ nm and height $H_{NW} = 15$ nm. High uniformity of the width of the nanowires is achieved due to, in part, the low line edge roughness of HSQ [11]. Fig. 1(d) shows a cross-sectional SEM image of reference nanowires with $W_{NW} = 150$ nm and $H_{NW} = 60$ nm. Crystal planes can be deduced from facet angles and crystal orientation. The nanowire facets are defined by {110} sidewalls and a (100) top-surface. The HSQ is subsequently removed in a buffered oxide etch. The dimensions of the nanowires are reduced to $W_{NW} = 25$ nm and $H_{NW} = 11$ nm by several cycles of ozone oxidation and diluted HCl native oxide etch.

A second selective area regrowth process is used to define the gate, where a single HSQ line is patterned across the nanowires [Fig. 1(e)] [12]. The width of this dummy gate line later defines the gate length L_g of the FinFET. A highly

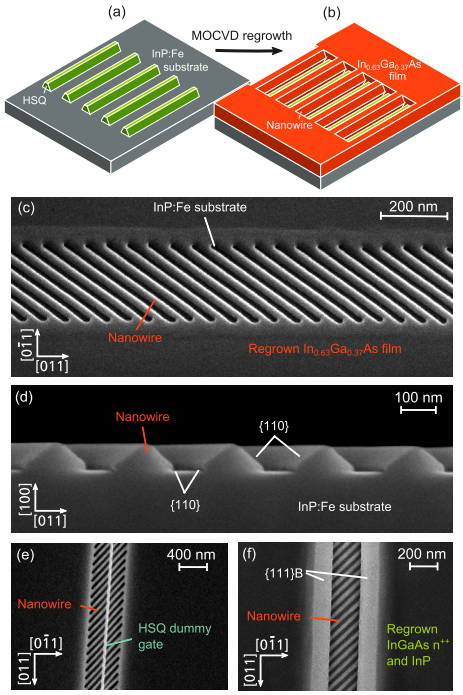

Fig. 1. (a) and (b) Selective area regrowth process. Thin strips of HSQ resist are patterned on InP:Fe substrate. After $In_{0.63}Ga_{0.37}As$ MOCVD regrowth, nanowires are formed in between the strips. (c) SEM image of selectively regrown nanowires. The 45° tilt enables the most suitable nanowire facets for device fabrication. (d) Cross-sectional SEM image of wider reference nanowires. Denoted crystal planes have been deduced from facet angles, which are 45°, and crystal directions. (e) SEM image of nanowires and an HSQ dummy gate patterned across. The dummy gate serves as a regrowth mask in the second MOCVD regrowth step, in which highly n-doped $In_{0.63}Ga_{0.37}As$ as well as support InP is grown. $L_g = 32$ nm for this device. (f) SEM image of the device area after the second MOCVD growth. The bright areas on each side of the nanowires are the {111}B facets of the n^{++} $In_{0.63}Ga_{0.37}As$ and InP. $L_g = 200$ nm for this device.

doped n^{++} ($N_D = 5\times10^{19}$ cm^{-3}) $In_{0.63}Ga_{0.37}As$ 40-nm-thick contact layer, as well as a 100-nm-thick sacrificial InP support layer is grown, after which the HSQ is stripped. Fig. 1(f) shows the nanowires after removal of the dummy gate. The facets of the contact layer are {111}B. One sample (etched sample) was exposed to several additional cycles of ozone oxidation and diluted HCl oxide etch. A gate-stack consisting of Al_2O_3/HfO_2 (5 and 30 Hz, respectively) and Ti/Pd/Au is deposited, after which the supporting InP layer is selectively etched away by a HCl solution, leaving a T-shaped gate [12]. The Ti/Pd/Au contact metal is deposited in a self-aligned manner by use of evaporation from a source tilted relative to the sample. Device fabrication is completed after device isolation, deposition of measurement pads and a forming gas annealing step at 350 °C. Fig. 2 shows a schematic of the final device structure.

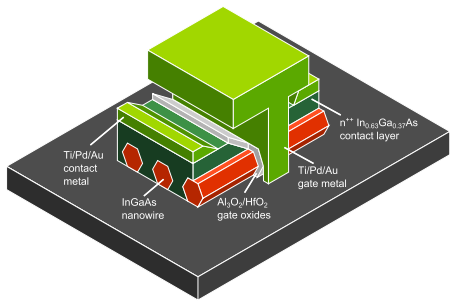

Fig. 2. Schematic of the fabricated FinFET device. The nanowires are shown aligned 90° relative the gate (instead of 45° as in the actual devices) and with symmetric hexagonal shape for clarity.

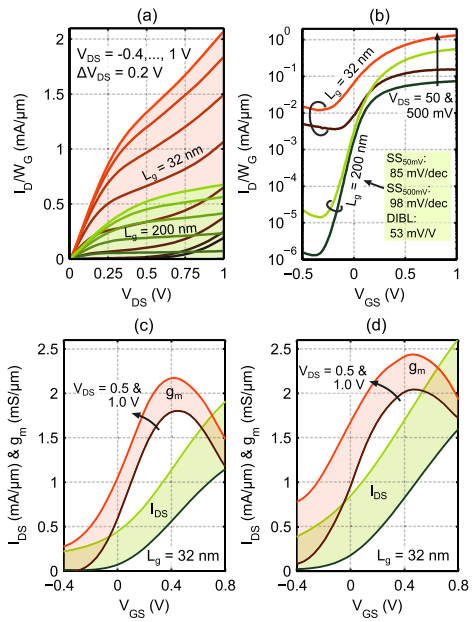

Fig. 3. (a) Output characteristics of $L_g = 32$ and 200 nm devices. (b) I_{DS} at subthreshold for the same devices. (c) Transfer characteristics of the $L_g = 32$ nm device at $V_{ds} = 0.5$ and 1 V. Peak $g_m = 1.8$ mS/μm at $V_{ds} = 0.5$ V and 2.15 mS/μm at $V_{ds} = 1$ V. (d) Transfer characteristics of an $L_g = 32$ nm device, which has been additionally digitally etched. Peak $g_m = 2.05$ mS/μm at $V_{ds} = 0.5$ V and 2.45 mS/μm at $V_{ds} = 1$ V.

As shown in Fig. 1(e) and (f), the nanowires are grown at an 45° angle relative the gate, i.e., the nanowires are grown in the [010]-direction and the gate in the [011]-direction. This is to obtain optimal facets, with regard to device

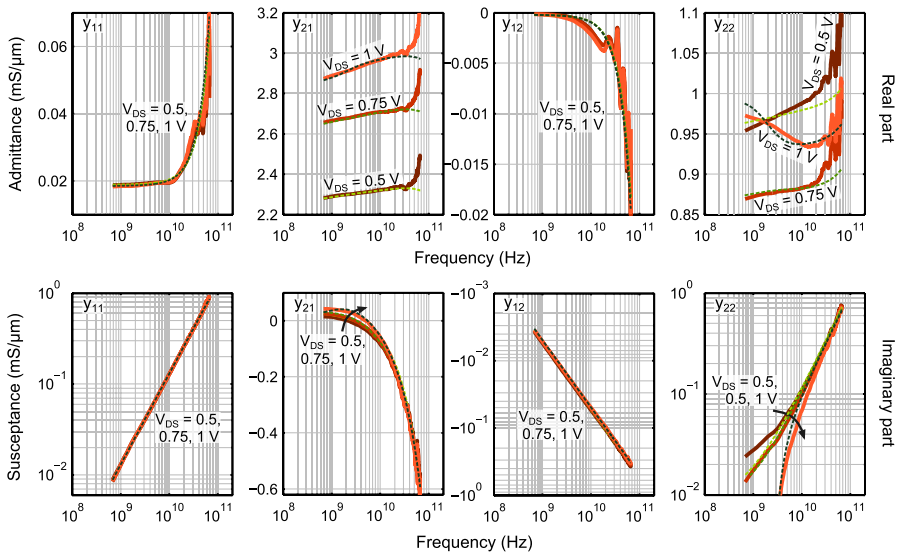

Fig. 4. Measured (red) and modeled (green) y-parameters for an $L_g = 32$-nm FinFET at $V_{gs} = 0.5$ V and $V_{ds} = 0.5$, 0.75, and 1.0 V. Solid lines: measured y-parameters. Dashed traces: modeled values extracted from the small-signal model in Fig. 6(b).

fabrication, for both the nanowires and the gate sidewalls, i.e., facets with a downward slope toward the resist mask. This results in an increase of the effective gate length $L_{\text{eff}} \leq \sqrt{2}L_g$, controlled by the W_{NW}/L_g ratio.

III. DC-Characterization

The output characteristics are shown in Fig. 3(a) for $L_g = 32$ and 200-nm devices. The normalization is performed against the total gated nanowire circumference, $W_{g,\text{NW}} = 6.5$ μm (200 nanowires). The total width of the gate metal is 14 μm. Reference planar MOSFETs on the same sample show 57% lower I_{ds} (normalized to total gated channel width) compared with the FinFETs. One cause may be reduced source and drain resistances due to larger contact area per channel area for the FinFETs. In addition, it has been reported that selectively regrown InGaAs nanowires become more Indium-rich than a corresponding film due to surface kinetics [13]. This will increase the electron mobility in the nanowires with respect to the film. The ON-resistance of an $L_g = 32$-nm device is 240 $\Omega\mu$m, and the total access resistance is 130 $\Omega\mu$m. Fig. 3(b) shows I_{DS} at subthreshold. The subthreshold slope (SS) for an $L_g = 200$ nm device is 98 mV/dec at $V_{\text{ds}} = 0.5$ V and 85 mV/dec at $V_{\text{ds}} = 0.05$ V, and the DIBL is 53 mV/V. For an $L_g = 32$-nm device, SS = 120 and 200 mV/decade, at $V_{\text{ds}} = 0.05$ and 0.5 V, respectively. Due to the small conduction band offset to the InP substrate of $\sim$200 meV, back-barrier leakage is likely significant. The off-state performance can thus be improved by insertion of, for instance, an InAlAs back-barrier. In addition, further scaling of nanowire dimensions will improve electrostatic control.

Fig. 3(c) shows transfer characteristics from dc-measurements. The peak dc-transconductance is $g_{m,\text{dc}} = 1.8$ mS/μm at $V_{\text{ds}} = 0.5$ V and 2.15 mS/μm at $V_{\text{ds}} = 1$ V. For the etched sample, transfer characteristics are shown in Fig. 3(d). These devices exhibit peak $g_{m,\text{dc}} = 2.05$ mS/μm at $V_{\text{ds}} = 0.5$ V and 2.45 mS/μm at $V_{\text{ds}} = 1.0$ V. Due to increased parasitic capacitances in the etched devices, RF characterization is shown here only for the nonetched sample.

IV. RF-Characterization

The scattering S-parameters of the FinFETs were measured from 40 MHz to 67 GHz using an Agilent E8361A vector network analyzer. Off-chip, two-port load-reflect-reflect-match calibration, as well as on-chip pad de-embedding using open and short pads was performed. The pad capacitances were $C_{\text{gs,pad}} = C_{\text{ds,pad}} \approx 10$ fF and $C_{\text{gd,pad}} \approx 1$ fF.

From the S-parameters a small-signal model was extracted. The measured and modeled y-parameters are shown in Fig. 4 at $V_{\text{gs}} = 0.5$ V for the $L_g = 32$-nm device which will be analyzed in this section. Fig. 6(a) shows the measured and modeled current gain $|h_{21}|^2$, unilateral power gain $|U|$, maximum available/stable gain (|MAG|/|MSG|) and the Rollett stability factor k at a bias corresponding to peak f_t. Dashed traces indicate values extracted from the small-signal hybrid-π model shown in Fig. 6(b). Extracted f_t and f_{max} are 280 and 312 GHz, respectively, at $V_{\text{ds}} = 1$ V and

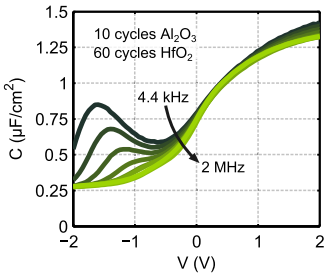

Fig. 5. Capacitance–voltage measurements of a MOSCAP using 10 cycles Al_2O_3 and 60 cycles HfO_2 and a postmetallization forming gas annealing step at 350 °C, measured at 4.4 kHz to 2 MHz. The frequency dispersion at high voltages is a sign of border traps in the oxide.

$V_{gs} = 0.4$ V. Fig. 7(a) and (b) shows f_t and f_{max} as functions of V_{gs} and V_{ds}. Peak f_{max} is 350 GHz.

For the small-signal model, we utilize a standard MOSFET model [14], with added terms due to border traps and impact ionization, which are important in III–V MOSFETs. For an ideal MOSFET, $g_m(\omega)$ and $g_d(\omega)$ are constant with respect to frequency, but as shown in Fig. 4 we observe increasing $g_m(\omega)$ and $g_d(\omega)$ (for $V_{DS} \leq 1.0$ V). This increase can be explained by the effect of border traps. In the low-frequency case, the gate bias partially modulates charging of border traps. These charges are effectively subtracted from I_{ds}, which causes a drop in g_m and g_d. At high frequencies, trap response is partially disabled by the trap charging time constant being longer than the period of the bias. Fig. 5 shows capacitance–voltage measurements from 4.4 kHz to 2 MHz of a MOS capacitor with 10 cycles Al_2O_3 and 60 cycles HfO_2, and a postmetallization forming gas annealing step at 350 °C. The frequency dispersion at high voltage is indicative of border traps [15]. To model this effect, we use the distributed border trap model from [15]. Assuming a constant border trap density for each value of V_{gs}, we numerically solve the potential at the top of the barrier ψ_s with respect to V_{gs} as a function of applied frequency. The transconductance and output conductance, which are $g_m(\omega) \propto \delta\psi_s(\omega)/\delta V_{gs}$ and $g_d(\omega) \propto \delta\psi_s(\omega)/\delta V_{ds}$, respectively, can then be calculated.

Border traps thus introduce a frequency-dependent element to g_m and g_d [16], as well as an extra frequency-dependent oxide loss [15]. The border trap density at a certain gate bias can be obtained by fitting the measured $g_m(\omega)$ to $g_{m,bt}(\omega)$ at low values of $V_{ds} < 0.5$ V, where impact ionization is negligible, obtaining $g'_m(\omega)$ and $g_d(\omega)$. The frequency dependence of $\mathrm{Re}(y_{21})$ and $\mathrm{Re}(y_{22})$ at $f < 50$ GHz can be well reproduced using this approach, assuming identical frequency dispersion for both $g_m(\omega)$ and $g_d(\omega)$. The steep increase in $\mathrm{Re}(y_{21})$ and $\mathrm{Re}(y_{22})$ at $f > 50$ GHz may be due to larger border trap density close to the interface.

Assuming a spatially constant concentration of traps inside the oxide in a fully distributed model, the border trap-related loss can be approximately modeled as $g = \omega g_0$. Such elements have been added at gate/source and drain/source to model the extra frequency-dependent loss.

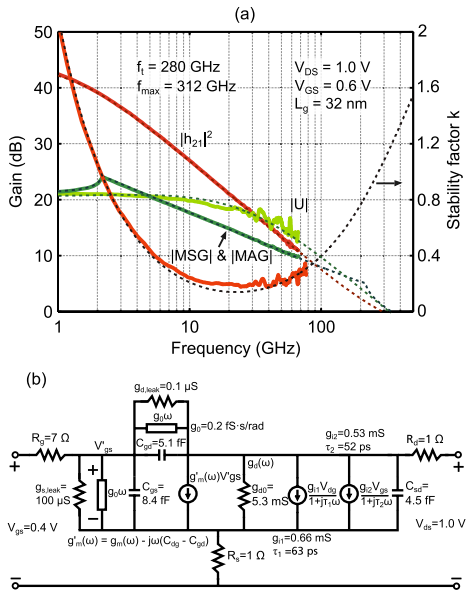

Fig. 6. (a) Small-signal current-gain $|h_{21}|^2$, unilateral power gain $|U|$, and MSG/MAG of an $L_g = 32$ nm device. Dashed traces: values extracted from the small-signal hybrid-π model. (b) Small-signal hybrid-π model for an $L_g = 32$-nm device with the best fit to the y-parameters in Fig. 4.

Empirical fitting to the numerical modeling shows that $\mathrm{Re}(g_m(\omega))$ can approximately be written as $g_{m,bt}(\omega) \approx g_{m0}(1 + \zeta_{bt} \ln(\omega/\omega_0))$ and $g_{d,bt}(\omega) \approx g_{d0}(1 + \zeta_{bt} \ln(\omega/\omega_0))$. g_{m0} and g_{d0} are $g_m(\omega_0)$ and $g_d(\omega_0)$. ζ_{bt} represents the density of border traps as well as the wave function decay into the oxide, at a given V_{gs}. If $g_m(\omega)$ and $g_d(\omega)$ increase logarithmically with frequency, that is thus a sign of oxide border traps.

At higher values of V_{ds}, impact ionization and band-to-band tunneling at the gate–drain region become of importance. These effects have been considered through two current sources between source and drain: $I_{i1} = g_{i1} V_{dg}/(1 + j\tau_1\omega)$, which is due to carrier generation from a strong drain electric field, and $I_{i2} = g_{i2} V_{gs}/(1 + j\tau_2\omega)$, which depends on the magnitude of the drain current [17]. g_{i1} is extracted by fitting g_d, g_{i1} and τ_1 against $\mathrm{Re}(y_{22})$.

As can be seen in Fig. 4, at low V_{ds}, $\mathrm{Re}(y_{22})$ is set by g_d and the border trap dispersion, which gives the slope of the curve. At $V_{ds} = 1$ V, impact ionization begins to dominate, indicated by a decreasing $g_d(\omega)$ at low frequencies. Using g_d and the border trap dispersion from low V_{ds}, g_{i1}, which gives the strength of the effect, and τ_1, which gives the transmission frequency, can be fitted to reproduce the data from $V_{ds} = 1$ V. Fig. 7(c) shows g_{i1} as a function of V_{gs} and V_{ds}, indicating increasing impact ionization for $V_{ds} > 0.5$ V, but a negligible effect for $V_{ds} \leq 0.5$ V. Subsequently, g_{i2} is extracted from

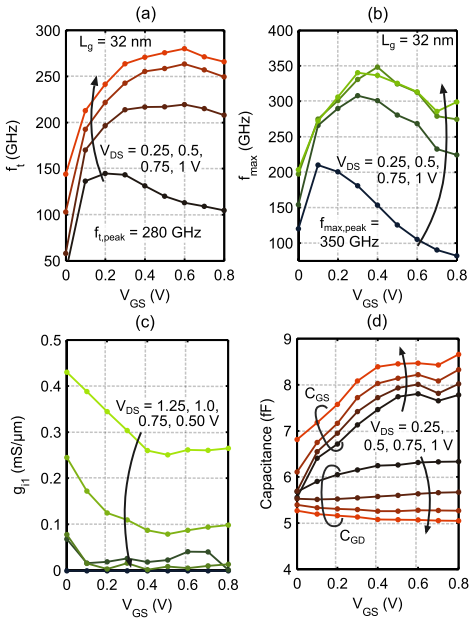

Fig. 7. Data shown here are for the same $L_g = 32$-nm device. (a) Summary of extrapolated f_t and (b) $f_{\max}$ as functions of $V_{\rm gs}$ and $V_{\rm ds}$. Peak values are $f_t = 280$ GHz and $f_{\max} = 350$ GHz. (c) Impact ionization small signal parameter g_{i1} as functions of $V_{\rm gs}$ and $V_{\rm ds}$, showing that impact ionization becomes strong at $V_{\rm ds} > 0.5$ V. (d) Gate/source and gate/drain capacitances extracted from the y-parameters. The values at $V_{\rm gs} = 0$ are the parasitic gate/source and gate/drain capacitances. The increase in $C_{\rm gs}$ as $V_{\rm gs}$ is increased corresponds to an intrinsic gate capacitance of 2 fF.

$\mathrm{Re}(y_{21}) = \mathrm{Re}(g'_m(\omega) - g_{i1} + g_{i2})$, again taking the border trap-induced dispersion into account. In this manner, excellent fits to the measured gains and stability can be achieved.

Using g_{i1} and g_{i2}, the RF-transconductance $g_m(\omega)$ can be extracted from $\mathrm{Re}(y_{21})$. The maximum value is $g_{m,\rm peak} = 3.13$ mS/μm at $V_{\rm ds} = 1$ V and 2.34 mS/μm at $V_{\rm ds} = 0.5$ V. These excellent values, together with the low $C_{\rm gg}$ and gate resistance, $R_g = 7\ \Omega$, explain the high f_t and $f_{\max}$. Using our expression of $g_{m,\rm bt}(\omega)$ at a frequency corresponding to dc and $\zeta_{\rm bt} = 0.006$, one obtains $g_{m,\rm bt}(\omega = 1\ \mathrm{Hz}) \approx 2.5$ mS/μm at $V_{\rm ds} = 1$ V. Accordingly, the cause of the g_m-frequency dispersion is attributed to impact ionization, and to a larger extent, border traps in the oxide.

Gate-to-source and gate-to-drain capacitances, $C_{\rm gd}$ and $C_{\rm gs}$, are shown in Fig. 7(d). For devices with $L_g = 32$ to 200 nm, $C_{\rm gd} = C_{\rm gs} \approx 6$ fF at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 0.25$ V. This corresponds to a total parasitic $C_{{\rm gg},p} \approx 12$ fF. $C_{{\rm gs},t}$ increases by 2 fF as $V_{\rm gs}$ is increased, corresponding to an intrinsic gate capacitance of 2 fF. This agrees well with an estimated $C_{\rm gg} = (2/3)\mathrm{WLC_{ox}}/(C_q + C_{\rm ox})$, where the quantum capacitance is $C_q = q^2 m^*/\pi\hbar^2$. With $m^* = 0.041 m_0$ we obtain $C_{\rm gg} = 1.8$ fF, which is in good agreement with the measured value. The RF-performance is thus strongly limited by the parasitic capacitances, which originate from the parallel-plate-like capacitance between the gate metal and the n^{++} source-and-drain epitaxial layer.

To further improve RF-performance, parasitic capacitances should be reduced. The parallel-plate-like capacitors between the gate metal and the source/drain contact layers each give $C_{{\rm gs}/d,\rm pp} = \epsilon_o \epsilon_r (t_c W_{\rm NW} + t_c S_{\rm NW})/t_{\rm ox,sw}$, where t_c is the thickness of the contact layer and $t_{\rm ox,sw}$ is the oxide thickness on the contact sidewalls. Thus, both $S_{\rm NW}$ and $W_{\rm NW}$ can be scaled down to reduce the parasitics [18]. Moreover, $t_{\rm ox,sw}$ can be increased by implementation of sidewall spacers.

V. Conclusion

We have shown here $\mathrm{In_{0.63}Ga_{0.37}As}$ FinFETs utilizing lateral nanowires formed by selective area regrowth. The large g_m together with low-parasitic capacitances and self-aligned contact formation device fabrication process, resulted in record-high high-frequency performance of extracted $f_t = 280$ GHz and $f_{\max} = 312$ GHz. A small-signal hybrid-π model was developed, which was able to accurately model the measured data. These devices show that selective area regrowth is a promising approach for channel-formation in future III–V MOSFET devices.

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Cezar B. Zota received the M.S. degree in engineering nanoscience from Lund University, Lund, Sweden, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Information Technology.

Guntrade Roll received the Ph.D. degree in electrical engineering from the University of Erlangen-Nuremberg, Erlangen, Germany, in 2012.

She currently holds a post-doctoral position on reliability of III/V transistors with Lund University, Lund, Sweden.

Lars-Erik Wernersson received the Ph.D. degree in solid-state physics from Lund University, Lund, Sweden, in 1998.

He has been a Professor of Nanoelectronics with Lund University since 2005.

Erik Lind received the Ph.D. degree in solid-state physics from Lund University, Lund, Sweden, in 2004.

He is currently an Associate Professor with the Department of Electrical and Information Technology, Lund University.

Paper VIII

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C. B. Zota, L.-E. Wernersson and E. Lind, "$In_{0.63}Ga_{0.37}As$ FinFETs using selectively regrown nanowires with peak transconductance of 2.85 mS/μm at V_{ds} = 0.5 V," *72nd Annual Device Research Conference (DRC)*, pp. 209–210, Jun. 2014.

$In_{0.63}Ga_{0.37}As$ FinFETs Using Selectively Regrown Nanowires with Peak Transconductance of 2.85 mS/μm at V_{ds} = 0.5 V

Cezar B. Zota, Lars-Erik Wernersson and Erik Lind
Department of Electrical and Information Technology, Lund University, Sweden, E-mail: Cezar.Zota@eit.lth.se

III-V materials such as In-rich $In_{1-x}Ga_xAs$ have attracted much attention for low-power applications due to their excellent electron transport properties. To suppress high off-currents in deeply scaled devices, multi-gate MOSFETs (MuGFETs) such as FinFETs, which have improved electrostatic integrity, may be employed [1]. We have previously demonstrated $In_{0.53}Ga_{0.47}As$ FinFETs utilizing selectively regrown nanowires as channel [2]. In this work we report on the next generation of these devices, with increased In-content in the channel, scaled down nanowire dimensions and improved contacts. A record-value of peak transconductance $g_{m,peak}$ = 2.85 mS/um at V_{ds} = 0.5 V and L_g = 52 nm is achieved. We also report on radio-frequency (RF) measurements, with extrapolated cut-off frequency of f_t = 281 GHz and maximum oscillation frequency f_{max} = 365 GHz.

Device fabrication proceeds on semi-insulating InP:Fe (100). Thin strips of hydrogen silsesquioxane (HSQ) are patterned by electron beam lithography. During metal-organic chemical vapor deposition (MOCVD) of 15 nm $In_{0.63}Ga_{0.37}As$, nanowires parallel to the surface are formed in between the HSQ stripes, as seen in Figure 1a. Due to surface kinetics and differences among precursor diffusion lengths, the composition of the nanowires ends up more In-rich than the nominal value [3]. The nanowire dimensions are scaled down using several cycles of Ozone oxidation and diluted HCl native oxide etch. The resulting nanowires have width/height = 25/10 nm. A second MOCVD regrowth step, of $In_{0.63}Ga_{0.37}As$ ($N_D = 6 \cdot 10^{19}$ cm^{-3}) and sacrificial InP, using a HSQ dummy gate strip patterned across the nanowires, defines the gate and source/drain regions, as seen in Figure 1b. After deposition of gate oxide (1 nm Al_2O_3/5 nm HfO_2) and metal (Ti/Pd/Au), the sacrificial InP is etched away, leaving a T-shaped gate. Contact metal (Ti/Pd/Au) is deposited in a self-aligned manner by use of evaporation from a tilted source. Mesa etching and pad metallization completes the process. Figure 2 shows a schematic of the final device except metal. Devices are measured before and after annealing at 350°C in forming gas.

Output characteristics for L_g = 28, 52 and 80 nm devices are shown in Figure 3. Figure 4 shows transconductance of an L_g = 52 nm device. At V_{ds} = 0.25 V, peak transconductance $g_{m,peak}$ = 2.0 mS/μm, at V_{ds} = 0.5 it is 2.85 mS/μm, and the maximum measured value is 3.3 mS/μm at V_{ds} = 1.0 V. Transconductance as a function of L_g is shown in Figure 5. L_g = 28 nm devices have degraded g_m due to short-channel effects. The parasitic InP transistors found between each fin contribute 40 μA/μm at $V_{ds} = V_{gs}$ = 0.5 V, and 0.10 mS/μm to $g_{m,peak}$ at L_g = 52 nm, as measured on reference devices. These currents were subtracted from the transconductance data shown here. L_g = 220 nm devices have SS = 150 mV/dec at V_{ds} = 0.5 V, which is strongly limited by leakage through the InP substrate.

Transmission line method (TLM) measurements are shown in Figure 6 for the regrown $In_{0.63}Ga_{0.37}As$ n^{++} contact layer. The specific contact resistivity is $\rho_c = 6.7 \cdot 10^{-8}$ Ωcm^2. The contact resistance is R_c = 22.8 Ωμm. R_{on} as a function of L_g is shown in Figure 7. R_{on} is 160 Ωμm at L_g = 52 nm, the intrinsic resistance is thus $R_{int} = R_{on} - 2R_c$ = 114.4 Ωμm.

RF-measurements were performed using a vector network analyzer at 40 MHz to 67 GHz. Figure 8 shows measured current gain (h_{21}), unilateral power gain (U) and maximum stable/available gain (MSG/MAG) for an L_g = 35 nm device. Dashed traces are the values of a hybrid-π model fitted to the measurement data. Extrapolated f_t and f_{max} are 281 and 365 GHz respectively, at V_{ds} = 1 V and V_{gs} = 0.4 V. Due to the three-dimensional nature of the channel, and the spacing between nanowires, FinFETs are vulnerable to parasitic capacitances. In these devices gate-to-drain/source parasitic capacitances are extracted to $C_{gs,p} = C_{gd,p} \approx 6$ fF, corresponding to a total parasitic $C_{gg,p} \approx 12$ fF. These parasitics originate from the parallel-plate-like capacitors between the gate metal and the n^{++} contact layer side-walls. As V_{gs} is increased, C_{gs} increases by ~2 fF, corresponding to an intrinsic gate capacitance $C_{gs,int} \approx 2$ fF. This agrees well with an estimation according to $C_{gs,int} = (2/3)WLC_{ox}/(C_q + C_{ox}) = 1.8$ fF. RF-performance is thus strongly limited by the parasitic capacitances. Maximum g_m extracted from the RF-measurements, i.e. the intrinsic transconductance, is $g_{m,int} \approx 4$ mS/μm.

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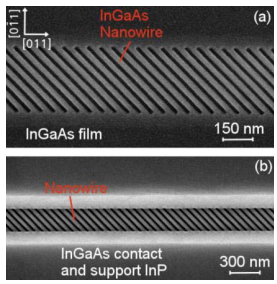

Figure 1: (a) SEM images of selectively regrown InGaAs nanowires. (b) Nanowires after growth of n^{++} $In_{0.63}Ga_{0.37}As$ contacts and sacrificial InP.

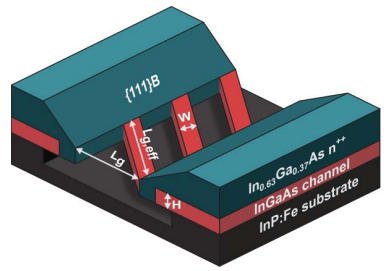

Figure 2: Schematic of final device except metal. $L_{g,eff}$ indicates the effective gate length due to the 45° tilt of the nanowires.

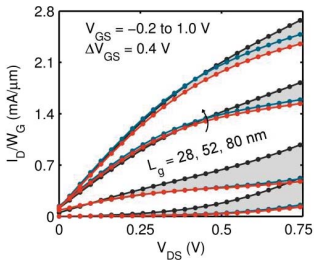

Figure 3: Output characteristics of devices with L_g = 28, 52 and 80 nm.

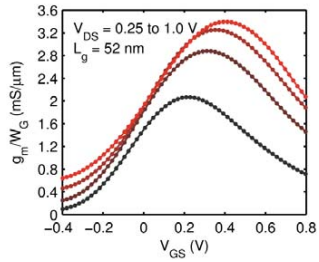

Figure 4: DC Transconductance of an L_g = 52 nm device. Peak value at V_{ds} = 0.5 is 2.85 mS/μm.

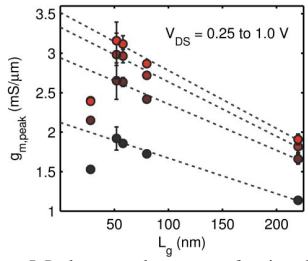

Figure 5: Peak transconductance as a function of V_{ds} and L_g.

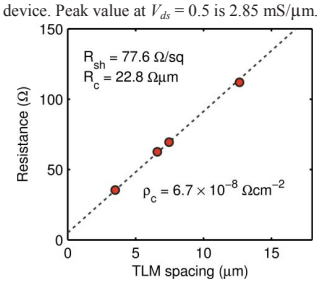

Figure 6: TLM measurements on the n^{++} $In_{0.63}Ga_{0.37}As$.

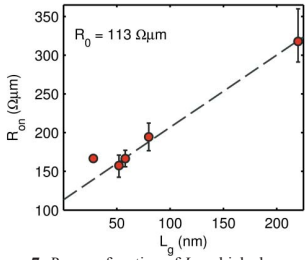

Figure 7: R_{on} as a function of L_g, which shows approximately linear dependence.

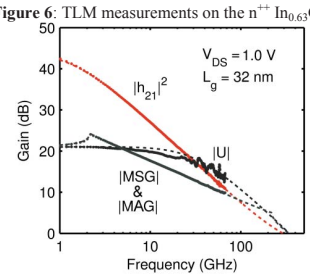

Figure 8: Small-signal current gain (h21), unilateral power gain and maximum stable/available power gain.

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Paper IX

Paper IX

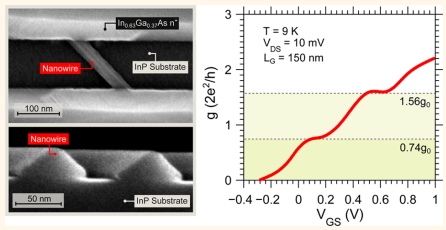
C. B. Zota, D. Lindgren, L.-E. Wernersson and E. Lind, "Quantized Conduction and High Mobility in Selectively Grown $In_xGa_{x-1}As$ Nanowires," *ACS Nano*, vol. 9, no. 10, pp. 9892–9897, 2015.

Quantized Conduction and High Mobility in Selectively Grown $In_xGa_{1-x}As$ Nanowires

Cezar B. Zota,*,† David Lindgren,‡ Lars-Erik Wernersson,† and Erik Lind†

†Department of Electrical and Information Technology and ‡Division of Solid State Physics, Lund University, Box 118, 22100 Lund, Sweden

ABSTRACT We report measured quantized conductance and quasi-ballistic transport in selectively regrown $In_{0.85}Ga_{0.15}As$ nanowires. Very low parasitic resistances obtained by regrowth techniques allow us to probe the near-intrinsic electrical properties, and we observe several quantized conductance steps at 10 K. We extract a mean free path of 180 ± 40 nm and an effective electron mobility of 3300 ± 300 $cm^2/V \cdot s$, both at room temperature, which are among the largest reported values for nanowires of similar dimensions. In addition, optical characterization of the nanowires by photoluminescence and Raman measurement is performed. We find an unintentional increase of indium in the $In_xGa_{1-x}As$ composition relative to the regrown film layer, as well as partial strain relaxation.



KEYWORDS: field-effect transistors · nanowire · electric transport · mobility · InGaAs · ballistic transport · selective regrowth · photoluminescence · Raman

Indium-rich $In_xGa_{1-x}As$ nanowires have gathered much research attention recently due to their excellent electron transport properties.[1] In particular, InAs nanowires have been shown to have a mobility at least an order of magnitude higher than that of silicon nanowires.[2,3] Moreover, the ease by which ohmic contacts are formed into $In_xGa_{1-x}As$ and the possibility of low-defect high-k oxide interfaces have made $In_xGa_{1-x}As$ one of the primary considerations as the replacement for silicon channels in n-type metal-oxide-semiconductor field-effect transistors (MOSFETs).[4−7] The implementation of III−V MOSFETs, such as $In_xGa_{1-x}As$, will likely be in the form of 1D nanowires with diameters less than 30 nm.[8] The use of nanowires as the channel in MOSFETs offers enhanced performance compared to traditional planar channels, through improved electrostatic control. The combination of high-mobility materials and short gate lengths (~30 nm) of state-of-the-art MOSFETs indicates operation in the ballistic or quasi-ballistic regime. Together with 1D channels, such devices display unique characteristics, notably quantized conduction and step-like features in the conductance at low temperatures.

Several methods of fabricating $In_xGa_{1-x}As$ nanowires have been reported. In particular, nanowires grown by the vapor−liquid−solid (VLS) technique, employing a metal particle catalyst, have been widely studied.[9] VLS-grown InAs nanowires, for instance, exhibit mobility ranging from 2000 to 5000 $cm^2/V \cdot s$ at nanowire diameters of <30 nm.[10] Etched-out $In_{0.70}Ga_{0.3}As$ nanowires have also recently been studied.[11] However, due to increased surface scattering, the mobility of nanowires with a diameter <30 nm is typically more than 2 orders of magnitude lower than bulk mobility.[10] For this reason, the preservation of high-quality nanowire side-walls must be a high priority.[12,13] In this work, we electrically and optically characterize selectively grown InGaAs nanowires that are parallel to the surface. We fabricate MOSFET test devices with very low parasitic resistances using a contact regrowth technique, allowing us to probe the near-intrinsic electrical transport properties of the nanowires. Multiple quantized conductance steps are

* Address correspondence to cezar.zota@eit.lth.se.

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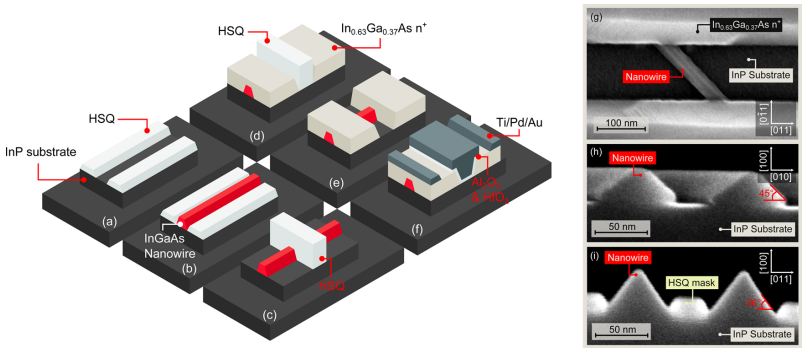

Figure 1. (a) HSQ is patterned on InP/Fe semi-insulating substrate using EBL. (b) $In_{0.63}Ga_{0.37}As$ is regrown by MOCVD using the HSQ as a growth mask. A nanowire is formed between the HSQ-covered areas. (c) HSQ is stripped by buffered oxide etch (BOE), and another HSQ film is applied and patterned as a thin line across the nanowire. (d) Highly doped $In_{0.63}Ga_{0.37}As$ is regrown by MOCVD. (e) HSQ is stripped by BOE. The highly doped regions on each side of the nanowire constitute the source and drain of the MOSFET. (f) Al_2O_3 and HfO_2 are deposited by atomic layer deposition (10 and 60 cycles, respectively). Metallization is performed by lift-off. (g) SEM image of the device corresponding to stage (e). (h,i) Cross-sectional SEM images of wider reference nanowires in two different directions.

observed at $T_L = 10$ K. We explain the characteristics by use of the ballistic MOSFET theory.[14] The extracted electron mobility obtained from the mean free path at room temperature is 3300 ± 300 $cm^2/V \cdot s$, among the highest reported for nanowires of any material system. Optical characterization reveals increased indium levels in the nanowires as well as partial strain relaxation as compared with planar film growth. These results show the potential of selectively grown lateral InGaAs nanowires for high-performance MOSFET devices. We would also like to highlight the potential use of nanowires with a long mean free path in the search for Majorana Fermions.[15]

METHODS

Figure 1a–f shows schematics of the fabrication process of the test device.[16] First, hydrogen silsesquioxane (HSQ) is patterned by electron beam lithography (EBL) on semi-insulating (100) InP/Fe. HSQ is transformed to SiO_2 when cured by electron beam exposure. This enables it to act as a growth mask during the subsequent metal–organic chemical vapor deposition (MOCVD) growth of 15 nm $In_{0.63}Ga_{0.37}As$, resulting in a nanowire composition of $In_{0.85}Ga_{0.15}As$ as obtained from optical characterization. Parallel to the surface, a nanowire is formed in the narrow space between HSQ-covered areas. Figure 1g shows a scanning electron microscopy (SEM) image of a single-nanowire device. Figure 1h,i shows cross-sectional SEM images of wider reference nanowires oriented with their length along the [001] and [011] directions, respectively. From the facet angles, we deduce that [001] nanowires are defined by {110} facets and [011] nanowires by {111}B facets. In order to obtain optimal facets of the subsequent contact regrowth layer, the fabricated devices utilize nanowires oriented along [001].

The dimensions of the nanowire are further scaled down by several cycles of digital etching through ozone oxidation and diluted HCl etching.[17] The root mean square surface roughness of the top nanowire surface is determined from atomic force microscopy measurements as <0.4 nm, below or at the resolution limit of the measurement system (Supporting Information). The final width and height of the nanowire are 28 and 10 nm, respectively. Subsequently, an HSQ line, which serves to define the gate length, L_G, of the device, is patterned across the nanowire, and a second MOCVD regrowth step of 40 nm $In_{0.63}Ga_{0.37}As$ n^{++} ($N_D = 5 \times 10^{19}$ cm^{-3}) is performed. The highly doped regions form the source and drain of the device and facilitate low contact resistances. Prior to atomic layer deposition of the gate oxide (10 cycles Al_2O_3 and 60 cycles HfO_2), the nanowires are passivated by sulfur treatment. Subsequently, gate metal (Ti/Pd/Au) is evaporated and deposited by lift-off. The gate oxide is then removed in the source and drain regions, using the gate metal as the mask, but remains under the gate metal overlap with source and drain as isolation. Ti/Pd/Au contact metal is deposited by lift-off of 600 nm from each side of the gate metal. Au pad metallization by lift-off finalizes the process.

RESULTS AND DISCUSSION

The conductance $g = dI_{DS}/dV_{DS}$ of a representative device is shown in Figure 2a. Two distinct step-like features, corresponding to two sub-band levels, are observed at $g_1 = 0.74g_0$ and $g_2 = 1.56g_0$, where $g_0 = 2q^2/h$. From the Landauer–Büttiker formalism, each sub-band is expected to increase the device

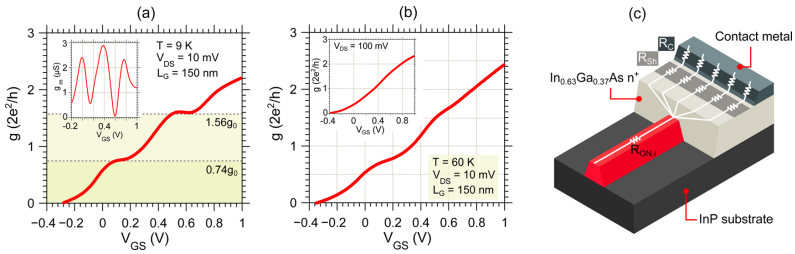

Figure 2. (a) Conductance $g = dI_{DS}/dV_{DS}$ *versus* V_{GS} of an InGaAs nanowire MOSFET at 10 K. Inset shows the transconductance $g_m = dI_{DS}/dV_{GS}$ for the same device and conditions. (b) $g-V_{GS}$ for the same device at 60 K. Inset shows $g-V_{GS}$ at large V_{DS}. (c) Schematic figure of the resistances in a device from the drain or source side. The total on-resistance is constituted by the intrinsic on-resistance of the nanowire, $R_{ON,i}$, and a parasitic resistance, R_P, which is a spreading access resistance constituted by the contact resistance, R_C, and the sheet resistance, R_{Sh}.

conductance by $g = Tg_0$, where T is the transmission. For fully ballistic transport, $T = 1$. We note that g_2 is approximately twice the level of g_1, which indicates that the transmission to each sub-band is similar. The further increased I_{DS} beyond g_2 is sign of a third sub-band level within the V_{GS} measurement range, which is also revealed by a third g_m peak in the inset. I_{DS} at higher V_{GS} was not measured due to the risk of device breakdown. Generally, the number of conductance steps visible in a given V_{GS} measurement range is determined by several factors: (i) The nanowire dimensions set the band structure, that is, the energy separation between sub-bands. (ii) L_G together with (iii) the mean free path determine the transmission. (iv) The gate capacitance and (v) the oxide interface trap density (D_{it}) determine the control of V_{GS} on the band structure in the nanowire. For example, high gate capacitance and low D_{it} will reduce the V_{GS} separation between conductance steps, allowing for more visible steps in a given V_{GS} range. At 60 K, the step-like features are much less distinct, as shown in Figure 2b. At V_{DS} = 100 mV, the steps are not visible (inset). Except for thermal broadening, we observe no apparent dependence of g_1 or g_2 on temperature, which implies that the dominant scattering mechanism is temperature-independent surface roughness scattering.[18] The steps are visible up to 120 K (see Supporting Information). Similarly, the device transconductance $g_m = dI_{DS}/V_{GS}$ is ideally 0 unless V_{GS} causes a sub-band to enter the conducting window, forming peaks at those energies. The conductance steps become less visible as eV_{DS} nears the energy separation between sub-bands or the sub-bands are sufficiently thermally broadened.

The mean free path of a single nanowire λ_s is determined from the transmission $T = \lambda_s/(\lambda_s + L_G)$, with the conductance for the first sub-band being $g_1 = Tg_0 \approx 0.74g_0$ and L_G = 150 nm. Thus, we obtain λ_s = 350 ± 50 nm for the first sub-band of a single device. The error margins are due to uncertainty in determining the exact value of T for the conductance step. A similar value was reported by Chuang *et al.*[18] for a single VLS-grown nanowire with d = 26 nm: $T \approx 80\%$ at L_G = 60 nm, corresponding to a peak λ_s = 280 ± 50 nm, and an average λ = 150 ± 40 nm is extracted from the L_G dependence.

To obtain an accurate value of λ_s, the parasitic resistances of the device must be calculated. Figure 2c shows a schematic of the resistances from the source or drain side in a device. The total on-state resistance of a device is $R_{ON} = R_{ON,i} + R_P$, where $R_{ON,i}$ is the intrinsic on-resistance and R_P is the parasitic spreading access resistance which comes from R_C and R_{Sh}. R_C = 25 Ω·μm is the contact resistance due to the ohmic metal contacts to the n^+ $In_{0.63}Ga_{0.37}As$ layer, extracted from on-sample transmission line method measurements. R_{Sh} is a contribution from the sheet resistance ($R_\square$ = 70 Ω/□) of the n^+ $In_{0.63}Ga_{0.37}As$ layer through the ∼100 nm distance between the contact metal and the nanowire. Using the measured values of R_C and R_{Sh}, we calculate the spreading access resistance R_P = 150 ± 50 Ω by COMSOL 3D simulation. This includes the resistance added from a possible Schottky barrier between the metal contact and the n^+ $In_{0.63}Ga_{0.37}As$ layer. This resistance is negligible compared to $1/g_0$ = 12.9 kΩ, which means that the calculation of λ_s from T is accurate.

To determine the average room temperature λ of our nanowires, we fabricated devices with 100 parallel nanowires and L_G from 50 to 225 nm (a total of 20 devices). Figure 3a shows an SEM image of such a device. Conductance steps are not visible in these devices due to the many parallel nanowires with slight width variations (±2 nm). To obtain λ, we use the resistance of a ballistic MOSFET in the on-state, described as

$$R_{ON} = \frac{h}{2q^2M\lambda}L_G + \frac{h}{2q^2M} + R_P$$

where R_P is the total parasitic resistance and M is the number of conducting sub-bands.[19] R_{ON} per nanowire for these devices is shown in Figure 3b. Due to the tightly packed parallel nanowires, R_P is larger than that

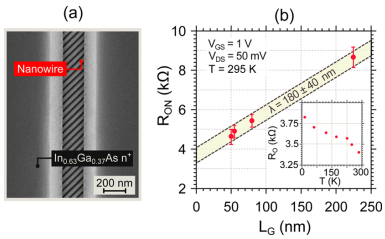

Figure 3. (a) SEM image of the MOSFET device with 100 parallel nanowires. (b) On-resistance per nanowire *versus* gate length for the same type of devices at room temperature. Inset shows on-resistance *versus* temperature for a single device with L_G = 50 nm.

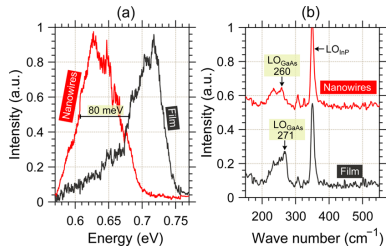

Figure 4. (a) Photoluminescence measurements for nanowires and $In_{0.53}Ga_{0.47}As$ film on the same sample. Band gap narrowing due to background doping is 80 meV. (b) Raman spectroscopy results for the same nanowires and film.

in the single-nanowire device. Source and drain contacts each add $R_C \approx 800\ \Omega$ and $R_{Sh} \approx 100\ \Omega$ per nanowire. Furthermore, the width of the highly doped contact region is approximately twice that of the total width of the nanowires, so the total parasitic resistance is $R_P = R_C \approx 800\ \Omega$, which can be compared to $R_{ON} \approx 4\ k\Omega$ at L_G = 50 nm. Using this value, we obtain an average $\lambda = 180 \pm 40$ nm at room temperature. The error margin comes from the spread in R_{ON} for devices at the same L_G, which may be due to several causes, such as nanowire width variations, contact resistance variations, and nanowire defects. This value of λ overlaps those reported for the VLS-grown vertical nanowires and compares favorably to those reported for etch-defined lateral nanowires.[18] For instance, Thathachary *et al.*[11] showed λ = 100 nm for W_{NW}/H_{NW} = 40/10 nm etch-defined lateral nanowires at room temperature utilizing gated Hall measurements.

The room temperature near-equilibrium electron field-effect mobility of our nanowires is $\mu_e = 3300 \pm 300\ cm^2/V\cdot s$, calculated from[19]

$$\mu_e = \frac{C_F q \lambda v_T}{2kT_L}$$

which comes from $D_n = \lambda V_T/2$ and the Einstein relation utilizing a correction factor $C_F = 2.75 \pm 0.25$, which comes from the degenerate conditions. We use $E_F - E_C = 87.5 \pm 12.5$ meV in our calculations, corresponding to 3−4 filled sub-bands. We note that this method of calculating the mobility from the mean free path is not influenced by D_{it} because D_{it} does not directly impact the transmission of each sub-band. Generally, D_{it} can have a significant impact on the extracted field-effect mobility in III−V field-effect transistors. This value of the electron mobility is close to the other reported values in $In_xGa_{1-x}As$ nanowires with similar dimensions formed by VLS growth.[20−24] For instance, Ford *et al.* reported VLS-grown InAs nanowires with a field-effect mobility of 1000−7000 $cm^2/V\cdot s$ for diameters of d = 10−40 nm.[10] For silicon nanowires, Kotlyar *et al.*[12] determined a field-effect mobility of 100−250 $cm^2/V\cdot s$ for d = 10−25 nm from simulations. The relatively high mobility in our nanowires may be due to a lack of stacking faults orthogonal to the current (as has been reported for VLS-grown nanowires[25]) and high-quality side-wall surfaces.

From R_{ON} in Figure 3b, we are also able to extract M using the estimated value of R_P. We obtain $M = 3.5 \pm 0.5$, which is in agreement with the value observed in the conductance plot, M = 3 at 10 K. We observe a slight increase of R_{ON} as T_L is lowered, as shown in the inset of Figure 3b for an L_G = 50 nm device. This may be due to a nonideal metal/semiconductor junction, forming a small Schottky barrier.

The composition and strain of the nanowires were characterized by photoluminescence (PL) and Raman spectroscopy. To obtain strong signals, we prepared samples with 20 μm × 10 μm areas covered with large reference nanowires (the cross section of which is seen in Figure 1h), well below the spot size of the laser. The dimensions of these nanowires are W/H = 50/30 nm. Two samples were prepared with $In_{0.53}Ga_{0.47}As$ and $In_{0.63}Ga_{0.37}As$ nominal epitaxial growth, respectively. The composition of the 2D layer outside of the nanowire area was confirmed by X-ray diffraction measurements to coincide with the nominal growth. Figure 4a shows the result of the PL measurement at 10 K using a 532 nm laser for the $In_{0.53}Ga_{0.47}As$ sample. The InGaAs peak of the nanowires is red-shifted by approximately 80 meV relative the $In_{0.53}Ga_{0.47}As$ film peak, which was measured outside the nanowire-covered area on the same sample. The background doping of the film layer was obtained from Hall measurements as $N_D \approx 5 \times 10^{17}\ cm^{-3}$. This causes band gap narrowing of approximately 80 meV, which we assume is identical for the nanowires. Using a 2D self-consistent effective mass Schrödinger−Poisson solver, we estimate that the nanowire size quantization increases the band gap by 15 meV, which is not accounted for in these calculations. This will cause a small underestimation of the calculated indium content and strain. The peak shift cannot directly be translated to a composition shift because any composition shift from $In_{0.53}Ga_{0.47}As$

will result in strain due to lattice mismatch to the InP substrate.[26] For instance, an increase of the indium composition can result in a maximum compressive strain up to 3.8% for InAs, which would cause a blue shift in the PL peak.

The Raman spectra of the same nanowires and $In_{0.53}Ga_{0.47}As$ 2D layer are shown in Figure 4b. The Raman spectrum of InGaAs contains four peaks resulting from incident laser photon interactions with the four transverse and longitudinal optical phonons (TO and LO), TO_{GaAs}, TO_{InAs}, LO_{GaAs}, and LO_{InAs}. While the TO−phonon interactions are generally weak, the LO_{GaAs} interaction will dominate even in indium-rich InGaAs. Therefore, the LO_{GaAs} peak can be used as a marker of composition.[27] We observe a shift of the nanowire LO_{GaAs} peak by approximately 10 cm^{-1} as compared with the 2D layer. Both the strain %, *s*, and indium fraction, *x*, in $In_xGa_{1-x}As$ will shift the LO_{GaAs} peak position and the position of the PL peak maxima.[26−29] By using a combined model of how *s* and *x* determine the peak position in both PL and Raman, *s* and *x* can be calculated (details are found in Supporting Information). Using this method, we find that the nanowires are $In_{0.78\pm0.03}Ga_{0.25\pm0.03}As$ with 0.77 ± 0.15% compressive strain if the regrown film is $In_{0.53}Ga_{0.47}As$. For the sample with nominal $In_{0.63}Ga_{0.37}As$ growth, we obtain $In_{0.85\pm0.03}Ga_{0.15\pm0.03}As$ with 1 ± 0.15% compressive strain for the nanowires. The composition shift of the nanowires may be explained by a local change of growth kinetics and diffusion, such as precursor flows, due to the HSQ mask. The expected strain in 2D layers of such compositions is 1.75 and 2.2%, respectively, indicating a partial strain relaxation mechanism in the nanowires.[26]

CONCLUSION

We have fabricated MOSFET devices to characterize the electron transport properties of selectively grown $In_{0.85}Ga_{0.15}As$ nanowires. The nanowires exhibit μ_e = 3300 ± 300 $cm^2/V\cdot s$, among the highest reported values for nanowires of similar dimensions. We also optically characterized our nanowires and found an unintentional increase of indium in the composition as well as partial strain relaxation. These results highlight the potential use of selectively regrown nanowires as the channel in high-performance electrical devices.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b03318.

Additional information, figures, and optical characterization (PDF)

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Paper X

Paper X

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Size-effects in indium gallium arsenide nanowire field-effect transistors

Cezar B. Zota[a] and E. Lind
Department of Electrical and Information Technology, Lund University, Lund 22101, Sweden

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We fabricate and analyze InGaAs nanowire MOSFETs with channel widths down to 18 nm. Low-temperature measurements reveal quantized conductance due to subband splitting, a characteristic of 1D systems. We relate these features to device performance at room-temperature. In particular, the threshold voltage versus nanowire width is explained by direct observation of quantization of the first sub-band, i.e., band gap widening. An analytical effective mass quantum well model is able to describe the observed band structure. The results reveal a compromise between reliability, i.e., V_T variability, and on-current, through the mean free path, in the choice of the channel material. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4961109]

III–V nanowires (NWs) with a high indium-content, such as InAs, InSb, and $In_xGa_{1-x}As$, have been studied widely, both as systems for the study of basic phenomenon, as well as channel materials in high-performance electrical devices.[1–3] For the former, strong spin-orbit coupling and a large Landé g-factor, together with a long mean free path—enabling quasi-ballistic transport—have highlighted these material systems as key candidates for the study of topological and helical states, as well as Majorana Fermions.[4] The long electron mean free path, typically in the order of 100–200 nm, correlated with the high electron mobility of these materials, also make them suitable for high-performance field-effect transistor (FET) applications.[5–7] Moreover, the nanowire shape offers the optimal geometric structure for strong electrostatic control in such devices, which is required for very short gate length devices with $L_G < 20$ nm.[8] Since the diameter of such devices is smaller than the effective Bohr radius (18–34 nm for $In_xGa_{1-x}As$, $x = 0.53$ to 1), this essentially describes a 1D system, which exhibits subband splitting, visible as quantized conductance at low temperature.[9] While there have been several reports on quantized conductance in InAs NWFETs, none have been on high-performance FETs.[10–13] In this work, we correlate a low-temperature study of sub-band splitting in high-performance InGaAs NWFETs with a study of the room-temperature performance of the same devices.

Threshold voltage, V_T, variability in MOSFETs with scaled 3D channels, such as FinFETs, has been much discussed recently.[14,15] Although 3D channel devices have smaller V_T variation caused by dopant fluctuations, quantization of the first sub-band, i.e., band gap widening, causes increased V_T shift due to NW width variations, which has a detrimental effect on, e.g., CMOS performance and reliability.[16] While there have been experimental demonstrations of V_T versus W_{NW} in scaled NWs, these have been at room-temperature without definite proof of sub-band quantization.[17,18] At room-temperature, a V_T increase is difficult to distinguish from a reduction in the drain current or the transmission, which is also expected to occur due to increased surface scattering. In this work, we experimentally demonstrate the effects of bandgap widening, as the result of quantization, on V_T in a way which is independent of surface scattering, i.e., by direct observation of bandgap widening.

The NWs were produced by selective area metal-organic chemical-vapor deposition (MOCVD) of $In_{0.65}Ga_{0.35}As$ on a semi-insulating InP:Fe substrate, utilizing a hydrogen silsesquioxane (HSQ) hard mask. The composition of the NWs ends up more indium-rich, approximately $In_{0.85}Ga_{0.15}As$, due to growth kinetics and interactions with the HSQ mask.[13] Each device uses one NW. The NW width, W_{NW}, i.e., the width of the base, is determined by the spacing between two patterned areas of HSQ and is varied between $W_{NW} = 18$ and 90 nm. The NW height, H_{NW}, is set by the growth conditions and is 8 nm for all devices. Figure 1(a) shows a schematic of the cross-section of a nanowire, and the facet denominations are deduced from the NW orientation and the 45° facet angles.[13] The surface of narrow NWs will be dominated by the {110} side facets, while for wider NWs, the (100) top-facet will dominate. FET fabrication proceeds with highly doped source- and drain-contact formation by selective area regrowth of n^+ $In_{0.63}Ga_{0.37}As$ ($N_D = 5 \times 10^{19}$). The gate length L_G is set by the width of the dummy-gate HSQ pattern used in this step and is 70 nm for all devices. Subsequently, mesa definition by H_3PO_4:H_2O_2:H_2O (1:1:25) etching is performed in order to isolate the terminals of the device. Ti/Pd/Au contact metal is patterned by lift-off. The gate oxide, 1 nm Al_2O_3/5 nm HfO_2, is deposited by ALD at 100/300 °C after sulphur passivation. Devices are then annealed for several hours at 100 °C in an N_2 ambient. Gate metallization of evaporated Ni/Pd/Au by lift-off completes the process. Figure 1(a) shows a false-color scanning electron microscopy image, and Figures 1(b) and 1(c) show schematic images of the finished device.

Figures 2(a) and 2(b) show the T = 300 K transfer characteristics at $V_{DS} = 0.05$ and 0.5 V of two representative devices with $W_{NW} = 30$ and 60 nm, respectively. The current density is normalized to the gated circumference. The peak transconductance of the $W_{NW} = 30$ nm device is 2.5 mS/μm, and the minimum subthreshold slope (SS) is 70 mV/decade, both at $V_{DS} = 0.5$ V. For the $W_{NW} = 60$ nm device, SS = 90 mV/decade. An important metric for digital FET applications,

[a]Author to whom correspondence should be addressed. Electronic mail: cezar.zota@eit.lth.se

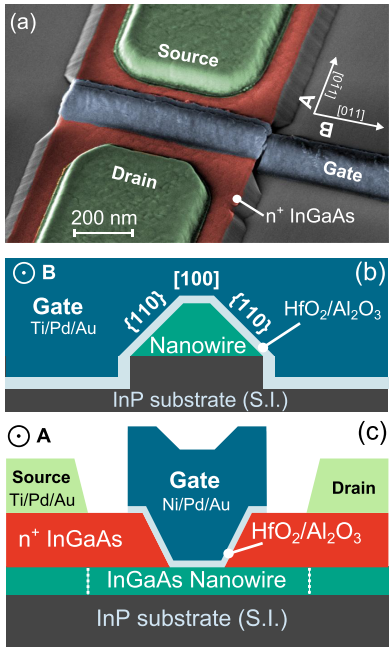

FIG. 1. (a) False-color SEM image of a fabricated device. (b) Cross-sectional schematic figure along the direction B, showing the NW facets, derived from facet angles and directions. (b) Schematic figure along direction A.

such as CMOS, is the on-current I_{ON} at a specific off-current I_{OFF} and a given voltage swing V_{DD}. I_{ON} is thus measured at $V_{DS} = V_{DD}$ and $V_{GS} = V_{GS,off} + V_{DD}$, where $V_{GS,off}$ is V_{GS} for which $I_{DS} = I_{OFF}$. For III–V FETs, $V_{DD} = 0.5$ V is typically intended. The $W_{NW} = 30$ nm device exhibits $I_{ON} = 430\ \mu A/\mu m$ at $I_{OFF} = 100$ nA/μm and $V_{DD} = 0.5$ V. This can be compared with the results described by, e.g., Kim *et al.* who reported $I_{ON} = 410\ \mu A/\mu m$ for tri-gated $In_{0.53}Ga_{0.47}As$ FETs.[19]

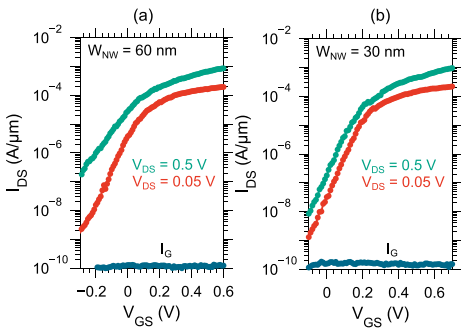

FIG. 2. Subthreshold characteristics of NWFETs with W_{NW} = (a) 60 nm and (b) 30 nm. I_G is the gate current leakage.

The minimum inverse subthreshold slope (SS) versus W_{NW} is shown in Figure 3(a) for 50 devices. Error bars show the standard deviation. $W_{NW} > 60$ nm devices exhibit degradation towards the limit of a planar FET using our technology, approximately 100 mV/decade. Below that, a significant improvement in SS is observed. The lowest observed SS at $V_{DS} = 0.5$ V is 64 mV/decade, i.e., near the limit of 60 mV/decade. A simple calculation of SS, extracted from a solution of Laplace's equation modeling the full 3D structure of the nanowire using COMSOL, is also shown. The SS is extracted from the potential variation at the center-bottom of the nanowire. The lower end of the experimentally determined values shows a good fit to the calculated values. The larger experimental SS is attributed to the effect of interface traps. The drain-induced barrier-lowering DIBL $= \Delta V_{GS}/\Delta V_{DS}$ measured at $I_{DS} = 1\ \mu A/\mu m$ follows a similar trend, 30 and 77 mV/V for the smallest and largest W_{NW}, respectively (Figure 3(b)).

The output conductance g_d, measured at $V_{GS} - V_T = 0.5$ V and $V_{DS} = 0.5$ V, is shown in Figure 3(c). A significant reduction is observed, from 0.35 mS/μm to 0.07 mS/μm, for the smallest W_{NW}. g_d is reduced not only by improved gate coupling but also by band gap widening through a reduction of impact ionization at the drain side.[20] These results show the effects of improved electrostatic coupling of the gate due to the 3D gate architecture. Figure 3(d) shows V_T, defined as V_{GS} at $I_{DS} = 100\ \mu A/\mu m$, versus W_{NW} at room-temperature. Dashed traces show an effective mass model of quantum confinement in a quantum well (QW) with the flat-band voltage used as a fitting parameter. The expected trend is observed, with larger V_T variability, $\Delta V_T = dV_T/dW_{NW}$, in narrow NWs. However, the same trend is expected as an artifact of increased

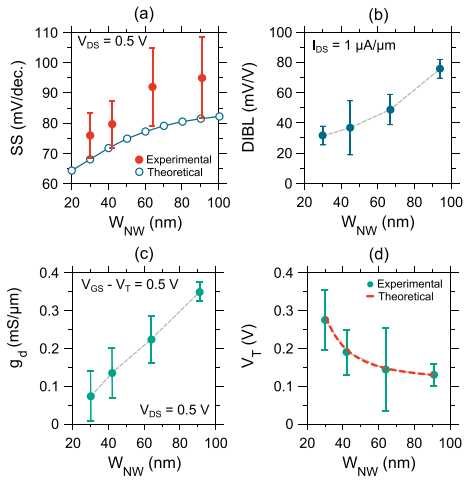

FIG. 3. (a) Drain-induced barrier-lowering versus W_{NW}, measured at $I_{DS} = 1\ \mu A/\mu m$. (b) Minimum subthreshold slope versus W_{NW}, measured at $V_{DS} = 0.5$ V. Empty markers show calculated SS, using COMSOL. (c) Output conductance versus W_{NW}, measured at $V_{GS} - V_T = 0.5$ V and $V_{DS} = 0.5$ V. (d) Threshold voltage versus W_{NW}, measured at $I_{DS} = 100\ \mu A/\mu m$ and $V_{DS} = 0.5$ V.

surface scattering. Next, we will show that this behavior is indeed due to bandgap widening.

A stability plot of the transconductance $g_m = dI_{DS}/dV_{GS}$ at $T_L = 11$ K is shown in Figure 4(a) for a device with $W_{NW} = 22$ nm ($dV_{DS} = 400\,\mu$V, $dV_{GS} = 6$ mV). The three diamonds of low transconductance are attributable to subband splitting. In the quantum capacitance limit ($C_{ox} \gg C_q$), the subband energy spacing, $\Delta_{n,n+1}$, is approximately determined from the difference between the horizontal corners of the diamonds, ΔV_{DS} (the difference between the left and the right corners of a diamond).[21,22] If $C_q \gg C_{ox}$, instead $\Delta_{n,n+1}$ is determined from the horizontal corners of the diamonds, rather than the difference between corners. Here, $C_{ox} > C_q$, therefore we assume the quantum capacitance limit. Assuming a 2DEG FET, this gives an error of approximately 25% (with $C_{ox} = 0.022$ F/m^2 and $C_q = 0.0155$ F/m^2). The gate leverage factor α, which relates to the oxide and quantum capacitance and the density of interface trap distribution of the device, can be determined from $\Delta V_{DS} = \alpha \Delta V_{GS}$, where ΔV_{GS} is the difference between the vertical corners of the diamonds (the difference in V_{GS} between the top and the bottom corners of a diamond). Qualitatively, $q\Delta V_{DS}$ represents the true subband energy separation, while ΔV_{GS} represents the required V_{GS} to shift the subbands by $q\Delta V_{DS}$, and α is the efficiency by which this occurs. Using this method, the subband energy spacings are $E_2 - E_1 = \Delta_{1,2} = 65 \pm 10$ meV and $\Delta_{2,3} = 85 \pm 10$ meV, and $\alpha = 0.4 \pm 0.1$. The error margins, estimated by the authors, are due to the uncertainty of determining the exact edge of the diamonds. The energy spacings extracted in this way are slightly overestimated due to omission of bias-channel charge self-consistency. Moreover, the obtained value of α is an approximation, since we assume constant quantum capacitance (implicit in α), which is not true above V_T. Figures 4(b)–4(d) show the conductance $g_d = \delta I_{DS}/\delta V_{DS}$ determined through successive I_{DS}/V_{DS} sweeps in DC biasing mode for $W_{NW} = 18$, 22, and 80 nm, respectively. The $W_{NW} = 18$ nm device shows two steps, $0.7G_0$ and $1.4G_0$, where G_0 is the quantum conductance $2e^2/h$. The mean free path λ is calculated from $\lambda/(L_g + \lambda) = T$, where the transmission T is obtained from T^*G_0 at each subband. $\lambda = 160$ nm is obtained for this device, which is similar to other reported values.[23] For $W_{NW} = 22$ nm (which corresponds to Figure 4(a)), three subbands are observed with average $T = 0.67$ and $\lambda = 140$ nm. The source and drain series resistances in these devices have been estimated by transmission line measurements and COMSOL simulations, and are 150 Ω, which is negligible compared to the total on-resistance.[13] We do not observe degenerate subbands, as has been reported for NWs with symmetric cross-sections.[11] The oscillations at the plateaus may be attributable to Fabry-Pérot interference or interface roughness scattering.[24,25] The $W_{NW} = 80$ nm device shows up to 9 subbands, denoted by the horizontal dashed traces, with $6.5G_0$ total conductance. The average subband transmission is $T = 0.72$ which gives $\lambda = 180$ nm.[26] Interestingly, there is no distinct trend of λ versus W_{NW}, the former which is expected to be reduced in scaled NWs due to increased surface scattering, as has been observed elsewhere.[27] This can be explained in part by excellent surface quality, in part by that H_{NW} is limiting surface scattering.

Fig. 4(e) shows V_T determined both from fixed I_{DS} ($100\,\mu$A/μm) at room temperature, and as the V_{GS} of the first quantized subband at $T = 11$ K (measured at half the step), for the same group of devices. Dashed traces show the

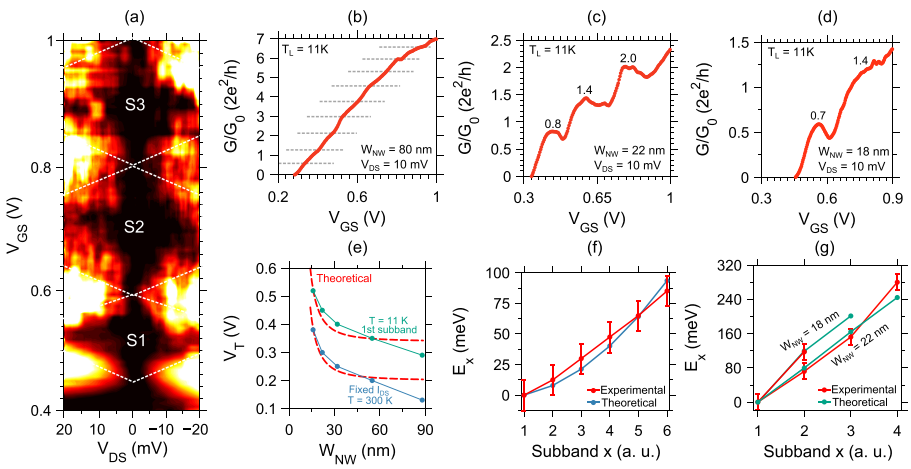

FIG. 4. Measurements at $T_L = 11$ K. The conductance $G = dI_{DS}/dV_{DS}$ and transconductance $G_m = dI_{DS}/dV_{GS}$ were determined as the approximate derivative of a set of I_{DS}-V_{DS} measurements with V_{GS} and V_{DS} steps of $100\,\mu$V. (a) Stability diagram of the transconductance for a device with $W_{NW} = 22$ nm. The color range indicates 1.5 to 12.5 mS with black corresponding to $g_m < 1.5$mS. (b) Quantum conductance G/G_0, where $G_0 = 2e^2/h$, for devices with $W_{NW} = 80$ nm, (c) 22 nm and (d) 18 nm. (e) Comparison of the threshold voltage defined both as the V_{GS} of the first subband at $T = 11$ K and at s fixed $I_{DS} = 100\,\mu$A/μm at room-temperature. Dashed traces show the first subband in the QW model. (f) Comparison of the xth subband energy level E_x in a $W_{NW} = 80$ nm device between measured data and a QW model. E_1 is set to 0 meV. Error bars show a 50 meV error due to uncertainty in defining the sub-band. (g) A similar comparison for $W_{NW} = 18$ and 22 nm devices.

energy of the first subband in an effective mass 2D quantum well model with infinite barriers (QWM), which fit well to the measured data. Since V_T defined from the subband edge in this manner is equivalent to the conduction band energy qE_C, these results are an experimental confirmation of band gap widening in narrow NWs.[28] The two methods of determining V_T yield very similar results except for a constant shift, which is mainly attributable to the arbitrary I_{DS} level chosen to extract V_T at room-temperature. The ΔV_T at $W_{NW} = 20$ nm is 13, 11, and 11 mV/nm for the fixed-I_{DS}, sub-band, and calculated QW method, respectively. This directly shows that the V_T shift for scaled NWs is due to 2D quantum confinement. Following the stronger bandgap widening of low effective mass materials, ΔV_T will be more severe in such devices. For instance, using our model, $In_{0.53}Ga_{0.47}As$ ($m^* = 0.041$) exhibits $\Delta V_T = 6.8$ mV/nm at $W_{NW} = 20$ nm. Through the choice of m*, thus there exists a trade-off between variability, i.e., ΔV_T, and I_{ON} (through λ) in future implementations of III–V CMOS.

We compare the observed subband energy levels with those from the QWM. The measured $V_{GS,n}$ for each subband is compared with the calculated $V'_{GS,n}$ using $qV'_{GS,n}/\alpha = qV_{FB} + E_n$, where V_{FB} is the flat-band voltage and E_n is the energy obtained from the QWM. V_{FB} is used as a fitting parameter. For the calculations, we use a rectangular cross-section, with the same cross-sectional area as the corresponding measured device. Figures 4(f) and 4(g) show the comparison between measured and theoretical values. Energy levels are relative to that of the lowest subband in each device. The experimental energy levels are measured at half the step height. Error bars show a 50 meV measurement error in estimating the V_{GS} of each level. The $W_{NW} = 18$ and 22 nm devices show excellent fit with $\alpha = 0.4$. The $W_{NW} = 80$ nm device shows a good fit with $\alpha = 0.25$. The difference in α can be correlated with, e.g., the measured SS of these devices, 69, 72, and 105 mV/decade for 18, 22, and 80 nm at $V_{DS} = 0.5$ V. The low SS of these devices implies that they are not operating near the quantum capacitance limit.

In conclusion, we have examined the effects of NW dimensions on room-temperature and low-temperature properties of InGaAs MOSFETs. Significant improvements in electrostatic-dependent performance metrics were observed in scaled down NWs. At low-temperature, quantized conductance due to subband splitting was observed. A mean free path of 160 ± 20 nm, which was dimension-independent in the examined range, was determined. The subband splitting was modeled accurately by an effective mass quantum well model. Finally, V_T at room-temperature was compared to that determined from the energy of the lowest subband at low-temperature. Excellent agreement was observed, which experimentally shows that subband splitting causes increased V_T and V_T variability in scaled NWs.

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Paper XI

Paper XI

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A Method for Determining Trap Distributions of Specific Channel Surfaces in InGaAs Tri-gate MOSFETs

Seiko Netsu, Markus Hellenbrand, Cezar B. Zota, Yasuyuki Miyamoto, and Erik Lind

***Abstract*— We present a method for estimating the trap distributions on each of the surfaces in a multi-gate MOSFET. We perform *I-V* hysteresis measurements on InGaAs Tri-gate MOSFETs with various channel widths (25, 60 and 100 nm) from which top surface and side wall trap distributions are determined. We show that the total trap distribution of a device can be expressed as a linear combination of the top surface and side wall trap distributions. The results show that the minimum trap density of the top InGaAs (100) surface is smaller than that of the {110} side walls by almost an order of magnitude. Since the nanowire constituting the channel in these devices is selectively regrown, rather than etched out, the different trap distributions can be explained by the specific surface chemistries of two surfaces.**

***Index Terms* - MOSFETs, high-*κ*, InGaAs, hysteresis, trap density, inter face trap, III-V, Multi-gate, FinFETs**

I. Introduction

III-V compound semiconductors such as InGaAs have been widely investigated as a promising n-type MOSFET channel material for future CMOS technology because of their higher electron mobility [1][2], which enables higher transconductance g_m and on-current at a given gate length. Although poor quality high-κ gate stacks have been considered as a crucial issue for realizing the use of III-V based MOSFETs in industry, several research groups have recently reported on $In_xGa_{1-x}As$ MOSFETs with g_m of about 3 mS/μm while achieving an acceptable high-κ gate stack quality with respect to the interface trap density [3][4][5]. Further improvement of the performance of III-V-based MOSFETs, the device reliability, for example Positive Bias Temperature Instability (PBTI) is another key research area for III-V based MOSFET [6]. Understanding the relative energies of the trap distribution in the high-κ oxide and charge carriers in the channel is a vital aspect of improving the device reliability and performance. However, in the case of multi-gate MOSFETs such as FinFETs, tri-gates, gate-all-around (GAA) and vertical nanowire (VNW) structures, it is difficult to determine the trap distributions separately for each of the channel surfaces. The trap distributions for each surface type can be assumed to be different due to surface chemistry and process-related roughness. In recent years, a simple trap evaluation method based on the hysteresis of *C-V* or *I-V* characteristics of MOSFETs has been proposed [7]. Even though this method is not suitable for estimating the trap distributions of different surface orientations separately, it is useful in investigating the total MOSFET gate stack properties.

In this paper, we propose a novel method for estimating the trap distributions of tri-gate MOSFET channel top surfaces [$N_{eff,\ top\ surface}\ (E)$] and side walls [$N_{eff,\ side\ wall}\ (E)$] based on the *I-V* hysteresis dependence of the ratio between top surface and side wall length of the channel. We investigate the *I-V* hysteresis of devices with channel widths of 25 to 100 nm. From the hysteresis data, the total trap distributions are estimated, then the trap distributions of the top (100) surface and the {110} side walls are separated. This method allows characterization of specific channel surfaces in MOSFETs without the need to fabricate several MOSCAPs, and offers a new way of identifying optimal channel surfaces.

II. DUT & Hysteresis Measurement

Fig. 1(a) shows a representative cross-sectional SEM image of nanowires used as the channel in these devices. These nanowires are taller than those used in the devices in order to clearly show the facet angles. The {110} surface planes are determined from the orientation of the nanowire and the 45 sidewall angle. Fig. 1 (b) shows a schematic image and the final dimensions of a nanowire used in the Tri-gate FETs evaluated in this work. The height of the channel is 7 nm, giving 10 nm total length for each of the {110} side walls. The gate length L_g, is 150 nm, and the device channel consists of a single nanowire. A 1+4 nm /Al_2O_3 / HfO_2 bilayer gate stack was used in these devices. Further details about device fabrication process and performance are shown in [5] and [8].

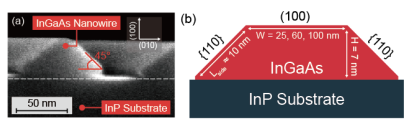

Fig. 1. (a) Cross-sectional SEM image of the FinFET channel. The surface orientations are (100) and <110> for the top and the side, respectively. (b) Schematic image of the channel structure evaluated in this paper.

We measured *I-V* hysteresis for devices with channel widths of 25, 60 and 100 nm, respectively. The measurements were carried out by sweeping the gate voltage from a starting voltage (V_{start}) to an end voltage (V_{end}), and then back to V_{start}. Each measurement was done on the same device unlike Ref. [7] In

S. Netsu and Y. Miyamoto are with the Department of Physical Electronics, Tokyo Institute of Technology, 152-8550, Tokyo, Japan (seikou.n.aa@m.titech.ac.jp).
M. Hellenbrand, C. Zota and E. Lind are with the Department of Electrical and Information Technology, Lund University, 221 00 Lund, Sweden.

order to reduce the effect of residual hysteresis from previous measurement, we started our measurement with small V_{end}, and then gradually increased V_{end}. Furthermore, at least one minute interval was taken until next measurement for the same reason. Hold time of each measurement point was 20 ms with each sweep consisting of 2000 points. We set $V_{start} = V_{th}$, and V_{th} of the measured devices was about ~~0.2V~~ *200 mV*. V_{end} varied as a parameter in the measurement. For each V_{end} the maximum hysteresis voltage was extracted. The effective trapped charge ΔN_{eff} is proportional to the hysteresis voltage $\Delta V_{hysteresis} = q\Delta N_{eff}/C_{ox}$ as described in [9]. Note that the average and standard deviation of V_{th} of each channel width devices, $\overline{V_{th}}$ and σ_{Vth}, are as follows; 1) W = 100 nm device: $\overline{V_{th}}$= 200 mV and σ_{Vth} = 30 mV. 2) W = 25 nm device: $\overline{V_{th}}$ = 200.5 mV and σ_{Vth} = 25 mV. Based on these small variation of V_{th}, we conclude that can set V_{start} as a fixed V_{th} = 200 mV.

III. Method For Separation of Trap Distributions From I-V Hysteresis Measurement

Next we show how to estimate the trap distribution of the top (100) surface and the {110} side walls from the *I-V* hysteresis data. The procedure is divided into two steps: 1) Estimation of 25 nm and 100 nm channel width device total trap distribution ($N_{eff,\ W=25\ nm}$ *(E)* and $N_{eff,\ W=100\ nm}$ *(E)*. 2) Estimation of the trap distribution of top surface and side wall from the results of 1).

First, the trap distributions of $N_{eff,\ W=25\ nm}$ *(E)* and $N_{eff,\ W=100\ nm}$ *(E)* were derived. Since ΔN_{eff} at each V_{end} is already known from the experimental result of $\Delta V_{hysteresis}$ *(*V_{ov}*)*, N_{eff} *(E)* can be derived by using equation (1) and (2).

$$\Delta N_{eff} = \int_{\varphi_{start}}^{\varphi_{end}} N_{eff}(E)dE \tag{1}$$

$$N_{eff}(E|N_{peak}, \mu_1, \mu_2, \sigma_1, \sigma_2) = N_{peak}\left(\frac{1}{\sigma_1\sqrt{2\pi}}\exp\left(\frac{-(E-\mu_1)^2}{2\sigma_1^2}\right) + \frac{1}{\sigma_2\sqrt{2\pi}}\exp\left(\frac{-(E-\mu_2)^2}{2\sigma_2^2}\right)\right) \tag{2}$$

where φ_{start} and φ_{end} are the surface potentials which correspond to V_{start} and V_{end}, respectively. The reference potential φ_{start} = 0 V was fixed to the threshold voltage. The surface potential for different surface orientation was assumed to be same, based on the fact that although the area ratio of (100) to {110} is different between channel width of 100 nm and 25 nm devices, there was no significant change in the V_{th}. Two Gaussian distributions were assumed for expressing N_{eff} *(E|*N_{peak}*,* μ_1*,* μ_2*,* σ_1*,* σ_2*)* in the same manner as in [7][10]; N_{peak} is the peak value of the trap distribution, μ its mean value and σ^2 its variance. Since the trap distribution has several sources, such as e.g. dangling bonds, vacancies and defects in the oxide [10], the two Gaussian distributions differ. N_{eff}, μ and σ^2 are fitting parameters in reproducing the measured $\Delta V_{hysteresis}$–V_{ov} relationship. In the simulation, we modeled the gate stack capacitance as the series combination of the oxide capacitance C_{ox} and the quantum capacitance C_q [11]. In order to consider the effects of traps, a trap capacitance C_{Neff} was connected to C_q in parallel. The surface potential and defect charge was subsequently calculated self consistently. Note that a change of quantized energy level due to band bending was neglected in this calculation.

In order to derive $N_{eff,\ top\ surface}$ *(E)* and $N_{eff,\ side\ wall}$ *(E)*, we assumed that $N_{eff,\ W=25\ nm}$ *(E)* and $N_{eff,\ W=100\ nm}$ *(E)* can be expressed as a linear combination of $N_{eff,\ top\ surface}$ *(E)* and $N_{eff,\ side\ wall}$ *(E)*. In the case of the height of the trap distribution, a linear combination of $N_{eff,\ top\ surface}$ and $N_{eff,\ side\ wall}$ gives $N_{eff,\ W=25\ nm}$ with appropriate coupling constants. Coupling constants are decided based on the ratio of top surface length (channel width) and total side wall length. The mean value μ and the variance σ^2 can be expressed in the same manner.

From the distributions $N_{eff,top\ surface}$*(E)* and $N_{eff,side\ wall}$*(E)* extracted from 25 nm and 100 nm devices, we then predicted the distribution $N_{eff,W=60nm}$ *(E)* for 60 nm devices. Comparing these predictions with the measured results of such a device provides a (self-consistent) means to verify the extracted distributions for different surface orientations.

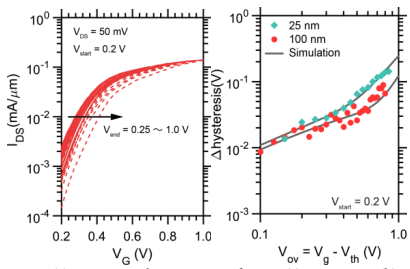

Fig. 2. (a) Hysteresis characteristics of W = 100 nm FinFET (b) Measured hysteresis data for different channel widths (W = 25 nm and 100nm) against simulation data (solid line).

TABLE I
PARAMETERS OF TRAP DISTRIBUTIONS

Channel width		Surface	
100 nm	μ_1 = 1.025, μ_2 = -0.975 σ_1 = 0.18, σ_2 = 0.5 N_{peak} = 8.0×10^{13}	Top surface (100)	μ_1 = 0.875 , μ_2 = -1.155 σ_1 = 0.167 , σ_2 = 0.514 N_{peak} = 5.3×10^{13}
25 nm	μ_1 = 0.975, μ_2 = -0.975 σ_1 = 0.2 , σ_2 = 0.475 N_{peak} = 12.5×10^{13}	Side Wall {110}	μ_1 = 0.645, μ_2 = -1.20 σ_1 = 0.235 , σ_2 = 0.420 N_{peak} = 21.6×10^{13}

IV. Results and Discussion

The *I-V* measurement of a 100 nm channel width tri-gate FET for different V_{end} is shown Fig. 2. The *I-V* hysteresis increases as V_{end} increases, indicating an increase also in the number of trapped charges.

Fig. 2 (b) displays the dependence of V_{end} on $\Delta V_{hysteresis}$ for channel widths of 25 and 100 nm. Solid lines were derived from best fits to the experimental data. The parameters used in this fitting are shown in Table. 1. As can be seen, the 25 nm device shows larger hysteresis than the 100 nm device over the entire range, suggesting the existence of a larger number of traps in the former. This was particularly noticeable in the ranges of higher over-drive voltages (V_{ov} ~ 0.7) where the Fermi-level crosses the steepest part of the trap distribution.

Fig. 3 (a) shows the trap distributions for 25 nm and 100 nm channel width devices, obtained by the fitting shown in Fig. 3

(a). As expected from the hysteresis, 25 nm channel width gate stacks contains higher trap densities. Fig. 3 (a) also includes the

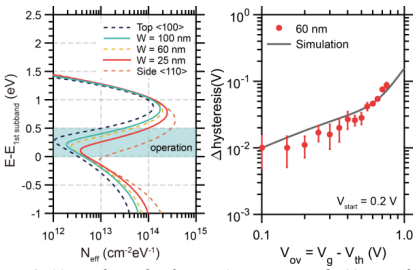

Fig. 3. (a) Fitted trap distributions (W = 25 nm and 100 nm, solid line), separated trap distributions (top-well and side-well, dashed line) and predicted trap distribution (W = 60 nm) (b) Experimental hysteresis data plot of W = 60 nm device. Solid line was predicted by using obtained top surface and side wall trap distributions.

trap distributions of the top surface and the side wall. The {110} side wall trap distribution is almost one order of magnitude higher than for the (100) top surface with respect to the minimum trap density. This tendency agreed with the previous results from high-κ/InAs gate stacks [12]. Since the channel width of 25 nm device has more area of side wall than top surface relatively in comparison with that of 100 nm device, the side wall properties have a great influence on its total properties, causing a higher trap density as shown in Fig. 3 (a).

The predicted hysteresis (solid line) of a 60 nm device and its measured hysteresis are shown in Fig.3 (b). Predicted hysteresis agrees well with measured data, giving validity to our assumption that the hysteresis is explained by a linear combination of the trap distributions of the top and side wall surfaces.

We also confirmed that our linear combination assumption was still valid when we changed V_{start} to V_{th}-0.2V. However, some limitations are worth noting; the extracted parameters of the trap distribution differed slightly from Table.1. due to the different charge state of the gate stack caused by the difference in V_{start}. Future work should therefore take into account this phenomena such that uniform trap distribution can be derived.

V. Conclusion

We have demonstrated a method for the evaluation of the trap energy distribution on different channel surfaces of InGaAs tri-gate MOSFETs. This method is based on a linear combination of the individual channel surface properties. Experimental observations confirmed the validity of this model. We derived the trap distributions of channel widths of 25, 60, 100 nm devices, respectively, from their I-V hysteresis and successfully modelled different distributions for different surface orientations. We showed that the minimum trap density of the (100) surface was approximately an order of magnitude smaller than that of the {110} surface, which agrees well with past studies [12].

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Paper XII

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C. Möhle, C. B. Zota, M. Hellenbrand and E. Lind, "1/f and RTS Noise in InGaAs Nanowire MOSFETs," *Microelectronics Journal*, accepted for publication, 2017.

1/*f* and RTS Noise in InGaAs Nanowire MOSFETs

C. Möhle[1], C. Zota[1], M. Hellenbrand[1], E. Lind[1]
[1]*Department of Electrical and Information Technology, Lund University, 22100 Lund, Sweden*
E-mail address of the corresponding author: erik.lind@eit.lth.se

***Abstract*—Low-frequency noise measurements were performed on high-performance InGaAs nanowire MOSFETs. 1/f noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. The minimum equivalent input gate voltage noise reported here is 80 $\mu m^2 \mu V^2/Hz$, among the lowest values for III-V FETs, and showing the feasibility of a high-quality, low trap density, high-k gate oxide on InGaAs.**

***Keywords*—InGaAs, MOSFETs, Nanowires, 1/f noise, RTS noise, Elastic tunneling**

1. Introduction

Due to their high electron mobility, III-V materials, such as InGaAs, are attractive as a channel material in high-performance field-effect transistors (FETs). Utilizing nanowires (NWs) as the channel in such devices offers improved electrostatic control and enables the use of highly scaled gate lengths [1]. However, due to the lack of a native oxide, the trap density in III-V FETs is typically high (compared with Si/SiO_2 devices), which can degrade the transistor performance and reliability significantly [2]. Thus, accurate and reliable measurements of the interface and oxide quality of III-V FETs are required for the device characterization and the process optimization. Conventional oxide characterization methods, such as C-V and charge pumping methods, cannot be used for ultra small devices without a body contact. Instead, low-frequency (LF) noise measurements can be utilized to analyze the performance and reliability of highly scaled devices [3].

In this paper, we present a low-frequency (LF) noise study (1/*f* as well as RTS noise) on high-performance InGaAs NW MOSFETs [4]. 1/*f* noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. Furthermore, a low equivalent input gate voltage noise of 80 $\mu m^2 \mu V^2/Hz$ is achieved, showing the feasibility of a high-quality gate oxide on InGaAs.

2. Device Fabrication

The $In_{0.85}Ga_{0.15}As$ NWs are formed on semi-insulating InP:Fe by selective area MOCVD growth using HSQ as a growth mask [5]. Each device consists of a single nanowire. Highly doped ($N_D \sim 5 \cdot 10^{19}$ cm^{-3}) InGaAs source/drain contacts are formed in a second growth step using an HSQ dummy gate (figure 1). Ti/Pd/Au source/drain metal is deposited by thermal evaporation. After surface precleaning by Ozone, $(NH_4)_2S$ (10%) for 20 min, and five cycles of in situ TMA1 pulses, Al_2O_3/HfO_2 (5/45 cycles, EOT ≈ 1.2 nm) is deposited as the gate oxide by ALD at 300/100 °C. Ni/Pd/Au gate metallization by thermal evaporation completes the process. A schematic of a fabricated device is depicted in figure 2. Details on the device fabrication can be found in [6].

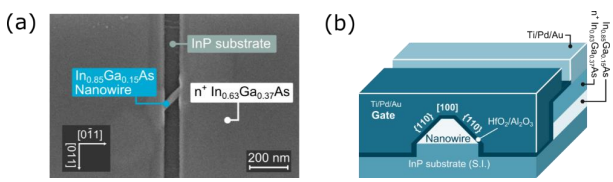

Fig.1: (a) SEM image (top view) after the nanowire growth. (b) Schematic figure of a fabricated device.

3. Methods and Results

Excellent DC performance was reported for these devices previously, with a peak transconductance of 2.9 mS/µm, a minimum subthreshold slope of 77 mV/decade and an on-current of 565 µA/µm (at I_{off} = 100 nA/µm), all at V_{ds}= 0.5 V, the highest reported on-current for any transistor [6]. Furthermore, it was shown that these transistors operate in the quasi-ballistic regime with a transmission of about 70 %, which was obtained from quantized conductance measurements at 10 K, and was shown to be valid also at room temperature [5].

Here, we performed 1/*f* and RTS noise measurements on devices with varying gate lengths (L_g = 50-85 nm) and gate widths (W = 27–100 nm). *W* refers to the gated perimeter of the nanowire.

For both types of measurements, a Lake Shore Cryotronics CRX-4K probe station was used to contact the transistors and to control the temperature. When performing the 1/*f* noise measurements, a low-noise current preamplifier (model SR570 from Stanford Research Systems) was utilized to supply a constant drain voltage of 50 mV and to amplify the drain current signal. The output of the current preamplifier was connected to a lock-in amplifier (model SR830 from Stanford Research Systems) to measure the drain current noise (S_{Id}). A Keysight B2912A source measure unit (SMU) was used to set the gate voltages and to monitor the source current during the measurements.

For the RTS noise measurements, only the Keysight B2912A SMU was utilized to set the drain and gate voltages and to measure the drain current.

The 1/*f* noise measurements show that the normalized drain current noise (S_{Id}/I_d^2) is inversely proportional to the gate area $A = L_g W$ (at a fixed drain current), indicating that the LF noise originates from the channel rather than from the source/drain resistance (figure 2 (a)). If the LF noise had arisen from the source/drain resistance instead, S_{Id}/I_d^2 would have been be independent of *A*.

In contrast to a previous study on highly scaled InGaAs GAA MOSFETs [3], our measurements show that number fluctuations (rather than mobility fluctuations) are the dominant LF noise source, as the normalized drain current

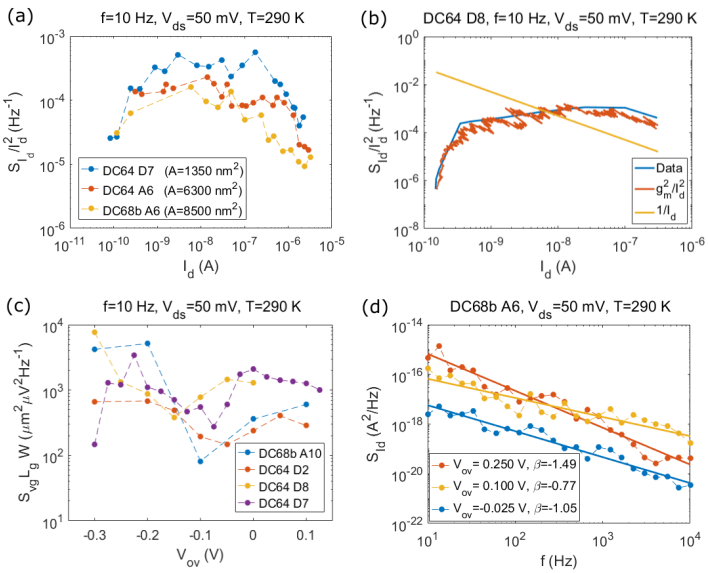

Fig.2: (a) Impact of the gate area scaling on the normalized drain current noise, showing that the LF noise originates from the channel. (b) The normalized drain current noise follows the transconductance in all devices, indicating that number fluctuations are the dominant noise mechanism. (c) Low values for the equivalent input gate voltage noise over a large gate voltage overdrive range for device DC68b A10 (L_g = 70 nm, W = 78 nm), DC64 D2 (L_g = 50 nm, W = 27 nm), DC64 D8 (L_g = 50 nm, W = 27 nm) and DC64 D7 (L_g = 50 nm, W = 27 nm). (d) Gate voltage dependence on the f^{β} noise exponent (β) for transistor DC68b A6 (L_g = 85 nm, W = 100 nm).

noise follows g_m^2/I_d^2 (instead of $1/I_d$) in all our devices. This observation is exemplified in figure 2 (b) for a single transistor with L_g = 50 nm and W = 27 nm, but is valid for all transistors (independent of L_g and W) and is here reported for quasi-ballistic devices.

As shown in figure 2 (c), we observe low values for the equivalent input gate voltage noise ($S_{VG} = S_{Id}/g_m^2$) over a large gate voltage overdrive ($V_{ov} = V_{gs}$-V_T) range with minimum values of 80 µm^{2}µV^2/Hz, demonstrating an excellent oxide quality in our devices. The corresponding trap density can be calculated by using [7]

$$N_t = \frac{fWL_G C_{ox}^2 S_{VG}}{q^2 k_B T \lambda} \text{ [cm}^{-3}\text{eV}^{-1}\text{]}. \quad (1)$$

In equation (1), C_{ox} is the oxide capacitance per unit area and λ is the tunneling attenuation length in the gate oxide, given by $\lambda = \left(\frac{4\pi}{h}\sqrt{2m^*\Phi_B}\right)^{-1}$ [7]. Assuming an effective electron mass of $m^* = 0.23\, m_e$ [8] in Al_2O_3 and an oxide barrier height of $\Phi_B = 2.4$ eV [9], the trap density is as low as ~ 9·10^{18} cm^{-3}eV^{-1}. This correlates with the low minimum subthreshold slope of 77 mV/decade in these devices.

Furthermore, a gate voltage dependence on the f^{β} noise exponent (β) is observed, which can be attributed to a spatially non-uniform trap distribution in the gate oxide (depicted in figure 2 (d) for a transistor with L_g = 85 nm and W = 100 nm). If the trap density close to the gate oxide/channel interface is higher (lower) than that in the interior of the gate oxide, β is larger (smaller) than -1. For a trap density that is uniform in depth, β = -1 [7]. In all our devices, β typically varies between -0.7 and -1.5 when sweeping the gate voltage overdrive from -0.2 V to 0.3 V. This clear gate voltage dependence on β indicates that relatively few traps limit the performance of the devices; otherwise the trap density would be more uniform in depth leading to β = -1 independent of the gate voltage (assuming there are no spatial preferences for the trap formations in the gate oxide).

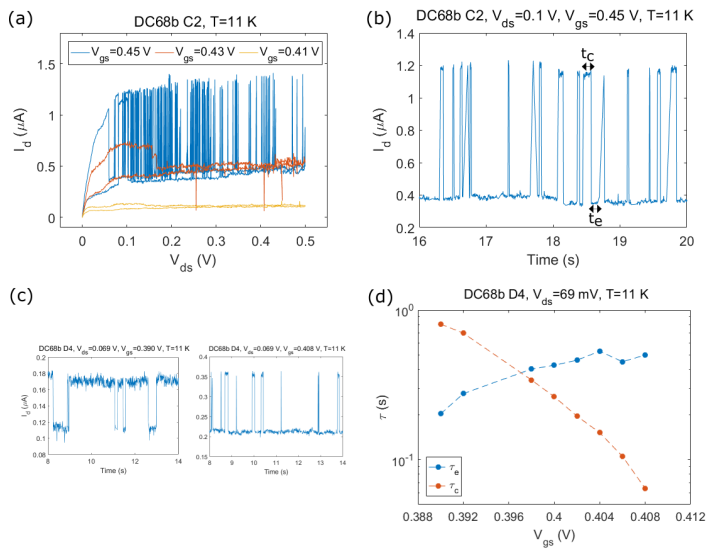

Fig.3: (a) Output characteristic for transistor DC68b C2 (L_g = 55 nm, W=32 nm) showing large drain current fluctuations. (b) Excerpt of the measured RTS noise signal at V_{ds}=0.1 V and V_{gs}=0.45 V (c) Excerpt of an RTS noise signal for transistor DC68b D4 (L_g = 70 nm, W=31 nm) at V_{ds}=0.069 V (fixed) and V_{gs}=0.39 V (left) and V_{gs}=0.408 V (right). (d) Variation of the capture and emission time constant with gate voltage for the same defect as in (c).

To study the impact of single trap states, we also performed low temperature RTS noise measurements. RTS noise signals were observed in ~2/3 of our devices.

In a small number of transistors, we found RTS noise with a large drain current amplitude (ΔI_D) of up to 1 µA. Figure 3 (a) shows the output characteristic of such a device and in figure 3 (b), an excerpt of the drain current signal is shown over time for V_{ds} = 0.1 V and V_{gs} = 0.45 V. At this bias point, the drain current amplitude is ~ 0.8 µA (relative drain current amplitude $\Delta I_D/I_D = 67$ %) and the characteristic capture and emission time constants (τ_c and τ_e, respectively) are: $\tau_c = 0.046$ s and $\tau_e = 0.267$ s. The different values of the time constants can be qualitatively explained by the position of the trap energy level relative to the semiconductor Fermi level. In this case, the trap energy level is located below the Fermi level, meaning that a large number of electrons have enough energy to tunnel elastically into the trap state, giving rise to a small τ_c. However, tunneling out of the trap state requires an empty state at the same energy level in the semiconductor, which is hindered when the trap energy level is located below the semiconductor Fermi level. This leads to a higher τ_e.

Figure 3 (c) and (d) show the impact of the gate voltage on the capture and emission time constant of a single defect in another device. τ_c and τ_e, vary with the gate voltage since the trap energy level is shifted relative to the semiconductor Fermi level. τ_c decreases with increasing gate voltage while the opposite trend is observed for τ_e. At the bias point, where $\tau_c = \tau_e \approx 0.38$ s, the trap energy level is aligned with the Fermi level and the trap depth in the oxide can be estimated using [7]:

$$z_t = \lambda \ln\left(\frac{\tau}{\tau_0}\right), \quad (2)$$

with τ_0 being the tunneling time constant for a trap state at the semiconductor/oxide interface. Assuming $\tau_0 = 10^{-10}$ [7], the trap depth is ~ 2.9 nm. The calculation of z_t bases on elastic tunneling of electrons to and from the trap state; possible effects of a quantized inversion layer were not considered.

Modeling of single trap induced subband fluctuations yields an RTS noise drain current amplitude between 0.05 to 0.7 µA for traps at a depth of around 2.9 nm, depending on the exact lateral position of the trap along the channel. These numbers are in good agreement with the measured RTS noise amplitudes, as shown in figure 3 (a)-(c).

4. Conclusion

In summary, we performed LF noise measurements on high-performance InGaAs NW MOSFETs, demonstrating number fluctuations as the dominant LF noise source and low values of 80 $\mu m^2 \mu V^2/Hz$ for the equivalent input gate voltage noise, showing the feasibility of a high-quality gate oxide on InGaAs.

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