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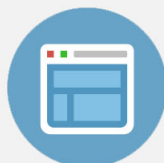
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## Surface and core contribution to $1/f$ -noise in InAs nanowire metal-oxide-semiconductor field-effect transistors

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By measuring  $1/f$ -noise in wrap-gated InAs nanowire metal-oxide-semiconductor field-effect transistors with transport dominating, controllably, in either an inner, core channel, or an outer, surface channel, it is possible to accurately evaluate the material quality related Hooge-parameter,  $\alpha_H$ , with reduced interference from the surface properties. The devices show low values of  $\alpha_H \sim 4 \times 10^{-5}$ . At forward bias, where the data suggest that the  $1/f$ -noise is dominated by the contribution from the high- $k$  interface, devices show low values of normalized noise spectral density. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4813850>]

The properties of III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) are continuously being improved and, in particular, nanowire (NW) devices are attractive due to their increased electrostatic control.<sup>1–4</sup> One area that needs further understanding is low-frequency-noise (LFN) that can provide vital information on both materials and interfaces.<sup>5</sup> The integration of high- $k$  oxides with the subsequent increase of dielectric permittivity in MOSFETs has enabled continued device scaling with reduced problematic leakage currents due to tunneling. There are, however, difficulties in realizing high quality high- $k$  dielectric films and interfaces on III-V semiconductors, and traps located in the oxide will generate fluctuations in the number of active channel carriers due to generation-recombination processes another contributing source for LFN is fluctuations in carrier mobility. From measurements of mobility fluctuations, a material specific quality measure parameter, the Hooge-parameter,  $\alpha_H$ , can be determined.

In this paper, we present a study of NW devices with the unique property of dual channel conduction. By measuring the  $1/f$ -noise in different regions of operation, where the drain current,  $I_{DS}$ , is dominated by either an inner (core) or by an outer (surface) channel, it possible to separate number fluctuations and mobility fluctuations and hence accurately evaluate the noise contributions stemming from the grown InAs NW material and the interface towards the applied high- $k$  film. Our data show low values for  $1/f$ -noise related to both interface and material.

45-nm-diameter InAs NW MOSFET devices are fabricated on a high-resistivity Si-substrate that is overgrown with a 300-nm-thick InAs contact layer.<sup>6</sup> The InAs layer promotes the nucleation and growth of NWs. The NWs are positioned with electron beam lithography, where placement of gold-discs that assembles the material is accomplished through a lift-off process. The growth is performed at 420 °C having a constant dopant flow of Sn with a molar fraction of  $1.07 \times 10^{-7}$ , corresponding to an estimated<sup>7</sup> doping concentration of  $N_D \sim 1 \times 10^{18} \text{ cm}^{-3}$ . After growth, the NWs are covered with a high- $k$  film consisting of 0.5 nm  $\text{Al}_2\text{O}_3$  deposited at 250 °C and

6.5 nm of  $\text{HfO}_2$  deposited at 100 °C, with the use of atomic layer deposition (ALD). From measurements of planar films, the relative permittivity is estimated to be  $\epsilon_r \sim 15$ . Device isolation is achieved by etching mesa structures from the InAs layer. The different fabricated electrical contacts to the NWs are separated with an inorganic spacer between the InAs mesa and the gate-metal, and an organic spacer between the gate-metal and top-metal, as shown in Fig. 1(a). The first separation layer is made with a 60-nm-thick  $\text{Si}_3\text{N}_4$  film deposited with plasma-enhanced chemical-vapor-deposition. A dry-etch procedure where an etched down resist covers the planar film is used to selectively remove the nitride from the sides of the nanowires. Gate formation is made with sputtering of W-metal and a partial removal process, where a socket is formed. The total gate length is given by the thickness of the sputtered metal (60 nm) plus the segment length of the socket, with a total gate length  $L_G \geq 200 \text{ nm}$ . The width of a device,  $W_G$ , is set by the NW circumference. The second separation layer is fabricated with a spin-on-resist, which is etched down to a thickness of

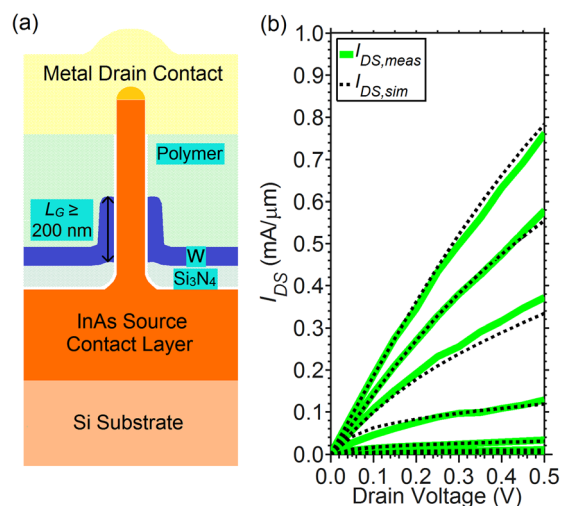


FIG. 1. (a) Schematic illustration of an InAs NW MOSFET showing the different contacts and separation layers. (b) Output characteristics for an InAs NW MOSFET with measured data,  $I_{DS,meas}$ , and simulated data,  $I_{DS,sim}$ , normalized to the nanowire circumference for  $V_{GS} = -0.5$ – $1.0 \text{ V}$ .

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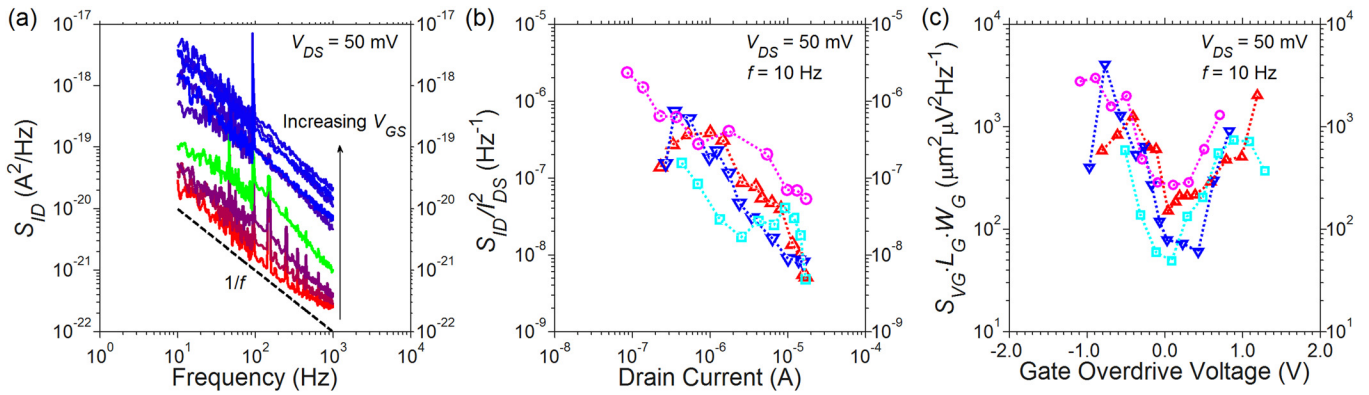


FIG. 2. (a)  $S_{ID}$  plotted versus frequency,  $f$ , for an InAs MOSFET with increasing  $V_{GS}$ . (b)  $S_{ID}/I_{DS}^2$  plotted versus  $I_{DS}$  and (c)  $S_{VG} \cdot L_G \cdot W_G$  plotted versus  $V_{OD}$ , both graphs showing the data of several devices.

approximately 300 nm. The sputtered top metal is contacting the source and gate through via-holes, while the drain contact is formed by direct metal contact to the top of the NWs.

Devices are electrically characterized with a Keithley 4200 SCS. Measurements of the gate leakage current,  $I_{GS}$ , show generally low levels with a typical value of  $I_{GS} = 1 \text{ pA}/\mu\text{m}^2$ . The output characteristics of a single NW InAs MOSFET device is shown in Fig. 1(b) together with data from fitting of a virtual source model,<sup>8</sup> to which we have added a NW core conduction. The high uniform doping used in the InAs NWs, causing a significant band bending towards the NW center, results in the formation of a parasitic conduction path at the radial core. The core conduction is modeled using velocity saturated Drude drift. By fitting the complete MOSFET model (virtual source surface conduction and Drude drift core conduction) to several devices, it is possible to determine a surface related mobility,  $\mu_{\text{surface}} = 1300 \text{ cm}^2/\text{Vs}$ . Based on the NW doping concentration ( $N_D \sim 1 \times 10^{18} \text{ cm}^{-3}$ ), we deduce a NW bulk mobility between  $\mu_{\text{bulk}} = 1300\text{--}4000 \text{ cm}^2/\text{Vs}$ . This agrees well with our expectation that the  $\mu_{\text{surface}}$  might be substantially lower than that of the bulk NW. To get an accurate fit to the measured data, estimations of the series resistance,  $R_{\text{series}} = 200\text{--}350 \Omega \mu\text{m}$ , are accounted for, corresponding to the

ungated segments of the NWs. This resistance agrees well with the measured on-resistance,  $R_{ON} = 320\text{--}500 \Omega \mu\text{m}$ .

For the  $1/f$ -noise measurements, a Synerge-Concept Programmable Gain and Bias Amplifier (transimpedance  $= 10^{-4} \text{ A/V}$ , AC-coupled) and a HP 89410A vector signal analyzer (DC to 10 MHz) were used. The current noise spectral density,  $S_{ID}$ , is measured for  $V_{DS} = 50 \text{ mV}$  between 10 Hz and 1 kHz and the data for an InAs MOSFET are shown in Fig. 2(a), with evident dependence of  $S_{ID}$  on increasing gate overdrive voltage ( $V_{OD} = V_{GS} - V_T$ ). In Fig. 2(b), the normalized current noise spectral density,  $S_{ID}/I_{DS}^2$ , for several devices is plotted against  $I_{DS}$ . In Fig. 2(c), the gate area normalized equivalent gate voltage noise spectral density,  $S_{VG} \cdot L_G \cdot W_G$ , is plotted against  $V_{OD}$ . The normalized noise spectral density measured on several devices show similar levels and the two best single NW MOSFET devices show  $S_{ID}/I_{DS}^2 = 5 \times 10^{-9} \text{ Hz}^{-1}$  and  $S_{VG} \cdot L_G \cdot W_G = 60$  and  $80 \mu\text{m}^2 \mu\text{V}^2/\text{Hz}$ , respectively, all values given at  $f = 10 \text{ Hz}$  and  $V_{DS} = 50 \text{ mV}$ . These measurements show an almost  $100\times$  reduction to our previous reported data,<sup>9</sup> and could be attributed to the insertion of an inner  $\text{Al}_2\text{O}_3$  layer, thus improving the interface properties.<sup>10</sup>

The subthreshold characteristics for a dual conduction device consisting of a single NW are shown in Fig. 3(a) (the same device as in Fig. 1(b)). In Fig. 3(a), the core conduction

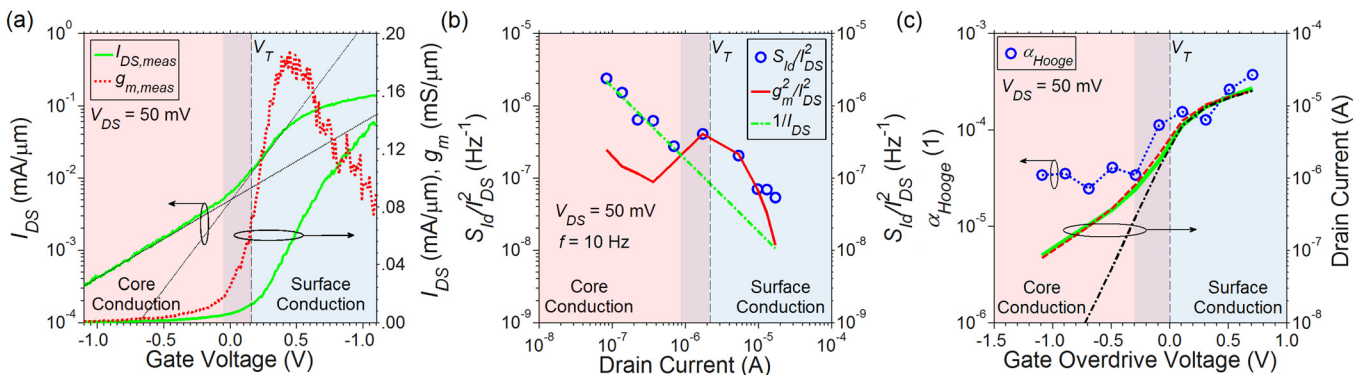


FIG. 3. Measured data for an InAs MOSFET device, where the two distinct regions of conduction, core and surface, have been indicated with a red and blue colored background area, respectively. The plots are showing (a) transfer characteristics, (b)  $S_{ID}/I_{DS}^2$  versus  $I_{DS}$ , and (c)  $V_{OD}$  dependence for calculation of the Hooe-parameter  $\alpha_{\text{Hooe}}$  (for  $\mu_{\text{bulk}} = 4000 \text{ cm}^2/\text{Vs}$ ). The measured  $I_{DS}$ , the green solid line, is in (c) fitted with a MOSFET model, with an inner channel, red dashed line, and without an inner channel, dashed dotted black line.

path is identified at large negative bias condition and it shows a subthreshold slope of about 960 mV/decade. The surface channel, identified just below the threshold voltage, has a steeper slope at about 410 mV/decade.

In Fig. 3(b),  $S_{ID}/I_{DS}^2$  is plotted versus  $I_{DS}$ . It is identified that the measured data follow either a  $1/I_{DS}$  or a  $g_m^2/I_{DS}^2$  pattern, depending on if the dominating conduction path is the core or the surface, respectively. To evaluate the various contributions to the noise level, we use data from the fitted MOSFET model combined with noise models. In the region where the current in the inner channel is dominating, the noise should not be associated with interface traps. Instead, the measured fluctuations should relate to mobility fluctuations with a noise level described by the expression for the  $\alpha_H$  according to Eq. (1).<sup>5</sup>

$$\frac{S_{ID}}{I_{DS}^2} = \frac{q\alpha_H}{fW_G L_G Q} [Hz^{-1}]. \quad (1)$$

In Eq. (1),  $q$  is the elementary charge, and  $Q$  is the channel charge concentration per unit area. Using Eq. (1) and experimental data for  $S_{ID}/I_{DS}^2$  together with calculated values for  $Q$  obtained from the fitted MOSFET model, values for  $\alpha_H$  can be calculated for the entire measured range. These data are shown in Fig. 3(c) for  $\mu_{bulk} = 4000 \text{ cm}^2/\text{Vs}$ . The same range of values can be calculated for other measured devices showing similar dual channel behavior.

Comparing our calculated value for  $\alpha_H$  to the value reported for a Si-pFINFET with channel width-height =  $0.030 \times 10 \mu\text{m}^2$  (HfO<sub>2</sub> dielectric),<sup>11</sup>  $L_G = 100 \text{ nm}$ , the value is found to be in the same range,  $\alpha_H \sim 10^{-5}$ . In a study of a 15-nm-thick InAs HEMT,<sup>12</sup>  $L_G = 250 \text{ nm}$ ,  $\alpha_H$  was determined as a function of the channel depth and determined to range between  $\sim 10^{-4}$  and  $5 \times 10^{-3}$ . It was found that the distance to the gate was correlated with increasing value of  $\alpha_H$  for a gate-channel distance of less than 20 nm. One, speculated, reasoning for this is larger surface roughness on the side of the channel which is closer to the gate. The impact of surface roughness scattering is also reported for a buried SiGe channel, where it was found that mobility related  $1/f$ -noise was improved by increasing the thickness of a Si-cap.<sup>13</sup> In a study of 30 nm wide InAs NWs with  $L_G = 2 \mu\text{m}$  (SiO<sub>2</sub> dielectric),  $\alpha_H$  was measured as a function of temperature and for a low temperature,  $T = 2 \text{ K}$ ,  $\alpha_H = 5 \times 10^{-4}$  was obtained.<sup>14</sup> The value was referred to as a lower bound for one- and two-dimensional InAs systems and this was argued on the basis that other studies reported similar lowest values. Two other studies of InAs NW FETs; one with 40-nm-diameter NWs and  $L_G = 35 \text{ nm}$  (HfO<sub>2</sub> dielectric),<sup>9</sup> and one with 27-nm-diameter NWs and  $L_G = 100\text{--}750 \text{ nm}$  (Al<sub>2</sub>O<sub>3</sub> dielectric),<sup>15</sup> report values of  $\alpha_H = 4 \times 10^{-3}$  and  $\alpha_H \sim 10^{-3}$ , respectively. The values for InAs NW channels in the literature are somewhat larger or comparable to the  $\alpha_H$  that we calculate for the surface channel  $\alpha_{H,surface} \sim 5 \times 10^{-4}$ . One of our main results is, however, that we can separate the core conduction from that of the surface and that our measurement technique provides data under transport conditions, where the influence of the surface properties on the  $\alpha_H$  extraction is strongly reduced.

For the bias region with measured  $S_{ID}/I_{DS}^2$  following  $g_m^2/I_{DS}^2$ , thus likely being related to number fluctuations, the volumetric gate oxide trap density,  $N_t$ , can be determined according to Eq. (2),<sup>5</sup>

$$N_t = \frac{fW_G L_G C_{ox}^2 S_{VG}}{q^2 k_B T \lambda} [\text{cm}^{-3} \text{eV}^{-1}]. \quad (2)$$

In Eq. (2),  $C_{ox}$  is the oxide capacitance per unit area and  $\lambda$  is the tunneling attenuation length in the gate oxide described by  $\lambda = (\frac{4\pi}{h} \sqrt{2m^* \Phi_B})^{-1} [\text{nm}]$ .<sup>16</sup> Here,  $m^*$  is the effective electron mass and  $\Phi_B$  is oxide barrier height. Assuming  $m^* = 0.23 \cdot m_0$  ( $m_0$  being the electron rest mass) and  $\Phi_B = 2.3 \text{ eV}$ ,<sup>17</sup>  $\lambda = 0.15 \text{ nm}$ , and this value is used for calculations of  $N_t$ . The oxide tunneling distance is given by  $z = \lambda \ln(1/2\pi f \tau_0)^{-1} [\text{nm}]$ ,<sup>5</sup> where it can be assumed that the time constant  $\tau_0 = 10^{-10} \text{ s}$ .<sup>5</sup> Calculation of the probed oxide depth for  $f = 10\text{--}1000 \text{ Hz}$  yields  $z = 2.0\text{--}2.7 \text{ nm}$ . For the device with data shown in Fig. 3,  $N_t \sim 8 \times 10^{22} \text{ cm}^{-3} \text{eV}^{-1}$ . Other devices with lower  $V_T$  show lower trap levels with  $N_t \sim 6 \times 10^{19} \text{ cm}^{-3} \text{eV}^{-1}$ . The relatively high trap density found suggests that the low temperature HfO<sub>2</sub> ALD film can be further improved. Other studies with higher deposition temperatures for HfO<sub>2</sub> report substantially lower values<sup>18</sup> with  $N_t \sim 7 \times 10^{18} \text{ cm}^{-3} \text{eV}^{-1}$ .

In summary, we have evaluated the level of  $1/f$ -noise in vertical InAs nanowire MOSFETs and achieved low levels of normalized  $S_{VG} \cdot L_G \cdot W_G$  noise. It is found that the noise contribution from the surface channel is stronger than the effects related to mobility fluctuations within the channel at forward bias.

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