Extrinsic and Intrinsic Performance of Vertical InAs Nanowire MOSFETs on Si Substrates

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Abstract—This paper presents DC and RF characterization as well as modeling of vertical InAs nanowire MOSFETs with $L_G = 200$ nm and Al$_2$O$_3$/HfO$_2$ high-$k$ dielectric. Measurements at $V_{DS} = 0.5$ V show that high transconductance ($g_{m} = 1.37$ mS/µm), high drive current ($I_{DS} = 1.34$ mA/µm), and low on-resistance ($R_{ON} = 287$ Ωµm) can be realized using vertical InAs nanowires on Si substrates. By measuring the $1/f$-noise, the gate area normalized gate voltage noise spectral density, $S_{V_{NOISE}} L_G W_{G}$, is determined to be lowered one order of magnitude compared to similar devices with a high-$k$ film consisting of HfO$_2$ only. Additionally, with a virtual source model we are able to determine the intrinsic transport properties. These devices ($L_G = 200$ nm) show a high injection velocity ($v_{inj} = 1.7 \times 10^7$ cm/s) with a performance degradation for array FETs predominantly due to an increase in series resistance.

Index Terms—MOSFET, RF, InAs, Nanowire (NW).

I. INTRODUCTION

Striving towards ultra-scaled devices, the transistor architecture and the material properties need consideration. The nanowire geometry offers advantageous electrostatic scaling [1] and the use of a high-$k$ gate dielectric allows reduced EOT without large gate leakage currents. InAs has a high injection velocity, $v_{inj}$, and allows simple fabrication of low resistance contacts [2][3]. High current densities have been demonstrated for thin InAs transistor channels [4].

In this paper we demonstrate DC characterization, modeling and RF characterization of FETs consisting of arrays of vertical NWs (a-FETs) [5][6][7]. Our data for a-FETs show a threefold improvement on earlier data and we achieve transconductance values above 1 mS/µm for individual nanowires. This is attributed to an improved bi-layer gate dielectric using Al$_2$O$_3$/HfO$_2$, as well as more reliable processing with a thin Si$_3$N$_4$ film, reducing the source series resistance [8]. From DC modeling, we identify the main limiting factors in the transistor layout.

II. DEVICE FABRICATION

Devices are fabricated on Si substrates cut from a 4” Si wafer covered by a 300-nm-thick InAs contact layer (ICL).

The Si is highly resistive and the InAs layer is grown without intentional doping ($n = 3 \times 10^{18}$ cm$^{-3}$) demonstrating a sheet resistance of 36 Ω/□. Definition of size and position of gold seed particles is made with electron-beam-lithography and growth of InAs nanowires is performed in an metal-organic-vapor-phase-epitaxy (MOVPE) growth chamber at 420 °C and with a Sn dopant flow corresponding to a doping level of $\sim 1 \times 10^{15}$ cm$^{-3}$ [9]. For a-FETs, NWs are placed in zigzag rows to reduce the parasitic capacitance within the array [10], with 300 nm spacing between each NW (see Fig. 1a and Fig. 1b). Devices are fabricated with 1, 52, 96, and 192 NWs and with two NW diameters; $D_{NW1} = 45$ nm and $D_{NW2} = 28$ nm [8]. Besides the difference in size of catalytic gold particles, the rest of the growth conditions are identical. The dielectric is deposited in a Cambridge Savannah ALD process with 10 cycles of Al$_2$O$_3$ at 250 °C and 60 cycles of HfO$_2$ at 100 °C, with a total thickness of 7 nm translating to an estimated EOT of 1.8 nm. The $D_{NW1} = 28$ nm have a thinner HfO$_2$ layer, yielding an estimated EOT = 1.3 nm. Subsequent to the ALD, the 2×2 cm$^2$ pieces are cleaved into 4 samples and each sample is thereafter processed individually. Devices are isolated by etching out source-mesas from the ICL in a wet-etch procedure. A 60-nm-thick source-to-gate spacer layer is fabricated in a process where a plasma-enhanced-chemical-vapor-deposited (PECVD) Si$_3$N$_4$-film (Fig. 1a) is conformally formed on the NWs. The film is then selectively removed on the sides of the wires, while keeping the lateral film intact by protecting it with a polymer etch mask in a SF$_6$ dry-etch process.
process (Fig. 1b). The sputtered W-gate is defined to 200 nm length by the thickness of an etched down polymer etch mask, SCS. For the gate-drain top spacer is fabricated with a spin-coated polymer resist which is etched-back to around 300 nm. The top contact metal consist of 250 nm sputtered Ti/W/Au. A schematic cross-section of a device is shown in Fig. 1c. The ICL acts as source, and the top metal as the drain contact.

III. MEASUREMENTS AND SMALL-SIGNAL MODEL

DC characterization is performed with a Keithley 4200-SCS. For the $D_{\text{tip}} = 45$ nm devices, transfer characteristics for a single NW FET (s-FET), two a-FETs (52 and 192 NWs, respectively) are shown in Fig. 2a, 2b, and 2c, respectively. The peak transconductance is reduced for a-FETs as compared with the s-FETs, and the data is presented in Table I. Plots of output characteristics are shown in Fig. 3a and 3b for an s-FET and an a-FET (52 NWs), respectively. In Fig. 3c, $g_{m}$ versus $V_{GS}$ for three s-FETs is shown. At $V_{DS} = 0.5$ V, the best device show $g_{m} = 1.37$ mS/µm. The s-FET device referred to as NW1 is the same in Fig. 3a and 3c. In Fig. 3d, transconductance for several devices have been plotted against NW circumference. Transconductance characteristics of the tabled s-FETs and a-FETs, respectively) are shown in Fig. 2a, 2b, and 2c, respectively.

Table I. Peak values listed for 45-nm s-FETs and a-FETs, devices show similar values (typically between -0.4 – 0.2 V) and there is no relation between $V_{T}$ and peak transconductance, $g_{m,\text{peak}}$. Quantifying $g_{m,\text{peak}}$-widths, the values for s-FETs and a-FETs do not differ, suggesting there is not a significant spread in $V_{T}$ within arrays that would cause a degraded maximum $g_{m}$. For reference, we have benchmarked our data with other high performance InAs and InGaAs NW FETs; a 13 nm planar XOI FET, $L_{G} = 230$ nm [14], a 25 nm diameter InAs/InP radial nanowire FET (Ω-gate, $D_{\text{tip}} = 45$ nm, $L_{G} = 170$ nm [15], a 15 nm in diameter lateral NW, $L_{G} = 100$ [4], and a top down rectangular GGA FET (20x30 nm), $L_{G} = 20$ nm [16].

Low frequency noise (LFN) characterization is made with a Stanford SR830 lock-in amplifier in series with a Stanford SR570 LNA. The current noise spectral density, $S_{ID}$, is
measured for $V_{DS} = 50$ mV and $f = 10$ Hz. A common measure of comparison is the deduced gate voltage noise spectral density, $S_{VG} = S_{ID}/I_{m}^2$, normalized to the gate area ($S_{VG}/W_G$). Data for 2 s-FETs and 2 a-FETs is plotted in Fig. 4. The lowest levels for all the measured devices are determined to range in the interval $S_{VG}/W_G = 310 - 410 \text{µV}^2/\text{Hz}$. Another common measure of comparison is the $S_{ID}$ normalized to the drain current, $S_{ID}/I_{DS}^2$. The lowest measured levels are $S_{ID}/I_{DS}^2 = 0.9 \cdot 10^{-19} - 1.5 \cdot 10^{-19} \text{Hz}^{-1}$ and $S_{ID}/I_{DS}^2 = 0.9 \cdot 10^{-19} - 2.0 \cdot 10^{-19} \text{Hz}^{-1}$, for two 52 NW a-FETs and two s-FETs, respectively. The measurements indicate that when accounting for the difference in total gate width, the extracted $S_{ID}$ for s-FETs and a-FETs show undeviating values. Further, comparing the $1/f$-noise to similar devices but fabricated with a high-$\kappa$ of HfO$_2$ only [15], the new devices improved the noise performance about one order of magnitude in terms of $S_{VG}/W_G = 5700 \text{µV}^2/\text{Hz}$ and even greater for $S_{ID}/I_{DS}^2 = 7.3 \cdot 10^{-19} \text{Hz}^{-1}$. The decrease in LFN can be related to the introduction of an Al$_2$O$_3$ film, which more efficiently can reduce the amount of sub-oxides [11]. For comparison, the ITRS roadmap states that for the year 2015, multi-gate MOSFET devices for mm-wave applications should comply with $S_{VG}/W_G = 10.3 \text{µm}^2/\text{µV}^2/\text{Hz}$ [17]. Further work is hence required to reach the target goals within the roadmap.

The RF characterization is performed using an Agilent E8361A network analyzer from 60 MHz to 40 GHz at a RF power of -27 dBm [5]. For measurements, a-FETs with 192 NWs was chosen on the premises of having a higher absolute $g_m$ and a SEM image of the InAs mesa structure of one such device is shown in Fig. 5a. The highlighted areas show the location of where contact vias and pads will be formed in later stages. The deduced current gain, $h_{21}$, and unilateral power gain, $U$, for the best device is shown in Fig. 5b, for which $f_s = 14.6$ GHz and $f_{max} = 30.0$ GHz at $V_{DS} = 1.0$ V, and $V_{GS} = -0.45$ V, and $-0.60$ V, respectively. The RF data are fitted to a standard MOSFET small-signal model [5] where the parasitic elements are included in Fig. 5c. For simplicity, impact ionization was not accounted for as it turned out to have negligible effect in the fitting to the measured data. Statistics over 4 devices show $f_s$ in an interval of 9.7-17.4 GHz and $f_{max}$ of 20.3-30.0 GHz, at $V_{DS} = 1.0$ V.

IV. DC DEVICE MODELING

To describe the transistor characteristics of the $D_{NW} = 45$ nm devices, a virtual source (VS) model is fitted to the measured DC data [18]. The model is based on a channel charge equation and also provides a coherent intrinsic gate capacitance [19]. Modeled devices are chosen on the premises of low $R_{ON}$ in combination with less pronounced impact ionization, thus being able to neglect the later. Since a direct measurement of the NW contact and channel resistivity is difficult, we do a simultaneous fit of the VS-model parameters with estimates of the source/drain resistance. For a s-FET (referred as NW1), assuming a NW resistivity of $1.0 \cdot 10^3 \Omega$cm [20] and a first spacer layer thickness of 67 nm (60 nm Si$_3$N$_4 + 7$ nm high-$\kappa$), we obtain $R_S = 65 \Omega$μm.
contact resistance is measured to be in the order of 2 Ω and is for simplicity counted as a constituent of the ICL. For the s-FET, the 18 Ω series resistance contribution from the ICL, corresponding to 2.5 Ωµm, can be ignored. Fitting the data in Fig. 3a gives $R_D = 141 \Omega\mu m$, equivalent to 300 nm resist top spacer thickness (translating to 160 nm non-gated resistive NW segment length, see Fig. 1c) and in agreement with the experimental implementation. At a gate length of $L_G = 200$ nm, we obtain values of mobility, $\mu_{\text{LOW-MFIELD}} = 1300 \text{cm}^2/V\text{s}$ and $v_{\text{inj}} = 1.7 \times 10^7 \text{cm/s}$. While the rather low mobility can be expected for a highly doped surface channel, the injection velocity is in the same range as is reported for an InAs HEMT of similar gate length [2] ($v_{\text{inj}} \sim 2 \times 10^7 \text{cm/s}$).

To analyze a-FETs, the fitted model for the s-FET is expanded and fitted to an a-FET with 52 NWs. The significant increase in $R_{\text{ON}}$ for a-FETs compared to s-FETs can in part be explained by the undoped ICL that adds 18 Ω source series resistance, see Fig. 6. In order to obtain a good fit, however, it is needed to reduce $v_{\text{inj}}$ by around 30% and also increase the resistivity of the NWs by a factor of around 4, and this fitting is shown in Fig. 3b. The decrease in $v_{\text{inj}}$ can be explained by longer channels for a-FETs as compared with the s-FET (as well as thicker spacer layers) due to the defining polymer resist, used for the etch-back of the gate, that tends to become thicker around arrays. The steep increase in series resistance can, however, not be explained simply by a thicker gate-drain separation. Instead, it must be considered that the doping incorporation of the surfactant Sn is higher for single NWs as compared to NWs grown in arrays due to the limited collection area for the a-FETs during the vapor liquid solid (VLS) growth. The radial band bending inefficiency for the 45-nm-diameter NW FETs, as described earlier, can effectively be modeled as a parasitic parallel conduction. For the measured s-FET in Fig. 3a, it is in the order of 0.25 mS/µm. For a-FETs, this value is about 4-6 times lower, however, the transfer characteristics are not significantly improved compared to s-FETs as the transconductance is reduced by a similar factor due to series resistance. The variance in characteristics between devices with equal number of NWs is thought to be related to diameter variation (NWs in arrays typically vary between 40 - 45 nm) in combination with variations of separation layer thicknesses over the sample. To compare the effect of the reduced $v_{\text{inj}}$ with the effect of...
external resistances, we plot in Fig. 3d calculated values for the extrinsic transconductance, $g_{m,ext}$, as a function of $R_{DN}$, using the VS model. In the plot there are two lines representing two values of $v_{TH}$ (the fitted s-FET and a-FET) corresponding to $L_e = 200$ nm ($g_{m,f,HS}$) and $L_e = 300$ nm ($g_{m,f,LS}$), respectively. Comparing the simulated data with the experimentally measured $g_{m,ext}$, a good fit can be obtained. This indicates that the external resistances are the major source for device performance degradation for a-FETs as compared with s-FETs. This can essentially be described using the conventional formula relating the extrinsic and intrinsic transconductance $g_{m,ext} = g_{m,int} / (1 + g_{m,int} R_S + g_{m,int} (R_S + R_D))$ [21]. Here $g_{m}$ is the output conductance. From the average experimental data for the s-FETs shown in Fig. 3c, we deduce a value for the intrinsic transconductance, $g_{m} = 2.4$ mS/µm. For the a-FETs, this value range between 0.5 – 0.7 mS/µm.

The total parallel resistance contributions from the un-gated segments of the NWs are shown in Fig. 6a and 6b for a 52 NW a-FET and a 192 NW a-FET, respectively. Comparing the normalized series resistance contributions attributed to the un-gated NW segments (omitting the ICL), $R_S = 265$ Ωµm and $R_D = 845$ Ωµm for the 52 NW a-FET, and $R_S = 270$ Ωµm and $R_D = 900$ Ωµm for the 192 NW a-FET. These values are quite close as expected (2% and 6% in difference for $R_S$ and $R_D$, respectively). For a 52 NW a-FET, the ICL (18 Ω) adds another 12 % to the total series resistance while for a 192 NW a-FET, the series resistance contribution from the ICL adds another 42 %. This explains why a 52 NW a-FET has better normalized DC performance than a 192 NW a-FET.

V. RF DEVICE MODELING

Performing electrostatic simulations of the capacitances of the de-embedded structure of 12x12 µm$^2$ [5], that is the overlapping source-gate and gate-drain areas, as indicated in Fig. 5a with the overlapping rectangles, the parasitic capacitances $C_{pg,p}$ and $C_{gs,p}$ are determined to 131 fF and 16 fF, respectively. The substantially larger $C_{pg,p}$ originates from the thinner source spacer layer and higher permittivity of the SiN$_x$ as compared with the drain spacer. Taking into account the low density of states for InAs, the high frequency intrinsic gate capacitance, $C_{g,INT}$ for 192 NWs is simulated to be in the interval of 6 fF to 23 fF for $V_{GS} - V_T$ varying between -0.5 V to 0.5 V, at $V_{DS} = 1$ V. Considering the low measurement gate bias and assuming that the $C_{g,INT}$ contribution in the middle of the given range, the simulated number ($C_{g,INT} = 5.95$ fF/µm) is 13 % larger than the number extracted from the measurement ($C_{g,INT} = 5.27$ fF/µm). Actual pad size difference compared to the patterned area as well as uncertainty in the spacer layer thicknesses and dielectric constants are likely the reasons for the deviation between measured and calculated capacitances. The extracted $g_{m,INT}$ of 0.53 mS/µm corresponds to a $g_{m,ext}$ of 0.36 mS/µm, which can be related to the maximum $g_{m,ext}$ measured at DC for the same device ($g_{m,ext} = 0.30$ mS/µm, 20 % lower). The low $V_{GS}$ in the measurement for maximum $f$ and $f_{max}$ suggest a shift in $V_T$ as compared to DC ($V_T = -0.45$ V for $V_{DS} = 1$ V). Both the shift in $V_T$ and the increase in $g_m$ can be related to slow traps that are not responding at higher frequencies, thus explaining the lowering of the $V_T$ and a frequency dependent $g_m$ [22]. Comparing the series resistances from the RF model extraction with those from the VS model fitting of the DC measurements, they are found to be fairly similar. The RF extraction gives $R_S = 34$ Ω and $R_D = 33$ Ω while the DC measurements translates into $R_S = 28$ Ω and $R_D = 33$ Ω.

VI. DISCUSSION

Based on the data presented in this paper we draw some general conclusions regarding III-V NWs and their implementation; although high intrinsic performance, that is high transconductance and drive currents, has been demonstrated in various forms of III-V nanowires [4][14][15][16], it is clear that the implementation of RF-compatible devices still is a challenge. Analysis of planar III-V MOSFETs [23] show that the control of the access resistance is one of the key parameters to increase the transconductance and to obtain attractive RF-properties. The method used in the here presented implementation, that is uniform doping of the transistor channel, needs further refinement beyond diameter scaling in order to avoid increase in the access resistance. Increased doping control may be one alternative to reduce the source/drain resistance [9]. Alternatively, the access regions may be regrown, although at the cost of parasitic capacitance [10]. A heterobarrier may also be included into the channel to increase the carrier control [24]. It appears that a combination of these approaches may be required to fully exploit the potential of the high III-V injection velocity for RF-compatible MOSFETs in either vertical or lateral geometry.

VII. CONCLUSION

The performance of s-FET performance has been evaluated ($g_{m,ext} = 1.37$ mS/µm). Based on a virtual source model we are able to accurately model and determine intrinsic transport properties including $v_{TH} = 1.7 \times 10^7$ cm/s. The performance is degraded by series resistance for devices consisting of arrays of NWs. The introduction of a thin Al$_2$O$_3$ film combined with an outer HfO$_2$ film may be responsible for the measured reduction in 1/f-noise compared to similar devices fabricated with HfO$_2$ only.

VIII. ACKNOWLEDGEMENT

We would like to acknowledge Mikael Eggard, Vladimir Drakinsky and Tomas Bryllert for assistance and Henrik Sjöland for valuable discussions.

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