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RF and DC Analysis of Stressed InGaAs MOSFETs

Guntrad Roll, Erik Lind, Mikael Egard, Sofia Johansson, Lars Ohlsson, and Lars-Erik Wernersson

Abstract—A complete reliability study of the DC and RF characteristics for InGaAs nMOSFETs with Al2O3/HfO2 dielectric is presented. The main stress variation at high frequencies is related to a threshold voltage shift, whereas no decrease is found in the maximum of the cut-off frequency and RF-transconductance. Constant gate stress leads to a charge build up within the gate oxide causing a threshold voltage shift. Furthermore, electron trapping at the drain side degrades the performance after hot carrier stress. The maximum DC-transconductance is reduced following constant gate bias stress, by an increase in charge trapping at border defects. These border defects at the channel/high-κ interface are filled by cold carrier trapping when the transistor is turned on, whereas they do not respond at high frequencies.

Index Terms—high-κ, InGaAs, MOSFET, reliability, RF

I. INTRODUCTION

II-V metal oxide semiconductor field-effect transistors (MOSFET) are promising candidates for future application that require low-power and high-frequency [1]. Due to the high electron mobility and large injection velocity, InGaAs n-channel transistors can reach high on-currents at low source-drain voltages [2]. Major process improvements, including high-κ to channel interface quality and source/drain series resistance have been made in the last few years [2]–[4]. Currently, there are only a few investigations of relevant reliability issues [5]–[7]. In this work, we investigate the key degradation problems of raised source/drain InGaAs transistors after hot carrier injection and bias temperature instability. A complete degradation study of the DC- and RF device characteristics is presented.

II. DEVICES AND MEASUREMENT

Figure 1(a) shows the basic structure of the investigated InGaAs nMOSFET. A SiO2-like dummy gate, on top of the not intentionally doped 10-nm-thick In0.53Ga0.47As channel, was used as hard mask for epitaxial MOCVD regrowth. The Sn doping concentration in the 40-nm-thick In0.3Ga0.7As source/drain is about 5.1013 cm−3. After dummy gate removal with a buffered oxide etch, the sample surface was treated with (NH4)2S (10%) for 20min. The gate oxide was deposited by ALD using 10 cycles of TMA and H2O at 300°C and 40 cycles of TDMAHf and H2O at 120°C. The Al2O3 and HfO2 layer have a thickness of approximately 1nm and 4.5nm. The metal electrodes were deposited by evaporation and a post metallization anneal at 400°C under N2 finished the process. The measured equivalent oxide thickness of this structure is 2.3nm. The total width of the two gate fingers is 15μm. A detailed description of the process can be found in [4].

Direct current (DC) and high frequency (RF) measurements were performed using a Keithley SMU and an Agilent PNA network analyzer with a frequency range of 40MHz to 67GHz. For S-parameter calibration, the off-chip load-reflect-reflect-match method and on-chip de-embedding short and open structures were used. Source- and drain resistances of 17Ω were determined using the channel resistance method. Constant DC stress at room temperature was applied and subsequently IdVg and S-parameters were measured. The IdVg was measured from -1V to +1V after positive stress and from +1V to -1V after negative stress. An initial recovery occurs at the starting bias of the IV sweep. The IdVg measurement was repeated after the S-parameter measurement, showing no significant further recovery due to the parameter determination. The recovery process was not analyzed in this study. The threshold bias was determined taking the point and slope of the maximum transconductance and extrapolating the linear function to zero current. Especially the increase in transconductance (gm) with frequency (f), deduced from the RF measurements (Y21-parameter), was analyzed (Fig. 1(b)). The gm(f) dependence in high-κ InGaAs MOSFETs is generally modeled by cold carrier trapping into the oxide [8]–[10]. A similar model is used to explain the small stable IdVg hysteresis found also in early high-κ/silicon devices [11]. Using the gm(f)-frequency increase, the amount of charges trapped at border defects (Nbd) and tunneling depth (xm) was calculated based on an elastic tunneling model (eq. 1) [9], [10]. It should be noted that the model assumes a constant capture cross section and neglects inelastic trapping, as used in recent Si/SiO2 stress models [12].

\[ N_{bd}(x_m) = \frac{(C_s + C_{ox}) \cdot g_{mi}}{e^2 \lambda g_{mi}^2(f)} \cdot \frac{\partial g_{mi}(f)}{\partial \ln(2\pi f)} \]  

\[ x_m = \frac{\lambda \cdot \ln(f_{mi}/f)}{f_{mi}} \]  

Here, \( e \) is the elementary charge, \( g_{mi} \) is the transconductance at a frequency \( f_{mi} \) high enough that \( g_{mi} \) is constant, \( C_s \) and \( C_{ox} \) are the semiconductor- and the oxide capacitance, respectively. For the tunneling parameters, \( \lambda = 1.6 \times 10^{-8} \text{ cm} \) was chosen [10]. The measured trap density is also depending on the energy which is determined by the band bending at a certain gate bias and threshold bias \( (V_{th}, V_{th}) \).

III. RESULTS AND DISCUSSION

Figure 1(b) illustrates the change in measured RF characteristic due to positive bias temperature stress (PBTS). The RF-gm (≈ real part of Y21) is plotted taking the threshold shift \( (\Delta V_{th} = 0.095V) \) after PBTS into account. The gm(f) dispersion increases after stress. Figure 1(b) shows that the RF-gm curves overlap above 20GHz, which shows that they are only shifted by \( \Delta V_{th} \). The same trend is valid after negative bias temperature stress (NBTS). The maximum of the cut-off frequency \( (f_c) \), which is directly related to the gm maximum
Applying BTI stress leads to a degradation in $V_{th}$ and a decrease in the maximum transconductance ($g_{max}$) under DC conditions (Table I, Fig. 2). The degradation follows a power law. The time slope ($n$) is determined with an error due to the initial recovery [14]. The time slope of the $V_{th}$ degradation is stress bias independent within small variations. Applying a positive gate stress leads to a $V_{th}$ increase with a time slope of 0.25±0.06 independent of the gate length (Fig. 2(a)). Applying a negative gate stress leads to a $V_{th}$ decrease with a time slope of 0.17±0.04 (Fig. 2(a)). The $V_{th}$ reduction gets worse, with decreasing gate length (Table I), due to a higher initial trapping

$$
\text{TABLE I} \\
\text{KEY PARAMETER SHIFT AFTER STRESS}
\begin{array}{|c|c|c|c|}
\hline
\text{Unstressed} & V_D=0.525V & \Delta g_{max} & \Delta f_t \\
\text{Unstressed} & V_D=500\mu m & [mS/\mu m] & [GHz] \\
\hline
L_{Gate}=500\mu m & -0.04±0.14 & 0.98±0.14 & 163±40 \\
L_{Gate}=200\mu m & 0.12±0.01 & 0.79±0.01 & 100±11 \\
\hline
\text{BTI} V_G=V_{stress}, V_D=50V, 1500s, 25^\circ C, L_{Gate}=50nm & \Delta g_{max} & \Delta f_t \\
V_{stress} [V] & \Delta g_{max} [mS/\mu m] & \Delta f_t [GHz] \\
2 & -0.08 & 11 \\
3 & -0.19 & 11 \\
\hline
\text{NBTI} V_G=V_{stress}, V_D=50V, 1500s, 25^\circ C & \Delta g_{max} & \Delta f_t \\
V_{stress} [V] & \Delta g_{max} [mS/\mu m] & \Delta f_t [GHz] \\
-2.5 & -0.15 & 10 \\
-3 & -0.19 & 6 \\
\hline
\text{Unstressed} & V_D=0.525V & \Delta g_{max} & \Delta f_t \\
L_{Gate}=100nm & [mS/\mu m] & [GHz] \\
\hline
\text{HCl} V_G=V_{stress}, V_D=50V, 1500s, 25^\circ C, L_{Gate}=100nm & \Delta g_{max} & \Delta f_t \\
V_{stress} [V] & \Delta g_{max} [mS/\mu m] & \Delta f_t [GHz] \\
1 & -0.09 & 16 \\
\hline
\end{array}
$$

maximum $f_t$ and extrinsic DC-$g_{max}$ are given.

**Maximum $f_t$ outside S-parameter measurement range (0.1V to 0.8V).
InGaAs MOSFET with Al$_2$O$_3$ dielectric [6], but the $V_{th}$ shift was observed in both the subthreshold and inversion region for the S passivated InGaAs/Al$_2$O$_3$/HfO$_2$ gate oxide.

**IV. CONCLUSION**

The reliability characteristics of a raised source/drain InGaAs nMOSFET with high-$\kappa$ dielectric are investigated. Prestress border defects, available for cold carrier trapping, are responsible for transconductance frequency dispersion and current hysteresis. An increase in cold carrier trapping to border defects and a decrease in maximum DC transconductance with both positive and negative gate stress is observed. The threshold bias shift under constant positive and negative gate stress is mainly caused by charge accumulation, possibly deeper within the gate oxide. Those charges do not influence the maximum transconductance measured at high frequencies. The threshold bias related transconductance shift is the main factor for cut-off frequency variation. Hot carrier stress at a gate bias of 1V does not effect the cold carrier trapping when the transistor is turned on, but electron trapping increases the threshold voltage.

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**REFERENCES**


