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LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

RF-Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates

Sofia Johansson, Mikael Egard, Sepideh Gorji Ghalamestani, B. Mattias Borg, Martin Berg, Lars-Erik Wernersson, and Erik Lind

Abstract— We present DC and RF characterization of InAs nanowire field-effect transistors heterogeneously integrated on Si substrates in a geometry suitable for circuit applications. The field-effect transistor consists of an array of 182 vertical InAs nanowires with about 6 nm HfO₂ high-*k* gate dielectric and a wrap-gate length of 250 nm. The transistor has a transconductance of 155 mS/mm and an on-current of 550 mA/mm at a gate voltage of 1.5 V and a drain voltage of 1 V. S-parameter measurements yield an extrinsic cut-off frequency of 9.3 GHz and a extrinsic maximum oscillation frequency of 14.3 GHz.

Index Terms—high-*k*, InAs, MOSFET, nanowire, RF

I. INTRODUCTION

NANOWIRE based transistors are promising candidates for gate length scaling below 20 nm due to the improved electrostatic control of the channel as compared to planar devices. The cylindrical geometry also allows for a thicker body and gate oxide as compared to a planar gate geometry [1].

In_xGa_{1-x}As High Electron Mobility Transistors (HEMTs) with high indium content have demonstrated high transconductance, $g_m > 2$ mS/μm and maximum oscillation frequencies, $f_{max} > 1$ THz [2]. However, the HEMTs use a Schottky barrier gate, which may lead to large gate leakage currents as the gate-to-channel distance is scaled. To prevent this and to enable further scaling, the introduction of an insulating gate dielectric is required. III-V Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) using high-*k* gate dielectric are therefore being developed, already showing high g_m of 1.75 mS/μm at a gate length of $L_g = 75$ nm for a In_{0.7}Ga_{0.3}As FET [3] with TaSiO_x high-*k* dielectric.

We have developed a technology to fabricate arrays of

vertical epitaxial InAs nanowire high-*k* MOSFETs [4] utilizing wrap-gate contacts. For a gate length, $L_g = 50$ nm, InAs nanowire FETs on InAs substrate with $g_m = 0.6$ mS/μm (normalized to the circumference) and a subthreshold slope of 80 mV/decade have been achieved [5]. Earlier studies on an RF-compatible process on semi-insulating (S.I.) InP substrates have yielded a unity current-gain cut-off frequency, $f_t = 7.5$ GHz and a maximum oscillation frequency, $f_{max} = 22$ GHz, mainly limited by the parasitic capacitances in the vertical geometry [6]. InAs transistors have also previously been fabricated successfully from InAs nanowires directly grown on Si substrates. These, however, suffered from limitations due to the heterojunction between the InAs and the Si in terms of limited drive current [7], [8].

For the first time, we have epitaxially integrated the vertical InAs nanowires on a Si substrates using a thin and highly conductive InAs epitaxial layer grown by a buffer layer technology. Conventional planar III-Vs grown on Si substrates usually requires a thick (about 1μm) buffer layer in order to reduce the dislocation density sufficiently for good device performance. Since the nanowires constitute vertical devices, and the nanowire growth geometry is resilient against defects in the buffer layer, the otherwise stringent demand on the crystal quality of the buffer layer can be relaxed.

We now show DC and RF-characterization of InAs MOSFETs on Si substrate with high device yield in a process suitable for circuit integration. The obtained $f_t = 9.3$ GHz is higher than what was earlier achieved on InP substrate even though the gate length is longer in these devices. Similarities can be seen between the transistors on either substrate, both in terms of DC and RF characteristics. Finally, a small-signal model of the transistors based on the measured data is presented.

II. DEVICE FABRICATION

A. InAs Epitaxial Layer

A 260-nm-thick InAs epitaxial layer was first grown on a highly resistive Si<111> substrate ($\rho > 100$ Ωm) by Metal Organic Vapor Phase Epitaxy (MOVPE). Prior to growth, the Si substrate was cleaned with a standard RCA cleaning recipe followed by an HF etch. Four InAs nucleation layers were grown as a buffer layer at low temperature and annealed at

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S. Johansson, M. Egard, S. Gorji Ghalamestani, B. M. Borg, and E. Lind are with Solid State Physics, Lund University, Lund, Sweden. M. Berg, and L.E. Wernersson are with Electronics and Information Technology, Lund University, Lund, Sweden. (corresponding author is S. Johansson, phone: +46-46-222-7689; fax: +46-46-222-3637; e-mail: sofia.johansson@ftf.lth.se).

high temperature to enable good crystal quality of the epitaxial layer. The precursors used were trimethylindium (TMIn), arsine (AsH₃), and tetraethyltin (TESn), where TESn was added to give n-type Sn-doping in the epitaxial layer. A resistivity of 1.5 μΩm was deduced from Hall measurements together with an electron concentration of $3.7 \cdot 10^{19} \text{ cm}^{-3}$ and a mobility of $1.1 \cdot 10^3 \text{ cm}^2/(\text{Vs})$. A detailed description of the growth of the InAs layer can be found elsewhere [9].

B. Device Fabrication

InAs nanowire arrays were grown on the planar layer, by the Vapor-Liquid-Solid (VLS) method [10], to form the channel material in the transistors. For this purpose Electron Beam Lithography (EBL) was used to define arrays of Au discs on the InAs layer through thermal evaporation and a standard lift-off process. The nanowire diameter is set by the size of the Au discs, in the range of 25 to 40 nm. Nanowire arrays were formed by placing the Au disc in zigzag patterned double rows with a pitch of 300 nm. From these, nanowires were grown to a length of 1 μm by MOVPE at 420°C with the same precursors as for the planar layer. The nanowires were uniformly n-type doped with Sn at a flow of 11 sccm. This corresponds to a doping of about $2 \cdot 10^{18} \text{ cm}^{-3}$ [11].

After nanowire growth, the samples were transferred to a Savannah 100 Atomic Layer Deposition (ALD) system where a conformal layer of HfO₂ high-*k* dielectric, acting as the gate oxide, was deposited. The dielectric was deposited in 80 cycles at 250°C (5-7 nm HfO₂) with tetrakis(dimethylamino)hafnium (TDMA-Hf) and H₂O as precursors, starting with a TDMA-Hf pulse. One sample was also treated with a post deposition anneal (PDA) in a forming gas ambient in a rapid thermal processing (RTP) system at 300°C for 30 min, while another sample was kept as a reference. A typical nanowire array after high-*k* deposition and PDA is shown in Figure 1a. The array consists of in total 190 nanowires divided into five double rows, separated by a distance of 2 μm.

Mesa structures for device isolation were fabricated from the InAs planar layer by standard contact UV-lithography and wet etching in buffered oxide etch (BOE) and H₃PO₄:H₂O₂:H₂O. The mesa structures form epitaxial source contacts that are compatible with RF measurements. The resulting structure is shown in Figure 1b.

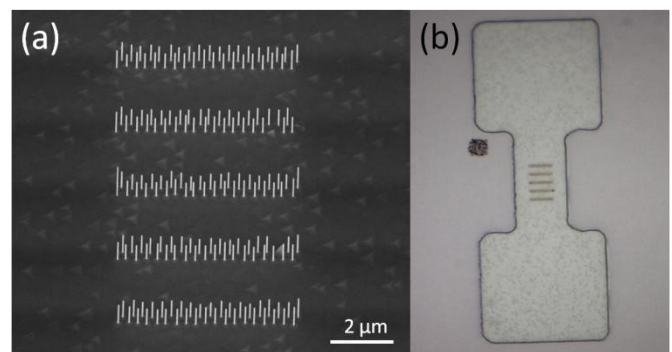


Figure 1. (a) SEM image of a nanowire array after deposition of HfO₂ and PDA. The scale bar is 2 μm and the sample is tilted 30°. The small triangular islands between the nanowires origin from the epitaxial growth of InAs. (b) Top view of an epitaxial InAs source contact mesa structure with a nanowire array and HfO₂ coverage.

The gate and drain contacts were processed on the nanowires in a layered fashion separated by organic spacers [4]. The source-gate spacer was achieved by spinning a S1800

series photoresist and ashing it to a thickness of about 150 nm. The wrap-gate metal of 60 nm W (planar thickness) was deposited by DC sputtering and etched back to a gate length of about 250 nm assisted by a thinned down photoresist and reactive ion etching (RIE) in a SF₆ and Ar gas mixture. The gate-drain spacer was applied in the same way as the source-gate spacer and was then used as an etch mask for removing the gate oxide from the upper part of the nanowires in a BOE wet etch. Finally, Ti/W/Au drain metal was deposited by sputtering. The vertical structure of the transistor is illustrated in Figure 2. UV-lithography was used for patterning of source pad, gate pad, vias and top metal layer. The UV-lithography masks were designed as a standard 50 Ω waveguide and the pitch between two adjacent devices were 100 μm. A micrograph of the layout is shown in Figure 3 with an inset showing the area defined as the transistor cell.

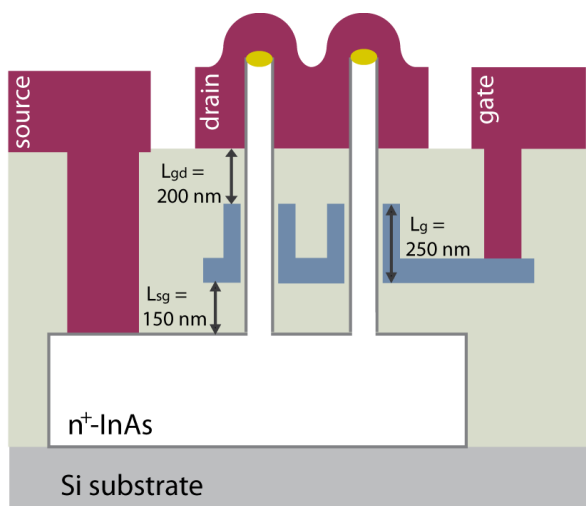


Figure 2. Schematic cross-section of the structure, showing the thicknesses of different layers.

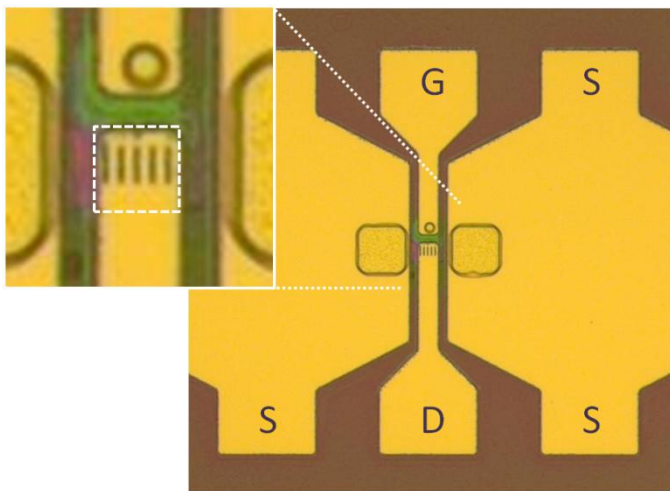


Figure 3. Top view of a completed device, showing the source (S), gate (G), and drain (D) pad layout. In the inset the 12 μm×12 μm transistor cell is indicated by a dashed line.

III. MEASUREMENTS

A. DC Characterization

Figure 4a and 4b show current-voltage characteristics typical for the InAs nanowire transistors, both with and without PDA treatment. Here, the source contact at the bottom of the nanowires is grounded, but the transistors show fairly symmetric characteristics. The PDA-treated transistor in Figure 4a consists of 182 nanowires with a diameter of 35 nm. Measurements by on-chip probing on this device show a peak extrinsic transconductance, $g_{m,max} = 3.1$ mS, and a maximum on-current, $I_{on,max} = 11.0$ mA, which corresponds to 155 mS/mm and 550 mA/mm, respectively, if normalized to the total circumference of the nanowires. The on-current of the devices presented here is similar to InAs nanowire FETs grown on an InAs substrate ($I_{on,max} = 760$ mA/mm) [5], which indicates a high crystal quality of the nanowires in spite of the usage of an Si substrate. However, some DC performance is lost as a consequence of the many modifications in the process scheme for RF compatible devices and significant improvements are expected after processing optimization. The lower peak transconductance can in part be attributed to the fairly long un-gated region between the source and gate, 150 nm, that increases the access resistance. It is also noted that the off-current is larger than anticipated for these devices.

A comparison of the output characteristics between a PDA-treated transistor and a not annealed reference transistor is shown in Figure 4a and 4b. In general, the drain current levels are about 5-10 times higher in the PDA-treated transistors, while the reference transistors show better on/off behavior. The on/off ratio is about 2.5 for the annealed device compared to 50 for the reference. The gate leakage current is low for both devices, $I_g = 62$ nA/μm² at $V_g = V_d = 1$ V for the annealed device and $I_g = 1.6$ nA/μm² for the reference. The sample exposed to PDA was also contact annealed at 200°C at the end of the device fabrication, but this annealing showed only a minor effect compared to the PDA.

PDA may affect the oxide and oxide-semiconductor interface in many ways. It has been reported that PDA may passivate border traps in the oxide [12] and, hence, decrease the channel resistance. Another explanation to the observed effect might be an energy shift of the oxide trap density peak.

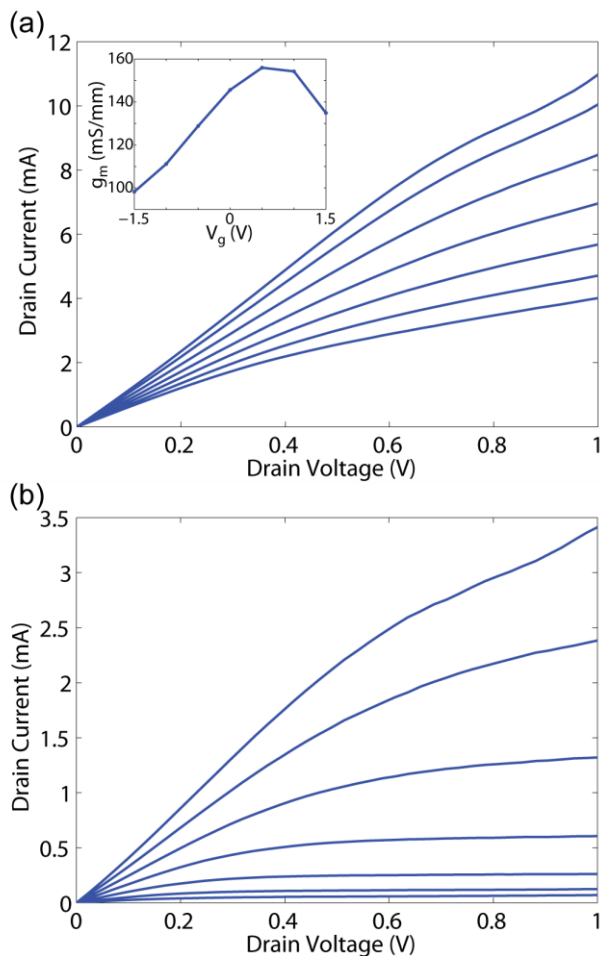


Figure 4. (a) Output characteristics of a PDA-treated transistor. The inset show the peak transconductance. (b) Output characteristics of a not annealed reference transistor. The gate voltages is varied from 1.5 V to -1.5 V in steps of 0.5 V.

In Figure 5 the on-currents, I_{on} , of the PDA-treated transistors with different nanowire diameters are illustrated. Here, a drain voltage, $V_d = 1$ V, and a gate voltage, $V_g = 1$ V, is used. All 32 transistors with nominally 190 nanowires on this sample are included. The nanowire diameters are 25, 30, 35, and 40 nm. The normalized on-currents show only a slight decrease with nanowire diameter down to 30 nm, although the access resistance, as deduced from DC measurements, is increased about a factor 2. This verifies the potential in scaling the nanowire diameter. The highest current levels are seen for nanowires with 40 nm in diameter with a mean value of 293 mA/mm and the lowest currents are seen for nanowires with 30 nm in diameter with a mean value of 220 mA/mm. The provided values are lower estimates of the on-currents as all transistors were normalized to 190 nanowires. The exact number of nanowires may in general be some percentages lower due to damage caused during device fabrication.

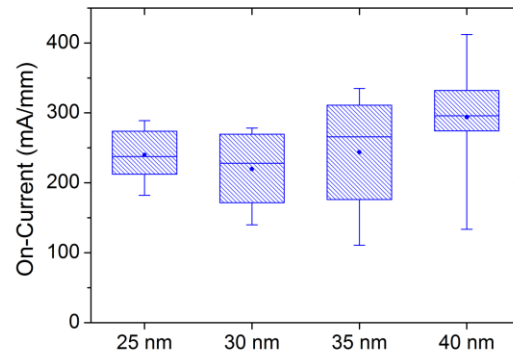


Figure 5. The normalized current for different nanowire diameters at $V_d = 1$ V and $V_g = 1$ V. The mean values are indicated by dots, the lower and upper border of the box indicate the 25th and 75th percentile, respectively and the end points indicate the minimum and maximum values. For simplicity all devices are normalized with 190 nanowires.

B. RF Characterization

The high frequency characteristics of the transistors are deduced from S-parameters measured with an Agilent E8361A network analyzer from 60 MHz to 20 GHz at an RF-power of -27 dBm. The measurements are conducted by on-chip probing on the standard 50 Ω pads shown in Figure 3. An off-chip Load-Reflect-Reflect-Match (LRRM) calibration is performed using a Cascade Microtech 101-1908 impedance standard substrate. The measured data is de-embedded by on-chip structures; the open structure resembles the transistor but without any conducting layers (including nanowires) inside the 12 $\mu\text{m} \times 12 \mu\text{m}$ transistor cell defined in the inset of Figure 3, and the short structure is simply a top metal layer short-circuited inside the transistor cell. In this way the device is defined as everything inside the 12 $\mu\text{m} \times 12 \mu\text{m}$ transistor cell. The de-embedding removes the parasitics from the large pads used for on-chip probing, but not the parasitics inside the transistor cell.

Deduced current gain, h_{21} , and unilateral power gain, U , for the transistor in Figure 4a is shown in Figure 6. Here, the transistor is DC biased at $V_g = -0.5$ V and $V_d = 1$ V. The obtained extrinsic unity current-gain cut-off frequency, f_t , is 9.3 GHz and the extrinsic maximum oscillation frequency, f_{max} , is 14.3 GHz. This is, to the author's knowledge, the highest f_t reported for any vertical nanowire transistor. As a comparison, it can be mentioned that the highest measured values on the not annealed reference sample was $f_t = 2.0$ GHz and $f_{max} = 2.7$ GHz. The lower f_t and f_{max} originates from the smaller extrinsic transconductance. We attribute this mainly to higher source/drain resistance of this device. A higher channel resistance originating from PDA can also not be ruled out. Comparison may also be made to reported measurements on lateral nanowires, showing $f_t = 7.5$ GHz and $f_{max} = 15$ GHz [13].

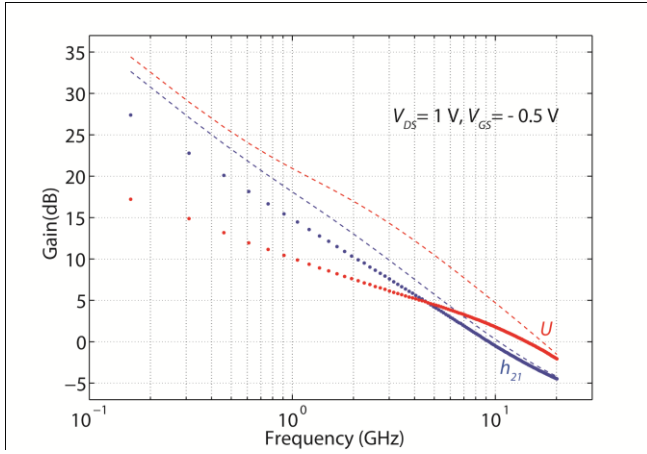


Figure 6. Unilateral power gain, U , and current gain, h_{21} from measured data (dots) and deduced from the small-signal equivalent model (dashed lines). The transistor is DC biased at $V_d = 1$ V and $V_g = -0.5$ V.

In Figure 7, f_i and f_{max} are plotted as a function of V_d and V_g . It can be seen that the highest values are obtained for the most negative gate voltages with peaks for $V_d = 1$ V. As seen in the DC data, g_m peaks for positive gate biases, while the output conductance is lower for negative gate biases. As a consequence, the highest f_i and f_{max} are at present found under bias conditions where g_m not is maximized.

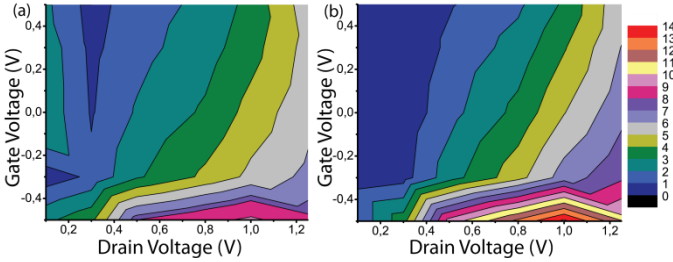


Figure 7. Mapping of (a) the unity current-gain cut-off frequency, f_i , and (b) maximum oscillation frequency, f_{max} , versus V_g and V_d . The colors represent frequencies from 0 to 14 GHz. 30 DC bias points were used for both maps.

IV. RF MODELING

From the measured S-parameters, a small-signal equivalent model is deduced, as shown in Figure 8. The dashed traces in Figure 6 are calculated from the small-signal equivalent model. The agreement between this model and the measured data is also shown in the Smith chart in Figure 9.

The model shown in Figure 8 is a standard FET model with the addition of two current-sources that model the impact ionization and band-to-band tunneling present in the InAs FET. The narrow bandgap of InAs makes it susceptible to impact ionization and band-to-band tunneling effects for large applied drain biases [14]. This leads to an increased output conductance due to both a direct increase in the drain electron current, as well as hole accumulation in the gate region. This will in turn cause a positive feedback mechanism similar to the kink-effects in SOI MOSFETs and InP-based HEMTs [15]. Following the approach in [15], these effects are

modeled using two frequency dependent current-sources described in (1) and (2). Due to the finite generation rate of impact ionization and band-to-band tunneling, the effects are expected to mainly be visible at lower frequencies, which is modeled using one effective generation rate, τ_i .

$$g_{i1} = \frac{g_{i10}}{1+j\omega\tau_i} \quad (1)$$

$$g_{i2} = \frac{g_{i20}}{1+j\omega\tau_i} \quad (2)$$

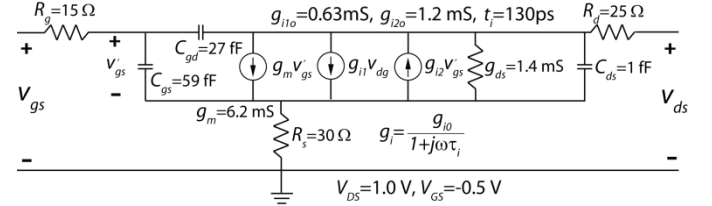


Figure 8. Small-signal equivalent model of the transistor.

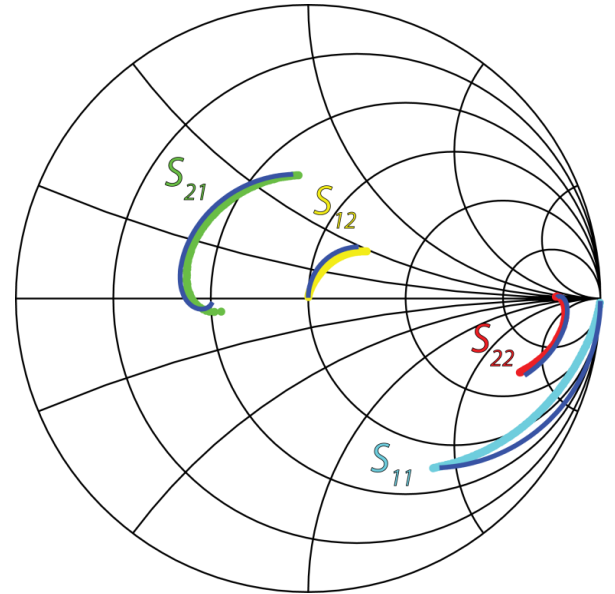


Figure 9. Smith chart showing the S-parameters from 60 MHz to 20 GHz. Different colors (cyan, green, yellow and red) represent the measured data. Dark blue lines represent modeled S-parameters.

For extraction of the model in Figure 8, the source resistance, R_s , and drain resistance, R_d , were first subtracted from the transistor characteristics. The initial value of R_s and R_d were estimated from DC measurements. These resistances were then used as initial parameters when optimizing the model with respect to the error in the Y-parameters, ϵ , between the measurements and the model, given by (3).

$$\epsilon = 25 \cdot \sum_{ij} \left(\sum_{freq} \frac{|measY_{ij} - simY_{ij}|^2}{|measY_{ij}|^2} \right) \frac{1}{N_{freq}} \quad (3)$$

The admittance of the intrinsic device is given by (4)-(7), provided that (8) is fulfilled, which is true for the frequency interval considered here.

$$y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2=0} = R_g \omega^2 (C_{gs} + C_{gd})^2 + j\omega (C_{gs} + C_{gd}) \quad (4)$$

$$y_{12} = \left. \frac{i_1}{v_2} \right|_{v_1=0} = -R_g \omega^2 C_{gd} (C_{gd} + C_{gs}) - j\omega C_{gd} \quad (5)$$

$$y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2=0} = g_m - g_{i1} - g_{i2} - \omega^2 C_{gd} R_g (C_{gs} + C_{gd}) - j\omega R_g (g_m - g_{i1} - g_{i2}) (C_{gs} - C_{gd}) - j\omega C_{gd} \quad (6)$$

$$y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1=0} = g_{ds} + g_{i1} + R_g \omega^2 C_{gd}^2 + \omega^2 R_g^2 C_{gd} (C_{gs} + C_{gd}) (g_m - g_{i1} - g_{i2}) + j\omega (C_{ds} + C_{gd}) + j\omega R_g C_{gd} (g_m - g_{i1} - g_{i2}) - j\omega^3 R_g^2 (C_{gs} + C_{gd}) C_{gd}^2 \quad (7)$$

$$\omega^2 (C_{gs} + C_{gd})^2 R_g^2 \ll 1 \quad (8)$$

The values of the different elements in Figure 8 are then deduced in a similar way as presented in [16]. However, the transconductance, g_m , and output conductance, g_{ds} , cannot be deduced in the low frequency limit as done in [16], as g_{i1} and g_{i2} influences Y_{21} and Y_{22} at low frequencies. Instead, after subtracting the influence of R_g on the device, g_m and g_{ds} can be deduced at a high frequency ($>1/\tau_i$), and g_{i01} , g_{i02} , and τ_i can be deduced from (9)-(11), as shown in Figure 10-12.

$$\frac{1}{\text{Re}(Y_{22}|_{R_g \text{ subst.}}) - g_{ds}} = \frac{1}{g_{i10}} + \frac{(\omega\tau_i)^2}{g_{i10}} \quad (9)$$

$$\frac{1}{\text{Re}(Y_{21}|_{R_g \text{ subst.}}) - g_m} = \frac{1}{g_{i10} + g_{i20}} + \frac{(\omega\tau_i)^2}{g_{i10} + g_{i20}} \quad (10)$$

$$\frac{-\omega}{\text{Im}(Y_{22}|_{R_g \text{ subst.}}) - \omega(C_{ds} + C_{gd})} = \frac{1}{g_{i10}\tau_i} + \frac{(\omega\tau_i)^2}{g_{i10}\tau_i} \quad (11)$$

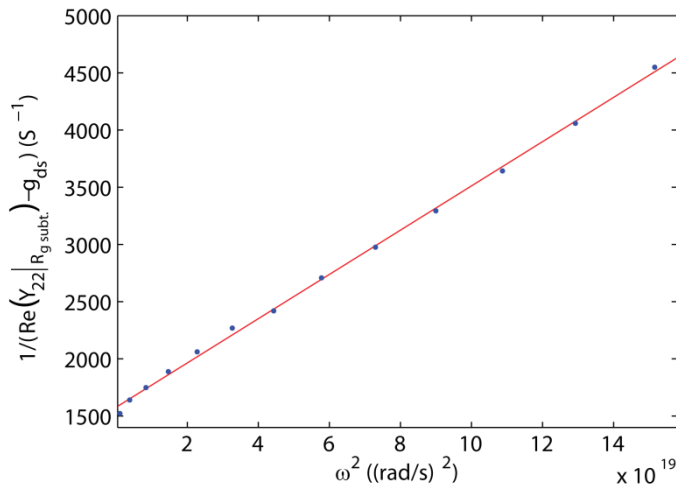


Figure 10. Frequency dependence of (9) for extraction of g_{i10} .

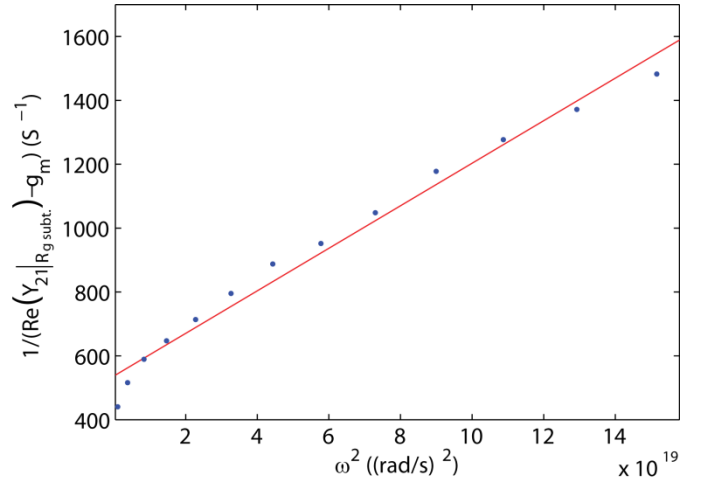


Figure 11. Frequency dependence of (10) for extraction of g_{i20} .

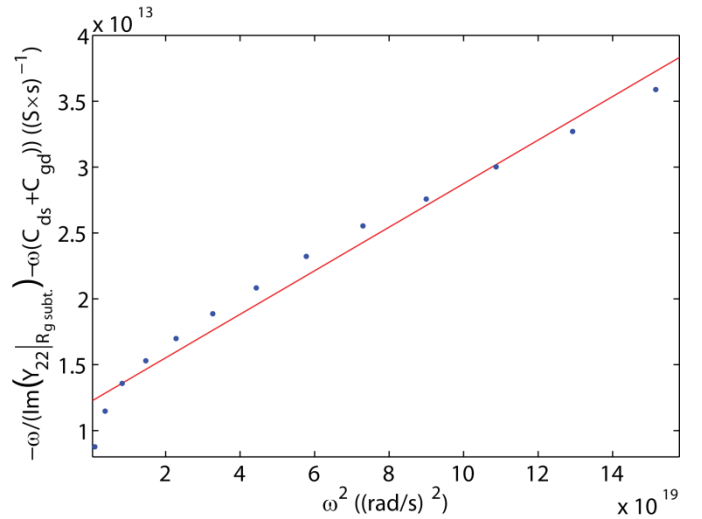


Figure 12. Frequency dependence of (11) for extraction of τ_i .

The model maps the effect of impact ionization, however, additional elements need to be included in order to fully model the input of the device. The total error, defined in (3) is 2.2 %. Fairly good agreement between modeled and measured h_{21} is also evident from Figure 6. However, U deviates from the simulated data, showing a roll-off close to -10 dB/decade, rather than at the expected -20 dB/decade. From the small-signal model, we have identified this discrepancy to originate from a frequency dependent loss on the input, which is not included in the model. One possible explanation is that this is an effect related to border traps in the oxide [17]. More investigations are, however, needed to pin-point the origin. Interestingly, a non-ideal behavior is also seen on measurements on arrays of lateral InAs wires on a flexible substrate [18].

In the model, an intrinsic transconductance of $g_{mi} = 6.2$ mS is deduced. This is a factor of 2 higher than the extrinsic transconductance, $g_m = 3.1$ mS, which fits fairly well with theory.

The contribution from the intrinsic capacitance is estimated to be $L_g \cdot n \cdot C_i = 34$ fF. This means that a large part of the deduced total gate capacitance, $C_{gg} = C_{gd} + C_{sg} = 86$ fF, originates from parasitic capacitance, mainly created by the

relatively large overlap between the source, gate and drain pads in the vertical geometry. A reduced pad overlap realized by high resolution lithography, such as EBL, for critical pad features will hence improve the RF performance. Simulations also show that the parasitics can further be reduced by decreasing the intra-nanowire pitch [19].

The epitaxial InAs mesa structure contributes with 5Ω to R_s . This value can be reduced by increased doping or by scaling the metal-to-nanowire distance. The contact resistance between the epitaxial mesa structure and the metal is calculated from DC resistance measurements to 15Ω . Optimizations of this contact resistance would, hence, lower the total source resistance obtained in the model, $R_s = 30 \Omega$, significantly. Finally it may also be noted that the effect of impact ionization and band-to-band tunneling may be reduced by band-gap engineering in the channel, where a barrier is introduced to reduce the dynamic processes [20].

V. CONCLUSIONS

We have in summary demonstrated the integration of vertical InAs nanowire FETs on an Si substrate. The transistors show good DC performance, with a $g_m = 0.155$ S/mm and $I_{on} = 0.55$ A/mm, combined with an $f_t = 9.3$ GHz. An RF-model is also presented. The RF performance is mainly limited by parasitic gate-source and gate-drain capacitances. Further scaling of the source/drain line widths will allow for better RF performance.

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