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InAs/GaSb Vertical Nanowire TFETs on Si for Digital and Analogue Applications

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Abstract

Vertical InAs/GaSb nanowire TFETs with diameters of 20 nm and 25 nm have been fabricated and characterized. The influence of diameter, gate-placement, and nanowire numbers have been studied. The best device shows a subthreshold swing of 68 mV/dec at V_{DS} = 0.3 V and 26 µA/µm at V_{DS} = 0.3 V and V_{GS} = 0.5 V. It achieves a self-gain larger than 100 with high transconductance efficiency.

Introduction

Tunneling Field-Effect Transistors (TFETs) is a leading contender steep slope transistor for future low power VLSI applications. In low-power digital and analogue applications the TFETs need to provide high currents at low drive voltages [1-2]. A structure with desirable properties is a vertical InAs/GaSb nanowire, which can provide high on-currents (I_{on}) due to the broken band gap and the low channel effective mass [3-4], and additionally the gate-all-around geometry provides good electrostatic control [5]. In this work, we vary the transistor layout using inorganic spacer technology and characterize the performance with a particular focus on analog applications.

Device fabrication

InAs/GaSb nanowires were grown directly on a 200-nm-thick n^+-InAs buffer layer on a highly resistive Si (111) substrate (ρ=5.5 kΩ-cm) using MOVPE [6]. The number and diameters of the nanowires were defined using Au-seed particles prepared with EBL and lift-off. After growth, the InAs segment of the nanowires have diameters of either 40 nm or 45 nm. The length of InAs-segment and GaSb-segment is 300 nm and 250 nm, respectively. The bottom half of the InAs is n-doped by tetraethyltin (TESn) with an estimated concentration of 10^{18} cm^{-3}. The upper half of the InAs, which is the position of the channel region, was unintentionally doped with an estimated background carrier concentration of 10^{17} cm^{-3}. The GaSb segment is p-doped with an estimated concentration of 10^{19} cm^{-3} using diethlyzinc (DeZn). The number of the nanowires in each TFET is varied from 1 to 8. The InAs diameter is reduced to 20 nm or 25 nm by utilizing digital etching. The nanowires are covered with a high-k bilayer of 1 nm Al_2O_3 and 4 nm HfO_2 with an estimated EOT of 1.4 nm. The drain-gate spacer is fabricated using EBL exposed hydrogen silsesquioxane (HSQ), where the final thickness of the HSQ spacer (0-170 nm) is defined by the used dose [7] for different devices avoiding organic spacers [8]. As the HSQ thickness is increased, the overlap of the gate-metal on the drain-side decreases while it increases on the source-side overlapping the GaSb. Reactive sputtering is used to deposit a W gate metal. The physical gate-length, approx. 300 nm, is set by spinning on and etching back an organic film with O_2-plasma and reactive ion etching of W using SF_6. A gate-source spacer is fabricated using organic spacer. A Ni/Au top-metal is finally defined. The final structure and process-flow can be viewed in Fig. 1 and 2, respectively. A SEM image of a nanowire with gate is shown in Fig. 3.

Experimental results and discussion

In Fig. 4 and 5 the output and transfer characteristics for a 20 nm diameter TFET with the best subthreshold swing (*S*) is presented, achieving a *S* and I_{on} of 68 mV/dec at V_{DS} = 0.3 V and 26 µA/µm at V_{DS} = 0.3 V and V_{GS} = 0.5 V. This device shows also the lowest DIBL of 5 mV/V. Output data from a 25 nm diameter TFET with the highest I_{on} is presented in Fig. 6, achieving a *S* of 138 mV/dec at V_{DS} = 0.3 V and 127 µA/µm at V_{DS} = 0.3 V and V_{GS} = 0.5 V. In Fig. 7 the devices with the best subthreshold swing for each HSQ thickness are compared for the two diameters, where the best *S* is obtained on the nanowires with 20 nm diameter for every HSQ thickness. The improved electrostatics for the 20 nm TFET is confirmed in Fig. 8, with a lower *S* for these devices independently of the number of nanowires in the device. The lowest *S* is measured for a TFET consisting of one nanowire only, and although the number of the nanowire increases from 1 to 6 the *S* increases only from 68 mV/dec to 81 mV/dec for the best devices. Similarly the I_{min} only weakly increases, Fig. 9. The R_{on} for the TFETs with 20 nm and 25 nm diameter is decreased, as shown in Fig. 10, when the HSQ is thinner and the gate position is lowered, reaching a lowest R_{on} of 1.6 kΩ µm. In Fig. 11, the self-gain (g_m/g_d) of the devices with the best currents for 20 and 25 nm is compared. The device with 20 nm nanowires exhibits higher self-gain, but at lower g_m, verifying the improved electrostatics and the lower drive current. In Fig. 12 the self-gain of the device with best *S* is presented, demonstrating that the improved electrostatic control enhances both on- and off-state performance, reaching a self-gain of 100. In Fig. 13 the 20 nm device with the best I_{on} is compared to the 20 nm device with best the *S*. The TFET with the best *S*, shows a higher transconductance efficiency (g_m/I_{DS}) at higher self-gain. At V_{DS} 0.3 V, a self-gain of about 100 can be obtained at g_m/I_{DS} up to 35 for g_m up to 120 µS/µm as demonstrated in Fig. 13. The fabrication technique used allows fabrication of operational TFETs with 11 nm diameter as shown in Fig. 14, demonstrating an *S* of 123 mV/dec at V_{DS} = 0.3 V and an I_{on} of 1.8 µA/µm at V_{DS} = 0.3 V and V_{GS} = 0.5 V. In Fig. 15 the device with best S is benchmarked against [9], achieving lowest slope at higher I_{DS} and higher I_{on}.

Conclusion

Diameter scaling has a strong impact on the electrostatic control in vertical InAs/GaSb TFETs verified by better *S*, DIBL and g_m/g_d. Furthermore, increasing the number of nanowires does not considerably impact S. The TFETs with the best *S*, achieve an *S* and I_{on}, of 68 mV/dec and 26 µA/µm at V_{DS} = 0.3 V. It shows a self-gain >100 with high transconductance efficiency.

Acknowledgment

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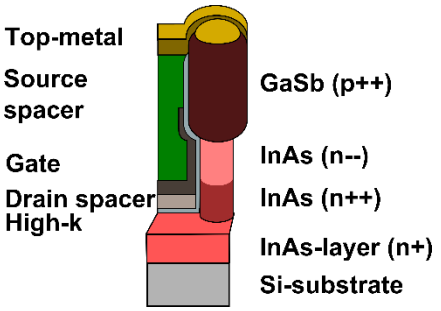

Fig.1 Schematic of the TFET

- Definition of Au-seed particles
- MOVPE growth of nanowires
- Digital etching
- Apply high-k
- HSQ drain-gate spacer using EBL
- Sputter on Tungsten
- Define gate-length
- Gate-pad definition with UV-lithography
- Organic source-gate spacer
- Etch out gate-via and drain-via
- Sputter on Nickel and Gold
- Define gate, drain and source contact-pads with UV.

Fig. 2 Process flow

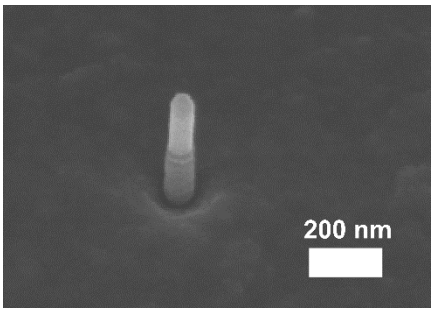

Fig.3 SEM image of InAs/GaSb nanowire with InAs covered by the gate-metal and only GaSb visible.

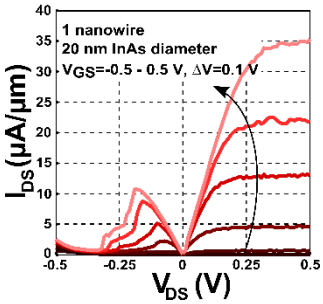

Fig. 4 Output data from the 20 nm device with best subthreshold swing.

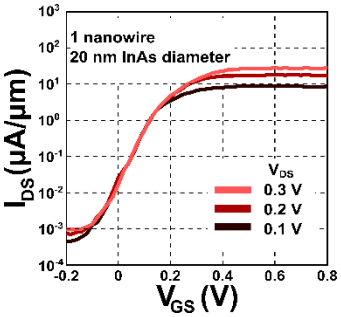

Fig. 5 Transfer data from the 20 nm device with best subthreshold swing.

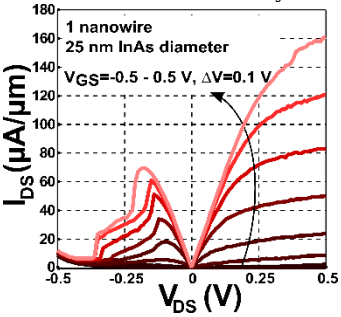

Fig. 6 Output data from the 25 nm device with highest I_{on}.

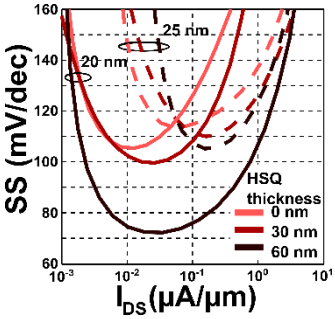

Fig. 7 Subthreshold swing vs I_{DS} for V_{DS} = 0.3 V for devices with best S for 20 and 25 nm TFETs with different HSQ thickness

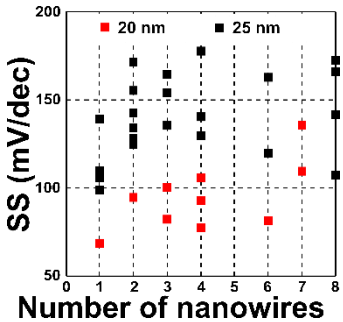

Fig. 8 Subthreshold swing vs number of nanowires in the device for V_{DS} = 0.3 V.

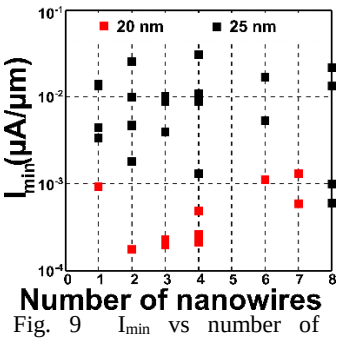

Fig. 9 I_{min} vs number of nanowires in the device for V_{DS} = 0.3 V.

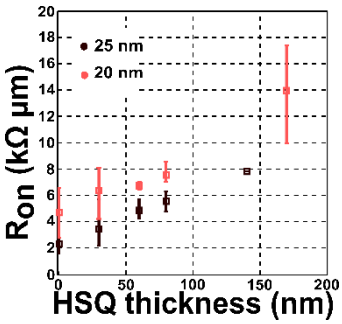

Fig. 10 R_{on} vs HSQ thickness.

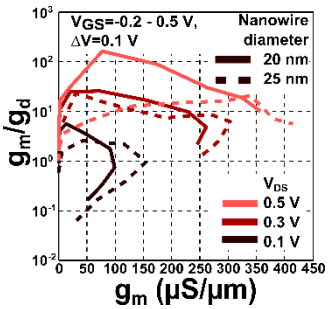

Fig. 11 Comparison of self- gain for devices with best currents for 20 nm and 25 nm TFETs, respectively.

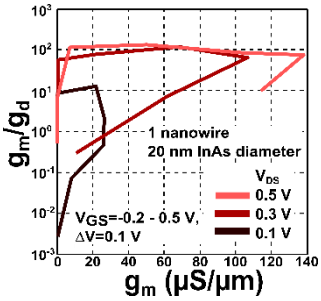

Fig. 12 Self-gain for the 20 nm TFET with best subthreshold slope.

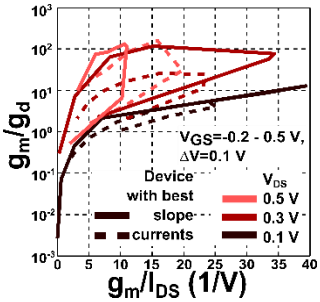

Fig. 13 Comparison of transconductance effeciency between 20 nm TFETs with best subthreshold slope and highest on-current

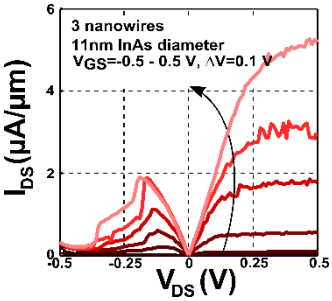

Fig. 14 Output data for 11 nm diameter TFET.

TABLE I
BENCHMARKING

Parameter	Best device	Dewey [9]
Minimum point SS (V_{DS} = 50 mV)	66 mV/dec	58 mV/dec
Current for lowest SS (V_{DS} = 50 mV)	9.2 nA/μm	0.8 nA/μm
On-current (I_{off} = 10 nA/μm, V_{DS} = 0.3 V, V_g-$V_{g,off}$ = 0.3V)	11.28 nA/μm	1.3 nA/μm

Fig. 15 Benchmarking best device against Intel data from IDEM 2011 [9].