III-V Heterostructure Nanowire Tunnel FETs

Lind, Erik; Memisevic, Elvedin; Dey, Anil; Wernersson, Lars-Erik

Published in:
IEEE Journal of the Electron Devices Society

DOI:
10.1109/JEDS.2015.2388811

2015

Document Version:
Publisher's PDF, also known as Version of record

Received 5 September 2014; revised 7 October 2014 and 13 November 2014; accepted 11 December 2014. Date of current version 22 April 2015.
The review of this paper was arranged by Editor D. Esseni.

Digital Object Identifier 10.1109/JEDS.2015.2388811

III-V Heterostructure Nanowire Tunnel FETs

ERIK LIND, ELVEDIN MEMIŠEVIĆ, ANIL W. DEY, AND LARS-ERIK WERNERSSON

Department of Electrical and Information Technology, Lund University, Lund 221 00, Sweden

CORRESPONDING AUTHOR: E. LIND (e-mail: Erik.Lind@eit.lth.se)

This work was supported in part by the Swedish Research Council (VR), in part by the Swedish Foundation for Strategic Research, in part by the Knut and Alice Wallenberg Foundation, and in part by the European Union Seventh Framework Program E2SWITCH under Grant 619509.

ABSTRACT In this paper, InAs/GaSb nanowire tunnel field-effect transistors (TFETs) are studied theoretically and experimentally. A 2-band 1-D analytic tunneling model is used to calculate the on- and off-current levels of nanowire TFETs with staggered source/channel band alignment. Experimental results from lateral InAs/GaSb are shown, as well as first results on integration of vertical InAs/GaSb nanowire TFETs on Si substrates.

INDEX TERMS Tunnel field effect transistors (TFET), InAs, GaSb, III-V, broken gap.

I. INTRODUCTION

Tunneling Field-Effect Transistors (TFETs) are among the most promising devices for achieving very low power operation, due to the possibility to achieve a steep inverse sub threshold slope below the thermionic limit of 60 mV/decade [1], [2].

Atomistic modeling has shown that TFETs potentially can outperform CMOS at low supply voltages [3], [4] TFETs with inverse slopes below 60 mV/decade have been demonstrated in several geometries and material systems, although with low on-currents [2], [5].

To achieve a large on-current, material combinations with small effective tunneling mass, and narrow staggered or broken channel band gaps are needed [3], [6]. Device operation is further enhanced through a very strong electrostatic gate coupling, for which the coaxial gate all around geometry is ideal. These points suggest a device design utilizing the 6.1Å III-V materials in a 1D nanowire geometry [7]. Broken or staggered bandgap InAs/AlGaSb TFETs have demonstrated high on-currents, although currently with larger subthreshold slopes [8]–[10]. In fact, the evolution of the III-V nanowire TFETs may be regarded as an extension of the III-V Metal-Oxide-Semiconductor Field-Effect Transistors in planar and non-planar geometries [11]. In this paper, we first present a simple analytic model for the current levels in staggered band gap 1D TFETs, based on the Wentzel–Kramers–Brillouin (WKB)-approximation. Status for InAs-GaSb TFET results will be presented, as well as recent experimental achievements demonstrating integration of vertical nanowire InAs/GaSb TFETs on Si substrates.

II. 1-D TUNNEL FET MODEL

A. ON-CURRENT

We describe the n-type TFET on-current in a 1D, single subband nanowire using the Landauer-Buttiker formalism as

$$I_{on} = \frac{2q}{h}\int_{E_{v,s}}^{E_{c,c}} T(E)\, f_0\,(E, E_{Fs})\, dE \approx \frac{2q}{h}\int_{0}^{qV_{on}} T(E)\, dE \qquad (1)$$

where $E_{\mathrm{v,s}}$ is the source valence subband edge, $E_{\mathrm{c,c}}$ the channel conduction subband edge, $T(E)$ the transmission probability describing the tunneling between the valence to the conduction band, E_{FS} the source Fermi energy, and f_0 the Fermi-Dirac distribution function [2]. This is assuming that the drain voltage is large enough to suppress any back injection from the drain to the source. If the source is not degenerately doped, $f_0 \approx 1$ inside the valence band of the source.

The allowed window for tunneling between source and drain is $\mathrm{q}V_{\mathrm{on}}$, as shown in Fig. 1(b). Using $E_{\mathrm{v,s}} = 0$ as the reference energy, we then obtain the approximate equation for I_{on}. Due to quantization for narrow band gap nanowires, the relevant sub band edges and effective band gap will increase with reduced nanowire diameter [12].

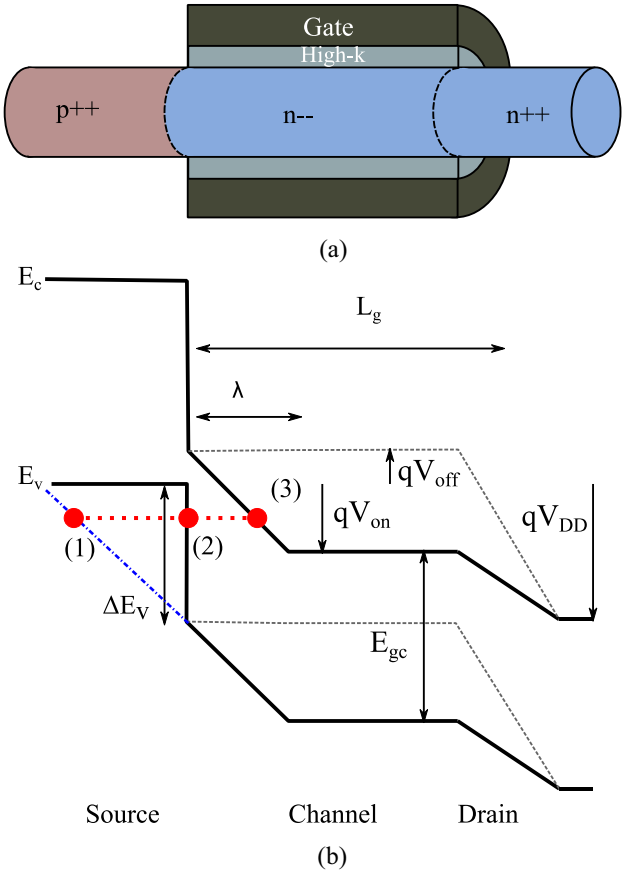

FIGURE 1. **(a) Schematic illustration of a nanowire n-TFET. (b) Idealized schematic band diagram of a staggered band gap 1-D TFET, with a p^+ source and n^- channel region. At $V_{GS} = 0$ V, we assume that the channel sub band edge is aligned to the source sub band edge. Solid lines are band edges for the device in the on-state, dotted lines corresponds to the off-state. For a staggered band gap, the tunneling occurs from points (2)–(3), whereas for a homojunction TFET (dash-dotted line) the tunneling would occur from (1)–(3).**

To calculate the transmission probability T(E), the WKB approximation

$$T(E) = \exp\left(-2\int_{x_1}^{x_2} |k_x(E)|\, dx\right) \tag{2}$$

is utilized, where the imaginary wave vector k_x is obtained through the Kane 2-band k·p model [13], where x_1 and x_2 are the classical turning points.

Assuming that the TFET is operating in the quantum capacitance limit with ideal electrostatics and ignoring any potential drop in the source, we can as shown in Fig. 1(b) approximate the electric field along the nanowire direction as

$$\varepsilon \approx \frac{E_{gc} - \Delta E_v + qV_{on}}{q\lambda}, \tag{3}$$

where λ is determined from Poisson's equation and approximately corresponds to the geometric length scale. As shown in Fig. 1(b), E_{gc} is the channel band gap and qV_{on}

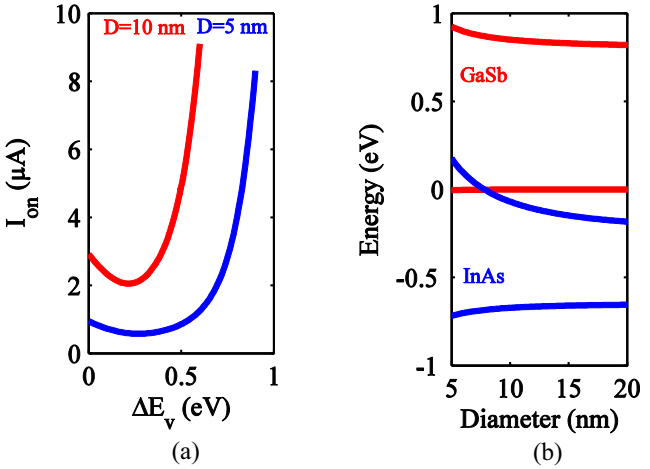

FIGURE 2. **(a) Calculated on-current for $D = 10$ nm and $D = 5$ nm InAs channels as a function of the ΔE_V. $\Delta E_V = 0$ corresponds to a homojunction device and $\Delta E_V = E_g$ to a just broken band gap. (b) Calculated conduction and valence sub band edges for GaSb and InAs, assuming a bulk valence band offset of VBO = 0.56 eV.**

is the shift in band edges due to the applied voltage, For a constant electric field, the 2-band model results in $Im(k_x) = \frac{1}{\hbar}\sqrt{\frac{2m^*}{E_{gc}}}\sqrt{E_{gc}^2/4 - q^2\varepsilon^2x^2}$. For the heterojunction TFET, the classical turning x_1 is modified as indicated in Fig. 1(b). We obtain the integration limits to $x_2 = E_{gc}/2q\varepsilon$ and $x_1 = -E_{gc}\ /2q\varepsilon + (\Delta E_v - E)/q\varepsilon$, with E measured with respect to the valence band edge.

After integration, we obtain

$$T(E) = \exp\left(-\frac{\sqrt{m^*}E_{gc}^{\frac{3}{2}}}{2\sqrt{2}q\varepsilon\hbar} \times \left[\frac{\pi}{2} - \left(\sqrt{1-y_s^2}y_s + sin^{-1}(y_s)\right)\right]\right), \tag{4}$$

where

$$y_s(E) = 2\left(\frac{\Delta\ E_v - E}{E_{gc}}\right) - 1;\ \ 0 < E < \Delta\ E_v \tag{5}$$

accounts for the increased transmission due to the staggered band gap. Note that at tunneling energies $E > \Delta E_v$, $y_s = -1$ and T(E) becomes equal to the conventional homojunction transmission expression. For a broken band gap, $y_s = 1$ and T(E) becomes unity.

Equation 1 is numerically integrated using equations (3-5) to obtain the on-current for a staggered band gap system.

Fig. 2(a) shows calculated on tunnel currents for two InAs channels, with $D = 5$ nm ($E_g = 0.9$eV, $m^* = 0.05\ m_0$) and $D = 10$ nm ($E_g = 0.6$ eV, $m^* = 0.04\ m_0$) [12] as a function of the valence band offset ΔE_v, assuming $V_{ON} = 0.3$V and $\lambda = 5$ nm. Quantization will shift the sub band edges in the InAs channel, and we are here assuming a theoretical GaSb-like source providing the appropriate band alignment. The larger band gap for thinner nanowires leads to a reduced tunnel current for a non-staggered band alignment, but the

on-current can be recovered by increase of the ΔE_v. The higher effective mass for thinner nanowires will also lead to a decreasing transmission due to a high tunneling mass in the channel, as visible in (4). For 2nm $< D <$ 25 nm the InAs lowest sub band mass for (111) InAs wires can be well approximated from $sp^3d^5s^*$ modeling as $\frac{m^*}{m_0} = 0.02 + 0.1682 \cdot D^{-1.04}$ [14].

For small valence band offsets, the current decreases with respect to ΔE_v. This is due to the reduced built-in ε-field as shown in (3), which leads to a decreases in the on-current. A key finding here is thus that the magnitude of ΔE_v needs to be a substantial part of E_{gc} to be beneficial. While simple, the calculated on-current corresponds well to the more advanced atomistic, self-consistent modeling for similar on-bias conditions. For comparison, an $I_{ON} \approx 100$ μA/μm is obtained from tight binding calculations on a $D = 5$ nm InAs/GaSB TFET [4], compared with 150 μA/μm from the WKB-model. For a $D = 10$ nm InAs/AlGaSb TFET, a 4-band k·p calculation reports $I_{ON} = 175$ μA/μm [15], whereas the WKB-model gives $I_{ON} = 210$ μA/μm. This suggests that the WKB-model can be used to qualitative estimate the on-current in a very simple manner.

The band alignments for the InAs/GaSb system will vary with changing nanowire diameter. Fig. 2(b) shows results from band structure calculations [12], [16] as the nanowire diameter is varied. Quantization is stronger for InAs as compared with GaSb, mainly increasing the conduction band energy. A broken band gap is expected to exist for diameters larger than about 8 nm. At 5 nm, we expect $\Delta E_v = 0.18$eV. For large diameters, ΔE_v can experimentally be changed to achieve $\Delta E_v > 0$ through usage of an AlGaSb source or an $In_{1-x}Ga_xAs$ channel.

B. OFF-CURRENT

In order to estimate the minimum off-current in the TFET, we also consider direct source-to-drain tunneling. Thermal diffusion current as well as drain-edge tunneling is thus ignored. For the direct tunneling, the potential barrier can here roughly be approximated as a square [13], assuming λ is small compared to the gate length, resulting in an expression for the tunneling current as

$$I_{off} \approx \frac{2q}{h} \int_{E1}^{E2} exp\left(-\frac{2\sqrt{2m^*}L_g}{\hbar}\sqrt{E\left(1-\frac{E}{E_{gc}}\right)}\right) dE, \quad (6)$$

where E is taken with respect to the top of the channel sub band, and E_1 and E_2 defines the tunneling window between the source valence band edge and drain conduction band edge. A low off-current thus requires larger E_{gc} and m^*, as well as a long L_g.

C. TOTAL CURRENT

Fig. 3 shows the complete calculated current for a $L_g = 20$ nm device with a $D = 5$nm InAs nanowire channel with $\Delta E_v = 0.18$ eV, assuming that the valence and conduction band are aligned for $V_{gs} = 0$ V.

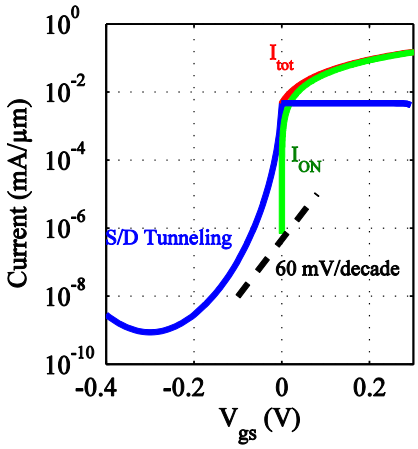

FIGURE 3. Simulated tunnel currents for a InAs-based TFET at $V_{DS} = 0.3$ V. The on-current, direct source-to-drain current, and the total combined current as well as a 60 mV/decade reference line are displayed.

For $V_{gs} > 0$, the current is dominated by tunneling through the staggered band, increasing strongly with increasing V_{GS} while the direct source-to-drain tunneling remains almost constant, with a slight decrease at larger V_{GS}. The largest contribution to the source-to-drain tunneling is from to carriers tunneling close to the channel conduction band edge, remaining constant at $V_{GS} > 0$, whereas it is determined by the direct source-to-drain tunneling at lower V_{gs}, since there is no overlap between the source and channel bands. Devices with long gate lengths should show similar on-currents as shorter devices, but with reduced source-to-drain leakage, as long as the charge transport in the InAs channel is not limiting the device performance.

The off-state current can, for an ideal device, be reduced substantially below the 60mV/decade limit, with an on-current of $\sim$ 100 μA/μm at $V_{DS} = 0.3$V. We also expect a very weak temperature dependence, mainly originating from the small change in band gap with temperature. Experimental III-V devices, often show an inverse subthreshold slope >> 60 mV/decade, with a clear temperature dependence in the off-current, indicating additional leakage currents.

D. PARASITIC EFFECTS

There are several factors increasing the off-current and subsequently the subthreshold swing for TFETs. For example, trap assisted tunneling [17], [18], interface defects [19], phonon assisted tunneling [4] and band tails [20] all can contribute to excess off-current.

From a detailed balance analysis [17], a simple expression for trap assisted tunneling current can be obtained as

$$I_{TAT} \propto N_T T_T(E)\, e^{\frac{E_C - E_T}{kT}}, \quad (7)$$

where N_T is the trap concentration, $T_T(E)$ the tunneling probability into a trap state from the source and E_T the trap energy. If the trap density and tunneling probability is high enough, the off-current can be dominated by the trap

assisted tunneling. The exact shape of I_{OFF} then depends on the spatial positions for the traps within the transistor and their energy distribution, but in general the excess current leads to a degraded subthreshold swing. For short gate length nanowire TFETs, single traps can lead to degraded slopes [21]. A strong reduction in the concentration of traps is thus a key element to achieve sub 60 mV/decade operation.

Interface traps also reduce the minimum subthreshold swing, due to the reduced band movement with respect to the applied gate voltage [19]. Standard MOS electrostatics yields

$$\delta E_{gc} = \frac{qC_{ox}}{C_s + C_{ox} + q^2 D_{it}} \delta V_{gs}, \tag{8}$$

where C_s is the semiconductor capacitance, and D_{it} the interface trap density. While Si TFETs have low D_{it} values, III-V high-κ interfaces can have substantially higher amount of interface traps. InAs, relevant for staggered band gap TFETs, typically have U-shaped D_{it} profiles, with increasing D_{it} towards the valence band edge and into the conduction band [22], limiting the subthreshold slope also for a TFET. However, there have recently been strong improvement in the high-κ quality, with InAs channel planar MOSFETs having demonstrated 70 mV/decade swing [23].

III. LATERAL NANOWIRE TFETS

State-of-the-art all-III-V nanowire TFETs have been demonstrated using lateral GaSb/InAs(Sb) nanowires [9]. We here present an overview of our work on lateral III-V nanowires, as well as the first experimental results from integration of vertical InAs-GaSb nanowire TFETs on a Si substrate. Lateral nanowire devices are based on nanowires grown on a host substrate and then transferred to a device wafer. This allows for a higher flexibility in the nanowire growth, suitable to explore their transport properties. It is, however, a more difficult route to effective device integration.

A. FABRICATION

The nanowires were grown on GaAs substrates using randomly dispersed Au-aerosols as seed particles through the vapor-liquid-solid growth using Metal-Organic Chemical Vapor Deposition (MOCVD) [24], by first growing a seed GaAs segment, followed by the GaSb source and finally the InAs channel and drain. The GaSb had a source doping $\sim N_A = 10^{18} - 10^{19}$ cm^{-3} and the InAs channel doping was approximately 10^{17} cm^{-3}. A neck was formed at the heterojuction by in-situ annealing that helped to constrict the current [25]. The nanowire diameter around the tunneling junction was 45 nm, at which the quantization effects are small. We thus expect this TFET to have a broken band gap, with band offset of about 0.2 eV.

Device fabrication was performed by random dry transfer of nanowires from the GaAs substrate to a Si/SiO_2 wafer. Source and drain Ni-electrodes were formed by electron beam lithography (EBL) and thermal evaporation. An Al_2O_3/HfO_2 (10/70 cycles) high-k oxide (EOT$\sim$1.8 nm) was deposited by atomic layer deposition (ALD). Ni-gate metal (Gate length $\sim$ 200 nm, with a 100 nm source overlap) was deposited through EBL and thermal evaporation, forming a device with a source overlap of 5 nm and an effective gate length of 290 nm. Fig. 4(a) shows a schematic illustration of the device.

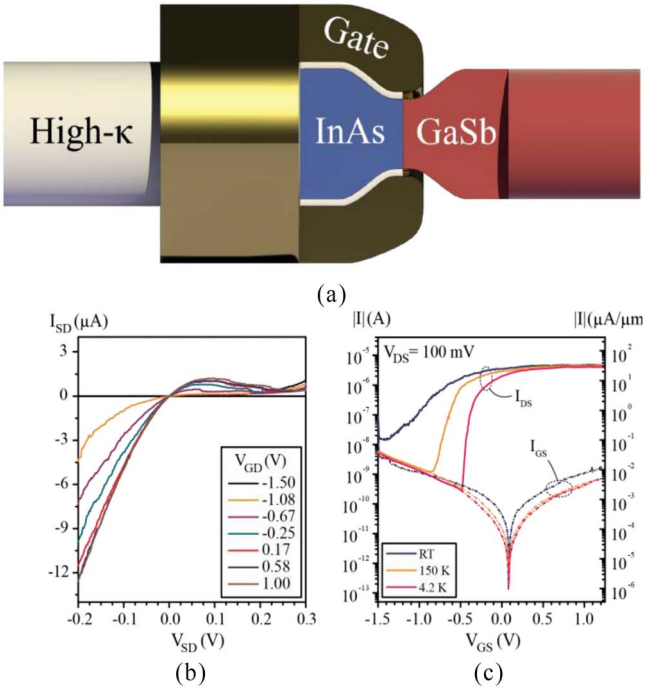

FIGURE 4. (a) Schematic illustration of a InAs/GaSb TFET. (b) Output characteristics, showing the Esaki-diode NDR behavior. (c) Temperature dependent transfer characteristics (solid lines) and gate current (dashed lines).

B. ELECTRICAL RESULTS

Fig. 4(b) shows the output characteristics, demonstrating Esaki like behavior with negative differential resistance (NDR) and a peak current density $J_{peak} = 90$ kA/cm^2 in the reverse bias direction. Fig. 4(c) shows the measured transfer characteristics obtained at $V_{DS} = 0.1$ V for temperatures between 4.2K to 300K. An temperature insensitive maximum on-current of $I_{on} = 30$ μA/μm at $V_{DS} = 0.1$ V was obtained, increasing to $I_{on} = 130$ μA/μm at $V_{DS} = 0.3$ V [9]. The high drive current capability is connected to the measured high current densities at reverse bias (3.4 MA/cm^2 at -0.5 V) for InAs/GaSb nanowire Esaki diodes following an optimization of the doping profile within the nanowires [26].

The minimum inverse subthreshold slope is 300 mV/decade at room temperature and shows a temperature dependency, decreasing down to 17 mV/decade at $T = 4.2$ K. This is indicating that the off-current at room temperature is strongly limited by trap assisted tunneling. Growth optimization to reduce point defects, as well as an improvement in high-κ quality, are essential parts for

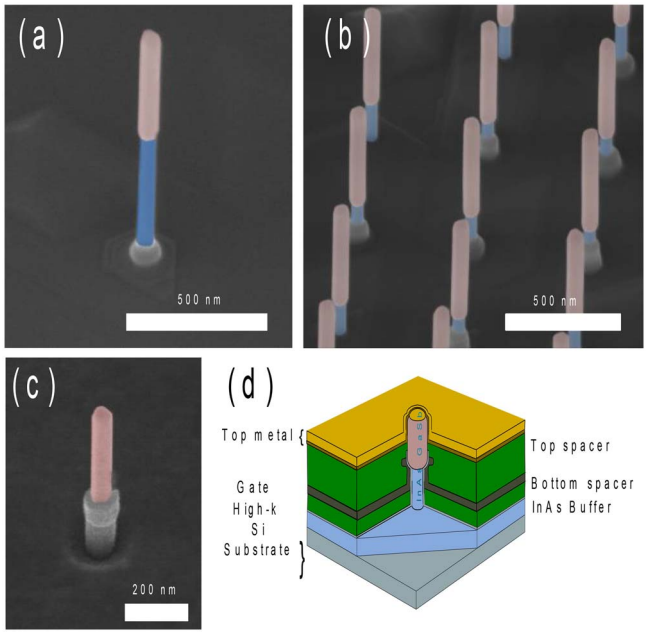

FIGURE 5. **(a)–(c) Colored SEM image of InAs (bottom)/GaSb (top) nanowires grown on a Si substrate. (a) Single nanowire and (b) array of InAs/GaSb nanowires. (c) SEM image after gate formation. The GaSb segment is colored. (d) Schematic illustration of a vertical TFET.**

achieving an improved subthreshold slope. The minimum off-current at low temperatures is limited by gate leakage.

IV. VERTICAL NANOWIRE TFETS ON SI SUBSTRATES

Large scale device applications for III-V TFETs require integration of the TFETs on Si substrates, as well as exact placement of the individual devices, which is difficult for the transfer process utilized for the lateral nanowire transistors. Direct or template guided nanowire growth on Si substrates have previously been demonstrated [27], as well as InGaAs/Si-based TFETs [28]. In this paper, we use VLS-type nanowire growth on thin InAs buffer layers grown on (111) Si substrate [29]. A key benefit of this approach is that we avoid any barrier associated with the InAs/Si interface [30], leading to a reduced access resistance. Previously, we have used this technology to demonstrate high performance vertical InAs n-type MOSFETs on Si-substrates [31], and we here show implementation of InAs/GaSb TFETs utilizing the same technology.

A. FABRICATION

The fabrication starts with growth of a 200-nm-thick n-type ($N_D \sim 3 \times 10^{18}$ cm^{-3}) InAs buffer layer on a Si (111) substrate, which will act as the drain electrode. Through electron beam lithography and thermal evaporation, Au-seed particles with diameters between 30 and 40 nm are defined. Using the Au-seeds as catalysts, MOCVD-based VLS-type of growth is performed, growing a 300-nm-long InAs drain/channel segment followed by 500 nm GaSb source, as shown in Fig. 5(a). The lower part of the InAs stem was n-type doped using tetraethyltin (TESn), with nominally no doping inside the channel, with estimated doping levels about 10^{17} cm^{-3}. The GaSb segment was uniformly p-doped with diethylzinc (DEZn) to about $N_A = 10^{19}$cm^{-3}.

Fig. 5(a) shows a single nanowire, and Fig. 5(b) shows a nanowire array, showing the possibility for controlled position of the nanowires. The difference in length between the nanowires in the arrays and the single nanowire is due to the difference in accessible material for the individual nanowire during growth. After the nanowire growth, the diameters were trimmed by 4 digital etching step, reducing the wire diameter to $D = 30$ nm for the InAs segment. Directly after the growth, a 1/5 nm Al_2O_3/HfO_2 high-k oxide (EOT$\sim$1.4 nm) is deposited using thermal ALD.

After etching the drain mesa for device isolation, a 200-nm-thick organic layer is deposited through a spin-on and ash process, for device planarization and to implement a vertical spacer. A tungsten gate is subsequently deposited through reactive sputtering, where the gate length is set by a second spin-on and dry etch process. In this way, a gate-all-around geometry with a gate length of 350 nm is formed on the wires, with a source overlap of roughly 100 nm on the GaSb segment, as shown in Fig. 5(c). A second planarization layer is added as a gate-source spacer, followed by removal of the high-k on the top of the wires. Drain and source contacts, as well as probing pads are formed through thermal evaporation and lift-off, finalizing the device processing. Fig. 5(d) shows a schematic cross-section of the completed device. While these wires have large diameters, further scaling is feasible. We have previously demonstrated InAs nanowire FETs with diameters down to 15 nm [32], and further device diameter reduction through digital etching can be applied. Shorter gate-lengths can also be fabricated, for example, through evaporated gates. The key technical challenge for a vertical TFET geometry is the alignment of the gate to the tunneling junction.

B. VERTICAL DEVICE RESULTS

Fig. 6(a) and (b) shows the measured room temperature charateristics for the vertical InAs/GaSb n-TFET on a Si substrate. A minimum inverse subthreshold slope of $\sim$ 130 mV/decade is measured at $V_{DS} = 50$ mV, and a maximum on-current of 5 μA/μm at $V_{DS} = V_{GS} = 0.5$ V. In the reverse output characteristics, a very weak negative differential resistance is observed for large positive gate voltages with a peak current density $J_{peak} = 3.5$ kA/cm^2 The on-current is 10-20$\times$ lower as compared to lateral devices presented here. We attribute this difference mainly due to a different heterointerface at the GaSb/InAs junction, due to the growth dynamics. This is discussed further in Section V. For $V_{DS} = 0.5$ V the devices show a larger off-state leakage, and a degraded subthreshold swing, with a minimum value of $\sim$ 210 mV/decade. Devices without any digital etching steps show substantially larger values for the off-state leakage at $V_{DS} = 0.5$ V, with a minimum off-current around 1 μA/μm

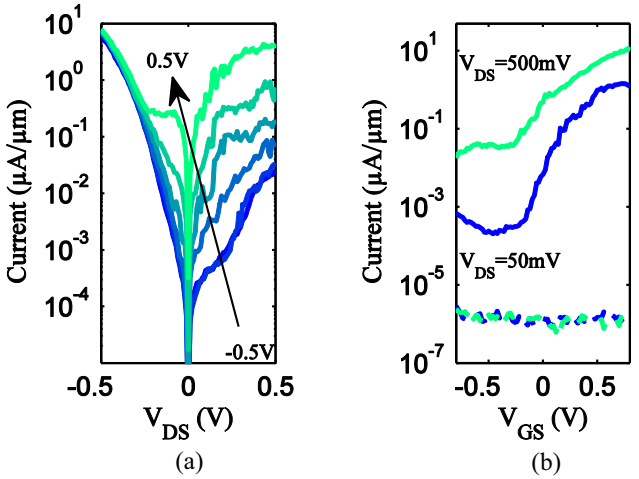

FIGURE 6. (a) Room temperature output characteristics ($\Delta V_{GS} = 0.2$ V). (b) Transfer characteristics (solid lines) and gate leakage (dashed lines) for a single nanowire InAs/GaSb vertical nanowire TFET on a Si substrate. The nanowire diameter is $D = 30$ nm.

and similar on-current as an etched device. The gate leakage current does not influence the transfer characteristics, as shown in Fig. 6(b). These metrics demonstrate a substantial improvement as compered to previous reported values for the InAs/GaSb nanowire heterojunctions, where the GaSb segment has been grown on the InAs segment [33].

V. VERTICAL/LATERAL COMPARISON

Currently, the lateral devices show a similar subthreshold slope as the vertical devices and a larger current density. A key difference in the device performance of the devices presented in this paper can be attributed to growth, as the vertical TFETs are fabricated using an n^+ InAs buffer layer, acting as part of the source electrode. This requires the nanowire growth of GaSb on top of InAs, which typically introduce an $In_{1-x}Ga_xAs$ segment at the heterojunction [33], leading to a strongly reduced drive current capability. This can explain why the vertical TFET currently shows degraded on-performance as compared with the lateral transistor. However, lateral TFETs processed earlier from such (GaSb on InAs) nanowire devices have shown low $I_{ON} = 0.02$ $\mu A/\mu m$ [33], demonstrating that the work here is a substantial improvement over earlier results, in spite of the more advanced vertical processing.

The reverse heterojunction (InAs on GaSb), has resulted in substantially higher current levels as discussed for the lateral device presented here [9], [34], with a similar subthreshold slope. It may serve as a reference level for the possible drive currents. When the nanowires are grown in this direction, the swtching at the heterointerfaces does not introduce any InGaAs barrier, but leads to a $In_{1-x}Sb_xAs$ gradient in the active region [35]. For a vertical device integration, this type of growth mode requires either usage of a p^+ GaSb substrate, or local wrap-type drain contacts around the base of the nanowire. Both approaches add considereable processing challenges.

This comparison shows that vertical nanowire TFETs based on GaSb segments grown on InAs nanowires could provide good drive current capabilities, when the growth dynamics of the heterojunction growth switching is improved.

VI. CONCLUSION

An analytical model for the on-current of a staggered bandgap, 1D nanowire InAs/GaSb-type n-TFET has been developed, which can be used to easily estimate the ideal on-current behavior for a TFET. The first vertical VLS-type InAs/GaSb TFET on Si substrates has also been demonstrated. Substantial improvement in the device performance is expected through growth optimization. The current III-V nanowire technology has been used to demonstrate TFETs with fairly large nanowire diameters, and a direct comparison with 1D models is thus not feasible. However, the vertical nanowire technology is scalable towards the technologically important regime with diameters below $D = 10$ nm.

REFERENCES

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, no. 7373, pp. 329–337, 2011.

[2] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE,* vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[3] U. E. Avci and I. A. Young, "Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9 nm gate-length," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 4.3.1–4.3.4.

[4] M. Luisier and G. Klimeck, "Performance comparisons of tunneling field-effect transistors made of InSb, Carbon, and GaSb-InAs broken gap heterostructures," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Baltimore, MD, USA, 2009, pp. 1–4.

[5] L. Knoll *et al.*, "Inverters with strained Si nanowire complementary tunnel field-effect transistors," *IEEE Electron Device Lett.,* vol. 34, no. 6, pp. 813–815, Jun. 2013.

[6] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization," *J. Appl. Phys.,* vol. 104, no. 6, Sep. 2008, Art. ID 064514.

[7] Y. Zhu and M. K. Hudait, "Low-power tunnel field effect transistors using mixed As and Sb based heterostructures," *Nanotechnol. Rev.,* vol. 2, no. 6, pp. 637–678, 2013.

[8] Z. Guangle *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 μA/μm at VDS = 0.5 V," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 32.6.1–32.6.4.

[9] A. Dey *et al.*, "High-current GaSb/InAs (Sb) nanowire tunnel field-effect transistors," *IEEE Electron Device Lett.,* vol. 34, no. 2, pp. 211–213, Feb. 2013.

[10] R. Bijesh *et al.*, "Demonstration of In0.9Ga0.1As/GaAs0.18Sb0.82 near broken-gap tunnel FET with ION = 740 μA/μm, GM = 700 μA/μm and gigahertz switching performance at VDS = 0.5 V," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 28.2.1–28.2.4.

[11] H. Riel, L.-E. Wernersson, M. Hong, and J. A. del Alamo, "III–V compound semiconductor transistors—From planar to nanowire structures," *MRS Bulletin,* vol. 39, no. 8, pp. 668–677, 2014.

[12] Y. M. Niquet *et al.*, "Electronic structure of semiconductor nanowires," *Phys. Rev. B,* vol. 73, Apr. 2006, Art. ID 165319.

[13] Z. Qin, L. Yeqing, C. A. Richter, D. Jena, and A. Seabaugh, "Optimum bandgap and supply voltage in tunnel FETs," *IEEE Trans. Electron Devices,* vol. 61, no. 8, pp. 2719–2724, Aug. 2014.

[14] E. Lind, M. P. Persson, Y.-M. Niquet, and L. E. Wernersson, "Band structure effects on the scaling properties [111] InAs nanowire MOSFETs," *IEEE Trans. Electron Devices,* vol. 56, no. 2, pp. 201–205, Feb. 2009.
[15] E. Baravelli, E. Gnani, R. Grassi, A. Gundi, and G. Baccarani, "Optimization of staggered heterojunction p-TFETs for LSTP and LOP applications," in *Proc. 71st Annu. Device Res. Conf. (DRC)*, Notre Dame, IN, USA, 2013, pp. 67–68.
[16] W.-F. Sun, M.-C. Li, and L.-C. Zhao, "Ab initio study of electronic structures of InAs and GaSb nanowires along various crystallographic orientations," *Comput. Mater. Sci.,* vol. 50, no. 2, pp. 780–789, 2010.
[17] G. Hurkx, D. Klaassen, and M. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Device,* vol. 39, no. 2, pp. 331–338, Feb. 1992.
[18] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent I-V characteristics of a vertical In0.53Ga0.47As tunnel FET," *IEEE Electron Device Lett.,* vol. 31, no. 6, pp. 564–566, Jun. 2010.
[19] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology.* New York, NY, USA: Wiley, 1982.
[20] M. A. Khayer and R. K. Lake, "Effects of band-tails on the subthreshold characteristics of nanowire band-to-band tunneling transistors," *J. Appl. Phys.,* vol. 110, no. 7, Oct. 2011, Art. ID 074508.
[21] M. G. Pala and D. Esseni, "Interface traps in InAs nanowire tunnel-FETs and MOSFETs—Part I: Model description and single trap analysis in Tunnel-FETs," *IEEE Trans. Electron Devices,* vol. 60, no. 9, pp. 2795–2801, Sep. 2013.
[22] J. Wu *et al.*, "Al2O3/InAs metal-oxide-semiconductor capacitors on (100) and (111) B substrates," *Appl. Phys. Lett.,* vol. 100, no. 13, 2012, Art. ID 132905.
[23] S. Lee *et al.*, "High performance raised source/drain InAs/In0.53Ga0.47As channel metal-oxide-semiconductor field-effect-transistors with reduced leakage using a vertical spacer," *Appl. Phys. Lett.,* vol. 103, no. 23, 2013, Art. ID 233503.
[24] B. M. Borg and L.-E. Wernersson, "Synthesis and properties of antimonide nanowires," *Nanotechnology,* vol. 24, no. 20, 2013, Art. ID 202001.
[25] B. M. Borg *et al.*, "Diameter reduction of nanowire tunnel heterojunctions using in situ annealing," *Appl. Phys. Lett.,* vol. 99, no. 20, Nov. 2011, Art. ID. 203101.
[26] B. M. Borg *et al.*, "Influence of doping on the electronic transport in GaSb/InAs (Sb) nanowire tunnel devices," *Appl. Phys. Lett.,* vol. 101, no. 4, 2012, Art. ID 043508.
[27] M. Borg *et al.*, "Vertical III-V nanowire device integration on Si (100)," *Nano Lett.,* vol. 14, no. 4, pp. 1914–1920, 2014.
[28] K. Tomioka and T. Fukui, "Current increment of tunnel field-effect transistor using InGaAs nanowire/Si heterojunction by scaling of channel length," *Appl. Phys. Lett.,* vol. 104, no. 7, Feb. 2014, Art. ID 073507.
[29] S. G. Ghalamestani, M. Berg, K. A. Dick, and L.-E. Wernersson, "High quality InAs and GaSb thin layers grown on Si (111)," *J. Cryst. Growth,* vol. 332, no. 1, pp. 12–16, 2011.
[30] C. Rehnstedt, T. Martensson, C. Thelander, L. Samuelson, and L.-E. Wernersson, "Vertical InAs nanowire wrap gate transistors on Si substrates," *IEEE Trans. Electron Devices,* vol. 55, no. 11, pp. 3037–3041, Nov. 2008.
[31] S. Johansson, E. Memisevic, L. E. Wernersson, and E. Lind, "High-frequency gate-all-around vertical InAs nanowire MOSFETs on Si substrates," *IEEE Electron Device Lett.,* vol. 35, no. 5, pp. 518–520, May 2014.
[32] A. W. Dey *et al.*, "High-performance InAs nanowire MOSFETs," *IEEE Electron Device Lett.,* vol. 33, no. 6, pp. 791–793, Jun. 2012.
[33] B. M. Borg *et al.*, "InAs/GaSb heterostructure nanowires for tunnel field-effect transistors," *Nano Lett.,* vol. 10, no. 10, pp. 4080–4085, 2010.
[34] B. Ganjipour *et al.*, "High current density Esaki tunnel diodes based on GaSb-InAsSb heterostructure nanowires," *Nano Lett.,* vol. 11, no. 10, pp. 4222–4226, 2011.
[35] M. Ek *et al.*, "Formation of the axial heterojunction in GaSb/InAs(Sb) nanowires with high crystal quality," *Cryst. Growth Design,* vol. 11, no. 10, pp. 4588–4593, 2011.

ERIK LIND received the Ph.D. degree in solid-state physics from Lund University, Lund, Sweden, in 2004. He is currently an Associate Professor with the Department of Electrical and Information Technology, Lund University.

ELVEDIN MEMIŠEVIĆ received the M.S. degree in engineering nanoscience from Lund University, Lund, Sweden, in 2012, where he is currently pursuing the Ph.D. degree from the Department of Electrical and Information Technology.

ANIL W. DEY received the Ph.D. degree in electrical engineering physics from Lund University, Lund, Sweden, in 2013. He is currently a Post-Doctorate with the Department of Electrical and Information Technology, Lund University.

LARS-ERIK WERNERSSON received the Ph.D. degree in solid-state physics from Lund University, Lund, Sweden, in 1998. He has been a Professor of Nanoelectronics at Lund University, since 2005.