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A 100-MHz CMOS Wide-Band IF Amplifier

Henrik Sjöland and Sven Mattisson

Abstract— When the data rates of communication systems increase, wideband IF amplifiers are needed. It is also possible to use a single wideband intermediate frequency (IF) amplifier for a radio band with several narrow-band channels of varying strengths. The linearity is then critical, if intermodulation products are not to disturb weak channels.

We try to find a topology for this new amplifier application, suitable for integration in a standard CMOS process. To get low distortion, we use an output stage with high linearity, which is further linearized by feedback in a double-nested Miller configuration.

A 0.8- μm standard CMOS IF amplifier design with low distortion up to 20 MHz is presented.

I. INTRODUCTION

WIDE-BAND intermediate frequency (IF) amplifiers are needed in wide-band communication systems. They can also be used in, for instance, base stations to amplify several channels simultaneously, some at the sensitivity limit and others strong.

In this paper we try to find a suitable topology for such an amplifier. The nonlinear distortion must be minimized, since the intermodulation noise is critical for the performance. To accomplish this we have used an output stage with high linearity, based on cancellation of nonlinearities. The output stage is further linearized by feedback. A double-nested Miller compensation is employed to maximize the feedback around the output devices [1]–[3]. A fully differential topology is employed to cancel out even order distortion.

The aim was to build a wide-band amplifier in a standard 0.8- μm CMOS process with a large dynamic range up to 20 MHz. The noise should thus be minimized and the linearity maximized. In [5] it is shown how to calculate the required total harmonic distortion (THD) figure, in order for the intermodulation products to have less power than the noise, if the input signal is Gaussian. The THD is to be less than about 0.06% at 3.6 V_{pp} output. The voltage gain is to be 100.

An amplifier fulfilling the above demands was designed and fabricated. The bandwidth was about 100 MHz and the measured harmonic distortion at 20 MHz, 3 V_{pp} into 1 k Ω was 0.06%. At 20 MHz, the third-order intercept point, IP_3 , was 35 dBm = 33 dB-V referred to the output.

II. OUTPUT STAGE

To achieve high linearity, we decided to let the output stage work in class A. The best linearity and efficiency is achieved by using a push–pull configuration. If the output transistors

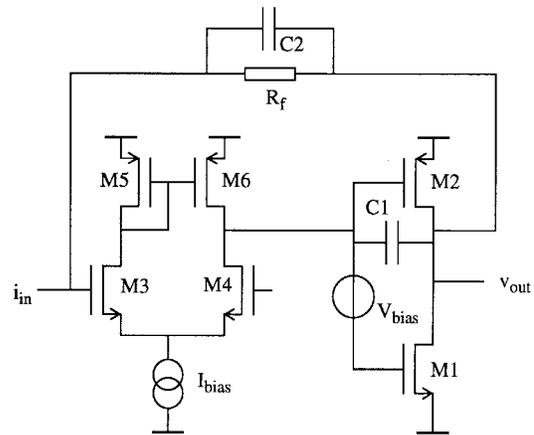


Fig. 1. The output stage.

are matched and have an ideal square-law characteristic, the transconductance of the push–pull stage is linear [4]. To further improve the linearity, we used a double-nested Miller topology with large feedback around the output devices; see Fig. 1.

There are conflicting requirements when selecting dimensions and quiescent current for the output transistors.

Class A operation at full output amplitude puts a lower limit on the quiescent current, and a large-output voltage swing combined with low distortion requires low effective V_{GS} , which results in wide transistors. In order not to load the driving stage too much, the size of the output transistors must, however, be limited. The second pole of the current-driven combination of the output devices and the feedback capacitor is located at

$$\begin{aligned} p_{2\text{nd}} &\approx -\frac{(g_{m1} + g_{m2})C_1}{C_L(C_{\text{gs1}} + C_{\text{gs2}} + C_1)} = \{C_1 = C_{\text{gs1}} + C_{\text{gs2}}\} \\ &= -\frac{(g_{m1} + g_{m2})}{2C_L}. \end{aligned} \quad (1)$$

A pole at a high enough frequency requires a certain minimum value of g_m of the output devices. Finally, the power consumption must be kept down, which limits the acceptable quiescent current.

The output stage resembles a two-stage operational amplifier with a transresistance feedback R_f , including a phase-compensation Miller capacitor C_1 . The push–pull stage is different, though, since a normal two-stage op-amp uses a single ended output stage. In addition to the push–pull stage, capacitor C_2 is also used in a nonstandard manner. It can be seen as a second nested Miller capacitor, or as a phantom zero feedback. It is important to note that the output devices are linearized by two nested feedback loops.

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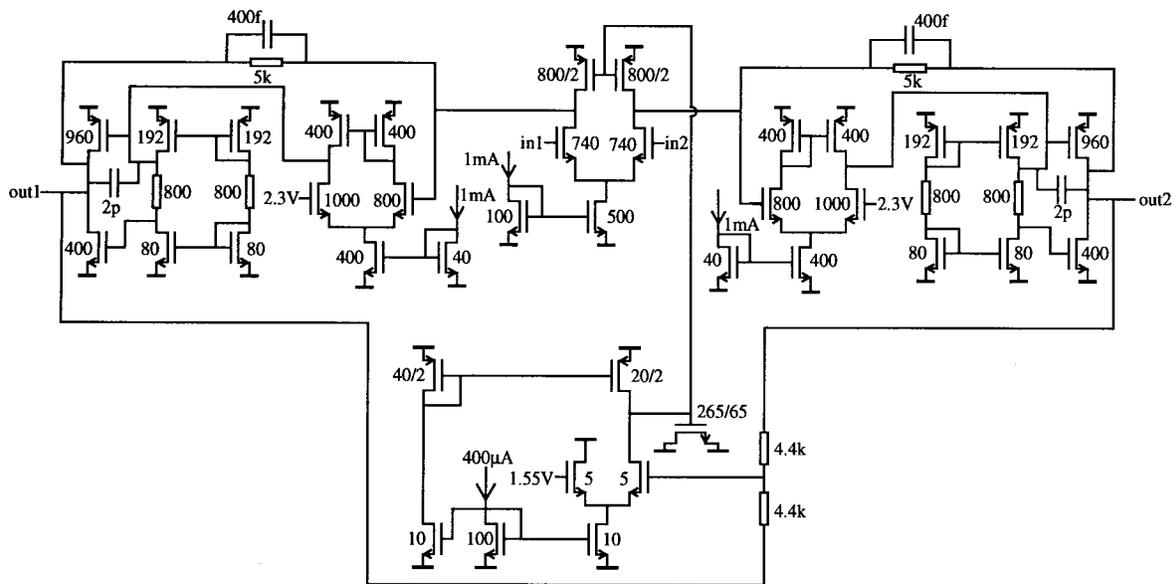


Fig. 4. The entire schematic with device parameters. Unless specified, the transistor length is 0.8 μm .

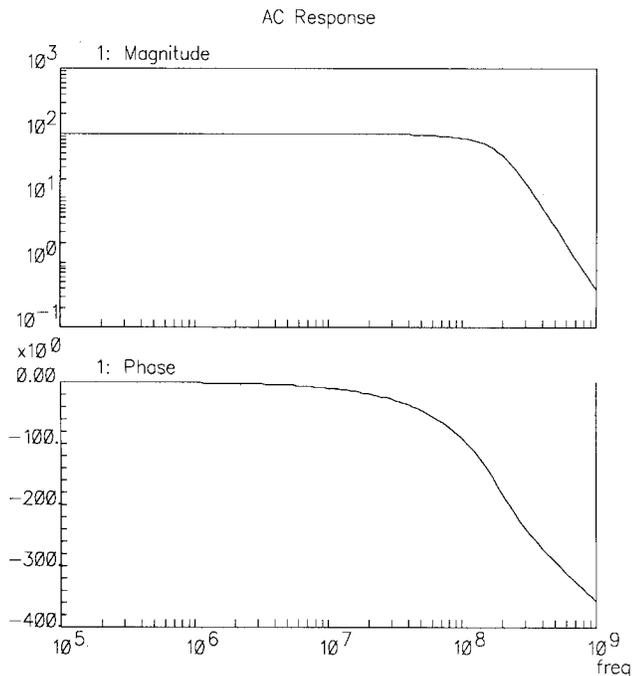


Fig. 5. Bode plot of the voltage gain with internal capacitive loading.

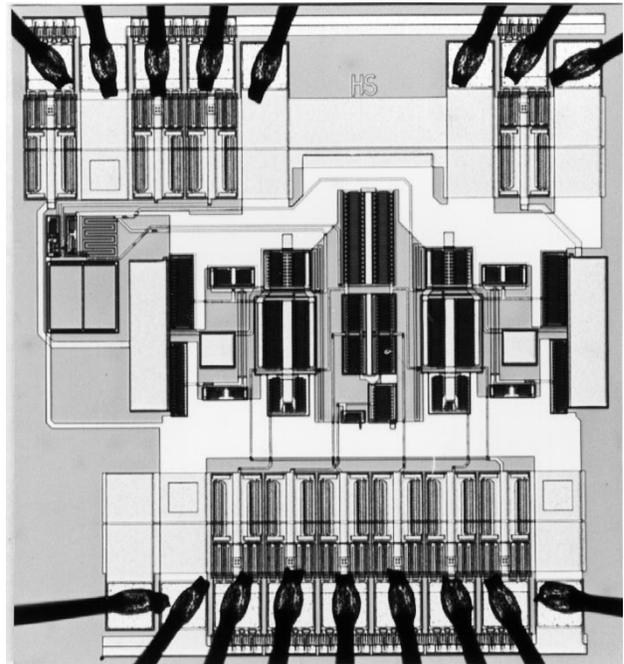


Fig. 6. Microphotograph of the amplifier.

internal load capacitances (pads) is shown in Fig. 5. The gain is flat in the operating band from dc to 20 MHz.

The total power consumption is 130 mW. This large figure can be explained by the balanced design and the demand for low noise and distortion over a large bandwidth. If more distortion can be accepted, the bias current of the LTP stages can be reduced, which will also increase the phase margin. If a differential output is not needed, the power consumption can be almost halved, as one output stage can be dispensed. The P devices of the input stage can then be connected as a current mirror, and the output stage can be biased by a current generator connected to its input.

The values above are about the same for common-mode input voltages in the range 1.4 to 3.5 V, which even exceeds the positive supply rail by 200 mV.

V. CONCLUSION

The simulation and measurement results show that we have designed an amplifier with high linearity from dc to 20 MHz. The design was made in a standard 0.8- μm CMOS process. It could be used as an IF amplifier in a base station to amplify several channels simultaneously or to amplify a wide-band signal.

TABLE I
MEASURED (M) AND SIMULATED (S) THD (1 k Ω)

	5MHz (M)	5MHz (S)	10MHz (M)	10MHz (S)	20MHz (M)	20MHz (S)
1 V _{pp} (out)	-	0.0016%	-	0.0016%	0.006%	0.0025%
2 V _{pp} (out)	0.013%	0.0068%	0.017%	0.0081%	0.026%	0.011%
3 V _{pp} (out)	0.037%	0.013%	0.035%	0.014%	0.062%	0.027%
4 V _{pp} (out)	0.066%	0.028%	0.060%	0.033%	0.16%	0.061%
5 V _{pp} (out)	-	0.11%	-	0.27%	-	0.75%
IP ₃ (output)	35 dBV	39dBV	35 dBV	39 dBV	37 dBV	37dBV

The topology is thus possible to use for high-performance CMOS wide-band amplifiers. High-performance requirements tend to result in larger power consumption than lower requirements. The topology is also suitable for variable gain amplifiers, as there is no feedback loop around the input stage.

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