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# Impact of source doping on the performance of vertical InAs/InGaAsSb/GaSb nanowire Tunnel Field-Effect Transistors

*Elvedin Memisevic, Johannes Svensson, Erik Lind, and Lars-Erik Wernersson*

Department of Electrical and Information Technology, Lund University,

Lund SE-221 00, Sweden

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ABSTRACT

In this paper, we analyze experimental data from state-of-the-art vertical InAs/InGaAsSb/GaSb nanowire Tunnel Field-Effect Transistors to study influence of the source doping on their performance. Overall, the doping level impacts both off-state and on-state performance of these devices. Separation of the doping from the heterostructure improved the subthreshod swing of the devices. Best devices reached a point subthreshold swing of 30 mV/dec at 100x higher currents than what Si-based TFETs has achieved previously. However, separation of doping from the heterostructure had a significant impact on the on-state performance of these devices due to effects related to source depletion. Increase of the doping level, helped to improve the on-state performance, which also increased the subthreshold swing. Thus, further optimization of doping

incorporation at the heterostructure will help to improve vertical InAs/InGaAsSb/GaSb nanowire TFETs.

## I. Introduction

The Tunneling Field-Effect Transistor (TFET) is considered to be one of the most promising steep-slope candidates, needed for future low-power applications [1,2]. Since the first considerations to use TFET as steep slope device [3,4] the development of these devices has advanced rapidly. A large number of different material systems (carbon nanotubes [3], silicon [5-7], silicon-germanium [4,8,9], silicon-III-V [10-12], III-V [13-30], 2D-materials [31,32]) and geometries (lateral [3,5-9,12-14,21,25,31,32], vertical [10,11,15-19,20,23,24,26-30]) have been utilized to demonstrate TFETs. However, most devices either exhibit a point subthreshold swing ($S_{MIN}$) below the thermal limit of 60 mV/dec or large currents. Yet, for TFETs to become a serious contender as a replacement for Complementary Metal-Oxide-Semiconductor (CMOS) in low power applications, devices that can achieve both characteristics simultaneously are necessary. So far, TFETs based on vertical InAs/InGaAsSb/GaSb nanowires have demonstrated the best performance with sub-thermal operation, reaching down to 48 mV/dec, combined with high currents [27-30]. However to optimize the devices, required for broader impact, a deeper understanding of the devices physics and the performance limiting factors is required. The impact of gate-overlap and the used heterojunctions with different band alignment on vertical InAs/InGaAsSb/GaSb nanowire TFETs have been reported in previous publications [28,30]. So far, the impact of source doping on the performance of these TFETs has not been studied. Previous studies, based on TFETs with other material systems [21, 25, 38], have demonstrated the importance of this parameter. Based on experimental data from devices with the nominally same heterojunction but with different doping levels, we here study the impact of source doping on the overall performance of vertical InAs/InGaAsSb/GaSb nanowire TFETs. The impact of the

source doping can be observed both for the on-state and off-state performance of these TFETs. Devices with the lowest doping levels exhibit the lowest subthreshold swing (30 mV/dec). However, the penalty of low doping is a reduced on-state performance manifested in low transconductance. Devices with highest source doping exhibit a better on-state, but with much higher current in the off-state that impacts the subthreshold swing. Output data of all devices exhibit negative differential resistance (NDR), which is an expected characteristic of a TFET. Both peak and valley currents increased with higher level of source doping. However, devices with highest doping exhibited lowest peak-to-valey-current-ratio due to large increase of excess currents. Overall, this study shows that with correct doping profile these devices can achieve an even lower subthreshold swing than what have been achieved so far reaching performance of Si-based TFETs although at a much higher current level.

## II. Theory

The backbone of CMOS Technology is the Metal-Oxide-Semiconductor Field-Effect transistor (MOSFET). The operation mechanism in MOSFET relies on thermally excited charge carriers that pass over the barrier in the channel region moving between source and drain. The height of the barrier is controlled by the applied gate voltage, which thereby controls when the transistor is switched on and off. As illustrated by the energy band-diagram in Figure 1 (a), it is only the high energy carriers in the Fermi-Tail that contribute to transport. Thus, an MOSFET working as a switch is fundamentally limited by the thermal distribution in the Fermi-tail (thermal limit). The subthreshold swing for a MOSFET relying on thermionic emission is [1,2]

$$S = \underbrace{\frac{dV_{GS}}{d\Psi_S}}_{BF}\underbrace{\frac{d\Psi_S}{d(log_{10}I_D)}}_{CM} \cong \underbrace{\left(1+\frac{C_S}{C_{OX}}\right)}_{BF}\underbrace{\frac{kT}{q}ln10}_{CM},$$

where $V_{GS}$ is the gate voltage, $\Psi_S$ is the surface potential at the interface between the semiconductor and high-κ, $I_D$ is drain current, $C_S$ is the semiconductor capacitance, $C_{OX}$ is the capacitance over the insulator, $k$ is Boltzmans constant, $T$ is temperature, and $q$ is elementary charge. Effectively, the subthreshold swing is determined by the body factor (BF) and the conduction mechanism (CM). For an MOSFET with ideal electrostatic control, the value of the body factor is 1. Thus at room temperature (293 K), the smallest voltage that is required to change the current with 1 decade is 58.1 mV (~ 60 mV). In a TFET the high energy carriers in the Fermi-tail are effectively filtered out by the bandgap of the source. Thus, only carriers with low energy are injected during the device operation. As Figure 1 (b) illustrates, switching of a TFET between off and on state relies on usage of gate voltage to raise and lower the bands of the channel region as in a MOSFET. When the device is in on-state, the bands of the channel are lowered and carriers from the source can enter the channel utilizing band-to-band tunneling (BTBT) as opposed to thermionic emission. Thus, a TFET with good electrostatic (BF ≈ 1) will be able to reach a subhtreshold swing below the thermal limit due to usage of different CMs.

However, as TFETs relies on a tunneling process it is difficult to reach as high currents as MOSFETs can at higher drive voltages ($V_{DS}$) [34]. Thus, high currents require a thin barrier, which is achieved by proper band alignment, high precision gate alignment to avoid source depletion, and sufficiently high source doping with an abrupt profile. The subthreshold swing is strongly influenced by imperfections in the channel materials used, such as defect states in the bandgap. These defects can be in the bulk of the material or, for example, at the interface to the gate dielectric. Usage of thin vertical nanowires, as described in this paper, allows for integration of materials with a large lattice mismatch due to radial strain relaxation, something difficult to achieve with bulk materials. This provides a necessary path for optimization of the heterojunction. Furthermore, the gate-all-around geometry that provides the best possible

electrostatics, is straightforward to implement with vertical nanowires [35-37]. However, even with well-optimized heterojunction and good electrostatics, source doping can increase the subthreshold swing due to formation of states in the bandgap. These will broaden the valence band-edge of the source and reduce how efficiently carriers in the Fermi-Tail are filtered out. Moreover, too high source doping will cause degeneracy, which will eliminate TFETs ability to filter out the charges. Furthermore, these extra states in the bandgap can introduce additional leakage paths that can worsen the off-state when there are very few charges in the channel. However, a too low source doping will make devices more susceptible to source depletion that will impact the on-performance of the devices due to increased tunneling length and increased barrier height [38]. Moreover, low source doping level will result in resistive loss and further reduce the current. Furthermore, a gate-overlap will deplete the regions of the source below the metal resulting in more access resistance. The source depletion can be described with following equation [38]

$$d_p \approx -\frac{\lambda}{2} + \sqrt{\frac{\lambda^2}{4} + \frac{E_g \varepsilon_r \varepsilon_0}{q N_A}},$$

where $E_g$ is band gap in the source, $\lambda$ corresponds to the geometric length and is determined from Poisson's equation, $q$ is elementary charge, $N_A$ is source doping, $\varepsilon_r$ and $\varepsilon_0$ are relative and absolute dielectric constant, respectively. As the equation shows, the impact of the source depletion depends on the material properties and level of doping. Thus to reduce the impact of source depletion would require as high doping level as possible. To design a well performing TFET requires a carefully chosen doping level, as both to high and to low doping level will have a negative impact on the performance.

## III. Device fabrication

Vertical InAs/$In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$/GaSb heterostructure nanowires, with different levels of source doping, were grown on three different samples. In devices from Sample A there is

no intentional doping in the source close to the junction and Zn is introduced first after 20 nm. The exact evaluation of the carrier concentration in the not intentionally doped InGaAsSb segment is a challenge, as the data will strongly be influenced by the contact properties. Our estimation based on studies on GaSb nanowires is a level in the range from $10^{17}$ to $10^{18}$ $cm^{-3}$ [39, 40]. Devices from Sample B [28, 29], used as references, had a fully doped source with an estimated carrier concentration of $10^{19}$ $cm^{-3}$. Devices from Sample C have an estimated source doping of $4 \times 10^{19}$ $cm^{-3}$. Prior to the growth of the nanowires, Au seed particles were patterned on an n+- InAs layer integrated on a highly resistive Si (111) substrate ($\rho > 12$ k$\Omega \cdot$ cm) [41], utilizing electron beam lithography and polymethyl methacrylate (PMMA)-based lift-off process. The patterns formed consisted of arrays with 1 to 8 Au-seed particles with a pitch of 1.5 μm and a diameter of 40 nm. The epitaxial growth was performed using metal-organic vapor phase epitaxy (MOVPE) utilizing the vapor-liquid-solid (VLS) growth method. Using the precursors Arsine ($AsH_3$) and Trimethylindium (TMIn), an InAs-segment was grown, where the bottom half of was n-doped using Tetraethyltin (TESn) to an estimated concentration of $10^{19}$ $cm^{-3}$ to form the drain region. The top half of the InAs-segment, which corresponds to the channel region of the device, was not intentionally doped and has an estimated background carrier concentration of $10^{17}$ $cm^{-3}$. The InGaAsSb source segment was grown using Trimethylgallium (TMGa), Trimethylantimony (TMSb) and $AsH_3$ ($X_{AsH3} = 2.7 \times 10^{-5}$) followed by a GaSb segment. The presence of In in the source segment is due the remaining concentration in the Au particle after InAs growth. Both the InGaAsSb and the GaSb segments were p-doped using Diethylzinc. The only difference between the samples is the level and position of the doping in the source segment with sample as described previously.

A SEM image of a nanowire after growth can be viewed in Figure 2 (a). The diameter/length of the segments were 40/200 nm (InAs), 44/100 nm (InGaAsSb), and 53/300 nm (GaSb). The doping profile for the different segments and the positions of the heterojunction is illustrated in Figure 2 (b). After growth, the diameter of the InAs segment was reduced from 40 nm to 20 nm through several cycles of digital etching using ozone to oxidize the surface and citric acid to remove the oxide. In this step, a GaSb-shell that was unintentionally grown on the InAs and InGaAsSb segments, was removed during the first cycles. Further cycles are performed to reduce diameter of the channel region, which helps to improve the electrostatics of the devices [20, 30]. The diameter of the InGaAsSb segments was also reduced to 25 nm, while there was no noticeable etching of the GaSb. Directly after etching, a high-κ bilayer (1-nm $Al_2O_3$/4-nm $HfO_2$) was applied using atomic layer deposition at temperatures of 300 °C and 120 °C, respectively. The estimated EOT for this layer was 1.4 nm. A 15-nm-thick $SiO_x$ bottom spacer, which separates the drain and gate layers, was deposited using thermal evaporation with rotation and no tilt. The sample was etched in diluted HF to remove the $SiO_x$ on the sidewalls of the GaSb-segment. To compensate for the etching of high-$\kappa$, 12 extra cycles of $HfO_2$ were deposited. A 60-nm-thick tungsten film was sputtered on the sample to form the gate layer. In subsequent steps, the gate length was set by spin coating the sample with an organic resist (S1800) and etching the resist back to the designed thickness with reactive ion etching (RIE). It was followed by removal of the exposed tungsten on the top part of the nanowires (W) using $SF_6$/Ar plasma with RIE as showing in Figure 2 (d). In the following steps, the gate pad was defined using UV lithography and RIE to remove the tungsten in the exposed areas. The top spacer, which separates gate and source layer, was fabricated using an organic spacer (S1800). The S1800 was applied using spin coating, followed by etchback with RIE to the desired thickness. Using UV lithography and RIE, via holes were defined. Prior to applying the top metal, the high-κ was removed from top of the nanowires and drain-via with

HF, followed by sputtering of 10-nm Ni and 150-nm Au. The probe pads were defined using UV lithography and wet etching. The final devices have a physical gate length ($L_g$) of 300 nm with an overlap of 100 nm. The effective channel length is ~100 nm, which corresponds to the undoped InAs segment. A schematic image of a finished device can be viewed in Figure 2 (e). For clarity, the thickness of the W was same for both lateral and vertical surfaces in the image, however on real devices the thickness of the tungsten was 60 nm a lateral surfaces and ~ 20 nm at vertical surface of the nanowires.

## IV. Results and discussion

The number of working devices on each sample was 52 at Sample A, 88 at Sample B, and 6 at Sample C. The data shown in this section are from devices with best subthreshold swing for each sample. These devices will be referred to as Device A, Device B, and Device C. (Statistical data from these samples is presented in Supplementary section). The currents are normalized to the circumference of the nanowire at the junction and the number of the nanowires in the device. Full electrical characterization of TFETs is performed by usage of transfer and output data. From transfer data, we can acquire subthreshold swing and transconductance. These parameters describe how effectively the gate voltage modulates the channel current in the off- and on-state. One unique characteristic for devices that relies on BTBT is the negative differential resistance (NDR) in the output characteristics. The peak current, in the ideal case, should only come from BTBT. Yet, in real devices with imperfections there are also contributions from parasitic current paths. In the valley region, where BTBT process is turned off, the only contribution to the current is thus from the parasitic leakage, like phonon assisted tunneling. Thus, for a well-performing TFET, the peak-to-valley-current (PVCR) ratio should be as high as possible. The transfer data in Figure 3 show that all three devices exhibit very good electrostatics with low drain-induced-barrier

lowering (DIBL) of 20 mV/V (Device A), 15 mV/V (Device B), and 35 mV/V (Device C). The impact of source depletion observable at higher $V_{GS}$ is decreasing with increasing source doping. This is confirmed by the increasing maximum transconductance ($g_m$): 9 μS/μm (Device A), 60 μS/μm (Device B), and 100 μS/μm (Device C) for drive voltage of 300 mV. All three devices exhibited negative differential transconductance due to source depletion. The lowest current is also increasing with the source doping, where Device A exhibit 10x lower off-current than the Device C. Yet, the gate current for all of these devices is 2-3 orders of magnitude lower that the lowest drain currents as shown in Figures 3 (d-f). In Figure 4, the subthreshold swing of devices is compared. Device A exhibits a point subthreshold swing $S_{MIN}$= 30 mV/decade at $V_{DS}$ of 100 mV. As the doping is increased, also the $S_{MIN}$ increases to 45 mV/decade (Device B) and 70 mV/decade (Device C). However, the lowest value of $S_{MIN}$ for Device A occurs at hundred times lower drain current as compared to other two devices. Furthermore, Device B operates in a much wider voltage and current range below the thermal limit than Device A due to the lower impact of source depletion. Device A and B are compared to TFETs from other publications in Figure 4 (b). Even if Device A is limited by the strong source depletion it still reaches approximately 40% lower $S_{MIN}$ compared to other III-V based TFETs [10, 21, 25-29] at drain current levels that are approximately two orders of magnitude larger than Si-based TFETs [7]. Output data from Device A, B, and C is shown in Figure 5. All three devices exhibit superlinear behavior and a negative differential resistance (NDR). Device A exhibits the strongest superlinear behavior and the lowest peak current. Device C exhibits the highest peak and valley current, but also the lowest peak-to-valley current ratio.

Both transfer and output data show the same trend of increasing on-current and peak current with increased doping. Furthermore, the combination of increased excess current in the valley in the output data and off-state in the transfer data indicates an increased number of leakage

paths due to larger number of doping atoms. Moreover, the increased subthreshold swing indicates that the efficiency to filter out the high-energy carriers is impacted by the source doping, possibly due to a larger number of energy states in the band-gap or changes in the electrostatics.

## Conclusion

Comparison of devices with different source doping concentrations shows that doping impacts a number of key properties of the vertical InAs/InGaAsSb/GaSb nanowire TFETs. Reduction of the doping improved the subthreshold swing, allowing devices to reach a $S_{MIN}$ of 30 mV/decade at $V_{DS}$ = 100 mV. The device with the lowest doping exhibited also lowest off-current in transfer data and excess current in output data. Thus removal of the dopants from the heterostructure eliminates states in the bandgap of the source which otherwise act as leakage paths [43]. However, the on-state of this device is strongly impacted by the source depletion. This effect is clearly reduced by increased source doping. This device exhibits a transconductance, which is 10x higher than the first device. However, this increase in doping deteriorates the subthreshold swing and off-current. Overall, we can see that by further optimization of the source doping vertical InAs/InGaAsSb/GaSb TFETs can achieve even better subthreshold swing than what have been done so far, opening a path for future optimization.

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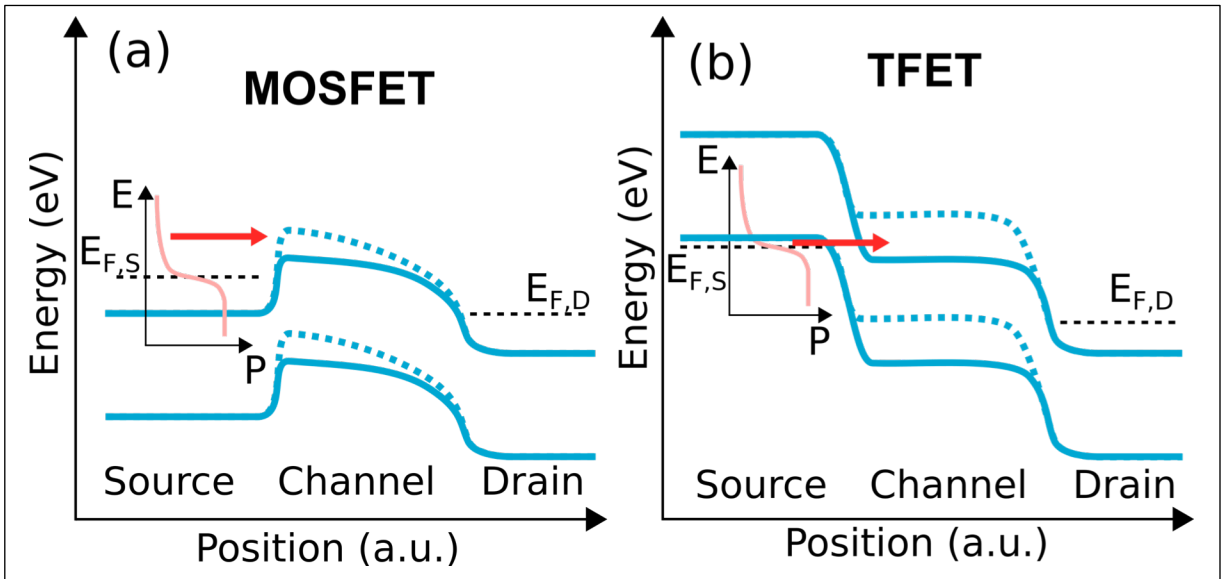


Figure 1(a) Energy band diagram for a MOSFET with applied drive voltage. (b) Energy band diagram for a TFET with applied drive voltage.

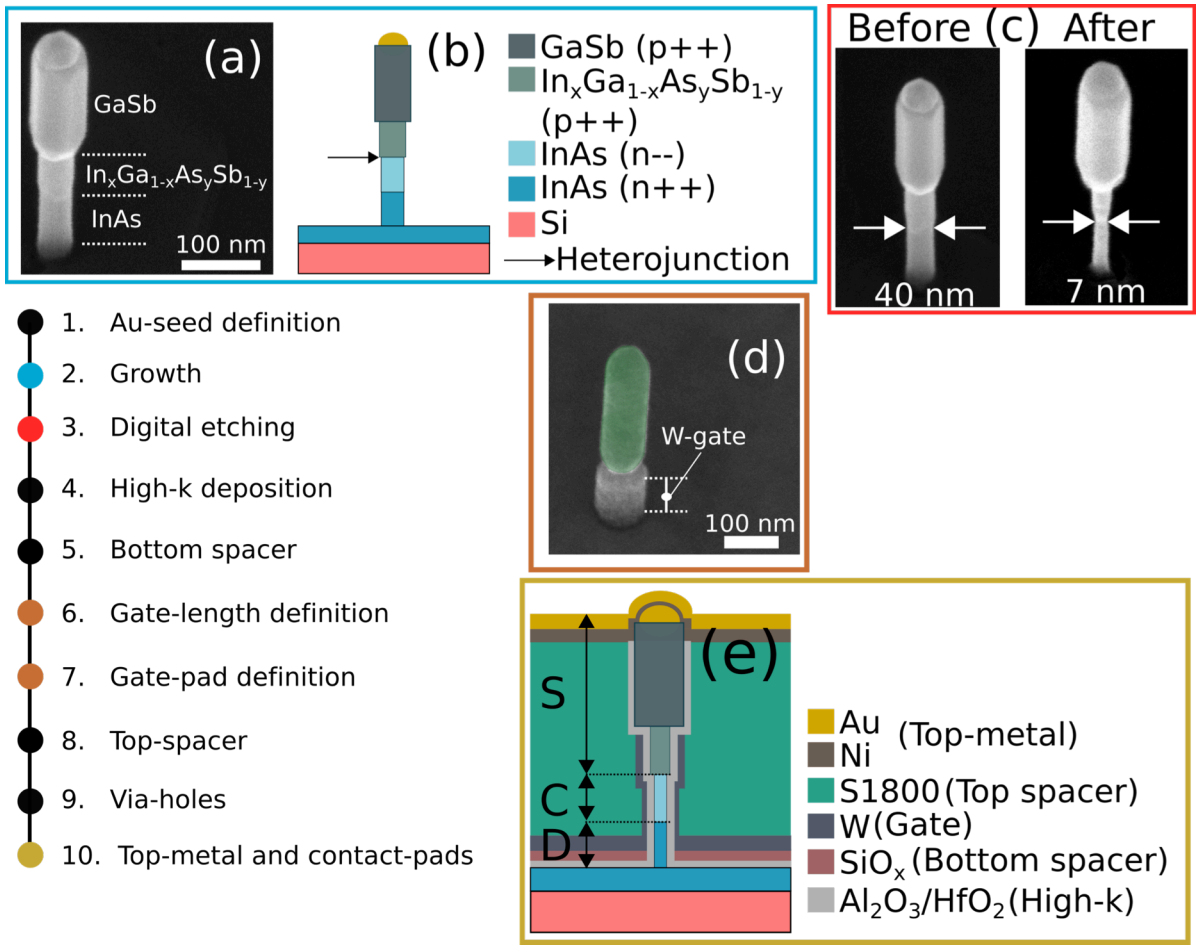


Figure 2 Flow chart of processing. (a) A SEM image of a nanowire after the growth. Bottom segment is InAs with bottom half doped which corresponds to the drain and top half is undoped, which is the channel region. Heterojunction is between InAs and $In_xGa_{1-x}As_ySb_{1-y}$ (x=0.32, y=0.72). (b) Illustration of nanowire, which shows different segments of the nanowire. Arrow indicates the heterojunction. (c) A SEM images that show how the thickness of channel region is reduced by using digital etching. The process allows for reduction of InAs-diameter down to 7 nm, however with a low yield. (d) A SEM image where the GaSb segment is colored in green. W-contact that forms the gate-all-around is surrounding the InAs and InGaAsSb. (e) Schematic illustration of a finished device, where letters mark different regions of the device D=drain, C=channel, and S=source.

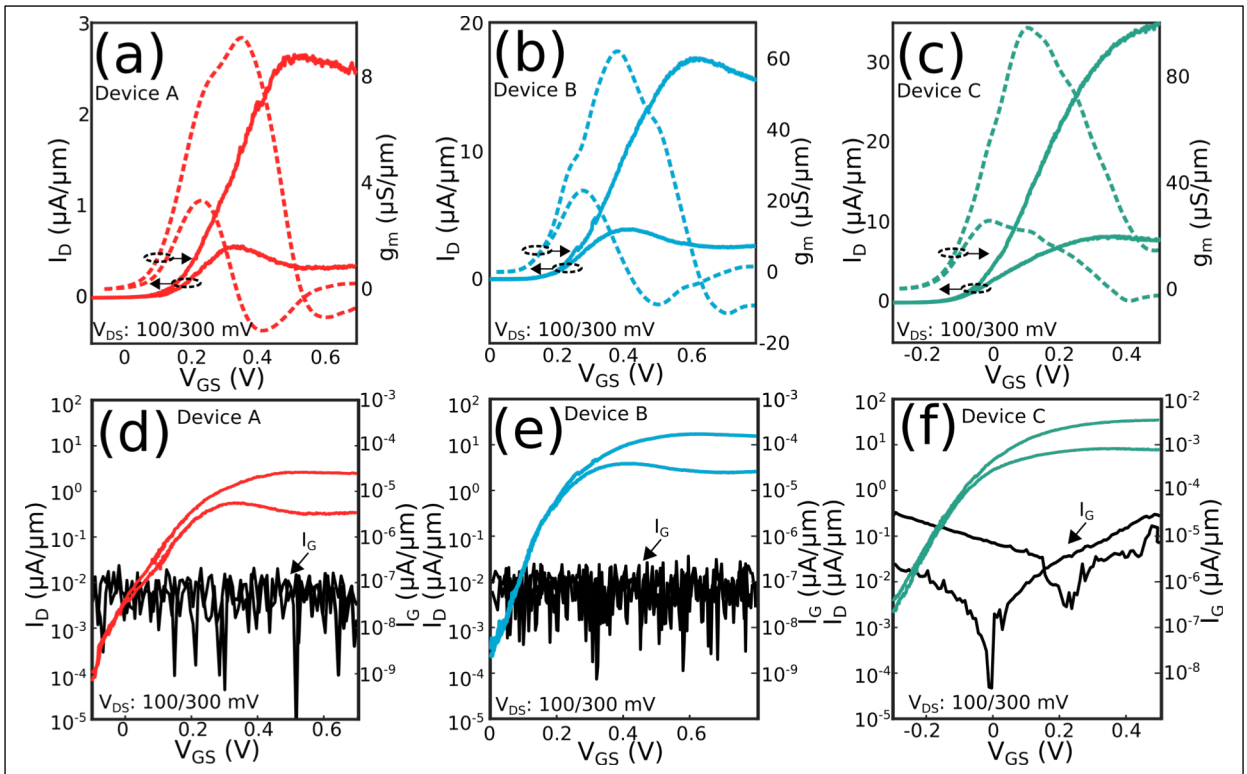


Figure 3 Transfer curves of devices with different doping. Figure (a, d) shows drain current from Device A, Figure (b, e) shows drain current from a Device B, and Figure (c, f) shows drain current from a Device C. The general trend observed is increasing transconductance with increasing doping. Same trend is observed for the off-current.

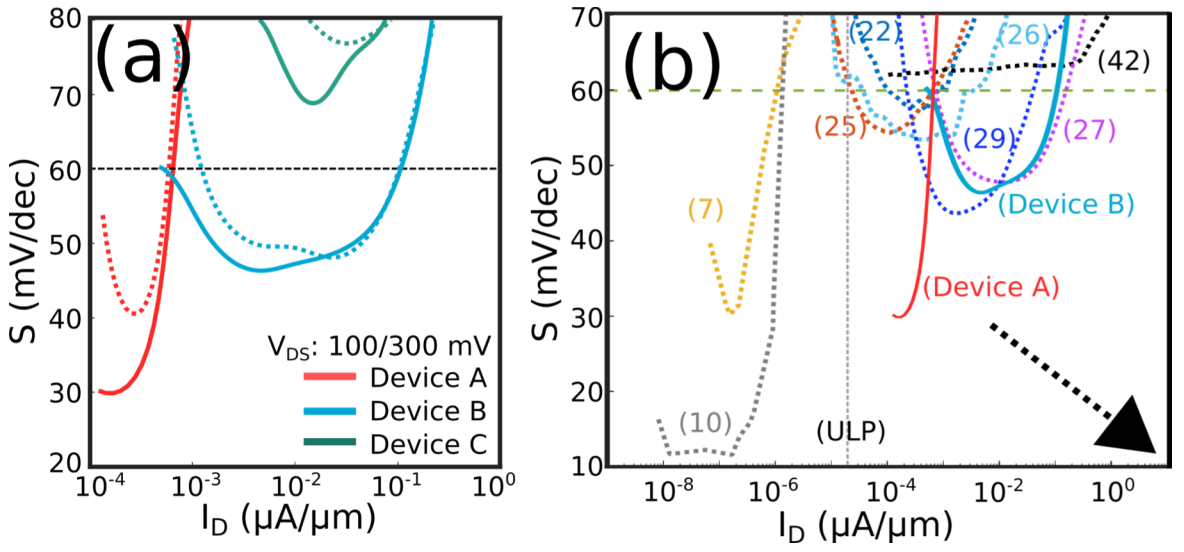


Figure 4 (a) Subthreshold swing as a function of drain current for devices presented in figure 3. The general trend is increasing $S_{MIN}$ with increasing source doping. Solid lines are for $V_{DS}$ of 100 mV and dotted line are for $V_{DS}$ of 300 mV. (b) Benchmarking of TFETs in this work with TFETs data published by the authors and other research groups. We have chosen to use data from Si or III-V based TFETs that have demonstrated ability to operate below thermal limit using drive voltages between 100-300 mV. All data, expect for (26), shown in this graph is for $V_{DS}$ of 100 mV. Data for (26) is for $V_{DS}$ of 300 mV. Data for (42) is for a Si FinFET with Lg = 16 nm. Off-current of transistors used in ultra low power (ULP) applications is set to 15-20 pA/um. Dotted ULP line marks this region.

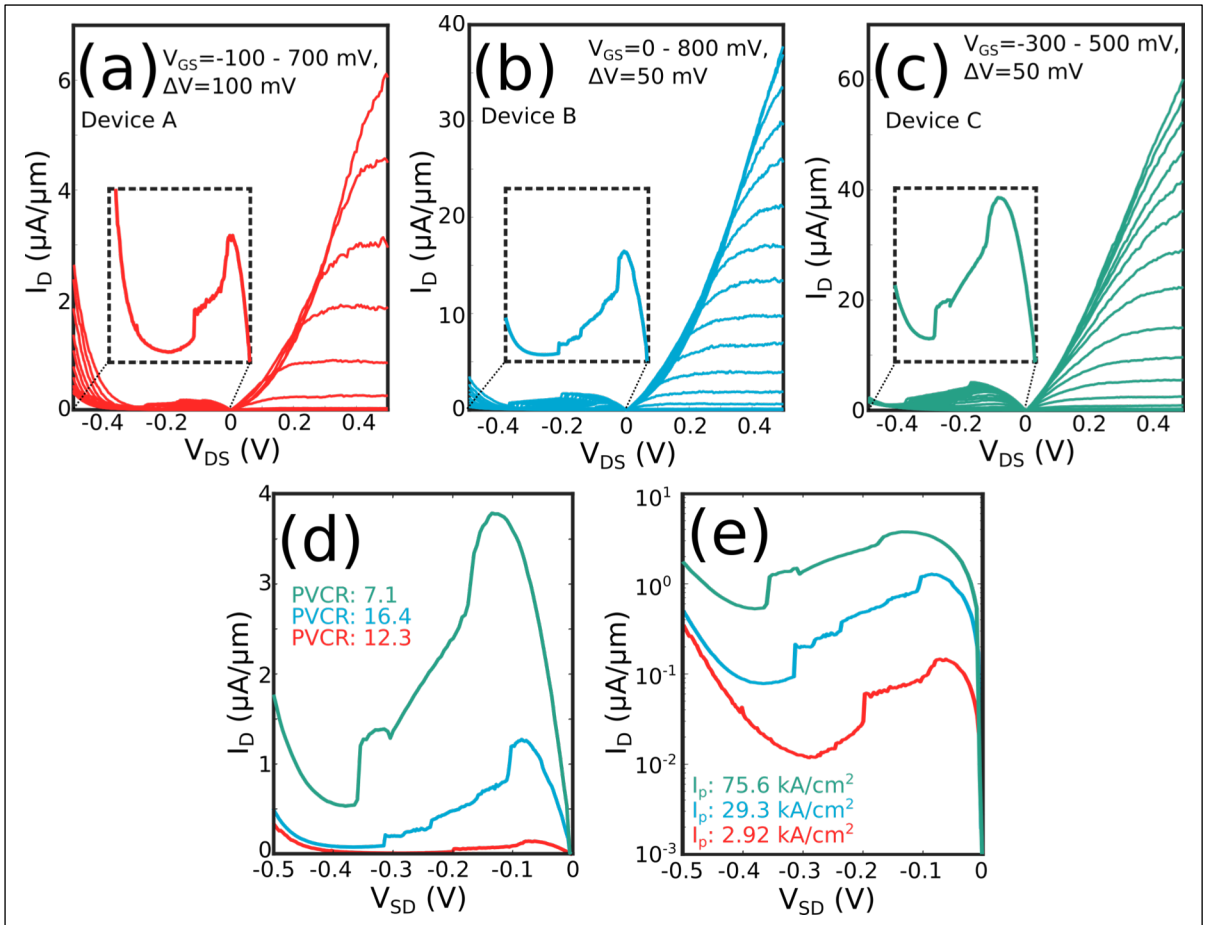


Figure 5 (a-c) Output data for the same devices presented in Figure 3, from Sample A (red), Sample B (blue) and Sample C (green). All three devices show negative differential resistance. In Figure (d and e) the NDR region of these devices are compared. The device from Sample B exhibits the highest peak-to-valley ratio, but not the largest peak current, which is exhibited by the device from Sample C. Both peak and valley currents are increasing with the doping. (Reverse sweep in figures (a-c) was performed with common drain configuration. Forward sweep in all figures was performed with common source configuration.)

Supplementary:

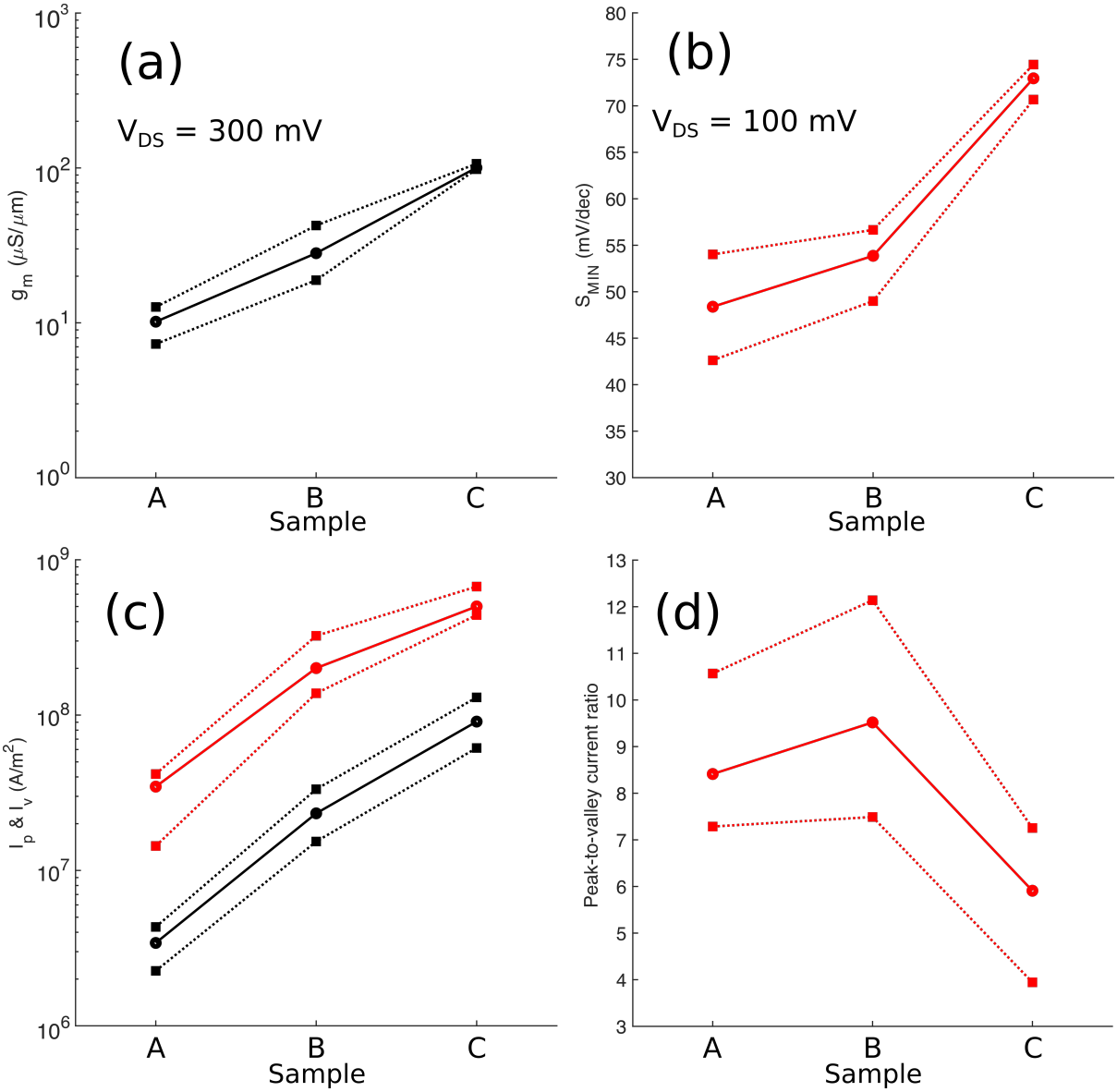


**Figure S1** Statistical data from the samples used in the article. The solid line represents median values, while the lower and upper dotted lines are for 25th and 75th percentile, respectively. Figure a and b show maximum transconductance and minimum point subthreshold swing, respectively. Peak and valley currents in Figure (c) are determined at $V_{GD}$, which results in highest PVCR during the sweep.