Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology

Törmänen, Markus; Sjöland, Henrik

Published in:
Proc. IEEE Radio Frequency Integrated Circuits Symposium

2009

Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology

Markus Törmänen and Henrik Sjöland

Department of Electrical and Information Technology, Lund University, Lund, SE-221 00, Sweden

***Abstract* — Two 24 GHz 130-nm CMOS receiver front-ends using System-on-Package (SOP) technology are demonstrated. CMOS dies featuring a two-stage LNA, a passive mixer, and output buffers are flip-chipped to a glass carrier featuring low loss baluns. One design uses glass baluns for both RF and LO input, whereas the other uses an active RF balun on-chip. The fully differential front-end measures; 20.7dB conversion gain, 7.8dB NF, -23.3dBm CP_{1dB}, -12.6dBm IIP3, 16.3dBm IIP2, and 44dB LO to RF isolation. The single-ended input front-end measures; 14.7dB conversion gain, 8.5dB NF, -21.1dBm CP_{1dB}, -10.4dBm IIP3, 17.6dBm IIP2, and 51dB LO to RF isolation.**

***Index Terms* — CMOS integrated circuits, Flip-chip devices, Frequency conversion, Microwave mixers, Microwave receivers.**

I. Introduction

The evolution of CMOS technology in the past decade along with its excellent integration capabilities has made it an attractive technology for microwave and millimeter wave wireless transceivers. Publications have shown good performance for CMOS receivers at 60 GHz [1], and 24 GHz [2], using single-ended topologies.

Differential receiver topologies are known to have higher linearity and better stability compared to single-ended ones, at the cost of higher power consumption. A disadvantage of differential topologies, however, is that the antenna signal typically is single-ended, and that a balun is needed to convert it to differential form. To achieve good noise performance the balun must have low losses, which makes it difficult to implement on a CMOS chip. The System-on-Package [3], SOP, concept can improve the performance by moving critical passive components like baluns from chip to a low loss glass carrier [4]. However, at microwave frequencies, reliable models for chip to carrier transitions are vital, otherwise package parasitics can seriously degrade the performance. An illustrative example of the SOP concept possibilities is shown in Fig. 1.

This paper presents measurement results from two different SOP front-ends. One front-end uses a fully differential chip, and the other has a chip with single-ended RF input. The single-ended chip features a novel active low noise balun, and the idea is to compare the performance of the two different solutions, one relying on SOP technology and the other mainly on CMOS integration. The CMOS dies are flip-chipped to glass carriers where low loss baluns are realized for RF and LO input signals (the chip with the single-ended RF input just uses an LO balun on the carrier).

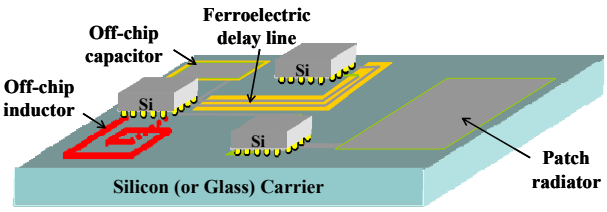


Fig. 1. Example of System-on-Package (SOP) possibilities.

II. Circuit Design

The block schematics of the two front-ends are shown in Fig. 2. The part implemented on the CMOS die consists of a two-stage LNA, a passive double balanced mixer, and open-drain IF output buffers.

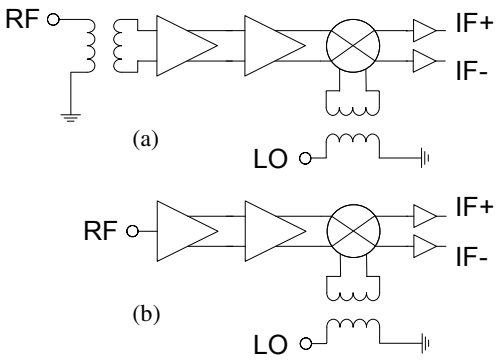
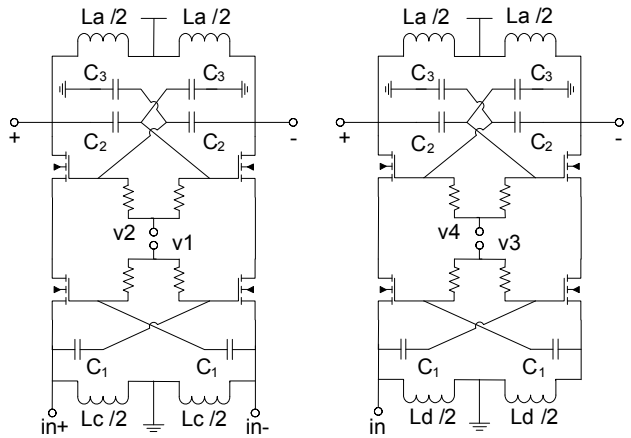


Fig. 2. Front-end block schematics. (a) Fully differential front-end using glass carrier baluns for RF and LO. (b) Front-end with single-ended RF input using glass carrier balun for LO.

The baluns, to generate the differential RF and LO signals, implemented on the glass carrier are also shown in the figure.

A. Chip design

The input stages of the two front-ends are shown in Fig 3. The differential front-end input stage consists of a common gate (CG) stage with cascode devices for increased isolation. Common-gate stages are known to provide wide band input match. Capacitive cross-coupling with capacitors C_1 is used for increased stability and noise performance. Techniques using capacitive-cross coupling at the input, or feed-forward noise cancellation, to improve the noise performance of LNAs are well known [5]-[7]. An inductorless active balun LNA with good wideband performance has also been reported [8]. However, with 130-nm CMOS inductorless techniques are not feasible at 24 GHz, so differential input and output inductors are used to tune the circuit to the operating frequency. The single-ended front-end input stage is similar to the differential one, except that one input terminal has been removed. The differential output signal is achieved through the capacitive cross-coupling and the coupling of the differential source inductor, Ld, [9].

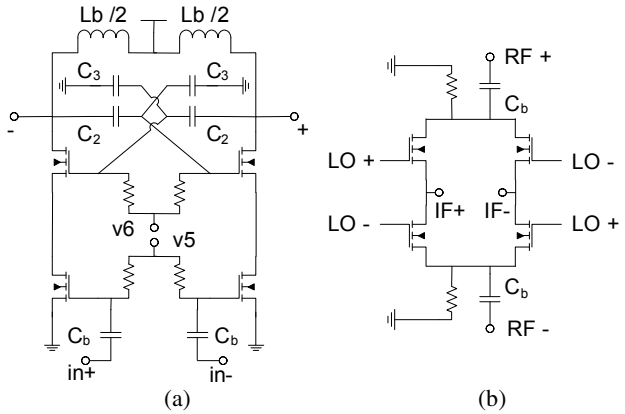


(a) (b)

Fig. 3. First stage of the LNAs. (a) The differential input stage. (b) The single-ended input stage.

A capacitive cross-coupling technique is used also at the output. The purpose is to further increase the differential signal isolation. Capacitors C2 and C3 form voltage dividers used to feed part of the output signal to the gate of the opposite side cascode devices [4]. Using this technique the currents due to the drain-source conductance of the cascode devices can be cancelled for differential signals.

Both front-ends have the same second stage of the LNA. It consists of a differential common-source (CS) stage with cascode devices and capacitive cross-coupling, as is shown in Fig. 4(a). The two stages of the LNA provide sufficient gain for a passive mixer to be used. The output of the second LNA stage is loaded by the input impedance of the mixer and is tuned to the operating frequency by the differential inductor Lb. The passive double-balanced mixer is shown in Fig. 4(b). The RF signal is AC-coupled to the mixer, preventing DC current, and setting the DC voltage to zero using the resistors.



(a) (b)

Fig. 4. (a) The second stage of the LNA. (b) The passive double-balanced mixer.

The LNAs use differential inductors. Their geometries were found using FastHenry in combination with an in-house inductor optimization software, Indentro [10]. The ADS Momentum tool was also used to simulate the interconnect to the inductors. The simulated inductor data for 24 GHz is shown in Table I. Patterned ground shields in metal 1 are used beneath all inductors to block capacitively coupled substrate losses.

TABLE I
INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
La	2	300	16.4	114.3
Lb	2	410	18.8	87.2
Lc	2	490	20.2	71.1
Ld	3	610	23.5	49.8

Also included on the chip for measurement purposes, shown in the block schematics of Fig. 2, are open-drain IF buffers designed to drive 50 ohm loads.

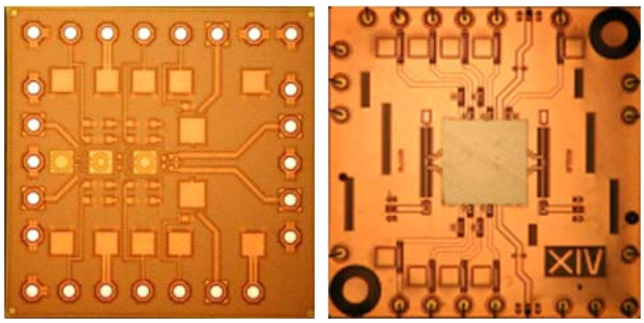
B. Glass carrier

The glass carrier is fabricated in STMicroelectronics commercial integrated passive process optimized for high-Q RF passive components. The carrier uses three metal layers. The baluns realized on carrier have a measured insertion loss of approximately 0.3 dB at the frequencies of interest.

III. LAYOUT

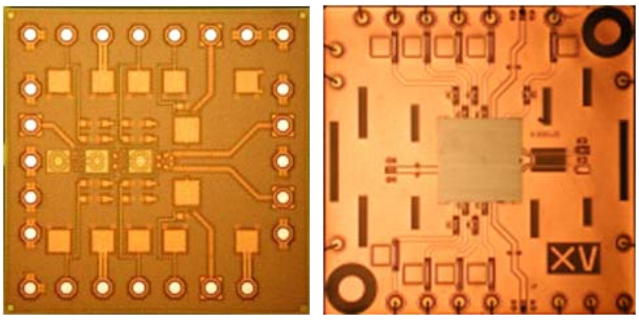
The CMOS dies were fabricated in a 6 metal layer, 4 Cu and 2 AlCu, 130 nm RF CMOS process from Infineon Technologies. Each front-end die version was flip-chipped to two different glass carrier designs, using two different versions of baluns, denoted hereon after as balun 1 (B1) and balun 2 (B2). This means that there are four different carrier designs in total.

A die microphotograph of the fully differential front-end is shown in Fig. 5(a). This chip mounted on a glass carrier using balun 1 for the RF and LO input signals is shown in Fig. 5(b). The chip can be seen in the middle of the figure and the baluns to the left and right of the chip.



(a) (b)

Fig. 5. (a) Die microphotograph of the fully differential front-end, 1.53 mm^2. (b) Photograph of the chip mounted on carrier using balun 1 for RF and LO input signals, 5x5 mm^2.



(a) (b)

Fig. 6. (a) Die microphotograph of the front-end with single-ended input, 1.53 mm^2. (b) Photograph of the chip mounted on carrier using balun 2 for the LO input signal, 5x5 mm^2.

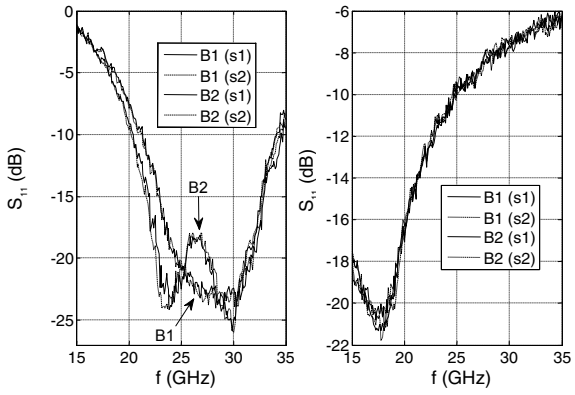
A die microphotograph of the front-end with single-ended input is shown in Fig. 6(a). This chip mounted on a glass carrier using balun 2 for the LO signal is shown in Fig. 6(b). The balun can be seen on the right side of the chip, and the RF input to the left of the chip, where a CPW line connects the RF input to the probing pads. The supply, bias and IF output signals were wire bonded from the carrier to a PCB. The supply and bias lines are decoupled using capacitors on the chip, carrier and PCB.

IV. MEASUREMENT RESULTS

There are four different designs, since each CMOS die type was flip-chipped to two different carriers using balun 1 and balun 2. Two samples of each design have been measured. The DC power consumption using a 1.2 V supply, excluding the open-drain buffers, is 28.6 mW for the fully differential front-end and 33.8 mW for the single-ended one. The two open-drain buffers consumed 12.5 mW altogether from a 1 V supply.

The measurements were performed with a probe station, using Infinity GSG probes from Cascade Microtech for the RF and LO inputs signals on the carrier. The IF outputs were connected to a Minicircuits balun, T2-1T (0.07 to 200 MHz), through bias-Ts.

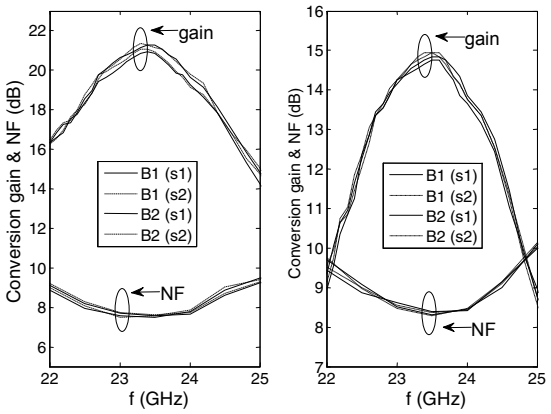
The measured input matching for both front-end versions is shown in Fig. 7. A second resonance is observed for the fully differential front-end using balun 2 in Fig. 7(a). The input matching shifted down in frequency for the front-end with single-ended input, although with S_{11} below -10 dB up to 25 GHz. This was probably due to improper modeling of the input CPW line on the carrier.



(a) (b)

Fig. 7. Input matching (two samples measured for each design). (a) The fully differential front-end. (b) The front-end with single-ended input.

The measured (de-embedded) conversion gain and noise figure is shown in Fig 8. The conversion gain was measured at an IF frequency of 3 MHz and the noise figure at 25 MHz. The fully differential front-end achieves a conversion gain of 20.7 dB and an NF of 7.8 dB, whereas the front-end with single-ended input achieves a conversion gain of 14.7 dB and an NF of 8.5 dB.



(a) (b)

Fig. 8. Conversion gain and NF (two samples measured of each design). (a) The fully differential front-end. (b) The front-end with single-ended RF input to the die.

The linearity was measured using two-tone tests, one for third order and one for second order intermodulation. The tones were chosen such that the intermodulation product to measure occurred at an IF of 3 MHz. A fifth order low-pass filter, with a cut off frequency of 5 MHz, was used when measuring the second order nonlinearity to prevent intermodulation of the first order IF output tones (placed at 20 and 23 MHz) in the spectrum analyzer. The measured linearity is summarized in Table II, where the result for each design is an average from two measured samples.

TABLE II
FRONT-END LINEARITY

Design	CP_{1dB} (dBm)	IIP3 (dBm)	IIP2 (dBm)
Diff. B1	-23.3	-12.6	16.3
Diff. B2	-24.5	-13.7	15.7
SE B1	-21.1	-10.4	17.6
SE B2	-21.5	-10.6	17.1

The LO to RF isolation has also been measured in the frequency band 22 to 25 GHz. In this frequency range the isolation is at least 44 dB for the fully differential front-end and at least 51 dB for the front-end with single-ended input.

V. CONCLUSION

Two SOP front-ends have been demonstrated, one using a fully differential CMOS die with low loss baluns on glass carrier for the RF and LO input signals. The other one using a single-ended RF input to the chip, converted to differential form in a novel merged low noise amplifier and balun, using a low loss balun on glass carrier only for the LO input signal.

The fully differential version achieves a conversion gain of 20.7 dB, NF of 7.8 dB, CP_{1dB} of -23.3 dBm, IIP3 of -12.6 dBm, IIP2 of 16.3 dBm, and an LO to RF isolation of 44 dB. The single-ended version achieves a conversion gain of 14.7 dB, NF of 8.5 dB, CP_{1dB} of -21.1 dBm, IIP3 of -10.4 dBm, IIP2 of 17.6 dBm, and an LO to RF isolation of 51 dB.

Although the single ended version uses one glass balun less, thanks to the novel low noise active balun its performance is not far from that of the fully differential design. If the input matching could be improved the performance would probably be even better.

ACKNOWLEDGEMENT

The authors wish to acknowledge the support of Ericsson AB for financing this research as part of the MEDEA+ project 2T401 HI-MISSION. They would also like to thank Infineon Technologies for access to their CMOS technology, STMicroelectronics for access to their glass carrier technology, and the Knut and Alice Wallenberg foundation for financial support in building up the high frequency measurement laboratory.

REFERENCES

[1] B. Razavi, "A 60-GHz CMOS Receiver Front-End," *IEEE JSSC*, vol. 41, no. 1, pp. 17-22, January 2006.

[2] X. Guan and A. Hajimiri, "A 24GHz CMOS Front-end," *Proc. IEEE ESSIRC*, September 2002, pp. 155-158.

[3] R. R. Tummala, "Packaging: Past, Present and Future," *IEEE 6th International Conference on Electronic Packaging Technology*, pp. 3-7, 2005.

[4] M. Törmänen and H. Sjöland, "A 20-GHz 130-nm CMOS front-end using baluns on glass carrier,"in *Proc. IEEE SCS*, November 2008, pp. 1-4.

[5] W. Zhuo, S. Embabi, J. Pineda de Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design," in *Proc. ESSCIRC*, September 2000, pp. 77-80.

[6] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling," *IEEE JSSC*, vol. 39, no. 2, pp 275-282, February 2004.

[7] A. Amer, E. Hegazi, and H. Ragai, "A Low-Power Wideband CMOS LNA for WiMAX," *IEEE TCAS-II*, vol. 54, no. 1, pp. 4-8, January 2007.

[8] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Ouput Balancing, Noise-Canceling and Distorsion-Canceling," *IEEE JSSC*, vol. 43, no. 6, pp 1341-1350, June 2008.

[9] H. Sjöland, "Merged Low-Noise Amplifier and Balun", US2008136528 (A1), US Patent Office, 2008-06-12

[10] N. Troedsson, http://www.indentro.com, 2009.