Efficient mm-Wave Transmitter Design in CMOS Technology

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Till min morfar
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Abstract

An increasing demand of higher data rates in wireless communication forces the industry to look to higher frequencies to find the required bandwidths. This thesis is about analog transmitters in CMOS for millimeter-wave communication, and it focuses on improving power amplifiers and frequency generation circuits, and increase their efficiency. This thesis starts with an introduction to millimeter-wave transmitters in CMOS, standards and beamforming. It then continues with a brief introduction to millimeter-wave power amplifier design and design of local oscillators at millimeter-wave frequencies. The last part of the thesis consist of six papers, which present eleven manufactured and measured millimeter-wave circuit designs. Paper I presents a two-stage, 65-nm CMOS, Class-A PA for the 60-GHz band. It employs capacitive cross-coupling neutralization for higher differential isolation and gain, without the need to increase the power consumption. It achieves 18.5 % peak-added-efficiency. Paper II presents a varactorless VCO in 65 nm CMOS, operating in the 60-GHz band. In paper III, the efficiency of the popular source-node filtering technique for improved phase-noise performance is investigated through measurements of two same-chip 60-GHz VCOs in FD-SOI CMOS. The filtered VCO achieves a state-of-the-art figure-of-merit of -187.3 dBc/Hz. Paper IV presents two FD-SOI CMOS VCOs for the 30-GHz and the 60-GHz band, that achieve ultra-low power consumption, also at full supply voltage. In paper V, a phase-locked loop in 28-nm FD-SOI CMOS for 5G transceiver systems is proposed. Its VCO operates at around 55 GHz. The paper describes the disadvantages of using a too high input reference frequency, but also proposes a new architecture that handles the increased settling time by mode-switching. It also includes a novel charge-pump current-mismatch mitigation technique based on feedback, and a novel wideband and low-power injection-locked divide-by-three circuit. The phase-locked loop consumes only 10 mW of power, has an integrated jitter of 176 fs, and demonstrates a state-of-the-art figure-of-merit of -245 dB. Paper VI describes a wideband injection-locked divide-by-two circuit in 28-nm FD-SOI CMOS. It achieves a locking range of 30 % at the low power consumption of 4.3 mW.

Populärvetenskaplig sammanfattning

Vi lever i en uppkopplad värld, där vi tar för givet att det alltid finns mobil- eller WiFi-täckning så att vi kan kontakta dem som vi bryr oss om, hitta rätt i en ny stad, finna nog med information att fatta ett beslut, eller helt enkelt bara roa oss. Detta är inte på något vis endast ett svenskt fenomen. Det finns idag 7,9 miljarder mobilabonnemang på jorden, vilket är 200 miljoner fler än vad det finns människor. En framtidsvision som redan håller på att hända är att inte bara människor, utan även föremål som t ex hushållsapparater, bilar och medicinska implantat skall kunna vara uppkopplade. I varje uppkopplad pryl finns det en sändare och mottagare, som kan omvandla de elektromagnetiska signalerna i luften till digitala data som vi har i våra datorer och telefoner. Eftersom signalerna i luften är analoga, så är även den del av sändaren och mottagaren som sitter närmast antennen analog. Just denna del, specifikt sändaren och dess ingående delar, är vad denna avhandling handlar om. För att en sändare skall passa i konsumentelektronik, måste den vara billig och dessutom strömsnål, så att batteriet håller länge. Billigare kan den bli om man gör den i en vanlig sorts kiselteknologi som kallas CMOS, och strömsnålare kan den bli om man noggrant går igenom varje liten del i sändaren och försöker att hitta nya sätt att spara ström. Sändare utsätts också hela tiden för hårdare krav. Ju bättre upplösning som filmen som vi vill streama har, desto mer data måste vi skicka samtidigt. När alla vill ha högre datahastigheter, tar utrymmet i luften som vi delar helt enkelt slut. Tänk dig ett rum, där alla skriker samtidigt. Ingen kommer att bli hörd och förstådd. Det finns redan många system för att utnyttja vårt gemensamma utrymme bättre, och det finns hårda krav på hur sändare får lov att sända för att störa andra så lite som möjligt. Ett system för att använda rummet bättre, är att alla pratar endast när det är deras tur. Ett annat snillrikt system efterliknar en situation där alla i rummet talar olika språk, vilket gör det lättare att urskilja en enskild person. Ibland använder avancerade system även trattar (antenner) för att se till att ljudet går mest i den riktning som man vill. Att alla pratar på olika frekvenser är ytterligare ett sätt, ungefär som om någon bara får tala med basröst, och någon annan bara i falsett. Men oavsett hur många finurliga sätt som man har kommit på, börjar platsen ta slut. Vad som ligger härnäst i utvecklingen är att tillåta och möjliggöra att kommunikationen kan ske på högre och högre frekvenser. Det är svårt, eftersom naturen har ordnat det så, att ju högre frekvenser som används, desto mer dämpas signalen i luften. Dessutom blir det svårare att använda den billiga och vanliga CMOS-kiselteknologin, eftersom de individuella transistorerna får svårare att hänga med och fungera korrekt. Vad sändarna som den här avhandlingen handlar om måste klara är att skicka rätt data med

en bärvågsfrekvens på upptill ungefär 65 GHz. Eftersom en elektromagnetisk signal med en frekvens mellan 30 och 300 GHz har en våglängd som är mellan en och tio millimeter, så kallas det här frekvensområdet för millimetervågor. Som en jämförelse använder inga mobiltelefoner i dagsläget frekvenser över 6 GHz. Det finns redan produkter som kan kommunicera kring 60 GHz, men jämfört med flera miljarder mobiltelefoner är de är extremt få, och för att kunna bli en del av vår vardag behöver de bli billigare, och förbättras genom att varje individuell del görs mer effektiv. Vi kallar kretsar för mer effektiva om de kan utföra sina uppgifter korrekt men med mindre förbrukad effekt, eller om de kan göra sin uppgift bättre med samma effektförbrukning som innan. Denna avhandling fokuserar på två delar av analoga millimetervågssändare: effektförstärkare, som ofta förbrukar mer än hälften av den totala effekten i en sändare och där varje uns av förbättring ger stora effekter, samt den grupp av kretsar som är ansvariga för frekvensgenereringen. En förstärkare som är ovanligt effektiv i sin klass har konstruerats, likaså en faslåst loop som utför sin uppgift lika bra som andra publicerade faslåsta loopar, men med mindre än halva effektförbrukningen. Olika förslag på ytterligare förbättringar av viktiga delar i faslåsta loopar har utvecklats, och lett till konstruerade och mätta spänningsstyrda oscillatorer och injektionslåsta delare som visar att dessa kretsar kan klara sin uppgift och samtidigt bara förbruka en femtedel till en tredjedel av vad som är standard. Sammantaget presenteras elva kretsar som alla innehåller exempel på hur millimetervågssändare kan bli mer effektiva.

Preface

This dissertation summarizes my academic work for a PhD degree in Electrical Engineering in the Analog RF Design group, at the Department of Electrical and Information Technology, Lund University, Sweden. This work was funded by the Swedish Research Council (Vetenskapsrådet) and the European Commission in the framework of the H2020-ICT-2014-2 project Flex5Gware (Grant agreement no. 671563). The chip fabrication was donated by STMicroelectronics. The dissertation is divided into two parts. The first part gives an introduction to the research field, and the second part consists of the included research papers, as listed below.

Included Research Papers

The main scientific contribution is derived from the following publications:

Paper I T. Forsberg, H. Sjöland and M. Törmänen, "A two-stage mm-wave PA with 18.5% PAE in 65 nm CMOS," in *Proc. of 2015 Asia-Pacific Microwave Conference (APMC)*, Nanjing, China, Dec. 6–9 2015, pp. 1–3. [1]

Paper II T. Forsberg, H. Sjöland and M. Törmänen, "A 65 nm CMOS varactorless mm-wave VCO," in *Proc. of 2014 International Symposium on Integrated Circuits (ISIC)*, Singapore, Dec. 10–12 2014, pp. 54–57.

Paper III T. Forsberg, J. Wernehag, A. Nejdel, H. Sjöland and M. Törmänen, "Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 5, pp. 509–511, May 2017.

Paper IV T. Forsberg, J. Wernehag, H. Sjöland and M. Törmänen, "Two Ultra-Low Power mm-Wave Push-Pull VCOs in FD-SOI CMOS," in *Proc. of 2018 Asia-Pacific Microwave Conference (APMC)*, Kyoto, Japan, Nov. 6–9 2018, pp. 1–3.

Paper V M. Abdulaziz, T. Forsberg, M. Törmänen and H. Sjöland, "A 10 mW mm-Wave Phase-Locked Loop with Improved Lock Time in 28-nm FD-SOI CMOS," *IEEE Transactions on Microwave Theory and Techniques*, pp 1–12, 2018. *Submitted.*

[1] Won Best Student Paper Award at the conference

Paper VI T. Forsberg, J. Wernehag, H. Sjöland and M. Törmänen, "A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CM," in *Proc. 2018 IEEE Nordic Circuits and Systems Conference (NORCAS)*, Tallinn, Estonia, Oct. 30–31 2018, pp. 1–4.

Related Publications

During my Ph.D. studies, I have also co-authored the following papers, which contain overlapping material, but are not considered a part of this dissertation.

- I. Din, S. Anderson, T. Forsberg and H. Sjöland, "A 24 GHz, 18 dBm, Broadband, Three Stacked Power Amplifier in 28nm FDSOI," in *Proc. of IEEE NORCAS 2018*, Tallinn, Estonia, Oct. 30–31 2018, pp. 1–4.
- A. Bondarik, T. Forsberg, D. Sjöberg, H. Sjöland and M. Törmänen, "Microstrip Antenna Array Integrated with a Two-stage mm-wave CMOS Power Amplifier," *IEEE Microwave and Wireless Components Letters*, 2018. *Submitted.*

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First of all, I would like to express my sincere thanks to my supervisor Markus Törmänen. One of the most impressive ways that his deep understanding of all subjects at hand manifests is his ability to swiftly find the core of the most complex technical problems and know where to focus to reach a solution. Without his guidance, none of this would have been possible. I will be forever thankful for the chance that I was given to do research in such an interesting field. I am also grateful to my co-supervisor, who is also my initial main supervisor, Henrik Sjöland. Not only is his knowledge of the field brilliant, he has also taught me about how to properly present my research, and he is a true role model when it comes ethical questions surrounding research in general. A huge thank you also goes to my co-supervisor Johan Wernehag, for his support in trying times and his ability to put thing into perspective.

Thank you also to all the people in the Integrated Electronics Systems group that made life in our corridor feel friendly and supportive. I will always remember fondly my fellow PhD students in the RF Analog group that I had the fortune to work with, and that brightened up my days. Thanks to Carl Bryant and Jonas Lindstrand for the circuits that we created once when time was short, thank you to Anders Nejdel and Waqas Ahmad for the collaboration to create pad designs that has since been used by me and many others. I would also like to extend a very special thank you to Mohammed Abdulaziz, who endured long sessions in the lab with me, striving to get our design to work. His untiringly positive outlook on things is truly inspiring and it has set a great example for me.

To all the people at EIT that provide invaluable technical and administrative support: I am grateful for your efforts. Thank you to Göran Jönsson, Andreas Johansson, and Martin Nilsson for maintaining the lab, and to Lars Hedenstjerna for making beautifully perfect parts that made my measurements possible. Thank you to Stefan Molund and Erik Johnsson for not giving up trying to fix all of my software issues. Thank you to Pia Bruhn, Anne Andersson and Elisabeth Nordström for your magical ability to make all my administrative task and questions seem trivial.

During my PhD studies I have been fortunate enough to be able to go to international conferences, through the financial support of ÅForsk, the IEEE Microwave Theory and Techniques Society, and the Royal Physiographic Society of Lund. For this, I am very grateful.

I would like to send a thank you to all the people involved in, and around, the Microwave Electronics Laboratory at Chalmers University of Technology, for allowing me to make some of my measurements with them, and for providing

such a welcoming and scientifically interesting environment.

I owe so much to my previous colleagues at Ericsson in Lund. Sometimes it is Lars Sundström or Peter Caputa that provides me with some invaluable piece of information to further my knowledge, sometimes it is Per Sandrup that helps me to get hold of some crucial software licenses in the middle of Christmas vacations, or Peter Herrder that lends me essential pieces of lab equipment, and always, it is everyone, just being wonderfully supportive.

I would also like to thank my family. To my mother Bodil, my father Bo-Göran, and my mother-in-law Birgitta, thank you for always being there for me. To my amazing sister Ulrika and to Daniel, thank you for being my role models for my academic undertakings, and for being generally awesome people. Thank you to Sven, my kind husband, who has patiently endured my long days before deadlines and never stopped believing in me.

Finally, to all the people that I was unable to mention here, thank you!

List of Acronyms

3GPP	3rd Generation Partnership Project
AM	Amplitude modulation
CML	Current-mode logic
CMOS	Complementary metal-oxide-semiconductor
CP	Charge pump
DAC	Digital-to-analog converter
dc	Direct current
DPD	Digital pre-distortion
FD-SOI	Fully depleted silicon-on-insulator
FOM	Figure of merit
GaAs	Gallium-Arsenide
HBT	Heterojunction bipolar transistor
IF	intermediate frequency
ILFD	Injection-locked frequency divider
ISM	Industrial, scientific and medical
LO	Local oscillator
mm-wave	millimeter-wave
NMOS	n-channel metal-oxide-semiconductor field-effect transistor
NR	New radio
OFDM	Orthogonal frequency-division multiplexing
PA	Power amplifier
PAE	Power-added efficiency
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PFD	Phase-frequency detector
PLL	Phase-locked loop
PM	Phase modulation
PMOS	p-channel metal-oxide-semiconductor field-effect transistor

PN	Phase noise
PPA	Pre-power amplifier
PSRR	Power supply rejection ratio
QAM	Quadrature amplitude modulation
RF	Radio frequency
SOI	Silicon-on-insulator
UTBB	Ultra-thin body and buried oxide
VCO	Voltage-controlled oscillator
WPAN	Wireless personal area network

List of Symbols

$\&$	Logical AND operation
β	Feedback factor
Δ	Difference
$\Delta\Phi$	Phase difference
Δf	Frequency difference [Hz]
λ	Wavelength [m]
ω	Angular frequency [rad/s]
$\omega_{carrier}$	Angular frequency of the carrier [rad/s]
ω_n	Natural frequency of a PLL [rad/s]
ω_{osc}	Angular frequency of oscillation [rad/s]
ω_{range}	Locking range of an ILFD [rad/s]
ω_{res}	Resonance frequency [rad/s]
ϕ_{in}	Input signal phase
ϕ_{out}	Output signal phase
ω_{res}	Resonance frequency [rad/s]
ζ	Damping factor of a PLL
η	Drain efficiency of a PA [%]
θ	Angle [rad]
A	Amplification, gain
B	Noise integration bandwidth [Hz]
C	Capacitance [F]
C_i	Capacitance i [F]
C_{filter}	Filter capacitance [F]
C_{par}	Parasitic capacitance [F]
C_t	Tank capacitance [F]
CLK	Clock signal
CP_{1dB}	1-dB compression point in a PA [dBm]
DN	The "down"-signal to a CP

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F	Amplifier noise factor
f	Signal frequency [Hz]
f_0	Output frequency of an ILFD [Hz]
f_{bb}	Baseband signal frequency [Hz]
f_{corner}	Flicker noise corner in a VCO [Hz]
f_{fb}	Feedback signal frequency to the PFD in a PLL [Hz]
f_{in}	Input signal frequency [Hz]
f_{LO}	Local oscillator signal frequency [Hz]
f_{max}	Maximum signal frequency [Hz]
f_{min}	Minimum signal frequency [Hz]
f_{osc}	Signal oscillation frequency [Hz]
f_{out}	Output signal frequency [Hz]
f_{ref}	Reference signal frequency [Hz]
f_{res}	Resonance frequency [Hz]
f_T/f_{max}	Frequency of unity current gain/unity power in a transistor [Hz]
G	Gain [dB]
g_m	Transistor transconductance [S]
$H(s)$	Transfer function in the Laplace plane
I	Current [A]
I_{cp}	Charge-pump current [A]
I_{inj}	Injected current [A]
I_{osc}	VCO oscillation current [A]
k	Boltzmann constant $[m^2 \cdot kg \cdot s^{-2} \cdot K^{-1}]$
K_{VCO}	VCO gain [Hz/V]
$\mathscr{L}(\Delta f)$	Single-sided PN [dBc/Hz], at distance Δf Hz from the carrier
L_{filter}	Filter inductance [H]
L_t	Tank inductance [H]
M_i	Transistor i
N	PLL division ratio between output and input signal frequencies

P	Power [W]
P_{dc}	dc power consumption [W]
P_{in}	Input signal power [W]
P_{out}	Output signal power [W]
$P_{out,max}$	Maximum saturated output signal power [W]
Q	Quality factor
R	Resistance [Ω]
R_i	Resistance i [Ω]
R_L	Load resistance [Ω]
r_o	Transistor output resistance [Ω]
R_P	Parallel loss resistance [Ω]
RST	Reset signal
T	Signal cycle time [s]
T_{ref}	Reference signal cycle time [s]
UP	The "up"-signal to a CP
V	Voltage [V]
$V_{b,high}$	dc bias voltage for high-side injection in an ILFD [V]
$V_{b,low}$	dc bias voltage for low-side injection in an ILFD [V]
$V_{b,inj}$	dc bias voltage for high-side injection in an ILFD [V]
V_{bias}	dc bias voltage [V]
v_{ctrl}	Control voltage in to the VCO in a PLL [V]
V_{osc}	Oscillation voltage [V]
V_{in}	Input signal voltage [V]
V_{out}	Output signal voltage [V]
V_{var}	Control voltage to the varactor [V]
V_b	dc bias voltage [V]
VDD	dc voltage supply [V]
X_L	Load impedance [Ω]

Introduction

Chapter 1

Introduction

1.1 Motivation

In today's fast-paced world, we have come to take wireless data access for granted. Wherever we go, we expect cellphone or WiFi coverage to aid us in getting in touch with those important to us, finding our way, acquire enough information to make a decision, or simply to entertain ourselves. The number of cellphone subscribers is steadily rising, and already today there are more than 7.9 billion subscriptions in the world – that is 200 million more subscriptions than there are people [1]. It is expected that in the future, subscribers can also be objects, such as home appliances, cars, or medical implants. Hence, the global mobile data traffic is growing fast, and it is forecasted to keep growing at an even faster pace, as in shown in Fig. 1 [2]. The expected required data speeds are rising along with it. The higher the quality of the photos or movies that we send, the more data needs to be transferred rapidly. This data is modulated onto a signal of a specific carrier frequency when sent though the air, and the wider the frequency span that it spreads over around the carrier frequency, the more data it can carry. But we all share the same air, and if everyone yells at the same time, no one will be heard. Several standards for wireless communication try to solve this problem, restricting when and what each access node can send and employing complex techniques that minimize cross-talk. Soon, however, that will not be enough either. So far, almost all carrier frequencies for wireless communication have been below a few GHz, because wireless communication at higher frequencies is hindered by physical phenomena such as higher in-air attenuation, higher penetration loss, and more shadowing effects from obstructing objects. However, going to higher carrier frequencies for wireless communication is a necessary step in the continuous data revolution. Some future communication frequencies are in the millimeter-wave (mm-wave) range. The name "mm-wave" refers to frequencies between 30 GHz and 300 GHz, where wave-lengths are in the range of 1-10 mm. During the past years, a few systems have demonstrated the feasibility of mm-wave

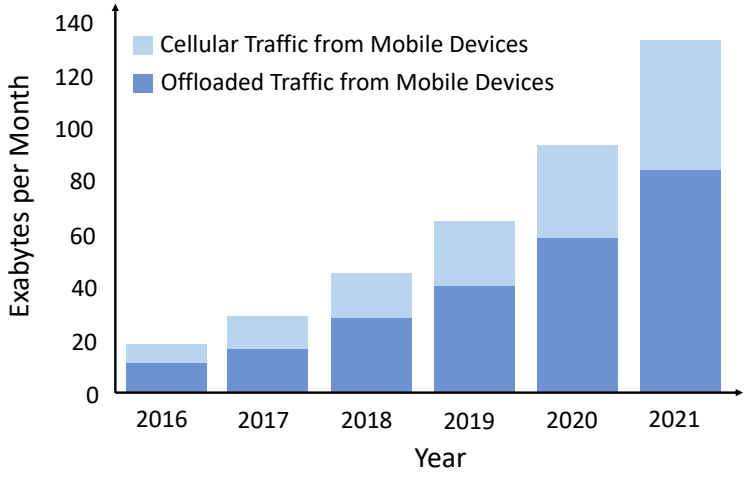


Figure 1: Global mobile data traffic, with forecast. Offloaded traffic is wireless traffic though for instance WiFi or Bluetooth, i.e. not through cellphone networks. Based on [2].

communication, and are today commercially available. However, this does not mean that all problems are solved. To reach a bigger market, the electronics need to be even cheaper. They also need to use less power and still meet the same requirements, which will make batteries last longer and benefits both personal economy and the environment. Going for cheaper circuits often mean using CMOS technology, because it is readily available and adapted for mass-market production. It also facilitates integrating more of the system on the same chip. However, it has some drawbacks compared to other technologies, that need to be addressed and mitigated when designing the transceiver circuits. The cost of manufacturing circuits in CMOS rises with the physical size of the circuit, so they also need to be kept as small as possible. All of these desired traits are interconnected and have complex trade-offs. Some are not entirely understood yet, and all of them are subject to attempts of circumvention.

The aim of this thesis is to investigate how some aspects of mm-wave transmitter circuits in CMOS can be made more efficient, meaning that they are able to perform their task while using both a smaller area and/or a lower power consumption than previous art.

1.2 Outline of the Thesis

The thesis is organized as follows:

Chapter 1 presents the motivation for the dissertation, and its organization.

Chapter 2 introduces mm-wave radio transmitter systems, their building blocks and some commonly used performance metrics.

Chapter 3 explores mm-wave power amplifier design.

Chapter 4 focuses on efficient frequency generation circuits.

Chapter 5 gives summaries and conclusions of the included papers along with the author's contribution.

Chapter 6 provides a discussion with suggestions for future work.

Paper I presents a mm-wave class-A power amplifier with high efficiency.

Paper II presents a varactorless mm-wave voltage controlled oscillator.

Paper III presents an empirical investigation of the impact of using a noise-reducing architecture in mm-wave voltage controlled oscillators.

Paper IV presents two ultra low-power mm-wave voltage controlled oscillators.

Paper V presents a mm-wave analog phase-locked loop for 5G applications, with very low power consumption and an improved lock time.

Paper VI presents a wideband injection-locked divide-by-two circuit.

Chapter 2

mm-Wave Radio Transmitters

This chapter introduces CMOS analog mm-wave transmitter systems. It discusses the environment in which they will work, and presents challenges and solutions related to their design on architecture level.

2.1 Communication at mm-Wave Frequencies

During the past decade, commercial interest in communication on mm-wave frequencies has steadily grown. Expanding to higher frequencies will alleviate the existing congestion in the spectrum below 6 GHz, and at the same time it also promises wider continuous bandwidths and higher data rates. Some frequency ranges in the mm-wave spectrum have attracted special interest, and they will be discussed next. It important to note that since mm-wave communication still has shortcomings, most new standards at mm-wave frequencies are extensions of already existing standards, and their primary use is as a complement to the existing infrastructure.

2.1.1 60 GHz

Around 60 GHz, a worldwide free Industrial, Scientific and Medical (ISM) band offers bandwidths of several GHz. Its allocation depends somewhat on geographical location, as is shown in Fig. 2. One of the reasons to place an ISM band around 60 GHz is because of the increased atmospheric attenuation due to oxygen molecules, see Fig. 3. This means that networks operating on this frequency will by necessity be very local, in practice only within a single room. For a specific sort of networks, this is not a disadvantage, since small networks also mean increased privacy, less interference from other nearby users operating at the same frequency, and a larger potential for frequency reuse.

The first standardized wireless personal-area network (WPAN) in the ISM band to offer Gbit/s data rates is IEEE 802.15.3c, which targets applications such as kiosk downloading, conference ad-hoc systems and video streaming. It divides the band into 4 channels, and each is 2.16 GHz wide [3], as is shown in Fig. 2.

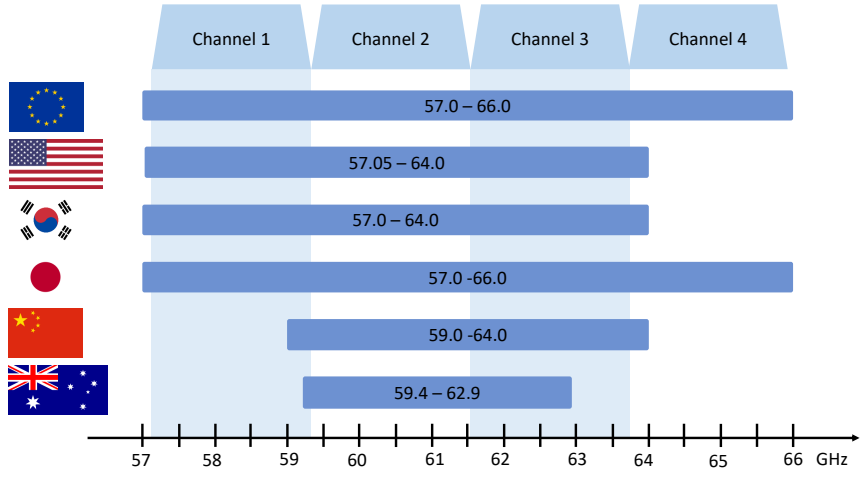


Figure 2: Frequency allocation of the ISM band around 60 GHz, comprised of four subchannels. Based on [3].

The WiFi standard 802.11ad, also known by its previous trade name WiGig, is also implemented in the ISM band. It keeps the proposed division into 4 channels. Although 802.11ad also supports more simple modulation schemes, the primary modulation scheme is orthogonal frequency division multiplexing (OFDM). Using this scheme together with 64-point quadrature amplitude modulation (64QAM), the highest data rates mentioned in the standard reaches 6.75675 Gbit/s, making it one of today's fastest wireless technologies. This puts very stringent requirements on the hardware, and usually also leads to a high power consumption. For this reason, other modes are also available in the standard, that better suits handheld, battery-powered devices. However, all 802.11ad-enabled devices are capable of at least 1 Gbit/s [5].

In the ISM band around 2.5 GHz, new standards have continuously developed over time. Some become very well used, like WiFi and Bluetooth, others become important in niche applications or simply fail to get traction. The same can be expected also for the 60 GHz band. Except for the WPAN and WiFi standards mentioned above, several other standards are already in different stages of development.

2.1.2 70, 80, and 90 GHz

Around 80 GHz, the mm-wave E-band also offers wide bandwidths, without the limitations of high atmospheric attenuation that affects the 60 GHz ISM band. It is, however, more dependent on weather conditions, and the signal will be more attenuated in rainy conditions. The E-band is a licensed band for

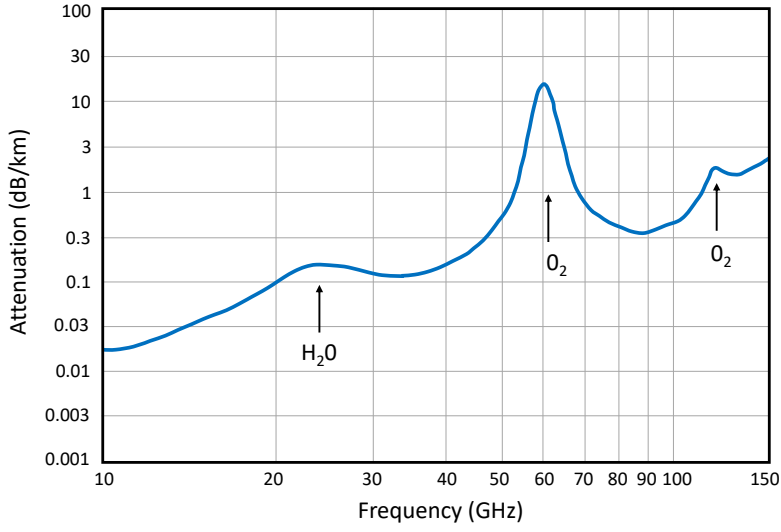


Figure 3: Total attenuation due to atmospheric gases at sea level. Based on [4].

communication, and it consists of three parts of spectrum: 71 to 76 GHz, 81 to 86 GHz, and 92 to 95 GHz. One of its primary planned uses is backhaul for cellular networks. Backhaul is, by definition, a wired or wireless point-to-point communication link. For cellular communication, it denotes the link between a base station and the main switch board. This kind of wireless backhaul in the E-band is especially well suited for the small cells that are anticipated in population-dense areas, where the distance between nodes is no more than about a kilometer [6].

2.1.3 30 GHz

Another of the high-interest frequency ranges is located around 30 GHz. Here, the cellphone industry see a way forward for cellular communication. From the first tentative steps [7], the spectrum around 30 GHz is now becoming integrated into the 3GPP standards, under the name new radio (NR). The planned allocation of spectrum in different parts of the world is shown in Fig. 4, along with the first two named bands. The standard explicitly states that many more bands will be defined within the frequency range in the future. In each band, OFDM will be the primary modulation, and bandwidths up to 400 MHz will be supported [8].

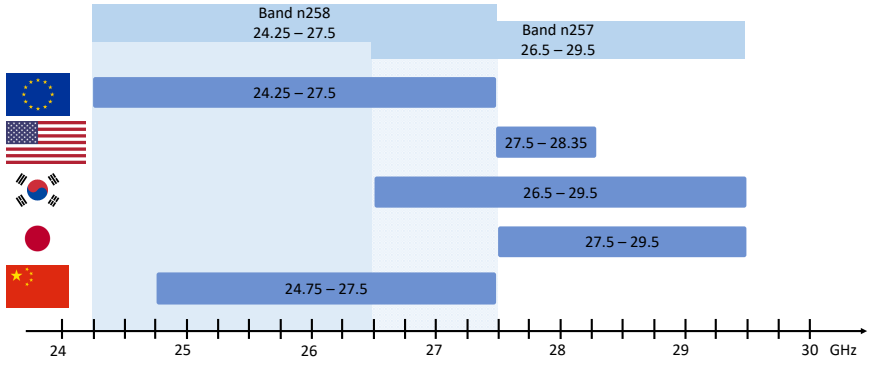


Figure 4: Planned spectrum allocation and band definitions for 5G NR. Based on [8].

2.2 Transmitter Architectures

The basic function of an analog transmitter is summarized in Fig. 5. First, the digital-to-analog converter (DAC) converts the baseband digital signal into an analog one. The analog signal will in practice have some levels of harmonics, noise, and unwanted tones. In each moment, the signal is characterized by its amplitude and phase. Next, mixer(s) upconvert the signal to the target frequency. An ideal mixer multiplies the two input signals in the time domain, and in the frequency domain is creates the sum and difference of the signals. The mixing operation is dependent on the presence of a locally generated frequency signal of good quality. How to create a local oscillator (LO) signal is further discussed in chapter 4. Since the transmitter almost always share a chip with one or more receivers, and they also need an LO signal for their frequency translation, the LO is often also providing signals for the receiver. Finally, in the last step of the transmitter, some amplification of the up-converted signal is needed before it is sent to the antenna. The amplification can be variable or fixed, and it consists of a power amplifier (PA), which is sometimes preceded by a pre-power amplifier (PPA). Power amplifiers are presented in chapter 3. At lower frequencies, filters are usually needed between each stage of the transmitter. However, at mm-wave frequencies, the required filtering can be alleviated, as the individual circuit blocks are tuned to the intended frequency range, providing some filtering.

Generally, transmitter front-ends use either a homodyne or superheterodyne architecture. Both architectures were first described almost a hundred years ago, and both are still commonly used today.

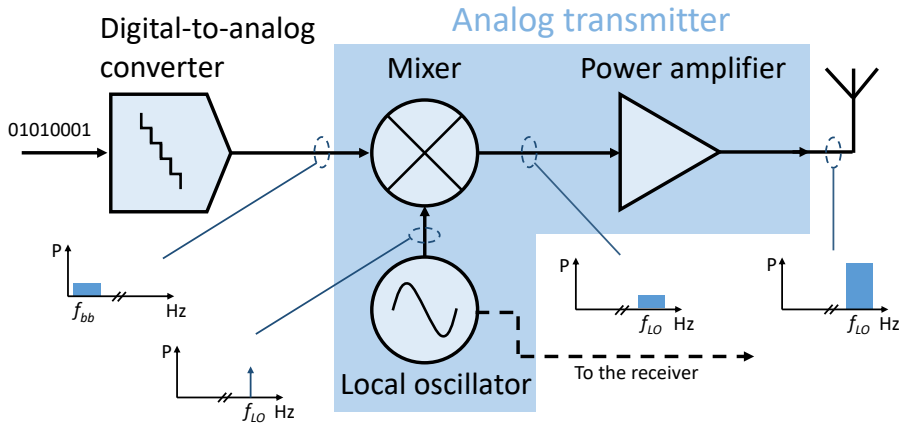


Figure 5: Basic functions of an analog transmitter.

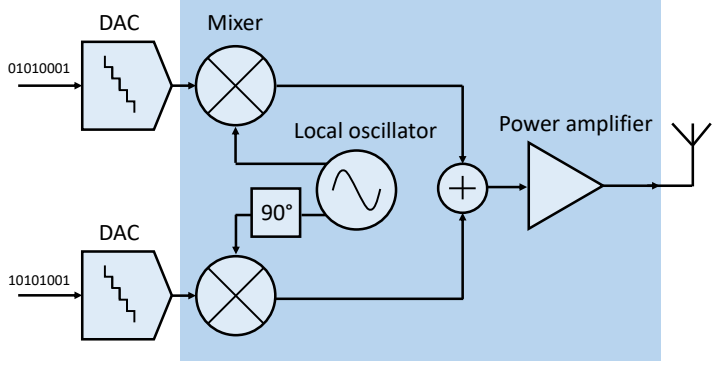


Figure 6: Homodyne transmitter.

2.2.1 The Homodyne Transmitter

The basic principle of a homodyne transmitter is shown in Fig. 6, where I/Q modulation is used. I/Q is short for in-phase and quadrature, and it refers to the practice of using two sinusoidal LO signals that have the same frequency, but are 90° out of phase. Conventionally, the I signal is a cosine waveform, and the Q signal is a sine waveform. This provides a powerful way to create any signal, because any signal can be generalized as

$$x(t) = A(t)cos[\omega_{carrier}t + \phi(t)] \tag{1}$$

$$= A(t)[cos(\omega_{carrier}t)cos(\phi(t)) - sin(\omega_{carrier}t)sin(\phi(t)], \tag{2}$$

where the information is carried by the phase and amplitude. Hence, with the baseband signals defined as

$$x_{baseband,I}(t) = A(t)cos(\phi(t)) \tag{3}$$

$$x_{baseband,Q}(t) = A(t)sin(\phi(t)), \tag{4}$$

it is clear that this architecture can be used to create any signal. For the overall performance of the transmitter, it is very important that the phase difference does not deviate from 90°. An advantage of the homodyne architecture is that it is straightforward, and that it does not require a multitude of subcircuits. However, it demands that all analog parts work at the output frequency, which makes the design more difficult at mm-wave frequencies. The matching between the subcircuits will require more attention, and the local oscillator design will become challenging, especially in terms of noise and balance in the quadrature generation. Also, the PA may disturb and cause pulling in the local oscillator, as it will be working on almost the same frequency.

Some examples of demonstrated homodyne transmitters in CMOS for mm-wave applications can be found in [9–11].

2.2.2 The Superheterodyne Transmitter

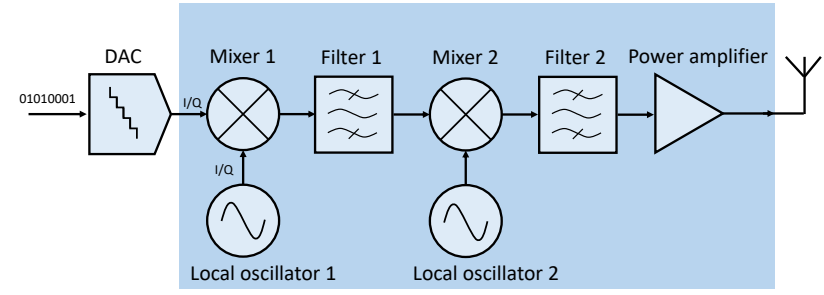
The basic principle of a superheterodyne transmitter is depicted in Fig. 7(a), illustrated as a two-step, single-sideband transmitter. The digital signal is first up-converted to an intermediate frequency (IF), and unwanted signals are removed by a filter. The signal is then upconverted again, using a second mixer and a second LO signal, to the intended carrier frequency.

In practice, the first LO and mixer are often responsible for the quadrature. Since they will operate at lower frequencies than the LO and mixer in the homodyne transmitter, the design will be less challenging. A disadvantage of this architecture is that it introduces additional circuits. However, at mm-wave frequencies, the filters will be less bulky, and the filters can fit on-chip if the IF is chosen carefully. Some recent examples of demonstrated superheterodyne transmitters in CMOS for mm-wave applications can be found in [12–16].

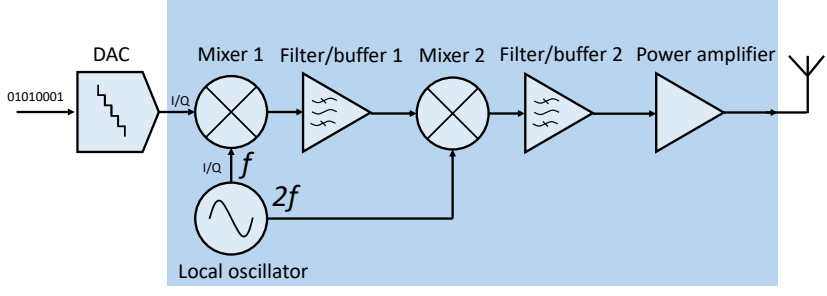
A special case of the superheterodyne transceiver is the sliding-IF architecture. Instead of keeping the IF constant, both LO frequencies move together. One advantage of this is that transmitter may not need multiple LOs. Each LO can be, for example, half of the transmitter carrier frequency, or they can be multiples of each other. Fig. 7(b) shows an architecture that has demonstrated promising results in mm-wave receivers [17].

2.2.3 Transmitter Architectures for Beamforming

Transmission on mm-wave frequencies is, as previously mentioned, difficult due to the high propagation loss. Every obstacle, such as walls or even raindrops,



(a)



(b)

Figure 7: (a) Superheterodyne transmitter. (b) Sliding IF transmitter.

will seem large to the small-wavelength signals. At around 60 GHz the high atmospheric attenuation due to oxygen molecules will add to the attenuation. However, the signal will not only face difficulties going from antenna to antenna. Using CMOS technology for cost and integration benefits will also mean choosing an inferior technology for high-frequency power applications. As technologies are down-scaled, the supply voltage is also scaled down, and the maximum voltage swing the transistors can handle without breaking is also lower. Additionally, the transistor gain decreases with increasing frequency. Hence, it can be difficult to even get a high power output signal to the antenna.

One way to address this problem is to maximize the signal from the antenna by making it increasingly directional, which ensures that all the power arrives at the correct target. Increasing the size of the antenna aperture will increase the directionality of the antenna [18], but also make it a lot more bulky and impractical. To steer the beam in one direction would also require moving the whole antenna. However, an advantage of high frequency communication is that the wavelengths are short and the antennas can thus be small. Instead of

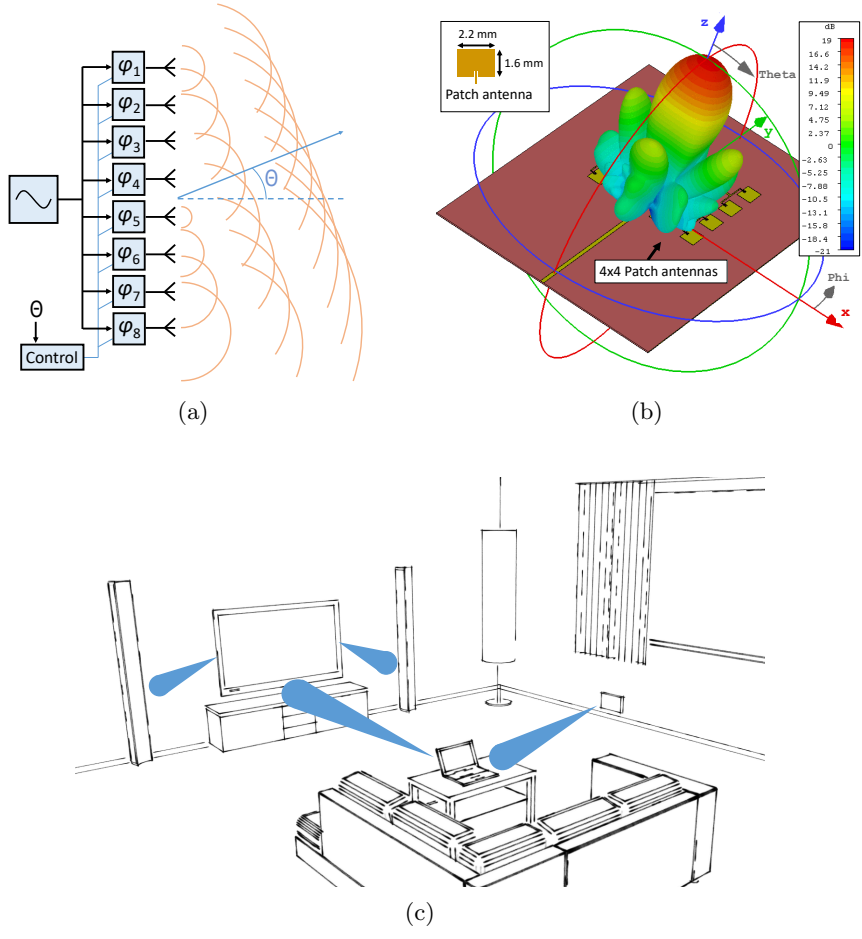
scaling up one antenna, it is possible to use many small, but carefully placed antennas, and make them work together. This configuration is called a phased array of antennas. Even if the signal from each antenna may be weak, many added signals will combine into a stronger signal. By controlling the phase of the signal that is sent from each sub-antenna in the array, they can be forced to create one, directional beam. This technique is called beamforming, and the basic principle is presented in Fig. 8(a). Changing the phase of each signal will quickly shift the beam to point somewhere else, without the need to physically move any antenna. This technique is called beam steering. Figure 8(b) and (c) show examples of this.

To summarize, beamforming and beam steering inherently means using many antennas in an array, and to carefully and continuously control the phase of the signal at each antenna. In practice, also the amplitude to each antenna is controlled, to suppress sidelobes of the signal. The phase shifting circuitry has to be able to produce a wide range of phases, with high resolution and linearity. The phase shift can, in theory, be implemented anywhere in the transmit chain, and each implementation has its advantages and disadvantages.

In one of the extreme cases, the phase shift is performed in the digital domain, and is thus simply called digital beamforming. This requires one DAC and a whole analog transmitter for each antenna. Depending on how challenging the LO signal distribution is, it may be possible to use one LO for all transmitters. In any case, the size of the whole circuit will increase, and the power consumption will drastically increase. However, this solution gives excellent precision, reconfigurability, and spectrum usage due to almost unlimited degrees of freedom.

In the other extreme case, the phase shifters are placed as close to the antenna as possible. The phase-shifting circuits are most often implemented as passive structures, such as delay lines. In this case, only one transmitter is needed for the whole phased array. However, the phase shifting will interfere with the matching between the PA and the antenna, and introduce losses. For these reasons, phase shifting circuitry can be placed before the PA instead. Examples of this can be found in for instance [19], which employs a switched-delay phase shifter, and in [20], which instead has an active vector modulator. The approach to place the phase shift before the power amplifier will create a need for as many PAs as there are antennas in the phased array. However, this suits CMOS PAs very well, since they are less expensive than specialized technologies that have better power-handling capabilities. In any case, when implementing the phase shift at mm-wave frequencies, obtaining enough precision and resolution is difficult. Placing the passive phase shifting circuits in the beginning of a superheterodyne transmitter chain, or simply right after the DAC, will make the control easier, but it will also mean that a larger portion of the transmitter have to be duplicated for each antenna. Another way of creating a phase shift, that does not require passive structures and that has demonstrated the ability

to create a wide range of phase shifts with high resolution, is to perform the phase shift inside the frequency generation circuitry [17].



(a) (b)

(c)

Figure 8: (a) The principle of beamforming, illustrated with a phased array of eight antennas. Each phase shift equals a small time delay of the signal. With the correct timing, the signals from the antennas will create common wavefronts, that move in a defined direction. (b) An example of beam steering. Simulated 60-GHz radiation pattern of a beam and its sidelobes, from a 4x4 phased array of patch antennas on a printed circuit board (PCB). Figure courtesy of Dr. A. Bondarik. (c) An example of how beam steering can be used as a high-speed data wireless interface.

Chapter 3

mm-Wave Power Amplifiers

The PA is the last block in the transmitter before the antenna, and it must be able to deliver the required power to transmit the information, and at the same time meet the requirements on linearity, bandwidth and dc power consumption. This chapter will give an introduction to design considerations for mm-wave power amplifiers (PAs).

So far, the market for hand-held communication devices have favored PAs in technologies like GaAs HBT, that have good power-handling capabilities and work well at high frequencies. CMOS technologies struggle with delivering gain and power at high frequencies, and the limited output voltage swing before the devices break lowers the attainable maximum output power. However, as mentioned in chapter 2.2.3, an individual CMOS transmitter will not necessarily have to deliver as much power if it is used together with other PAs and a phased array of antennas. In that setting, the lower price of CMOS PAs actually makes it preferable. Also, this has huge integration advantages, if the rest of the transmitter is also designed in CMOS technology.

3.1 PA Metrics

The following metrics are the most commonly used metrics to describe a PA.

The **gain** of the PA is the ratio between the average input power P_{in}, in W, and the average output power P_{out}, in W, delivered to the load, i.e. $A = P_{out}/P_{in}$. If all quantities are expressed in decibels, then $G[dB] = P_{out}[dBm]–P_{in}[dBm]$.

When P_{in} is increased, P_{out} will also increase, but only up until the **maximum output power** $P_{out,max}$ is reached. Already before that point, the gain will have decreased. The **1 dB gain compression point** (CP_{1dB}) expresses where the gain has dropped 1 dB compared to the expected value. It is usually related to the output power, in dBm.

Compared to the other parts of a transmitter, the PA consumes a relatively large amount of the total power. Hence, an important metric is the **power consumption** (P_{dc}), and also how efficiently the power is used. The **drain**

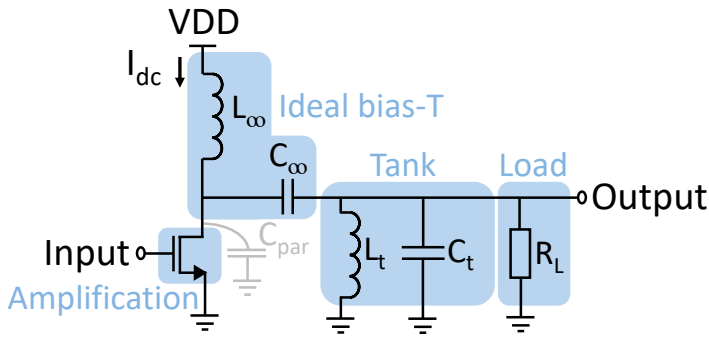


Figure 9: Principle of an ideal tuned PA.

efficiency is defined as $\eta = P_{out}/P_{dc}$. However, since it does not include the input signal power, another metric called the **power-added efficiency** (PAE) is often used instead. It is defined as $PAE = (P_{out} - P_{in})/P_{dc}$.

Since mm-wave PAs are tuned circuits their wideband operation, i.e. their **tuning range**, is also considered.

3.2 PA Fundamentals

An idealized representation of a mm-wave PA is shown in Fig. 9. In this example, the amplification is provided by a transistor in a common-source configuration. The transistor is biased through an ideal bias-T, with an infinite inductance towards the voltage supply VDD that only allows dc to pass through, and an infinite capacitance towards the load. Emphasizing the tuned nature of the PA, the load consists of the explicit load resistance R_L, but also a capacitance and an inductance that in this case forms a parallel resonant tank. The parasitic capacitances of the transistor, C_{par}, will be included in C_t, and likewise, R_L will include the resistive loss in the tank. The resonance frequency of the output circuitry is $f_{res} = 1/(2\pi L_t C_t)$.

3.2.1 Output Matching

As an example, if the aim is to deliver 20 dBm of output power to a 50 Ω load, which is a typical antenna impedance, it will lead to a peak output voltage that is over 3 V. Since this will risk breaking the transistor, an impedance matching network will be placed between the PA and the antenna, to make R_L look smaller when seen from the PA. An example of this is shown in Fig. 10(a) and (b). When transforming R_L in this way, the high output voltage becomes a high output current instead, but the delivered power stays the same. Consequently, the PA transistor must be able to handle large currents to deliver the necessary

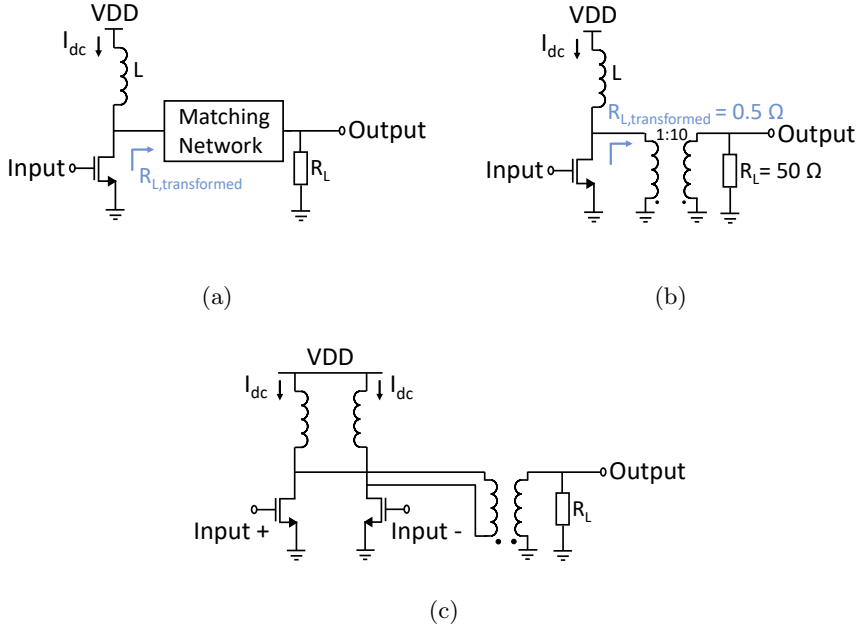


Figure 10: (a) PA with output matching network. (b) PA with a transformer. (c) Differential PA with a balun.

output power. To be capable of that, the transistor size has to be large, and that in turn leads to a high input capacitance. To prevent the high input capacitance from excessively loading the previous stage, i.e. the mixer, PAs are often built with cascaded stages with increasingly large transistors in each stage.

Another reason for the importance of the output matching network is that it plays a role in terminating unwanted harmonics, but at the same time it must have a wide enough bandwidth for the signal. The matching network will be a part of the tank and set the resonance frequency of the PA. When designing a mm-wave amplifier, a design goal for the matching network is to provide the load impedance that maximizes the output power, called power matching or large signal matching. Off-chip matching networks and baluns for single-ended to differential conversion are usually feasible at lower frequencies where packaging capacitances are small. However, at mm-wave frequencies, baluns and inter-stage matching between cascaded PA stages are naturally designed on-chip. Figure 10(c) shows a differential PA with a balun on the output.

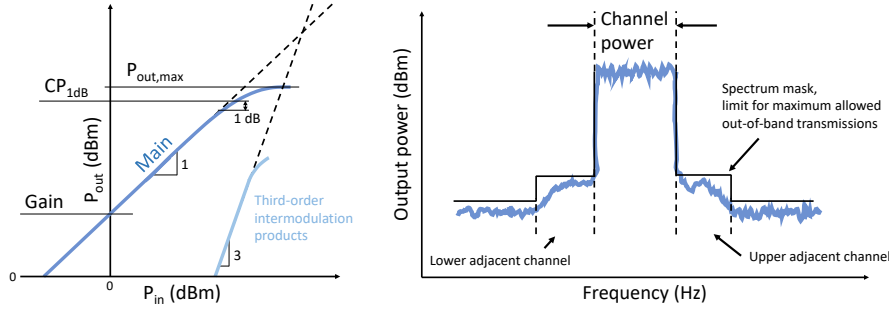


Figure 11: Effects of PA nonlinearities. (a) Relation between input power and output power, and the power in the unwanted third-order intermodulation product. (b) A modulated signal with adjacent channel leakage.

3.2.2 Differential PAs

One of the necessary initial design choices for a PA is whether to use a differential or a single-ended PA topology. Both have advantages and disadvantages. A single-ended PA can be more straight-forward to design. However, the mixer in a transmitter usually has a differential output signal, which benefits a differential PA, but a balun is still needed at the PA output for differential-to-single-ended signal conversion to interface the antenna. Physically, the balun may not consume so much more space, because it can double as a part of the output matching network, as shown in Fig. 10(c). A drawback is that passive components in the transmit chain result in increased signal losses. Other advantages of the differential approach are reduced even-order harmonics, increased dynamic range and less coupling to the LO path.

3.3 PA Classes

Two parameters in PAs are especially dependent on each other, namely the efficiency and the linearity.

The efficiency of a PA is very important, because the PA itself can easily consume more power than all other transmitter parts combined. As an example, if a PA with 50 % drain efficiency has to deliver 30 dBm of power (1 W), it will consume 2 W. The efficiency of a PA will also decrease with input power for almost all PA topologies, and it is rare for any PA to work at its maximum output power for longer periods. Usually, it is working with signals at least a few dBs below their maximum capacity, because modern modulation schemes have high peak-to-average power ratios (PAPR).

Linearity is of concern because it can lead to amplitude compression and

spectral regrowth, which in turn lead to high adjacent channel leakage, see Fig. 11(a) and (b), respectively. Any PA is inevitably nonlinear, since they operate with large signals, but the nonlinearity can be more or less severe, depending on design choices. More complex signal modulation schemes will lead to higher linearity requirements. To estimate the linearity, CP_{1dB} can be measured with a single-tone input, and the intermodulation products can be measured using two input tones. Other nonlinear effects are for instance AM/AM and AM/PM conversion, which is when input amplitude changes create gain and phase variations.

The trade-off between efficiency and linearity is made visible by categorizing PAs into different classes. The most established classes are A, AB, B, C, D, E, F, and inverse F. Generally, the more linear the class is, the less efficient it is. Roughly, the classes fall into two categories: PAs in which the transistor works as a voltage-controlled current source (A to C), and PAs in which the transistor works as a switch (D to inverse F). In the first category, an input sinusoidal signal will, more or less, look like an amplified version of itself at the output. In the second category, the output signal will have lost basically all information that was contained in the amplitude. A very powerful way to correct nonlinearities in PAs is to use digital predistortion (DPD) of the signal. This method uses knowledge obtained though PA calibration to preshape the signal in the digital domain, in a way that counteracts the nonlinearities of the PA. However, DPD may consume a significant amount of power and has its limits. Hence, it cannot always be relied upon to fix the shortcomings of the analog designs.

3.3.1 Class-A PAs

Class-A PAs are among the most straight-forward to design. A PA in class A has a very linear operation, but also the lowest maximum efficiency. However, sometimes the transmitter requires high linearity, which makes class A a good choice despite its low efficiency. Fig. 12 shows class A operation. To ensure that the output signal is always amplified as linearly as possible, the transistors in a class-A amplifier are always on. Since they conduct during the whole period of the sinusoidal input signal, their conduction angle is 360°. The highest efficiency that can possibly be attained is when the output signal is at its maximum voltage swing. However, the maximum drain efficiency will not be reached in real amplifiers, for a number of reasons. The large signals will change the transconductance of the transistors over the period of the signal, and forcing the amplifier to work with too high output voltage while also pushing high currents may cause long-term damage to the circuit. Additionally, the output matching network will add loss, making the maximum theoretical drain efficiency a less realistic goal.

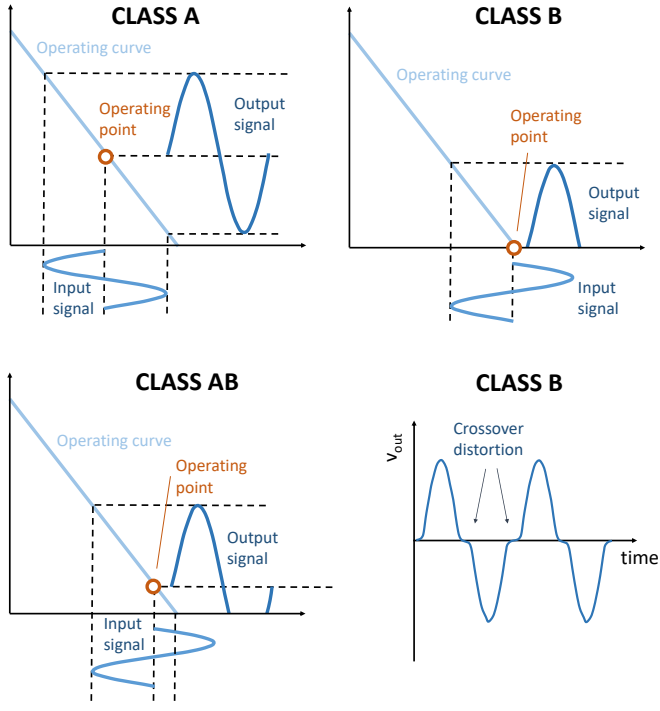


Figure 12: Drain current versus drain-source voltage in class-A, class-B, and class-AB operation. Crossover distortion in class B operation.

3.3.2 Class-AB PAs

The term class-AB is slightly ambiguous. While a class-A PA is linear and has a conduction angle of 360°, a class B PA has a conduction angle of 180°. Traditionally, it is consists of two transistors that work in parallel, and each one is only conducting half of the time. This is achieved by biasing the transistor so that it is not on during the full period. The output will still be quite linear, but suffer from distortion in the transition period, where the voltage is close enough to zero to prevent conduction in any of the transistors. Class B operation is shown in Fig. 12, along with class AB operation. Class AB is just a way of expressing that the PA has a conduction angle between 180° and 360°. It has been demonstrated that advanced CMOS processes are now fast enough to allow mm-wave class AB CMOS PAs that can provide enough linearity for the complex modulations used in the 60 GHz band [16, 21].

3.4 Techniques for mm-Wave PA Efficiency Enhancement

Since the design of the class-A PA presented in this thesis, techniques for enhancing the efficiency in mm-wave PAs have demonstrated increasing maturity. Some examples are given below.

Pushing into deep class AB operation is one way of increasing the efficiency, which have demonstrated good overall performance also at mm-wave frequencies. Except for the negative impact on linearity, it may also cause the power gain to drop. However, an attractive way of increasing the gain and stability of a PA is to use capacitive cross-coupling neutralization, which counteracts the gate-drain capacitance [22]. Figure 13 shows capacitive cross-coupling neutralization in a differential PA. Examples of mm-wave PAs in class AB can be found in [16, 21, 23–25].

Another example is outphasing architectures, where the signal is split into two parts before the PA: one contains the phase information of the signal, and the other one contains the amplitude information. The signals are then amplified separately using nonlinear, but efficient switching PAs. Finally, the signals are combined before the antenna. This architecture has attracted a lot of interest [26–28], and challenging design aspect is the implementation of the final combiners, which may introduce loss and distortion.

Progress in efficiency enhancement has also been made by using dual-mode PAs, which can switch between high-power and low-power mode depending on the momentary transmitter need [23, 29–31]. Some also include frequency reconfigurability [32]. They suffer from the same kind of difficulties as the outphasing designs, with challenging output power combiner design and layout floor planning, but demonstrate state-of-the-art performance.

Even Doherty PAs, a topology that has proven invaluable at lower frequencies to battle low efficiencies at power back-off, have been successfully demonstrated in CMOS at mm-wave frequencies, for instance in [33–36]. However, Doherty PAs are difficult to adapt to wideband operation.

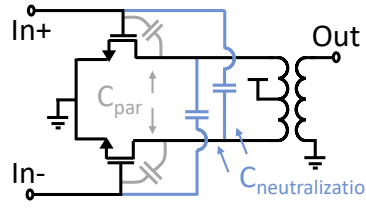


Figure 13: Example of cross-coupling neutralization in a differential PA. The optimal neutralization capacitance matches the parasitic gate-drain capacitance of the transistors.

3.5 Techniques for High Output Power

To obtain high output power from CMOS PAs, one of two paths is typically chosen [37]. The first is to use a high supply voltage and stacked transistors, which is possible without exceeding breakdown voltages if a silicon-on-insulator (SOI) CMOS technology is used [38, 39]. The second is to use passive power combination networks to add the power from several individual PAs. Although the power combination networks are inevitably lossy and degrade the efficiency, they are capable of achieving high maximum output powers [40–42]. An example of a parallel-series combiner is shown in Fig. 14.

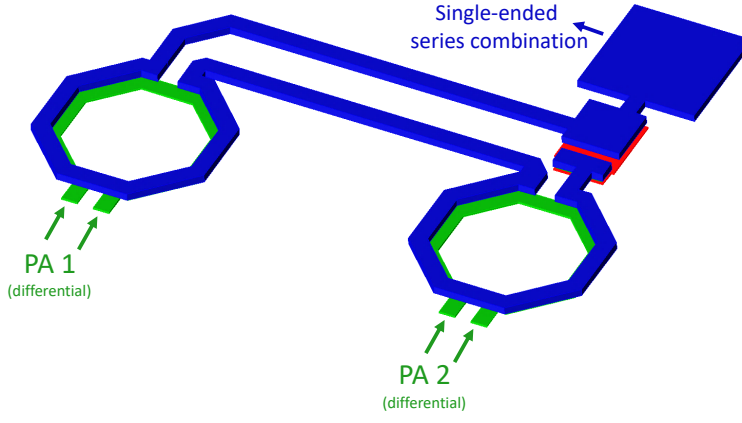


Figure 14: Example of a series power combiner for CMOS PAs.

Chapter 4

mm-Wave Frequency Generation

An integral part of any transceiver is the local oscillator. In a homodyne transceiver design, it provides the carrier frequency signal, onto which the data to be transmitted is modulated. In a superheterodyne transceiver, one local oscillator signal is required for each mixer. In each case, the LO needs to be able to produce a wide range of frequencies with enough output power, and add as little noise as possible to the signal to be transmitted.

This chapter will first discuss voltage-controlled oscillators (VCOs), and then phase-locked loops (PLLs) will be introduced. For both, some common metrics, design challenges, and solutions at mm-wave frequencies will be presented.

4.1 Voltage Controlled Oscillators

An oscillator can generally be described as a highly non-linear circuit that converts dc power into an output ac waveform. The frequency of its output signal is set using a control signal, which is most commonly a voltage. This chapter briefly covers the VCO fundamentals and a closer look at the cross-coupled VCO topology, along with some design considerations and examples.

4.1.1 VCO Metrics

When designing a VCO for a transceiver system, the most common design considerations concern the following properties of the VCO.

The **Frequency range** (Hz) of the VCO declares what frequencies the VCO can synthesize. Unless stated otherwise, it is inferred that all frequencies within the range are possible to create. In the middle of the frequency range is the **center frequency** (Hz), which should coincide with the center frequency of the targeted frequency band. The VCO **tuning range** (Hz), is expressed in GHz as f_{max}–f_{min}, or in percent as $100 \cdot 2 \cdot (f_{max} - f_{min})/(f_{max} + f_{min})$. Designing the tuning range so that the VCO covers a wider frequency span than the intended frequency band is needed to account for variations due to process and operation temperature. In practice, some connections between the

two exist. For instance, achieving a higher tuning range is more difficult at a higher center frequency because parasitic capacitances will limit the range of the variable capacitance. Connected to the frequency range is also the VCO gain, defined as output frequency change per control voltage change (Hz/V). A high gain makes it possible to cover a wide tuning range, but may also be problematic if the VCO gets too sensitive to small variations, i.e. noise, on the control voltage. The ideal frequency vs control voltage function within the frequency range is a straight line with a constant gain, but in practice the gain often varies. For instance, if an NMOS varactor is used for the frequency tuning, the result will be an S-shaped curve with less gain close to the minimum and maximum input control voltage.

Depending on the intended use of the VCO, some **output requirements on waveform, power, voltage swing and drive capability** must be met. The VCO will drive mainly capacitive loads, such as mixers, dividers or buffer amplifiers. Generally, the loss in a passive mixer will be less, the higher the input voltage swing from the VCO is. In an ideal case, the VCO output would be a square wave that switches as abruptly as possible. In practice, the output will be more of sinusoidal shape because the higher harmonics will be filtered out by the relatively narrow-band VCO.

The **Phase noise** (PN) of the VCO profoundly affects the performance of the whole transceiver circuit. The phase noise metric describes how much the frequency of the VCO signal statistically deviates from the intended frequency. In practice, all VCOs will exhibit this kind of noise, and it has trade-offs with both the tuning range and the power consumption. The phase noise is measured in dBc/Hz at some offset from the VCO oscillation frequency, often expressed as $\mathscr{L}(\Delta f)$.

The **power consumption** (P_{dc}), in W, of a VCO is always important, especially if the VCO is to be a part of hand-held battery-powered devices. It is also an important parameter to consider, as both the phase noise and the tuning range can be directly improved by increasing the power consumption.

The VCO may also be more or less sensitive to unintended inputs from its surrounding environment. **Pushing** and **power supply rejection ratio** (PSRR) concerns the sensitivity to changes in the supply voltage, like a voltage drop or supply voltage noise. **Pulling** is when the VCO frequency is changing with the load impedance.

The VCO **figure-of-merit** (FOM) combines some of the most important metrics above into one number, to facilitate comparison between different VCO designs. To assign fair weights to the different parameters, the most used FOM is built upon the heuristic Leeson model of phase noise in oscillators [43], where known trade-offs in VCO design are established. This FOM has unit dBc/Hz and it is calculated as

$$FOM = \mathscr{L}(\Delta f) - 20log(f_{osc}/\Delta f) + 10log(P_{dc}/1mW), \tag{5}$$

where $\mathscr{L}(\Delta f)$ is the the phase noise in dBc/Hz, measured at distance Δf Hz from the carrier oscillation frequency f_{osc} in Hz, and P_{dc} is the power consumption in W. Obviously, a FOM will always be general as it does not take into account the specific requirements of individual applications.

4.1.2 VCO Fundamentals

The simplest model of a basic VCO is a linear feedback model, as shown in Fig. 15. Considering only the dependence of frequency in the amplification $A(\omega)$ and the feedback path $\beta(\omega)$, the relation between input and output voltage can be expressed as

$$V_{out} = \frac{A(\omega)}{(1 - (A(\omega) \cdot \beta(\omega)))} V_{in} \tag{6}$$

When some frequency ω_{res} makes the denominator of Eq. (6) equal to 0, the gain will also be infinite, and an oscillation will spontaneously start. An oscillation can also start at all frequencies within the 3-dB frequency bandwidth of the circuit, provided that it is initiated by the ever-present device noise. However, as the oscillation amplitude increases and eventually stabilizes at some amplitude, both the amplification and the feedback in the system also become dependent on the oscillation amplitude V_{osc}. The criteria for oscillation will then instead become $|\beta(\omega_{osc})A(0)| > 1$ and $|\beta(\omega_{osc})A(V_{osc})| = 1$ and $\angle(\beta(\omega_{osc})A(V_{osc})) = 360°$. In other words, the gain around the loop exceeds 1 at startup, and the oscillation is sustained when the phase around the loop is 360° and the gain around the loop is 1.

4.1.3 The Cross-Coupled Oscillator

A very commonly used architecture for CMOS VCOs, appreciated for its versatility and ease-of-use, is the cross-coupled design. One of its most basic forms is shown in Fig. 16, but countless variations of its basic structure exist. This

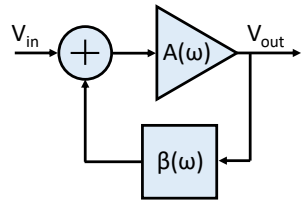


Figure 15: A linear feedback model of a VCO.

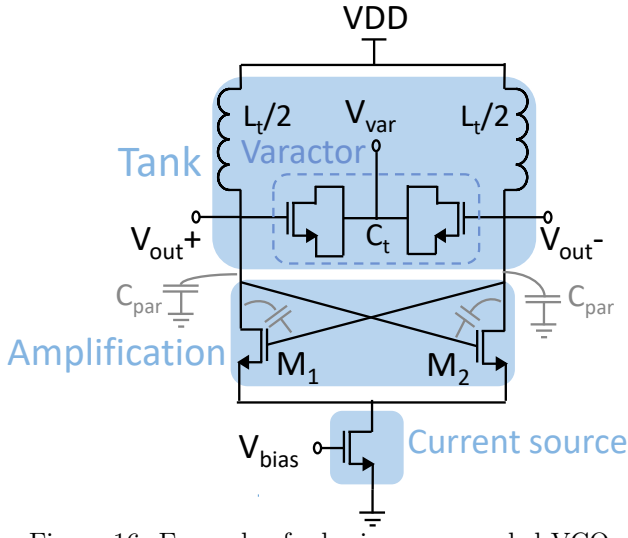


Figure 16: Example of a basic cross-coupled VCO.

VCO generates a differential output signal, taken from the drain terminals of the NMOS devices M_1 and M_2. The signal in the example figure will be sinusoidal, with some harmonic content. The signal will ideally swing around VDD, with a swing of VDD.

The self-oscillation frequency is set by the tank, which consists of an inductance L_t and a capacitance C_t. Both of these circuit elements will also contribute to a parallel loss resistance R_P. The loss resistance R_P will also include the output resistance of the transistor, r_o. C_t also includes the parasitic capacitances C_{par}. The self-oscillation frequency will be $f_{osc} = 1/(2\pi\sqrt{L_t C_t})$. To be able to tune the self oscillation frequency, a part of C_t is often made variable, and in the example in Fig. 16, the variable part is a varactor.

At the self-oscillation frequency, the value of the tank impedance will be just R_P. The voltage gain of each common-source stage is then $-g_m R_P$. Hence, the oscillation criterion becomes $g_m R_P > 1$. In practice, g_m is always designed with some margin to account for process and temperature variations. A variable current source at the source nodes of $M1$ and $M2$, as depicted in Fig. 16, provides an additional possibility to adjust g_m. In some applications, however, it is simply omitted to permit more voltage headroom in the circuit.

4.1.4 VCO design for Low Phase Noise

Phase noise is a very central concept in VCO design. It has been extensively researched for many decades [43–46], and new research into the phenomenon still results in new insights [47, 48].

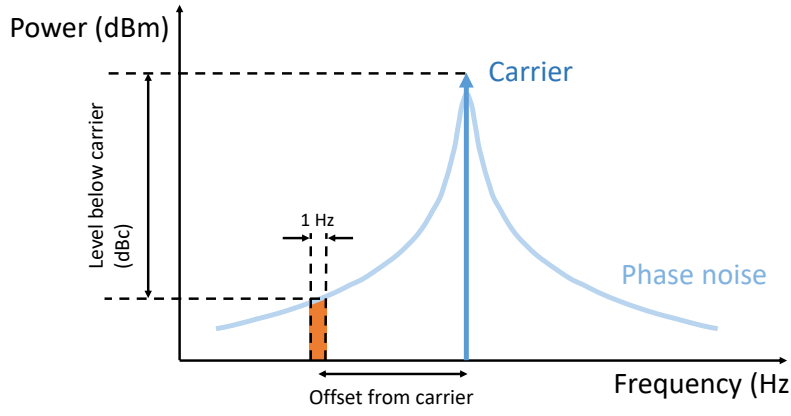


Figure 17: Phase noise.

Ideally, the output of the VCO is a single, stable frequency. If this was the case, the signal that is up- or downconverted with the VCO signal will be a perfect, frequency-translated version of itself, and even closely spaced channels can coexist without interference. However, in reality there will be random phase fluctuations. Intuitively, the signal more often stays close to its intended frequency, and more rarely occurs further away from it. Hence, the output of the VCO has a skirt-like spectrum centered around the oscillation frequency, see Fig. 17. In a transmitter, it will lead to spectral regrowth, and it can make symbols in complex modulation schemes uninterpretable. Since the LO is often also used for the receiver chain, it is worth noting that a receiver is even more vulnerable to LO phase noise.

A complete analytical model of phase noise in oscillators in every silicon technology is very difficult to develop, since the noise is a small perturbation of a large signal present at the transistors, and hence small-signal approximations can not be used. Even if the noise cannot be expressed in an analytical model, measurements and modern simulation tools can still be used to predict and understand phase noise. Already in 1966, Leeson formulated a simple model that describes phase noise in LC feedback oscillators [43]:

$$\mathscr{L}(\Delta f) = 10log\left[\frac{FkTB}{2P_{carrier}}\left(1+\left(\frac{f_{osc}}{2Q\Delta f}\right)^2\right)\left(1+\frac{f_{corner}}{\Delta f}\right)\right] \qquad (7)$$

where $\mathscr{L}(\Delta f)$ is the single-sided phase noise at distance Δf Hz from the carrier, F is the amplifier noise factor, k is the Boltzmann constant, T is the temperature in Kelvin, B is the bandwidth of integration for the noise (typically set to 1 Hz), f_{osc} is the frequency of oscillation in Hz, Q is the quality

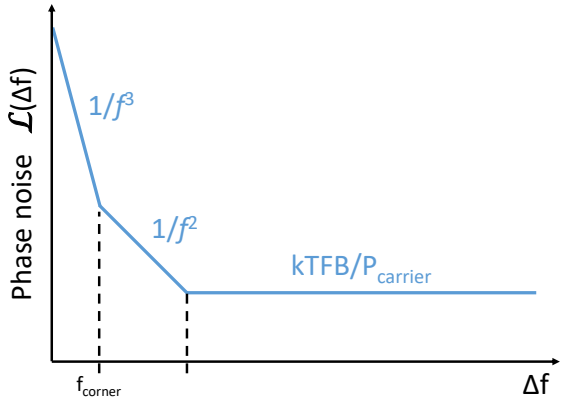
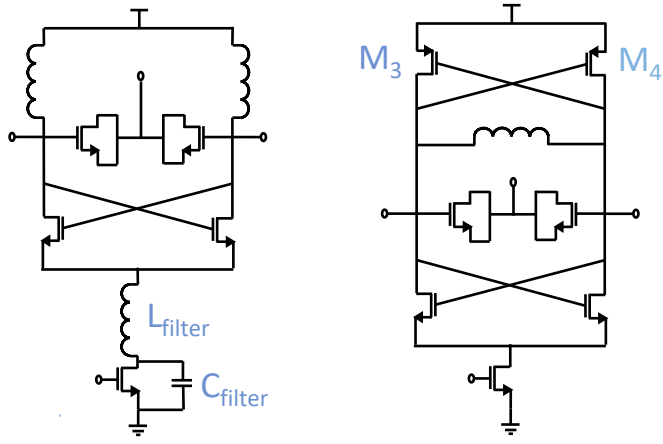


Figure 18: Phase noise regions.

factor of the tank, and f_{corner} is the flicker noise corner. To summarize, there are three distinguishable regions of the phase noise behaviour, see Fig. 18. Far from the carrier, the phase noise will be effectively white. Closer to the carrier, inside the bandwidth set by the Q of the tank, the phase noise will increase as $1/f^2$, i.e. 20 dB/decade. In the region closest to the carrier, the flicker noise will be dominant, and the phase noise will increase as $1/f^3$. Most often, the regions closest to the carrier are the ones of interest, and for VCOs, the noise at 1 or 10 MHz offset from the carrier is often quoted. The frequency that separates the $1/f^2$ and $1/f^3$ regions is called the flicker noise corner.

From Eq. 7, it can be concluded that the most influential contributor to phase noise is the Q value of the tank, and the lower the value, the higher the phase noise. Hence, trying to create a more wideband VCO using a tank with a lower Q-value results in high phase noise. Also, the VCO voltage swing should be maximized to reduce phase noise, but still stay within safe operation limits of the transistors. The noise from each individual transistor should also be kept as low as possible, as should the noise originating from outside sources. Among these are noise from buffers, on the supply voltage or on the control voltage input. The amplitude limitation mechanism of the VCO also plays a part, as the noise performance will be degraded when the transistors stay in triode for too long during each cycle. The phase noise performance will be optimized when the resonance tank is on the verge of being current limited. As identified in [49], the NMOS transistor in the tail current source will spend most of its time in triode, meaning that the current will not stay constant, and neither will the drain current of the cross-coupled transistors. Effectively, the VCO will sample the noise at twice the oscillation frequency when the differential voltage is zero, and actually half the noise from the current source lie around frequencies



(a) (b)

Figure 19: Basic VCO variations. (a) A low phase noise VCO with current source filtering. (b) A push-pull VCO for low power consumption.

close to the second harmonic. To address this, a very useful variation on the cross-coupled topology was presented in [50], see Fig. 19(a). It inserts a filter around the current source, tuned to twice the oscillation frequency. It also introduces a capacitor in parallel with the current source, to provide the noise from the current source transistor with a short path to ground. In practice, it trades area for phase noise, but this also makes it practical at mm-wave frequencies, because of the small geometries at shorter wavelengths.

4.1.5 VCO design for Low Power Consumption

As previously discussed, there is a trade-off between phase noise and power consumption. However, instead of sacrificing the phase noise performance, some other options exist. Several ultra-low power mm-wave VCOs based on the cross-coupled topology have recently been demonstrated [51–53]. One example that achieves low power consumption, by increasing the Q-value of the tank by increasing the size of the inductance and reducing the varactor size, is presented in [51]. As expected, the drawback is a very small tuning range. Many demonstrated ultra low-power VCO designs use lowered supply voltages [52,53],

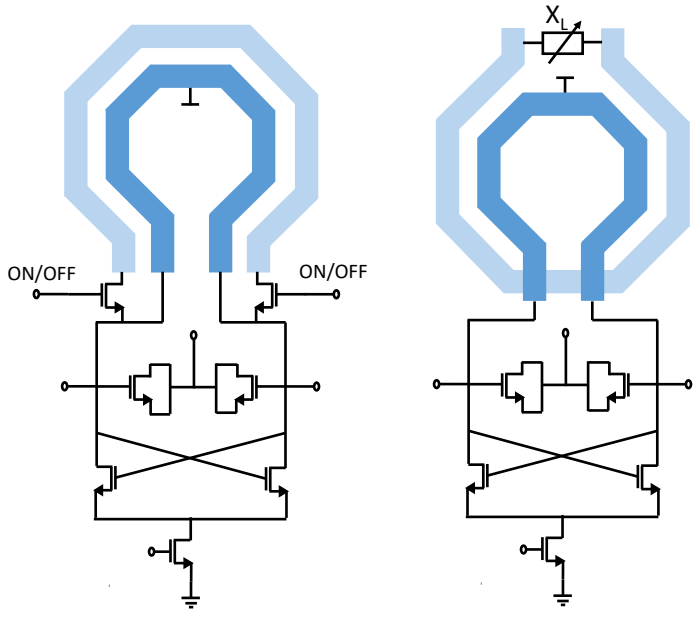
which can lead to excellent power consumption and low phase noise. However, the output voltage swing will be degraded, and a buffer may be required to follow the VCO, ultimately adding to the power consumption. A further drawback if this VCO design is that when put in a transmitter, a separate voltage domain has to be created. Another way to go is to extend the cross-coupled topology with another cross-coupled pair of PMOS transistors. An example of this topology, with PMOS transistor M3 and M4, is shown in Fig. 19(b). As demonstrated in Paper IV in this thesis, it can achieve ultra-low power consumption. One drawback is that the maximum output voltage swing will only be between 0 and VDD, but this can be preferable to ensure long-term stable operation of the VCO.

4.1.6 VCO design for Wide Tuning Range

If no extra measures are taken to expand the tuning range, a CMOS cross-coupled oscillator at 60 GHz with a reasonably sized varactor as the frequency-control mechanism typically has around 10 % tuning range. One reason for this is that varactors usually have low Q values at mm-wave frequencies, and that increasing the tuning range by increasing the varactor size would decrease the parallel resistance in the tank. To compensate for the lower signal swing, the cross-coupled pair transistors have to be larger, which in turn increases their parasitic capacitance, limiting their tuning range and lowering the maximum oscillation frequency.

Even if 10 % would be enough to precisely cover the ISM band in parts of the world, a wider tuning range is needed to ensure that the band is covered, also when variations in process, supply voltage and temperature cause the frequency range to shift. Hence, it is obvious that special measures must be taken to increase the tuning range, and during the past years this has attracted a lot of research interest [54–57].

Some main approaches can be distinguished. One is to circumvent the problem by designing a VCO that is working at lower frequency, and feed its signal to a multiplier, which creates the desired frequency [54]. It facilitates the VCO design, but the noise increases when the signal is upconverted. However, extracting and boosting a harmonic signal directly from a VCO as in [55], has demonstrated good phase noise performance as well. If the parasitic capacitances can be kept small and the Q-value high enough, it is possible to use a VCO directly at the intended mm-wave frequency and use a capacitance bank for the coarse tuning, as is commonly used in VCOs at lower frequencies. An example of this is [56], that employs a capacitor bank and a back-gate controlled varactor. Another solution is to create some coarse tuning by switching in different inductors in the tank, as demonstrated in for example [57]. The concept is presented in Fig. 20(a). The main challenges of these designs are the layout around the extra inductors, and the inevitable extra loss added by



(a) (b)

Figure 20: Basic VCO variations for increased tuning range. (a) A wide tuning range VCO with switched inductances. (b) A wide-band VCO with a transformer.

the switches. In [58] and [59] the effective impedance is tuned by changing the magnetic coupling between different coils, and yet another approach is to make the tank inductance part of a transformer, to be able to change the effective impedances in the tank by switching in different loads through the transformer [60]. An example of this concept is shown in Fig. 20(b).

Most of these methods for extending the tuning range would be compatible with the current-source filtering technique for improving the phase noise performance that is investigated at mm-wave frequencies in this thesis. This could lead to VCOs that are both wide-band and low-noise.

4.2 mm-Wave Phase-Locked Loops

Instead of simply using a VCO as the local oscillator in a tranceiver, it is common practice to instead employ a PLL for the frequency generation. A PLL is a circuit that contains a VCO to synthesize a frequency, but at the same time decreases the VCO phase noise at frequencies close to the carrier. The PLL is

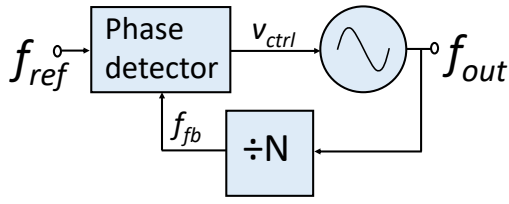


Figure 21: Basic PLL.

able to do this because the control voltage to the VCO will be controlled by a feedback loop that works in the phase domain, and forces the phase noise of the VCO to follow the phase noise of an input reference frequency. Since the reference frequency is generated at a lower frequency, it can be very clean from noise, especially if it is generated with a crystal oscillator. The basic concept of a PLL is shown in Fig. 21. The phase detector will detect any difference in phase between the input reference frequency, f_{ref}, and the divided version of the VCO frequency, f_{fb}. The output of the phase detector, V_{ctrl} will be the control voltage of the VCO.

4.2.1 PLL metrics

The following metrics are the most important in PLL design.

As for the VCOs, the **tuning range**, in GHz or percent, and the **center frequency** in GHz, are important parameters. Naturally, so is the **power consumption**, P_{dc}, in W. Also similar to the VCO, the phase noise, in dBc/Hz, is an important measure. In a PLL, the phase noise will often be presented as integrated over a limited frequency range and related to the output frequency. This is the **integrated average jitter**, called root-mean-square (RMS) jitter, which is measured in seconds. Depending on what PLL topology is used, different levels of unwanted spurs can appear in the output spectrum. Hence, the **output spur levels** in dBc must also be taken into account. Finally, the **lock time**, i.e. the time it takes for the PLL to lock to the desired output frequency in case of a frequency change, is an important parameter. For radars, another way to measure the speed of the PLL is often used, called the **slope**, in Hz/s.

4.2.2 PLL Architectures

The most popular type of PLL, for any application, was for many decades the analog PLL. Recently, subsampling PLLs [61,62], and also all-digital PLLs [63, 64] have made their way also into mm-wave designs and demonstrated excellent performance. However, this thesis will focus on analog PLLs, specifically the

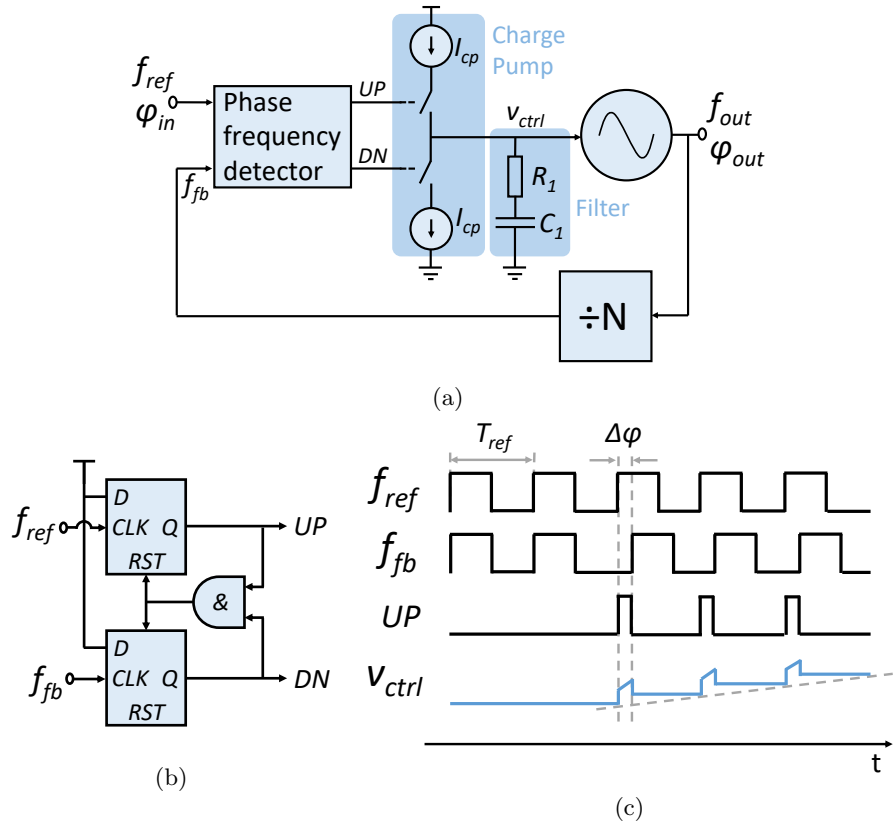


Figure 22: Type-II PLL. (a) Architecture. (b) PFD implementation with D-flipflops. (c) Waveforms in the phase-frequency detector and charge pump.

well-known charge-pump or type-II PLL, and ways to improve its architecture and parts.

Figure 22(a) shows a very common way to implement a PLL. An implementation of a phase-frequency detector (PFD) using resettable, edge-triggered D-flipflops is shown in Fig. 22(b). The PFD reacts to the phase difference on its inputs, se Fig. 22 (c). If the feedback signal arrives later than the reference signal, it will produce an output voltage on the UP terminal, lasting from the rising edge of the reference signal and until the rising edge of the f_{fb} signal. Ideally, it will not produce a DN signal, but in practical implementations there will be a short glitch. The UP signal will turn the upper switch on, and because the DN switch is off, current will flow into the filter capacitor, increasing the voltage in the node V_{ctrl}. This in turn changes the frequency of the VCO, and

if the loop is connected properly, makes the VCO output frequency closer to the correct one. Similarly, if the feedback signal leads the reference signal, the PFD will produce output voltage on the DN signal, and the lower switch will be on, and unload current from the filter capacitor and lower the value of V_{ctrl}.

The closed loop transfer function in the Laplace domain, for small signals, can be expressed as [65]

$$H(s) = \frac{\frac{I_{cp}K_{VCO}}{2\pi C_1}(R_1C_1s+1)}{s^2 + \frac{I_{cp}K_{VCO}}{2\pi N}R_1s + \frac{I_{cp}K_{VCO}}{2\pi C_1 N}} \tag{8}$$

where I_{cp} is the charge pump current, K_{VCO} is the gain of the VCO, R_1 and C_1 are the values of the filter components, and N is the division number in the feedback division chain. The charge-pump PLL has two poles in its transfer function, hence the name type-II PLL. Rewriting the denominator on the form $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is called the damping factor, and ω_n is called the natural frequency, gives

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_{cp}C_1K_{VCO}}{2\pi N}} \tag{9}$$

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1 N}} \tag{10}$$

and that the closed-loop poles are given by $\omega_{p1,2} = [-\zeta \pm \sqrt{\zeta^2 - 1}]\omega_n$. Having established that a PLL is a negative feedback system, and using these equations as a base, it is possible to look into the stability, noise performance, and tradeoffs in the design of a charge-pump PLL.

The PLL will reduce the noise by tying it to the input reference phase noise, but only close to the output frequency, within the bandwidth of the PLL. Here, the phase noise of the free-running VCO will be shaped by the transfer function. However, inside the bandwidth, the reference phase noise in a charge-pump PLL will be scaled up as N^2, and the noise from other circuits in the PLL, such as the charge pump, will be added. Hence, the bandwidth is often chosen to be around the intersection of the free-running VCO phase noise and the reference phase noise, see Fig. 23(a). However, other considerations also apply when deciding the bandwidth of the PLL. For instance, an often-used rule-of-thumb [66] is that the bandwidth should never be more than 1/10 of the reference frequency f_{ref} to ensure that the PLL acts as a continuous-time system. The bandwidth is also linked to the settling time of the PLL, i.e. how fast it will lock to a new frequency if a step is introduced in the loop. For small ratios between f_{ref} and the loop bandwidth, the settling time decreases with increasing bandwidth. However, for high ratios a phenomenon called cycle slips will make the setting time increase again. Figure 23(b) shows the settling behaviour of a PLL with visible cycle-slips. For f_{ref}-to-loop bandwidth ratios of

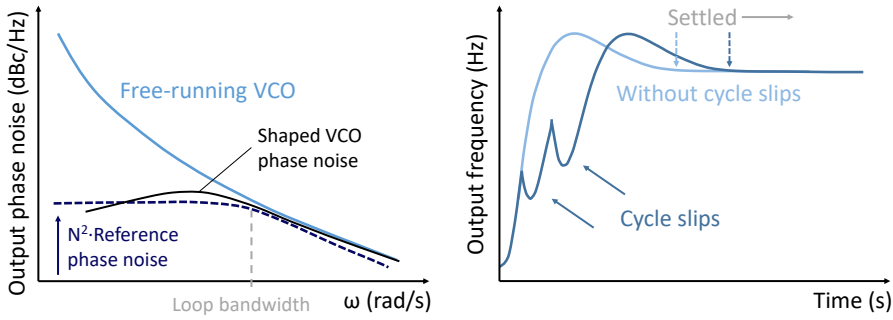


Figure 23: PLL loop dynamics. (a) Noise shaping in a charge-pump PLL. (b) Settling behaviour with and without cycle slips.

a hundred or more, the settling time will be excessively long [67]. Cycle slips are difficult to describe analytically, because they happen when the PFD is driven out of its range, and small-signal approximations are no longer valid. However, simulation tools are useful to evaluate the transient behaviour of a PLL design from a cycle-slip perspective. The bandwidth is also linked to the phase margin of the PLL, which needs to be optimized for stability and speed. The stability, i.e. the phase margin, must be designed with some extra headroom for process variations, but also because it is often degraded in practical charge-pump PLLs by an extra capacitor that is added to the filter. The reason for this addition is to remove ripple on V_{ctrl}, created by imperfections in the PFD, that result in very short and often mismatched pulses on V_{ctrl}, even when the loop has stabilized. The maximum reasonable size of the extra capacitance is often set to be 20 % of C_1, which maximizes the phase margin of the PLL, if ζ is chosen to be around 0.7. Additionally, introducing an extra capacitance also sets a maximum value for R_1 in the loop filter [65] .

From the brief explanation above, it is clear that there are many degrees of freedom when designing a charge-pump PLL. As in any design, the target application has to decide the system requirements. The environment will set what output frequencies the PLL must be able to synthesize, what input reference sources are available, if fractional-N operation is necessary, if the VCO needs to have a direct I/Q output, if the PLL must provide an extra modulation possibility, or phase shifting capabilities, and much more. The considerations here also tie into considerations for the entire tranceiver. Additionally, even if the architecture is optimized, each individual subcircuit of the PLL must also be carefully designed.

Some notable published CMOS implementations of charge-pump PLLs for the mm-wave frequency range from recent years can be found in [55, 68–72].

In [68], a fractional-N PLL for 5G applications demonstrates state-of-the-art noise performance, and in [69], a quadrature 60-GHz PLL with an inductorless divider chain and an in-phase injection-coupled VCO is presented. A successful strategy used in PLLs for the 60-GHz band presented in [55,70–72] is to design the PLL for operation on a lower frequency. To reach the 60-GHz band [71] uses a frequency tripler after the VCO, [70] presents a sub-harmonic quadrature injection-locked VCO, and in [55] the third harmonic of the VCO in a 20-GHz PLL is extracted and boosted. The PLL in [72] operates at RF frequencies, at a few GHz, and uses a set of different multipliers to cover many mm-wave bands.

4.2.3 Charge Pumps

The charge-pump concept is presented in Fig. 22(a). The main concern in charge-pump design is how to minimize pulse mismatch, i.e. when the current waveforms of the UP and DN pulses are not perfectly matched. It leads to ripple, noise, and spurs in the PLL output frequency spectrum. The problem sometimes originates from unmatched signal delays from the PFD, but there are many possible inherent causes within the charge-pump that may exacerbate the mismatch. Fig. 24 shows a straightforward implementation of a charge-pump. Many variations exist, and propose different ways to deal with imperfections that cause mismatch.

In the charge-pump in Fig. 24, the PMOS switch needs to have an inverted signal on its input to switch on, and as a first precaution against time delay, the inverting buffer in the UP path is matched by a transmission gate in the DN path. Other inherent causes of mismatch are affected by the transistor geometries. The individual transistors of the charge-pump are often made very wide, so that they can deliver current even when V_{ctrl} is close to ground or VDD. Large devices will have more parasitic capacitance and more space for storing charge in their inversion layers. This charge will be absorbed by the current sources when they are on, and dissipated when they turn off, causing unwanted nonlinear effects. Another nonlinear effect in charge-pumps is channel-length modulation, which is more dominant in short-channel devices. The channel-length modulation leads to mismatch because as V_{ctrl} changes, so does the drain source voltage of the current sources. This effect will always make one current source more effective at pushing current, while the other is less effective. A popular technique for reducing current mismatch due to channel-length modulation is presented in [73] Finally, random mismatches and transistor noise in the charge-pump also play a part in the PLL.

4.2.4 Dividers

The division in the PLL is done in steps, and often one or more of the steps are programmable to enable the PLL to synthesize different frequencies without

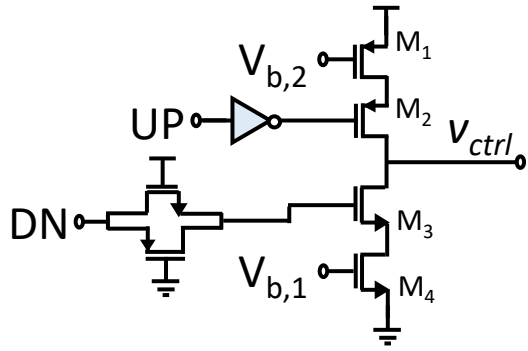


Figure 24: Charge pump transistor implementation.

having to change the input reference frequency. The most common choice for controlling these dividers is a sigma-delta modulator, which changes between division steps very fast and creates the desired frequency when averaged out. Closest to the PFD, the signal will have a lower frequency and more conventional digital divider designs can be used. At this position in the chain, the dividers can be programmable pulse-swallow dividers or dual-modulus dividers. Closer to the VCO, the frequencies that the dividers have to handle are higher. Faster logic is needed, such as current-mode logic (CML). A latch-based CML divide-by-two circuit is shown in Fig. 25 [74]. It is used in the divider chain of the PLL in paper V in this thesis, where it demonstrated good performance up to over 20 GHz.

When the divider speed needs to be even higher, as is the case of the first divider after a VCO that is operating at 60 GHz and above, a common choice is to instead turn to a tuned topology called injection-locked dividers (ILFDs). In their core they are similar to VCOs, and consequently often implemented as a cross-coupled VCO. To act as dividers, they are tuned to the divided output frequency, and the input signal to be divided is injected into the VCO in a way that makes it lock to it. Injection locking is of interest in many systems, and there are well-researched limits for when an injection lock can occur. The locking range for an ILFD is expressed as [75, 76]

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}} \tag{11}$$

where Q is the quality factor of the divider's LC tank, I_{inj} the magnitude of the injected current, and I_{osc} the magnitude of the free running oscillator current at f_0. It is clear that the more efficient the injection is, the wider the locking range becomes. A varactor can also be used in an ILFD to increase

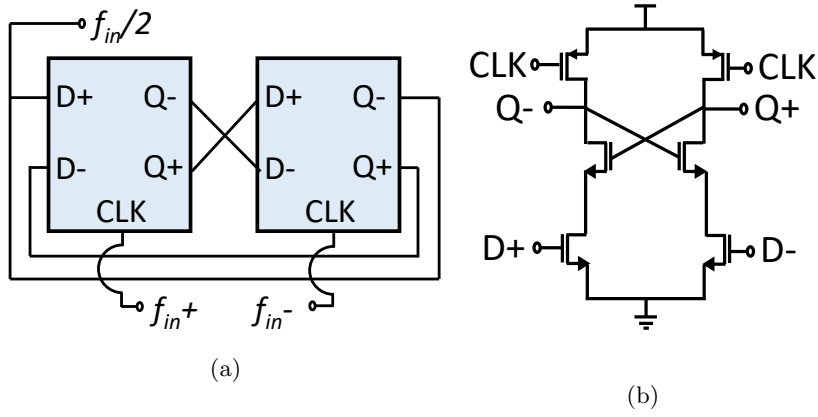
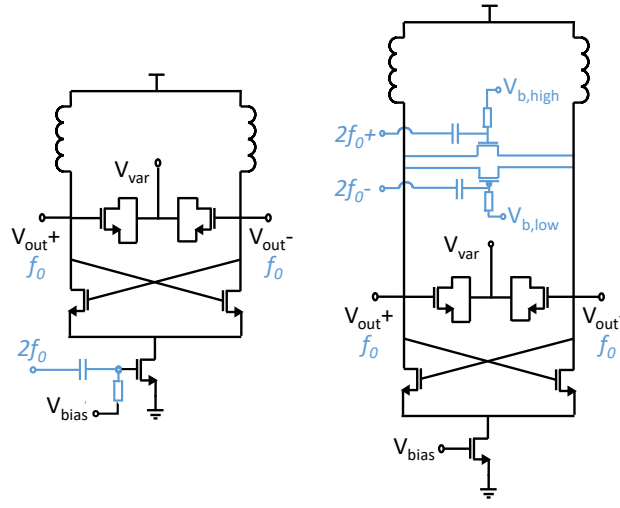


Figure 25: (a) High-speed latches in a tuned divide-by-two configuration. (b) Individual latch.

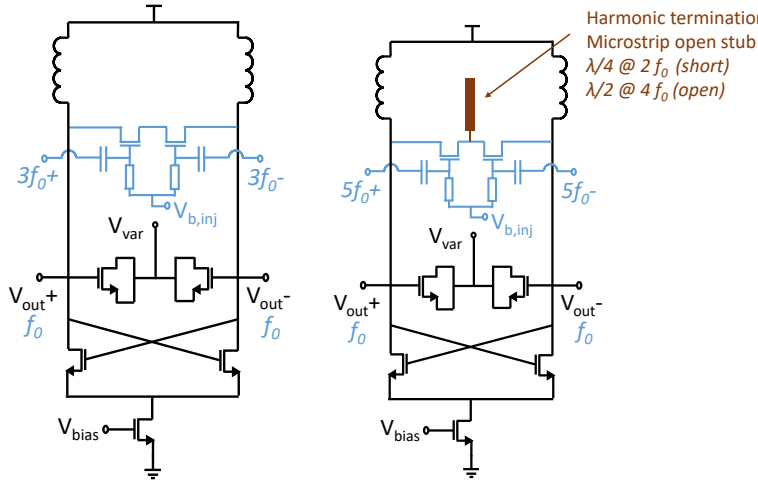
the locking range by tuning the circuit at the expense of complexity, loading of the tank, and larger chip area. Figure 26 shows two possible choices for injection of a signal at twice the output frequency. In the variation in Fig. 26(b), a differential signal is injected, which permits the use of the full output voltage swing of the preceding VCO. ILFD with higher division ratios have also been demonstrated. Figure 27(a) shows a divide-by-three ILFD. Here, the injected signal is at three times the self-oscillation frequency, and the transistors used for the injection will act as mixers and mix the input signal at $3f_0$ with the existing self-oscillation frequency f_0, creating even-order harmonics in the node between the injection transistors, where the second harmonic of the self-oscillation frequency naturally occurs [77]. A small change in this node, suppressing the second harmonic while favouring the fourth harmonic, as is shown in Fig. 27(b), makes the ILFD a divide-by-five circuit instead [78].

The output phase noise of an ILFD will generally be the same as the phase noise of the signal that it is locked on to, but it will increase at the edge of the locking range. Inside the locking range it will generally not introduce spurs, and because of its tuned nature, harmonics of the divided frequency will be suppressed.



(a) (b)

Figure 26: Injection-locked divide-by-two circuits. (a) Injection through the current source. (b) Direct differential injection.



(a) (b)

Figure 27: Injection-locked circuits. (a) Division-by-three. (b) Division-by-five.

Chapter 5

Paper Summary and Conclusions

This chapter presents summaries and conclusions of the results obtained in the included research papers. The author's contributions to each paper are also stated.

5.1 Summary

Paper I describes a two-stage, class-A PA for the 60 GHz ISM band. Each stage is differential and uses NMOS transistors in common-source configuration. To counteract the significant gate-drain capacitance at mm-wave frequencies, each stage is equipped with capacitive cross-coupling neutralization. It is implemented with NMOS transistors to ensure that it is matched to the transistors whose parasitic capacitances it should counteract. The input stage uses transistors that are dimensioned to cope with the large currents involved. The transistors of the subsequent output stage are 60 % larger. For measurement purposes, the PA has baluns at both the input and output, each carefully tuned to provide good input and output matching. Neither of the baluns are excluded from the calculations of the PAE. The inter-stage matching employs a 2:1 transformer, which is sufficiently wideband. The design was implemented in 65-nm CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured using on-chip probing and a network analyzer. The chip photo is shown in Fig. 28. The input and output matching is at their best around 67 GHz, where the gain also peaks. The maximum gain is 16.8 dB and the 3 dB bandwidth is 9 GHz, enough to cover the ISM band at 60 GHz. Operating from a 1.2 V supply voltage, its peak PAE is 18.5 %, well above other two-stage PAs presented before it. It has a maximum output power of 11.8 dBm, and a 1-dB output-related compression point at 8.4 dBm.
Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second and third authors.

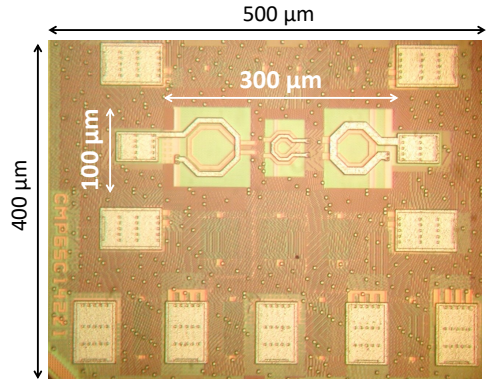


Figure 28: Chip microphotograph of the circuit in paper I.

Paper II describes a varactorless VCO, operating in the 60-GHz ISM band. At its core, it is a basic cross-coupled VCO. Instead of using a varactor for the frequency tuning, it changes the effective inductance seen by the cross-coupled NMOS transistors. This is achieved using an extra, in-phase branch, with its inductance placed right outside the coil of the primary inductance. The mutual inductance is dependent on the coupling factor and on the ratio between the currents in the two branches. The design was implemented in 65-nm CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photo is shown in Fig. 29. Changing the currents in branch 1 and 2, and consuming 6-30 mA from a 1.2 V supply, the frequency can be tuned from 62.2 to 65.1 GHz. The measured phase noise stays flat across the tuning range, and hence the best FOM of -182.4 dB/Hz is found at the highest frequency, when the current consumption is at its lowest. In all, the circuit demonstrates that a varactorless structure can lead to good phase noise performance. However, the architecture inherently narrows the tuning range.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second and third authors.

Paper III presents an empirical study of the efficiency at 60 GHz of a well-known technique of suppressing phase noise in VCOs. Two cross-coupled VCOs are manufactured: one baseline VCO, and one identical design except for the added noise source filtering at the current source. The filtering is implemented

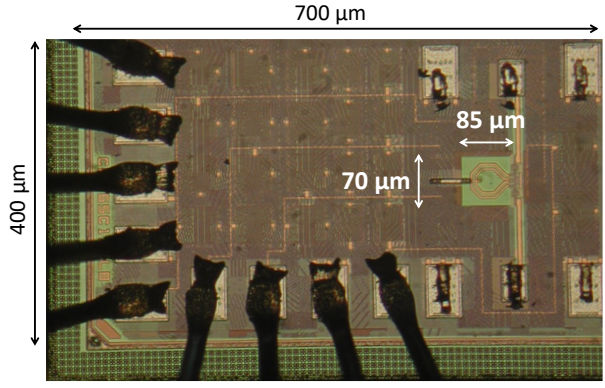


Figure 29: Chip microphotograph of the circuit in paper II.

with an inductance above the current source, tuned to twice the frequency of oscillation, to prevent the resistance of the cross-coupled pairs from loading the resonator in the switched stage. A capacitance is also inserted in parallel with the current source, providing a low-impedance path to ground for the noise generated in the current source. As this method of lowering the phase noise trades phase noise for area, it is especially interesting at 60 GHz, where inductors are small. However, the second harmonic will be at 120 GHz, closer to f_T and f_{max} of the technology, and it was not previously investigated if this would impact the efficiency of the method. Simulations show that the Q-value of the source inductance has a small impact on the efficiency, but the value of the inductance is more important. The VCOs were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photo is shown in Fig. 30. At 0.9 V supply, both VCOs consume 3.15 mW, and the filtered VCO achieves a FOM of -187.3 dBc/Hz, which was state-of-the-art performance at the time of publication. Both VCOs have a tuning range of about 11 %, and even with the extra inductance in the filtering VCO, their areas are competitive. The improvement originating from the filtering was measured to between 5 and 12 dB across the tuning range.

Contribution: I did the analysis, simulations, and layout. The second and fifth authors did the measurements. I did the manuscript writing, with assistance from the second and third authors. All was done under the supervision of the last two authors.

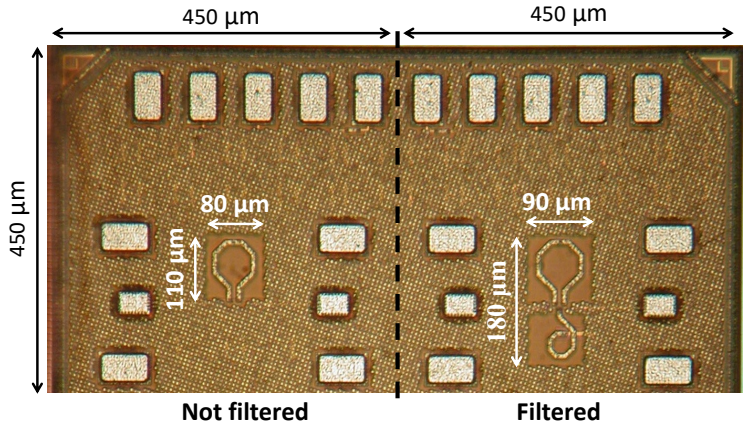


Figure 30: Chip microphotograph of the circuits in paper III.

Paper IV presents two ultra low-power VCOs for the 30 and 60 GHz bands. They both use a push-pull variation of the cross-coupled NMOS oscillator topology. The output voltage swing is restricted to the interval between 0 and VDD, which is lower than what can be achieved by the traditional cross-coupled architecture. Other potential drawbacks are that using a varactor for tuning may not be as efficient as in a basic cross-coupled topology, and that using two stacked transistors leaves less voltage headroom for the current source. The VCOs were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photos are shown in Fig. 31. Both VCOs have tuning ranges around 11 % in their intended bands. The measured power consumption at 1 V for the 30 GHz VCO is 1.06 mW, and 1.35 mW for the 60 GHz VCO. Hence, they both demonstrate ultra-low power consumption, that is on par with, or even lower, than previously published sub-threshold VCOs, but without the need for an additional voltage domain. They both have excellent FOMs, -188.4 dBc/Hz for the 30 GHz VCO, and -186.2 dBc/Hz for the 60 GHz VCO.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second, third and fourth authors.

Paper V presents a mm-wave analog phase-locked loop with a VCO operating around 55 GHz, with very low power consumption and an improved lock time. The intended application for the PLL is integration into a 5G transceiver,

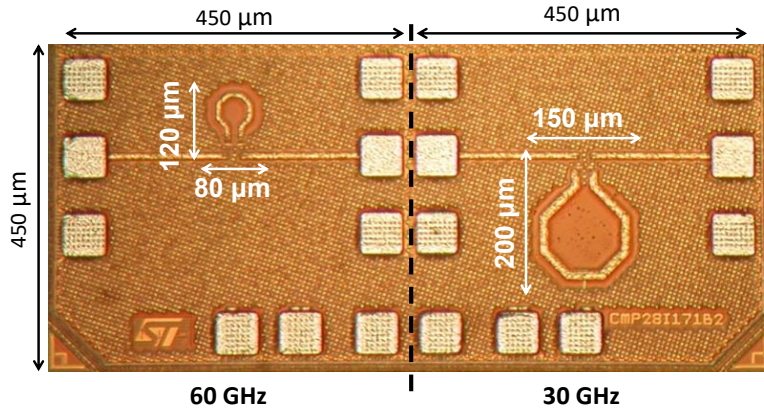
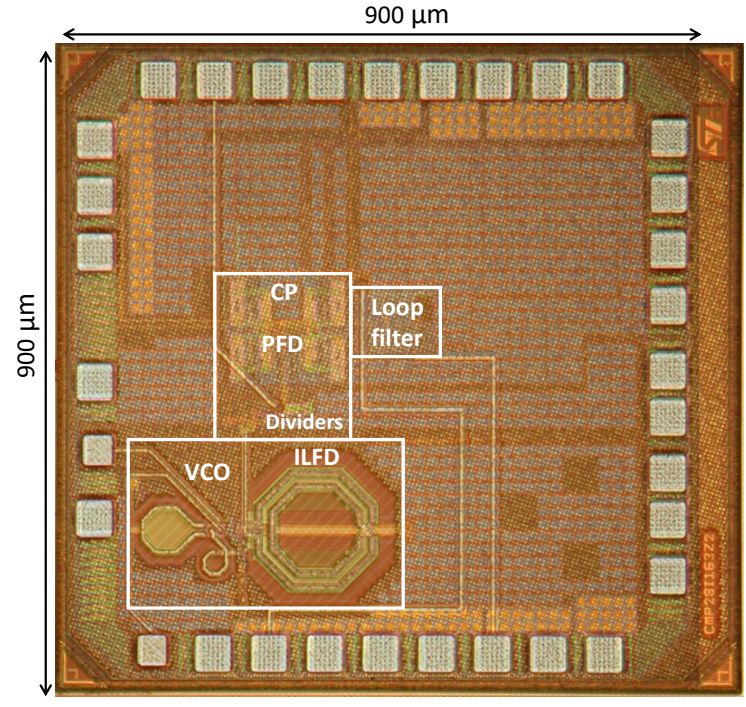
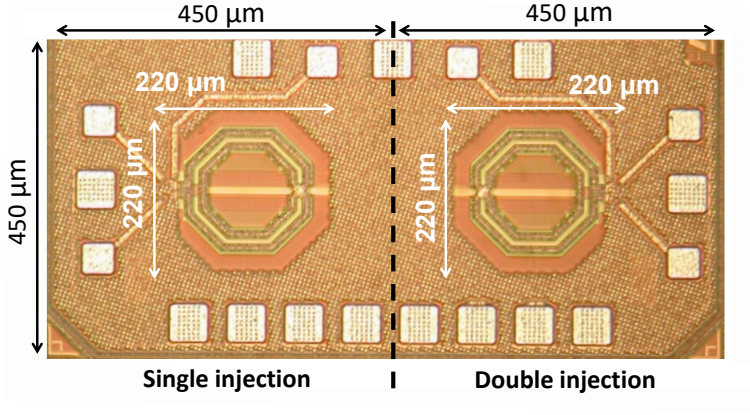


Figure 31: Chip microphotograph of the circuits in paper IV.

where another PLL for the RF bands already exists. This RF PLL can be used as the input for the mm-wave PLL and be responsible for channel selection and modulation, alleviating the demands of fractional-N division in the mm-wave PLL. At a first glance, the noise from the mm-wave PLL benefits from having a high input reference frequency of around 2.2 GHz, since the in-band noise adds as the division ratio squared. It also seems to imply that the PLL can use a higher bandwidth, and thus achieve a faster lock time. However, to keep the noise low, the bandwidth cannot be increased as much, and a low bandwidth coupled with a high reference frequency leads to cycle-slips and an excessively long lock-time. To address this problem, the proposed PLL employs a mode-shifting scheme, where it can operate in either a fast-locking or a low-noise mode. Both modes keep the same small-signal parameters, to ensure stability in both modes. When using the fast-locking mode to acquire a lock, the current in the charge pump is temporarily increased by a factor of 8, and the input reference frequency, as well as the divider chain in the PLL, are extended with divide-by-eight circuits. The PLL VCO uses the low-noise source-filtering design from Paper III. The VCO is followed by a divide-by-three injection-locked circuit. Traditionally, these are difficult to make wideband enough. However, the paper presents a novel double-injection topology that reuses the second harmonic present between the two injection transistors in parallel with the tank. This second harmonic signal is fed to the current source input, which creates a second injection path and increases the injection efficiency. Altogether, it makes the ILFD wideband enough to cover the whole VCO tuning range, while only consuming 0.5 mW. To verify the efficiency of the double-injection ILFD topology, two ILFDs are manufactured stand-alone, one with



(a)



(b)

Figure 32: Chip microphotographs of the circuits in paper V. (a) The PLL, overlayed with a semi-transparent layout. (b) The two versions of the ILFD.

and the other without the double-injection path, to facilitate a fair comparison. The PLL also includes a charge-pump with a novel current mismatch mitigation-technique based on negative feedback, and an improved operational amplifier that allows operation over a large common-mode range. Both versions of the ILFD, and the PLL, were implemented in 28-nm FD-SOI CMOS and the manufactured chips were mounted on PCBs with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with on-chip probes, a spectrum analyzer, and a phase noise analyzer. The chip photos are shown in Fig. 32. Measurements of the two stand-alone ILFDs show that the locking range of the double-injection topology is almost doubled compared to the single-injection topology at a fixed varactor voltage and at the same power consumption. Measurements of the PLL show that it has a record low total power consumption of 10 mW. Together with an excellent integrated jitter of 176 fs, it achieves a FOM of -245 dB. Additionally, it has a lock time of 3 μs, demonstrating that the architecture can overcome problems with excessive lock time associated with a high input reference frequency.

Contribution: Together with the first author, I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing. My primary responsibility was the mm-wave parts, but since no part of a PLL is independent of the others, we were both involved in all parts of the system. All was done under the supervision of the third and fourth authors.

Paper VI presents an injection-locked divide-by-two circuit for the 60 GHz band, stand-alone as well as integrated with the low-noise VCO from Paper III. The ILFD consists of a cross-coupled oscillator, which is injection locked by injecting a signal at around twice the frequency of self-oscillation. The efficency of the injection mechanism determines how wide the locking range is. To be able to use the full swing of a differential VCO, and create an efficent mechanism of injection, the signal is fed to the oscillator by direct differential injection. Simulations show that this creates a very wide locking range, which more than covers the tuning range of the VCO, even with process variations. One ILFD is integrated with the VCO to verify this. Both circuits were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with using on-chip probing, a spectrum analyzer, a phase noise analyzer, and a network analyzer. The chip photo is shown in Fig. 33. Measurements show that the widest locking range of 30 %, at -1.5 dBm of input power for the ILFD, is achieved at a power consumption of 4.3 mW from a 0.9 V supply. If the possibility to measure with even higher input power had been available, an even higher locking range could likely have been reported. Put together with the 60 GHz low-noise VCO from Paper III, the tuning range is set by the VCO to 10.2 %. The best measured phase noise from the VCO and ILFD combination is -111 dBc/Hz at 10 MHz offset from

the 28.5 GHz carrier.

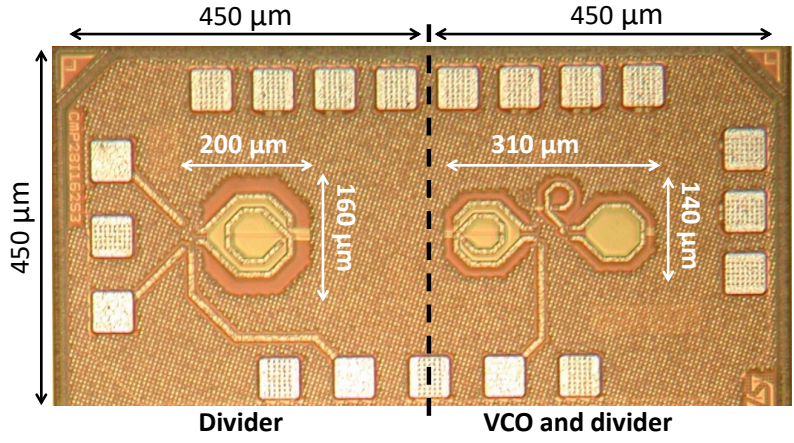


Figure 33: Chip microphotograph of the circuits in paper VI.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second, third and fourth authors.

Chapter 6

Discussion and Future Work

This dissertation presents several CMOS circuits that have been designed to be efficient parts of mm-wave transmitters. They have all been manufactured and verified by measurements.

A natural next step is to combine the different presented parts into complete, efficient transmitters. The presented PA, which demonstrates good performance when measured stand-alone, has already been integrated with mixers, a quadrature VCO and efficient injection-locked negative-resistance buffers into a sliding-LO transmitter for the 60 GHz band. It has been manufactured and my measurements show that the signal is properly upconverted and that the transmitter has wideband operation. However, the conversion gain is low. This was later confirmed in simulations to be mainly due to a mistuning of a passive structure, which reduces the input signal power to the PA. This structure could easily be re-tuned and manufactured again, as long as the silicon process is not discontinued. An improvement of this transmitter circuit should include a PLL with phase-shifting capability around the quadrature VCO, to make it viable for a 60 GHz beam-steering system.

The main drawback of the presented PLL is the limited tuning range. The most straightforward solution would be to increase it by increasing the size of the varactor, and thus accept the penalty of increased phase noise. However, the current-source filtering method used in the VCO to lower the phase noise could fit into many cross-coupled VCO topologies, also those a wider tuning range. At the same time, the PLL could also be extended to include phase-shifting possibilities by injecting current into the charge pump.

The PLL was designed to ultimately be a part of a whole homodyne transmitter for the 5G bands around 30 GHz. The signal from the 60 GHz VCO would be divided by the divide-by-two circuits presented in this thesis, to create a quadrature signal at 30 GHz. The dividers, which are low-power, have enough output power to directly drive a passive mixer for the upconversion. I have started this work and made initial simulations, but the transmitter still needs a power amplifier in the same technology node to be ready for manufacturing.

Finally, further integration with PCB antennas and on-chip high-speed DACs, in collaboration with other research groups, would be an interesting direction for future research.

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Paper I

Paper I

A two-stage mm-wave PA with 18.5% PAE in 65 nm CMOS

Therese Forsberg, Henrik Sjöland and Markus Törmänen, "A two-stage mm-wave PA with 18.5% PAE in 65 nm CMOS," in *Proc. of IEEE Asia-Pacific Microwave Conference (APMC)*, Nanjing, China, Dec 2015, pp. 1-3.

A Two-stage mm-Wave PA with 18.5% PAE in 65 nm CMOS

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***Abstract*— A two-stage mm-wave power amplifier (PA) is presented. Designed in a 65 nm CMOS process, the PA employs capacitive neutralization in each stage for increased differential isolation and gain. Baluns are used for single-ended input/output signal to balanced signal conversion, and the interstage matching consists of a 2:1 transformer. With a 1.2 V supply, at 67 GHz, measurements show a gain of 16.8 dB, a 1dB-compression point (P1dB) of 8.4 dBm and a saturated output power (Psat) of 11.8dBm, with a peak power added efficiency (PAE) of 18.5 %. The PA core occupies an area of 100 um x 300 um.**

***Index Terms*— PA, power amplifier, cross-coupling, neutralization, transformer-coupling, mm-wave, 60 GHz, CMOS, 65 nm, millimeter-wave.**

I. Introduction

High data-rate communication in the unlicensed band around 60 GHz has lately attracted a lot of interest. The wide bandwidth of 7 GHz combined with a high atmospheric attenuation makes it suitable for high throughput short-range standards such as IEEE 802.15.3c for wireless personal area networks and IEEE 802.11ad for wireless local area networks.

To introduce products using such standards to the market, it is critical that the component cost is kept low. A key factor in making transceiver designs more economically attainable is the use of large scale complementary metal oxide semiconductor (CMOS) technology for implementation. Continuous scaling of CMOS technologies has improved their capability to provide gain at higher frequencies and made it a viable choice also for the design of power amplifiers. However, supply voltage limitations in deep-submicron CMOS technologies reduce the achievable PA output power. To overcome this problem a promising approach is to use several PAs for the amplification, and employ output power combining of the amplified signals [1-3]. For each individual PA, a topology that provides sufficient gain, stability, linearity and efficiency is thus needed.

In this work, a two-stage PA implemented in 65 nm CMOS is presented. The objective has been to design a linear power amplifier that has a competitive efficiency and bandwidth. The PA is designed for 50 Ω single-ended input and output signals.

II. Theory and Design

The schematic of the design can be seen in Fig. 1. Class A operation is used to ensure high linearity of the PA. The core of each amplifying stage is a differential pair employing capacitive cross-coupling neutralization, which counteracts the significant effect of the gate-drain capacitance at higher frequencies, thus providing higher differential isolation and enabling higher gain without increasing the power consumption. The neutralization capacitances are implemented using off state transistor devices for improved matching. This alleviates process spread effects that might otherwise negatively impact the performance, and in severe cases even jeopardize stability. The interstage matching is realized with a transformer for a wide bandwidth operation. The transformer, seen in Fig 2, is designed to provide a 2:1 transformation ratio.

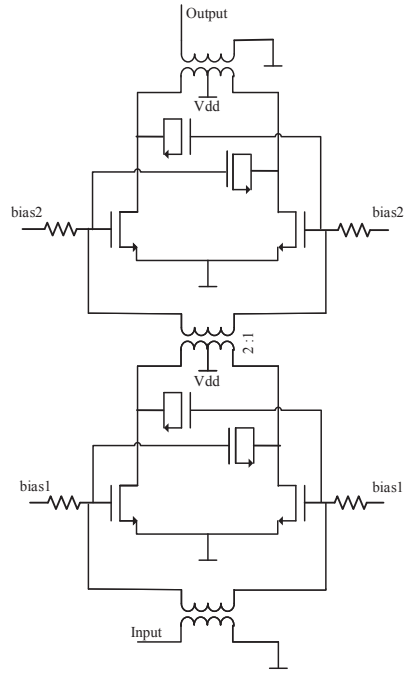

Fig. 1. Schematic of the two-stage PA with capacitive neutralization.

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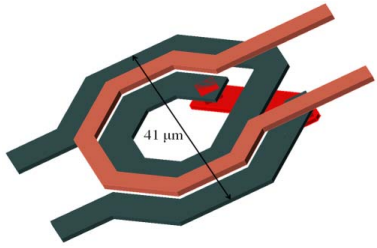

Fig. 2. The interstage matching transformer.

Both the transformer and the input and output baluns were simulated in ADS Momentum and their dimensions were tuned to make the entire system operate at the targeted 60 GHz frequency band. All three transformers are realized in the top metal layers. Simulations of the transformer show a coupling coefficient of 0.7 and a loss of 2 dB. The simulated loss in the input and output balun is 1.1 dB and 2.1 dB, respectively.

The bias is applied to the gates through 30 kΩ resistors, rather than through the transformer center tap, in order to avoid potential common mode instability. Simulations show unconditional stability at all frequencies.

The dimensions of the transistors in the differential pair are 60µm/65nm for the first stage, and 100µm/65nm for the output stage. The theoretical optimal size for the cross-coupling capacitances is when it equals the gate-drain capacitance of the amplifying devices [4]. Since the capacitance is realized with off state transistors, providing overlap capacitance at both drain and source, the widths of these devices are chosen approximately half the width of the corresponding amplifying device.

III. Measurement Results

The PA was implemented in the standard ST 65 nm processes with 8 metal layers. The die area of the PA, including the input and output matching, is 100 x 300 µm^2. Including pads the total chip size is 0.4 x 0.5 mm^2. The chip photo is shown in Fig. 3.

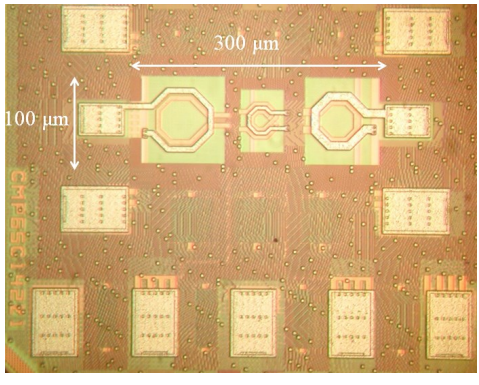

Fig. 3. Chip photo.

The chips were mounted on printed circuit boards, to which supply and bias signals were wire bonded. Infinity GSG microprobes from Cascade Microtech were used for the input and output signals. The S-parameters were measured using an Agilent E8361A network analyzer. To be able to measure the input-output power characteristics above the maximum output power of the network analyzer, an extra amplifier HXI HLNAV-383 was inserted before the device under test (DUT). The output power was recorded using a V8486A power sensor. The same sensor was also used to calibrate the input power to the DUT.

The S-parameters measurements are presented in Fig. 4 and Fig. 5. As can be clearly seen, both the input and output matching is good. The gain peaks at 16.8 dB around 67 GHz, and the 3 dB bandwidth is estimated to 9 GHz.

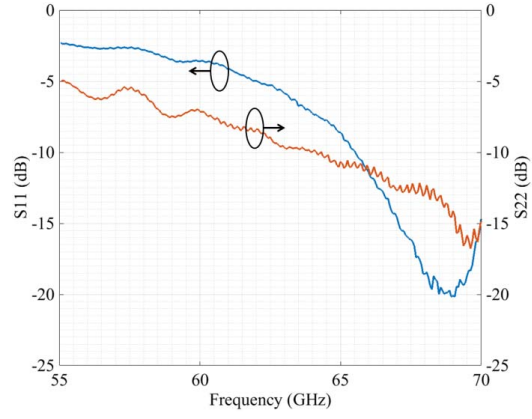

Fig. 4. Measured input and output matching.

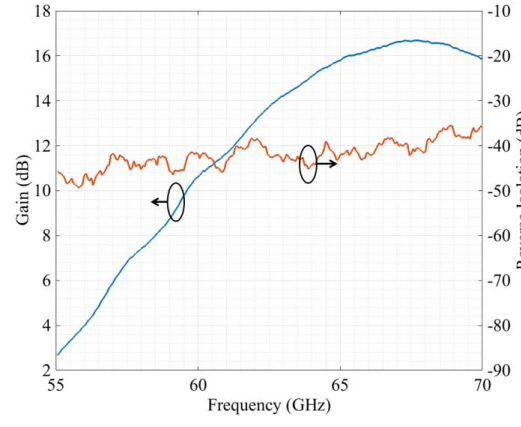

Fig. 5. Measured gain and reverse isolation.

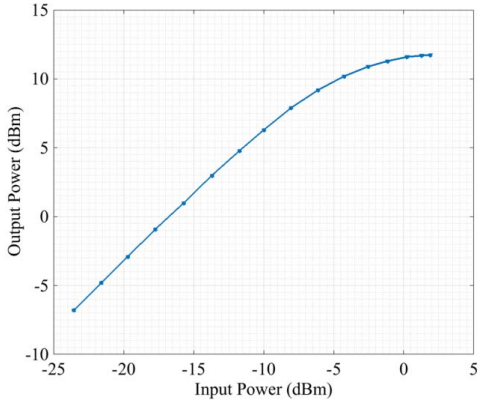

Fig. 6. Output power versus input power at 67 GHz.

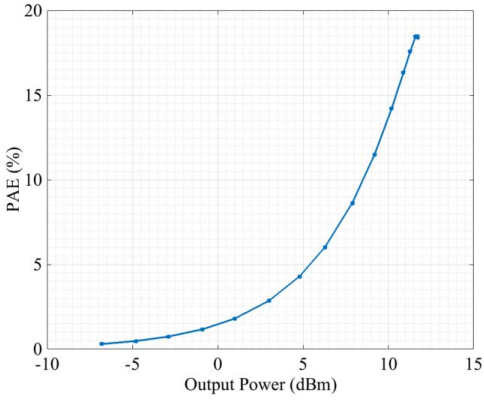

Fig. 7. Power added efficiency versus output power at 67 GHz.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED TWO- AND THREE-STAGE PAS.

Ref.	This work	[5]	[6]	[7]	[8]
CMOS Technology	65 nm	45 nm	28 nm	65 nm	65 nm
Supply Voltage	1.2	2	1	1.2	1
Frequency (GHz)	67	60	53	55[a]	60.5
Gain (dB)	16.8	20	13	12.1	10
P_{1dB} (dBm)	8.4	11.2	12	9.5	7.1
Psat (dBm)	11.8	14.5	13	12.2	11.5
Bandwidth, 3dB (GHz)	9	10[b]	27	[a]	8.5
PAE_{max} (%)	18.5	14.4	16	12.5	15.3
PAE_{1dB} (%)	9	[a]	[a]	7.7	[a]
Area (mm^2)	0.03	0.09	0.056	0.576	0.053

a. Not clearly expressed in the source article. b.1dB bandwidth.

In Fig. 6, the output power versus input power at 67 GHz is shown. The maximum output power is 11.8 dBm and the 1dB compression point is 8.4 dBm. Using a 1.2 V supply, the power amplifier has a peak power added efficiency (PAE) of 18.5%. The PAE as a function of output power is shown in Fig. 7. From this graph, it can also be seen that the PAE at the 1dB compression point is 9%.

The measured performance of the two-stage PA is compared with other similar published two- and three-stage CMOS PAs in Table I.

IV. CONCLUSION

A two-stage class A CMOS PA in 65 nm CMOS is presented. It has a competitive efficiency, also at the compression point. The bandwidth is enough to cover the unlicensed band at 60 GHz and the circuit is using a very small active chip area.

ACKNOWLEDGMENT

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Paper II

Paper II

A 65 nm CMOS varactorless mm-wave VCO

Therese Forsberg, Henrik Sjöland and Markus Törmänen, "A 65 nm CMOS varactorless mm-wave VCO," in *Proc. of 2014 International Symposium on Integrated Circuits (ISIC)*, Singapore, Singapore, Dec 2014, pp. 54–57.

A 65 nm CMOS varactorless mm-wave VCO

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***Abstract*— We present a cross-coupled 60 GHz differential LC voltage controlled oscillator (VCO) implemented in 65 nm CMOS technology. To eliminate the need for varactors, the frequency tuning is implemented using transformers in the resonator, where the effective inductance can be controlled by injecting current into the secondary windings. Measurements show an average current consumption of 15 mA from a 1.2 V supply, resulting in a minimum FOM of -182.4 dBc/Hz, and the frequency versus tuning current in the secondary is close to linear. The die area of the oscillator core, including the transformers, is 70 um x 85 um.**

***Index Terms*— VCO, mm-wave, 60 GHz, CMOS, 65 nm, millimeter-wave.**

I. Introduction

As the frequency spectrum at lower frequencies becomes more and more crowded, wireless communication will have to use higher frequencies for expansion. The unlicensed band that resides between 57 and 66 GHz has 7 GHz of bandwidth, slightly differently placed depending on country [1]. The standards IEEE 802.15.3c for wireless personal area networks (WPAN) and IEEE_802.11ad for wireless local area networks use these frequencies [2],[3], and complete millimeter wave transceivers for these standards and others have already been presented [4]-[6]. It is not unreasonable to believe that just like the unlicensed 2.4 GHz band, the millimeter wave band will also soon be filled with several competing or complementing standards that create a need for cheap and energy efficient transceivers. To implement such transceivers in cheap and energy-effective large scale complementary metal oxide semiconductor (CMOS) technology is an attractive choice [1].

A key component in any transceiver is the voltage controlled oscillator (VCO). When designing VCOs for the 60 GHz band the common choice involves a cross-coupled pair with an LC tank. The frequency is then tuned by changing the capacitance in the tank using varactors or switched capacitor banks in different structures [7], [8]. A typical example of this kind of LC VCO is shown in Fig. 1. For this circuit the oscillation frequency is given by Eq. 1 below.

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_{tot}}} \quad (1)$$

where C_{tot} includes both the varactor capacitance, the load capacitance, and the parasitic capacitance.

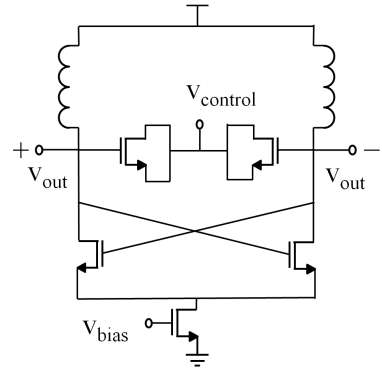

Fig. 1. Schematic of a typical cross-coupled VCO.

A high quality factor (Q) of the LC resonator is needed to achieve low phase noise and power consumption, but varactors have a low Q at millimeter wave frequencies [9], and besides that they are often associated with too much parasitic capacitance [7], [8]. Inductive tuning, implemented as a loaded transformer structure, is a way to get around this. Common solutions include switching on or off parts of the secondary coil. Low loss switches, however, are difficult to implement at millimeter wave frequencies. Usually the tank also includes a varactor [7], [10]-[13].

This paper proposes a method to tune the frequency without any varactor in the tank, or the need to switch inductances.

II. Theory and Design

The core of the varactorless mm-wave VCO is a basic cross-coupled design, as can be seen in Fig. 2. The capacitive part of the tank of is constituted by the inherent capacitance in the transistors together with the other parasitic capacitances throughout the circuit. The inductive part of the tank is the primary, inner coil of a transformer. The frequency of the oscillator is tuned solely by changing the effective inductance of the tank, which is changed by controlling the current in the second and third branch. These branches inject current in phase and antiphase, respectively, in the secondary, outer coil of the transformer.

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The tuning mechanism can be understood as follows. For two magnetically coupled inductors, the voltage v_1 of inductor 1 can be expressed as

$$v_1 = L_1 \frac{di_1}{dt} + L_m \frac{di_2}{dt} \quad (2)$$

where L_m is the mutual inductance. If i_2 is proportional to i_1, i.e. $i_2 = xi_1$, then the effective inductance of the first inductor can be expressed as $(L + xL_m)$, since

$$v_1 = L_1 \frac{di_1}{dt} + L_m x \frac{di_1}{dt} = (L + xL_m) \frac{di_1}{dt} \quad (3)$$

Assuming that $L_1 = L_2$, then the effective inductance can be re-written as $L(1+kx)$, since

$$L_m = k\sqrt{L_1 L_2} = k\sqrt{L^2} = kL \rightarrow L + xL_m = L + xkL \quad (4)$$

where k is the coupling factor between 0 and 1.

The effective inductance can thus be controlled by changing x, which is accomplished by tuning v_{b1}, v_{b2} and v_{b3}. For instance, tuning x between 0 and 1 gives an effective inductance range of L to $1.4L$, assuming $k = 0.4$, resulting in a frequency tuning range of 18%, as

$$\frac{f_{max}}{f_{min}} = \sqrt{1.4} = 1.18 \rightarrow 18\% \quad (5)$$

For this to work, however, the currents of the two inductors must be exactly in phase. Being 90 degrees out of phase would tune the resistance instead of the inductance. It is thus necessary to have the same resonance frequency in both tanks. Again, there is a contradiction between high Q and tunability. The frequency for which 90 degree shift occurs is, for a reasonable Q value of 20, separated from the center frequency by

$$\Delta f_{res} = \frac{f_0}{Q} = \frac{60GHz}{20} = 3GHz \quad (6)$$

That is, to obtain a wider tuning range it might be necessary to intentionally create a transformer with a lower Q value.

The purpose of the third branch in Fig. 2 is to decrease the effective inductance in branch 1, i.e. to generate negative values of x - contrary to the function of branch 2. When using this branch, the second branch should be turned off. This functionality, however, has not yet been verified.

The transformer was simulated in ADS Momentum and the dimensions were tuned to create a frequency span of 60 to 63 GHz together with the 22 µm wide transistors in each g_m stage. The coupled inductors are placed in the top metal layer, M7. Simulations show that the unloaded inductance of the primary coil is 72 pH and that it is 95 pH for the secondary coil. Also, simulations show that the quality factor is 11 for both coils and that the coupling coefficient is 0.42.

The signals from the VCO core branch were routed to two open drain buffers, which provide the measurement instruments with up to 5 dBm of signal power.

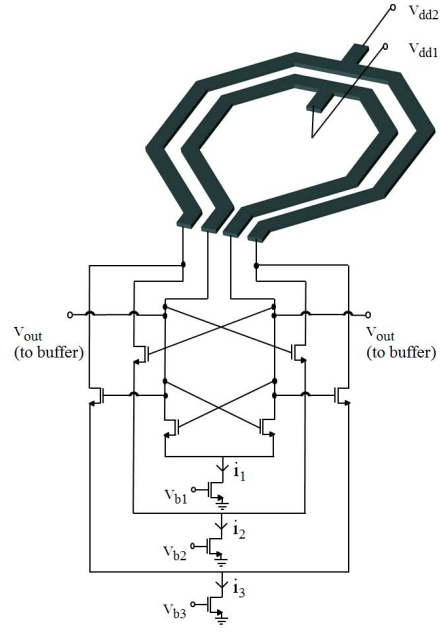

Fig. 2. Schematic of the varactorless VCO.

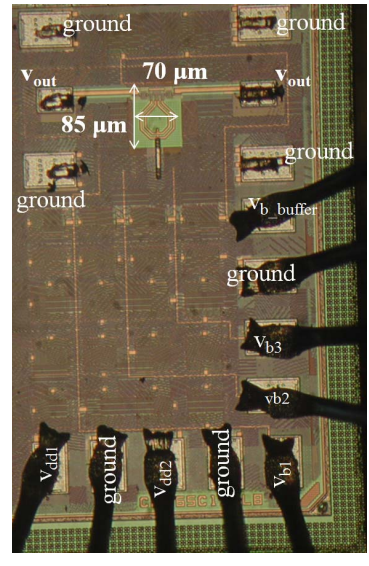

Fig. 3. Chip photo.

III. Measurement Results

The VCO was implemented in the standard ST 65 nm processes with 7 metal layers. The die area of the oscillator core, including the transformer, is 70 x 85 μm^2. Including pads the total chip size is 0.4 x 0.7 mm^2. The chip photo is shown in Fig. 3.

The chips were mounted on printed circuit boards, to which supply and bias signals were wire bonded. The high frequency signals were measured using Cascade Microtech GSG microprobes. A Rohde&Schwarz FSU Spectrum Analyzer with a range extender was used to measure the single-ended signal from one of the buffers. The phase noise was measured using an Aeroflex PN9000 phase noise measurement system, where the measured signal was an amplified version of the IF signal from the spectrum analyzer. The frequency tuning of the VCO was verified by keeping V_{b3} at 0 V, V_{b1} at 0.8 V, and changing V_{b2}. The result, in which the voltage-to-current characteristics of the bias transistor can be clearly seen, is shown in Fig. 4.

A more complete picture of frequency as a function of i_1 and i_2 is shown in Fig. 5. During the measurements the third branch was turned off. The data, consisting of 74 measurement points, show that the highest frequency of 65.083 GHz was attained for i_1 = 6.6 mA and i_2 = 0.001 mA. The lowest frequency of 62.198 GHz was attained when i_1 = 12.9 mA and i_2 = 15.9 mA, yielding a tuning range of 2.88 GHz or 4.5%. It was also found that the entire tuning range can be shifted by more than 1 GHz by changing the biasing of the buffers, and thus effectively change the capacitive load of the VCO the same way that a varactor would do.

Phase noise measurements and the corresponding FOM at 10 MHz offset for each frequency are presented in Fig. 6. In the phase noise measurement, both supply voltages, as well as V_{b1}, are set to 1.2 V, and the frequencies are swept by changing V_{b2} from 0.2 to 1.2 V in three steps. No corrections have been made in the phase noise data to account for added noise from the down conversion and 30 dB amplification of the signal. The best FOM of -182.4 dBc/Hz was found at the highest frequency, where the measured phase noise is low while the dissipated power is also at its minimum.

The measured performance of the VCO is compared with other recently published CMOS VCOs in Table I. As can be seen, this work has excellent phase noise and a small area. Although the tuning range may be on the low side, it may still be enough for the purpose, as many standards will eventually coexist in the millimeter wave band.

IV. Conclusion

A new varactorless VCO architecture is proposed in this paper. In contrast to previously published VCOs using inductive tuning methods, the tuning is carried out by continuously changing the effective inductance seen by the cross coupled pair. The measurement results show that the lack of a varactor leads to small size and a good phase noise performance.

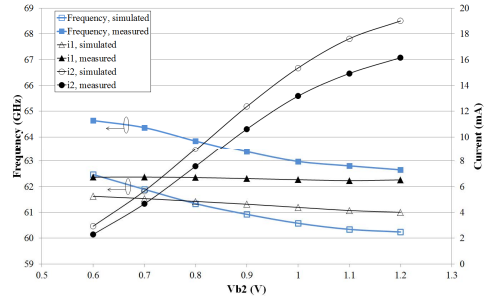

Fig. 4. Simulated and measured frequency and current consumption vs. v_{b2}.

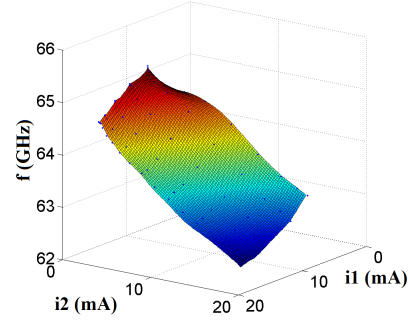

Fig. 5. Frequency vs i_1 and i_2.

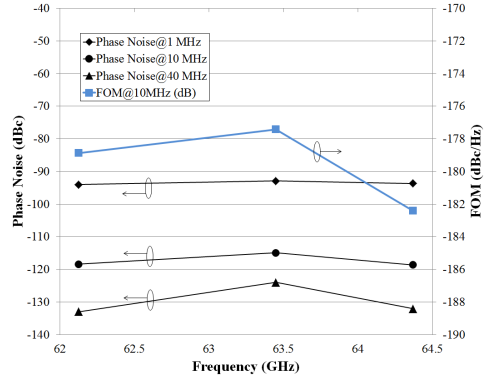

Fig. 6. Phase noise at 1, 10 and 40 MHz offset and FOM vs. frequency.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED TRANSFORMER BASED VCOS

Ref.	This work	[7]	[10]	[11]	[12]	[13]
Technology (CMOS)	65 nm	90 nm	65 nm	65 nm	90 nm	65 nm
Supply Voltage	1.2	0.7	1.2	1	0.43	1
Frequency (GHz)	63.7	56.75	73.8	61	61.7	59
Tuning Range (%)	4.5	16.07	41.1	14.2	4.81	5.4
Power consumption (mW)	6 to 30	8.7	8.4 to 10.8	6	1.2	16.5[e]
PN@10MHz (dBc/Hz)	-114.9 to -118.6	-118.8	-104.6 to -112.2	-110.8	-110[b]	-112[d]
FOM[a] (dBc/Hz)	-177.4 to -182.4	-184.3	-172 to -180	-179.3	-185[c]	-173.6
Area (mm^2)	0.006	0.1	0.03	0.031	0.007	0.21[f]

a. The figure of merit, FOM=(PN)-20 log(f_{osc}/Δf)+10log(P_diss/1mW).

b. Calculated as PN at 1 MHz -20 dB. c. Calculated from 1 MHz phase noise measurements.

d. Minimum measured figure reported. e. Including buffers. f. Including pads

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Paper III

Paper III

Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS

Therese Forsberg, Johan Wernehag, Anders Nejdel, Henrik Sjöland and Markus Törmänen, "Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 5, pp. 509–511, May 2017

Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS

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***Abstract*— Two 60-GHz band voltage controlled oscillators (VCOs) designed in a 28-nm ultrathin body and buried oxide fully depleted silicon on insulator (UTBB FD-SOI) CMOS process are demonstrated and compared. Both VCOs have identical cross-coupled nMOS cores and dissipate 3.15 mW from a 0.9-V supply. The first design uses a standard FET current source and achieves a figure of merit (FOM) of −181 dBc/Hz, whereas the second employs a filtered current source and achieves a state-of-the-art FOM of −187 dBc/Hz. The achieved 6-dB improvement demonstrates the efficiency of the filtering technique at millimeter wave frequencies and the feasibility of efficient low-phase noise designs in 28-nm UTBB FD-SOI CMOS. The active area of the filtered VCO is 90 μm × 180 μm and the standard VCO has an area of 80 μm × 110 μm.**

***Index Terms*— Analog integrated circuits, CMOS integrated circuits, low-phase noise, millimeter wave (mm-wave) integrated circuit, ultrathin body and buried oxide fully depleted silicon on insulator (UTBB FD-SOI) CMOS, voltage controlled oscillator (VCO).**

I. Introduction

INCREASING data rates demand increased bandwidth, such as the 7 GHz available in the unlicensed 60-GHz band, but also employment of more complex modulation schemes. These put stringent requirements on the phase-noise performance of the frequency generation circuitry.

Digital designs are moving to the smaller process nodes, and the analog designs must follow. Current state-of-the-art millimeter wave (mm-wave) CMOS VCOs [1]–[4] will thus be replaced by counterparts in process nodes, such as the 28-nm ultrathin body and buried oxide fully depleted silicon on insulator (UTBB FD-SOI). Indeed, this process also provides analog benefits, such as higher f_t and $f_{\max}$, higher intrinsic gain, and less parasitics. However, the high flicker noise of modern downscaled technologies requires efficient mitigation methods, such as employing a filter to resonate the differential pair source node at $2f_0$, and also to prevent tail current noise at $2f_0$ from creating phase noise [5]. Although this technique has already been applied at many different frequencies, including the mm-wave bands [6]–[10], it has not clearly been investigated what improvement in phase-noise performance that can be expected from it in CMOS VCOs at mm-wave frequencies.

In this letter, two 60-GHz band VCOs have been designed, fabricated, and characterized through measurements. Both VCOs have identical active cores, and one of them also uses the filtering technique of interest for improved phase-noise performance. The aim is to investigate the efficiency of the filtering technique at mm-wave frequencies and to create a high-performance VCO for the 60-GHz band.

II. Theory and Design

The differential cross-coupled *LC* oscillator topology is chosen for both designs as it is well known for its good phase-noise performance and ease of implementation [11].

The schematics of the implemented VCOs are shown in Fig. 1. Both VCO cores are designed to be as similar to each other as possible to facilitate a fair comparison. In the standard cross-coupled nMOS VCO, an FET current source is used. Phase-noise performance is optimized when the resonance tank is on the limit of being current limited. In this configuration, the design is susceptible to the noise generated in the current source transistor. To improve the flicker noise performance, its width is made three times the minimum channel length of the process.

Ideally, the current source should also have high impedance at $2f_0$ to prevent the triode resistance of the cross-coupled pairs from loading the resonator in the switched state. The second implemented VCO design, shown to the right in Fig. 1, thus employs a filter at the FET current source transistor [5]. A source inductor is used to resonate the parasitics of the source node at $2f_0$. Simulations show that while the tank waveform frequency contents of both VCO designs are almost identical, the second harmonic in the source node of the cross-coupled pair is three times stronger in the filtered design. A capacitor in parallel with the FET current source shunts high frequency noise from the current source to ground. However, low-frequency tail current noise can still cause phase noise due to the varactor nonlinearities [12]. In all, simulations show that for these designs, the maximum expected improvement in phase-noise performance at 10-MHz offset is 6.6 dB.

The varactors in both the designed VCOs consist of two transistors, dimensioned to give a desired tuning range of about 10%. The minimum channel length is used in order to maximize the varactor Q. The cross-coupled pairs are sized to provide enough loop gain to fulfill the oscillation criteria.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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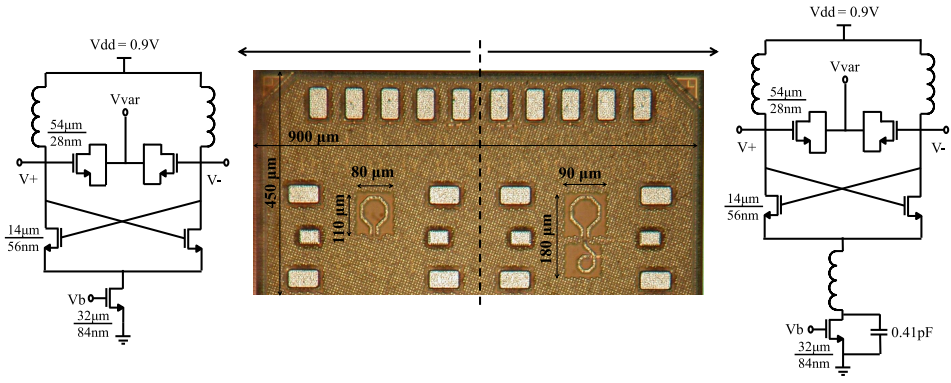

Fig. 1. Middle: chip microphotograph. Schematics of the cross-coupled nMOS VCOs. Left: standard design. Right: design with a filtered current source.

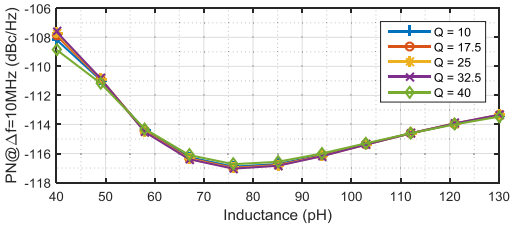

Fig. 2. Simulated phase noise at 10-MHz offset versus source filter inductor L and Q, at a varactor voltage of 0 V.

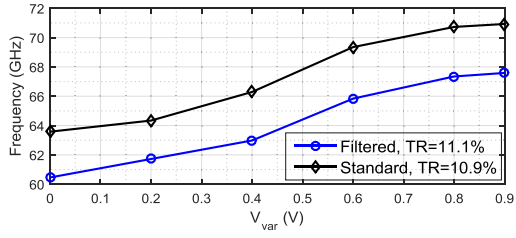

Fig. 3. Measured frequency tuning for both VCO designs.

All inductors were designed in the top metal layers and simulated in ADS Momentum. The tank inductance dimensions were tuned to make the two oscillators operate at the targeted 60-GHz frequency band.

Since the layout of the two VCO designs needs to be different in order to accommodate for the source node filtering in the second design, the parasitic capacitances and inductive coupling associated with the VCO tanks are slightly different. Thus, this also results in the inductance values having to differ slightly to ensure operation in the targeted frequency range. Simulations of the tank inductors show that the inductance values are 112 and 125 pH, each with an associated Q of 22.

The filter inductance value is 95 pH, with a Q of 18. Simulations show that the resonance frequency of the source node is important. As can be seen in Fig. 2, there is an optimal value of the inductance. Because of the steeper degradation on the lower side of the optimum, a slightly higher inductance value was chosen for the design to make it more robust to variations. The difference between the phase noise performance of the optimal inductance and the actual inductance is approximately 1 dB.

As for the impact of the Q of the filter inductance, simulations show that it is of minor importance to the filter noise reduction efficiency, as can be seen in Fig. 2.

For measurement purposes, the signals from the VCOs are routed to open drain buffers with approximately 5 dBm of output power.

III. Measurement Results

The two VCOs to be benchmarked were implemented in a 28-nm UTBB FD-SOI CMOS process with ten metal layers for interconnect from STMicroelectronics. The chip microphotograph is shown in Fig. 1. The chips were mounted on printed circuit boards, to which supply and bias signals were wire bonded. An Infinity GSG microprobe from Cascade Microtech was used for on-chip probing of the VCO buffer output signal. A Rohde & Schwarz FSU50 spectrum analyzer with a V-band frequency range extender, i.e., a subharmonic mixer, was used to measure the single-ended VCO buffer output signal. The phase noise was measured using an Aeroflex EuropTest PN9000 phase noise measurement system, and the measured signal was an amplified version of the downconverted VCO buffer output signal, at an intermediate frequency of 404.4 MHz, available from the spectrum analyzer.

Measurement results were obtained for both VCOs operating from a 0.9-V supply, each with a 3.5-mA core current, i.e., dissipating 3.15-mW dcpower.

The frequency tuning characteristics of the VCOs is presented in Fig. 3. The phase noise measurements along with the figure of merit (FOM) at 10-MHz offset are presented in Fig. 4, where the phase-noise improvement given by the filtering is clearly visible. At 1-MHz offset, the improvement in phase noise is measured to be between 5 and 12 dB. The best performance for both VCOs is at a varactor voltage of 0.2 V,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED 60-GHz CMOS VCOs

Ref.	Technology (CMOS)	Supply Voltage (V)	Frequency (GHz)	Tuning Range (%)	Power consumption (mW)	PN@10MHz (dBc/Hz)	PN@1MHz (dBc/Hz)	FOM[a] @10 MHz or 1MHz (dBc/Hz)	Area (mm2)
This work[b]	28nm FD-SOI	0.9	67.3	10.9	3.15	-109.9	-84.5	-181	0.088
This work[c]	**28nm FD-SOI**	**0.9**	**64**	**11.1**	**3.15**	**-116.5**	**-92.5**	**-187.3**	**0.162**
[1]	90nm bulk	1.2	61.3	8.44	7.2	-	-90.9	-178.1	0.34[d]
[2]	65nm bulk	1	61	14.2	6	-108.3	-	-176.2	0.031
[3]	130 nm	1.2	57.7	16.8	7.6	-124.8	-100.6	-186.3	0.201[d]
[6]	40 nm bulk	0.9	58	16	14	-	-91 to -94.5	-175 to -177	-
[7]	65 nm bulk	1	59	5.4	16.5 (incl. buffers)	-	-90.3	-167.3	-
[8]	90 nm bulk	1.2	83	0.8	13	-109.86	-83.21	-177	0.776[d]
[9]	65 nm bulk	1.2	70	6.5	7.2	-113.2	-	-181.8	0.048
[10]	65 nm bulk	1.2	56	17	15	-	-99.4	-182.2	-

a. The figure of merit, FOM=(PN)-20 log(f*osc*/Δf)+10log(P_diss/1mW). b. Standard VCO design. c. Filtered current source VCO design. d. Pads included.

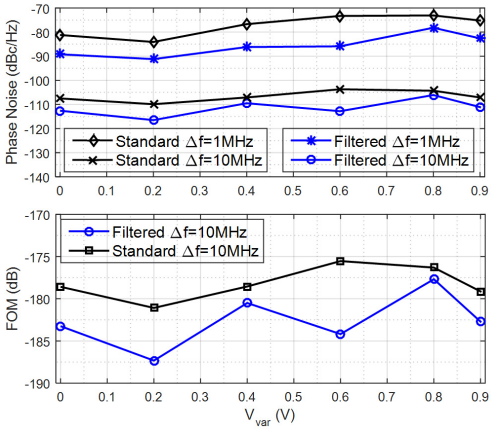

Fig. 4. Measured phase noise at 1- and 10-MHz carrier offset frequencies for both VCOs (top) and VCO FOM versus varactor control voltage (bottom).

where the phase noise at 10-MHz offset is improved by 6.6 dB and the filtered design achieves an FOM of −187.3 dBc/Hz.

The measured performance of the VCOs is compared with each other and to other recent published state-of-the-art 60-GHz band CMOS VCOs in Table I. The table also includes other mm-wave VCOs, which use the same filtering technique. Among the compared designs, both designs demonstrated here have the lowest reported power consumption. The filtered current source VCO design achieves an excellent phase-noise performance, and to the best of our knowledge, the highest reported FOM for a 60-GHz band CMOS VCO.

IV. CONCLUSION

This letter presents two measured cross-coupled nMOS VCO designs for the 60-GHz band in 28-nm UTBB FD-SOI CMOS process technology. While otherwise as identical as possible, one of design employs filtering of the current source. A comparison between the measured results empirically show that the improvement gained from the current source filtering technique is between 5 and 12 dB. The filtered VCO design achieves an excellent phase-noise performance and a state-of-the-art FOM of −187 dBc/Hz. It also has a good tuning range of 11 % and low-power consumption.

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Paper IV

Paper IV

Two Ultra-Low Power mm-Wave Push-Pull VCOs in FD-SOI CMOS

Therese Forsberg, Johan Wernehag, Henrik Sjöland and Markus Törmänen, "Two Ultra-Low Power mm-Wave Push-Pull VCOs in FD-SOI CMOS," in *Proc. of 2018 IEEE Asia-Pacific Microwave Conference (APMC)*, Kyoto, Japan, Nov 2018, 3 pages. Accepted.

Two Ultra-Low Power mm-Wave Push-Pull VCOs in FD-SOI CMOS

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***Abstract* — Two low-power mm-wave voltage controlled oscillators (VCOs) designed in a 28-nm fully-depleted silicon-on-insulator (FD-SOI) CMOS process are demonstrated, using a push-pull differential architecture. Measurement show that the first VCO has a 10.8% tuning rage centered at 30.3 GHz, and the second has a 8.9 % tuning range at 58.7 GHz. The 30 GHz VCO consumes 1.06 mW from a 1 V supply, and has a -119 dBc/Hz phase noise at 10 MHz offset, achieving a figure of merit of -188.4 dB. The 60 GHz VCO consumes 1.35 mW and has a -111.9 dBc/Hz phase noise at 10 MHz offset, achieving a figure of merit of -186.2 dB. Their active areas are 0.03 mm^2 and 0.096 mm^2, respectively.**

Index Terms — CMOS analog integrated circuits, mm-wave circuits, millimeter wave oscillators, voltage controlled oscillators, phase noise

I. Introduction

The ever-increasing demand for higher data rates in wireless communication requires wider bandwidths. As the frequency spectrum at lower frequencies becomes increasingly crowded, the available required bandwidths can instead be found at mm-wave frequencies. In the 7 GHz wide unlicensed band at 60 GHz, several standards, such as the IEEE 802.11ad for wireless local area networks, are already in place [1]. Moreover, several parts of the spectrum around 30 GHz will be used by the 5G standard. Since such communication standards target battery-operated consumer electronics, it means that it is imperative that the transceiver designs are low-power and low-cost.

It is desirable to use CMOS processes also for the analog parts of the transceiver to achieve low cost and high integration level. However, that may lead to higher power consumption in some parts of the transceiver. This is especially true for the frequency generation circuits in modern downscaled CMOS technologies due to higher flicker noise. The power consumption of the voltage-controlled oscillator (VCO) may thus need to be increased in order to obtain the necessary noise performance required to employ the complex modulation schemes that are a prerequisite for high data rates.

In this work, it has been investigated if ultra-low power mm-wave VCOs can be successfully implemented in 28-nm FD-SOI CMOS technology, especially in the unlicensed 60 GHz band and around 30 GHz.

II. Theory and Design

An attractive VCO topology for low-power operation, that is often used in different variations at RF frequencies [2]-[4], is shown in Fig. 1. To increase the attainable transconductance without increasing the current consumption, the basic differential cross-coupled NMOS LC oscillator topology is extended with a PMOS cross-coupled pair, in a push-pull configuration. This means that the current is effectively reused. Compared to the NMOS-only cross-coupled topology the output voltage swing will be lower, and limited to between ground and VDD. However, this also ensures safe operation of the transistors over time.

This current-reuse topology was chosen for the two VCO designs, one operating at around 30 GHz and the other around 60 GHz. To fit in a high performance mm-wave transmitter, a supply voltage of 1 V was used in the VCOs, thus avoiding the need of a separate low supply voltage domain. The drawn transistor dimensions that are equal in the two designs are indicated in Fig. 1.

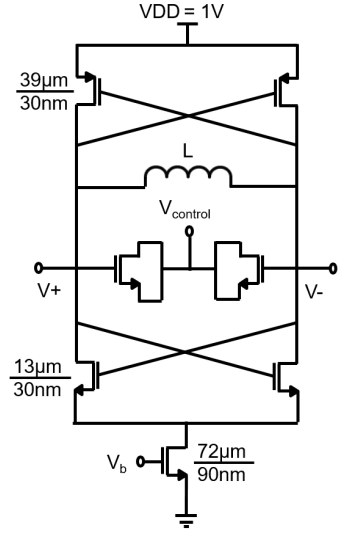

Fig. 1. Schematic of the push-pull VCOs.

Although the FET current source in the bottom both adds to the noise and decreases the voltage headroom available for the cross-coupled pairs, it is important to counteract amplitude variations due to process variations. Also, it facilitates the possibility to turn off the VCO without turning off the low-dropout regulator supplying the VCO. Its length was made three times the minimum channel length of the process to improve the flicker noise performance.

In the VCO tank, the varactors in both of the designed VCOs consist of two transistors, dimensioned to give a desired tuning range of about 10 %. To maximize the varactor Q, the minimum channel length was used. To tune the VCOs to the targeted frequency bands, the varactor of the 30 GHz VCO was designed to be twice the size of the varactor in the 60 GHz VCO. This also preserves the tuning range. Since the oscillation frequency is inversely proportional to the square root of inductance times capacitance, the inductance was also scaled up in the 30 GHz VCO. However, the ratio was slightly larger than 2 because the 30 GHz VCO parasitic capacitances are not scaled up. The inductors were designed in the top metal layer and simulated in ADS Momentum. The simulated inductance value for the 30 GHz VCO was 207 pH and 73 pH for the 60 GHz VCO.

The signals from the VCOs are routed to open drain buffers with approximately 5 dBm of output power for measurement purposes.

III. Measurement Results

The two VCOs were implemented in the STMicroelectronics 28-nm ultra-thin body and buried oxide fully-depleted silicon-on-insulator (UTBB FD-SOI) CMOS technology with 10 metal layers for interconnect. The chip microphotograph is shown in Fig. 2. The chips were mounted on printed circuit boards, from which the bias and supply voltages were provided through bond wires. The mm-wave single-ended output signals from the VCO output buffers were probed on-chip using an Infinity GSG microprobe from Cascade Microtech, and measured using a Rohde&Schwarz FSU50 spectrum analyzer equipped with an external V-band mixer. A down-converted version of the signal, available from the spectrum analyzer around the internal intermediate frequency of 404.4 MHz, was then amplified and sent to an Aeroflex EuropTest PN9000 phase noise measurement system.

Measurement results were obtained for both VCOs operating from a 1 V supply. The power consumption was 1.06 mW for the 30 GHz VCO, and 1.35 mW for the 60 GHz. The frequency tuning characteristics of the VCOs are shown in Fig. 3. The phase noise measurements for both VCOs, along with the figure of merit (FOM) at 10 MHz offset, are presented in Fig. 4 and Fig. 5, respectively. The best performance for both VCOs was at a varactor voltage of 0.1 V, where the 30 GHz VCO had a phase noise of -119 dBc/Hz and the 60 GHz VCO -111.9 dBc/Hz, both at 10 MHz offset from the carrier. The measured phase noise versus frequency offset for both VCOs at this varactor voltage is shown in Fig. 6, where the high flicker noise corner is visible.

The measured performance is compared to other recently published state-of-the-art low-power mm-wave CMOS VCOs in Table I. The designs demonstrated in this work achieve state-of-the-art performance. The 30 GHz VCO has the lowest power consumption of all compared designs. Both have about 10 % tuning range and work from a 1 V supply voltage.

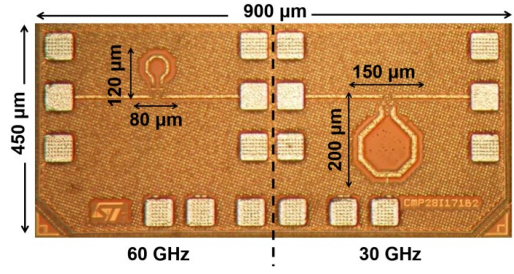

Fig. 2. Chip microphotograph.

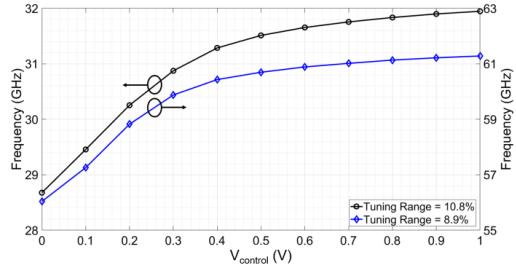

Fig. 3. Measured frequency tuning characteristics of the two VCOs.

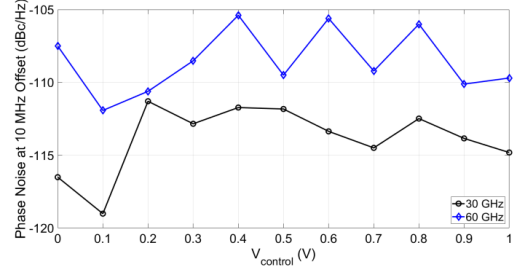

Fig. 4. Measured phase noise at 10 MHz offset from the carrier, for both VCOs.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED LOW-POWER MM-WAVE CMOS VCOS

Ref.	Tech. (CMOS)	Supply Voltage (V)	Frequency (GHz)	Tuning Range (%)	Power Consumption (mW)	PN @10MHz (dBc/Hz)	FOM[1] @10 MHz (dBc/Hz)	Area (mm^2)
This work	28 nm	1	30.3	10.8	1.06	-119	-188.4	0.096
This work	28 nm	1	58.7	8.9	1.35	-111.9	-186.2	0.03
[5]	90 nm	0.7	58.4	9.32	8.1	-91 (@1MHz)	-177.2 (@1MHz)	0.008
	90 nm	0.43	61.7	4.81	1.2	-90 (@1MHz)	-185 (@1MHz)	0.008
[6]	32 nm	0.6	30.4	7.6	4.56	-128	-190.9	0.3
[7]	65 nm	1	63.7	9.7	2	-110.86	-184.07	0.047
	65 nm	0.8	62.9	8.6	1.1	-108	-183.56	0.047
[8]	40 nm	0.7	55.5	25.4	10.5[2]	-122.3[2]	-183.7[2]	0.0672[2]

1. The figure of merit, FOM=PN-20 log($f_{osc}/\Delta f$)+10log(P_{diss}/1mW). 2. Including only the first buffer/amplifier stage.

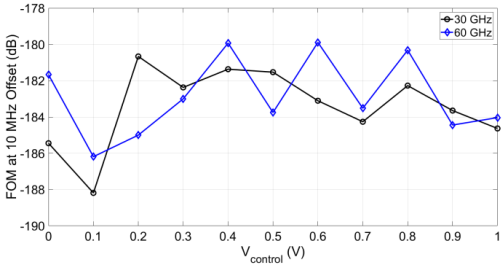

Fig. 5. Measured FOM at 10 MHz offset from the carrier, for both VCOs.

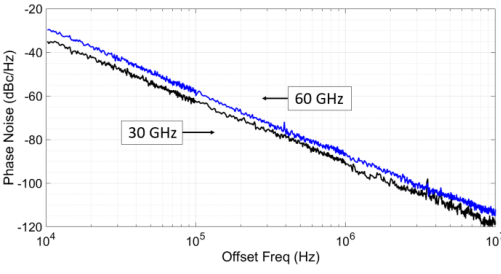

Fig. 6. Measured phase noise of the VCOs, at $V_{control}$ = 0.1 V.

IV. CONCLUSION

This paper presents two measured mm-wave push-pull VCOs, one operating at 30 GHz and the other one at 60 GHz, implemented in 28-nm UTBB FD-SOI CMOS technology. Both have a good frequency tuning range of about 10%, and FOMs comparable to other recently published low-power mm-wave CMOS VCOs. They both have a very low power consumption, with just over 1 mW each. This is achieved with a 1 V supply, avoiding the need for a dedicated low supply voltage domain for the VCO. To conclude, the results demonstrate the feasibility of low-power VCOs at mm-wave frequencies in down-scaled CMOS technologies.

ACKNOWLEDGEMENT

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Paper V

Paper V

A 10 mW mm-Wave Phase-Locked Loop with Improved Lock Time in 28-nm FD-SOI CMOS

Based on
Mohammed Abdulaziz, Therese Forsberg, Markus Törmänen and Henrik Sjöland, "A 10 mW mm-Wave Phase-Locked Loop with Improved Lock Time in 28-nm FD-SOI CMOS," submitted to *Transactions on Microwave Theory and Techniques*.

A 10 mW mm-Wave Phase-Locked Loop with Improved Lock Time in 28-nm FD-SOI CMOS

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***Abstract*—This paper presents a phase-locked loop (PLL) architecture that considerably improves the lock time. The architecture is demonstrated by a millimeter-wave PLL, that also features a novel double injection-locked divide-by-3 circuit and a charge-pump mismatch compensation scheme, resulting in state-of-the-art power consumption and jitter performance. The PLL is implemented in a low power 28-nm FD-SOI CMOS process and its output frequency is centred at 54.5 GHz. The in-band phase noise is between -93 and -96 dBc/Hz across the tuning range, and the integrated jitter is 176 fs to 212 fs. The total power consumption of the PLL is only 10.1 mW, resulting in a best case PLL figure-of-merit of -245 dB, and the active area is just 0.19 mm^2.**

***Index Terms*—60 GHz, 5G, charge pump, CMOS, divide-by-three, fast lock time, frequency synthesizer, ILFD, injection-locked divider, local oscillator, low phase noise, low-power, mm-wave, phase-locked loop, PLL.**

I. Introduction

PHASE-LOCKED LOOP (PLL) frequency synthesizers are key parts of today's wireless transceivers, and designing PLLs for millimeter-wave (mm-wave) communication standards is challenging from many aspects. Their phase noise limits the highest achievable modulation order [1], and they also need to have fast settling and be able to operate at low power in battery operated devices [2]–[4]. In particular, fast settling time is required for communication standards that support very high data rates, to avoid losing large amounts of data during frequency locking. In frequency-modulated continuous-wave (FMCW) radar applications a fast settling PLL is required to be able to receive baseband signals at higher frequencies, and hence reduce the impact of the high flicker noise corner in short-channel technologies [3], [4].

A frequency synthesizer operating at about 60 GHz can be used for direct conversion tranceivers in the unlicensed 60 GHz band, where for instance the WiGig/IEEE 802.11ad standard [2], future 5G standards [5], and high precision radars [3] will reside. Such a frequency synthesizer, followed by a divide-by-2 circuit, can also be used to generate quadrature signals for 28 GHz front-ends intended for emerging 5G applications. It can also be used as the local oscillator (LO) in dual-frequency conversion transceivers, by using the 60 GHz PLL output signal together with the divided 30 GHz or 20 GHz signals present in the PLL, depending on whether the first division step after the voltage controlled oscillator (VCO) divides by 2 or 3. Higher frequencies in the E-band can then be targeted. Clearly, high performance and low cost 60 GHz PLLs have many potential applications.

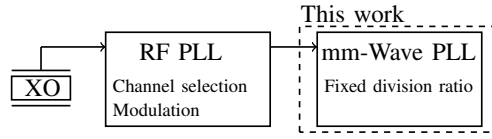

Fig. 1. Example of a mm-wave frequency generation architecture for 5G applications that utilizes the presence of an RF PLL.

The anticipated 5G wireless communication systems will support mm-wave links together with lower frequency cellular ones. This means that a mm-wave PLL operating with a high reference frequency (f_{REF}) may have another PLL as its input, instead of a crystal oscillator (XO). This has been the case in recent works and prior art, such as [6]–[8]. Similarly, a radio frequency (RF) f_{REF} can be provided by direct digital synthesis, which has been demonstrated in several state-of-the-art sub-millimeter frequency imaging radar systems [9]–[11]. Increasing f_{REF} is beneficial for the PLL noise performance, because when the f_{REF} noise is added to the PLL in-band noise it is first multiplied by the PLL division ratio squared. If the loop bandwidth is kept low, a PLL with high f_{REF} may also decrease the current consumption in the charge pump (CP). However, if not addressed properly, this approach will inevitably lead to problems with prolonged settling time. An additional advantage of using the PLL for cellular bands as an input to the mm-wave PLL in 5G systems, is that the RF PLL can provide the fine-grain resolution required for channel selection and/or modulation and thus simplify the design of the mm-wave PLL. The architecture of such a system is shown in Fig. 1.

In this paper a new PLL architecture is presented. Tuned to 56 GHz, the PLL is aimed at 5G applications, but it also has the more general goal of demonstrating an architecture that balances low noise, low power consumption and fast settling time, when a restriction is that the f_{REF} is several hundreds times the PLL loop bandwidth. The demonstrated PLL also

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features a novel double injection-locked divide-by-3 circuit, that achieves a wide lock range at low current consumption. Furthermore, the CP includes a novel current mismatch mitigation technique based on negative feedback. To support rail-to-rail output signals and hence wider VCO frequency range, the CP also features an improved operational amplifier that allows operation over a large common-mode range. The presented PLL shows competitive performance at a power consumption of just 10.1 mW, a value which to our knowledge is the lowest presented at such high output frequency. The PLL architecture is first introduced in Section II. Detailed description of circuit design is then presented in Section III. The measurement results together with a comparison to the state-of-the-art are then presented in Section IV. Finally, the paper is concluded in Section V.

II. PLL ARCHITECTURE

A conventional type-II PLL is shown in Fig. 3(a). Increasing f_{REF} is an effective technique to achieve lower phase noise [6]–[8]. Traditionally, using a higher f_{REF} means that the loop bandwidth can be higher, which in turn leads to an improved lock time. However, when the reference frequency becomes very high, the loop bandwidth is no longer limited by the reference frequency. Instead, if minimum jitter is targeted, the loop bandwidth should be chosen as the frequency where the VCO phase noise and extrapolated in-band phase noise at the PLL output intersect. Generally, for state-of-the-art mm-wave PLLs a typical bandwidth for optimum noise performance is in the order of a few MHz. If f_{REF} is then chosen to be about 2 GHz, the ratio of f_{REF} to loop bandwidth becomes very high. To still get the desired bandwidth when using such a high f_{REF}, either the loop filter (LF) capacitances must be increased, or the charge pump current (I_{CP}) must be reduced. Increasing the size of the LF leads to a large area for the capacitors, while reducing I_{CP} is an attractive way of reducing the overall power consumption. However, this will also limit the available output current from the CP that charges the filter capacitances, and the PLL lock time will be severely degraded due to so-called cycle slips, originating from nonlinear effects in the transient when the PLL is out of lock-in range [12]. An example of this is shown in Fig. 2, where the simulated VCO control voltage settling behavior for two PLLs with the same bandwidth is presented. One uses an f_{REF} that is 8 times higher, and to keep the loop bandwidth unchanged the I_{CP} is then also reduced 8 times. In the case of a high f_{REF}-to-bandwidth ratio, it can be seen that the cycle-slips prevents the PLL from approaching the correct frequency exponentially, and that the settling time is significantly prolonged.

It is thus clear that aggressively increasing the f_{REF} to obtain better noise performance affects the settling time, and that low phase noise and fast settling time are contradictory in this case. To solve this conflict of requirements we propose a PLL architecture that can achieve fast settling by disregarding the noise performance during PLL settling, and then seamlessly shift to a low noise mode at steady state, thereby achieving both fast settling and low noise. The proposed PLL architecture, that features two such optimized modes of operation, is shown in Fig.3(b). Fast settling mode is

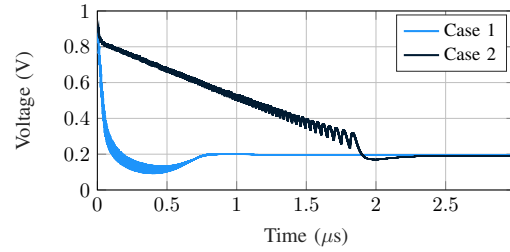


Fig. 2. Example of the impact of cycle-slips. Both cases have the same loop bandwidth, but f_{REF} is 8 times larger and I_{CP} is 8 times smaller in case 2.

enabled when SW_{fast} is set to logic 1. Both multiplexers then forward the signal divided by an extra factor N_2. The effective reference frequency becomes f_{REF}/N_2, and the divided VCO frequency to be compared to it by the phase frequency detector (PFD) becomes $\frac{f_{VCO}}{N_1 N_2}$. At the same time, the amplitude of the current pulses fed to the loop filter from the CP become $N_2 I_{CP}$. This mode has an increased maximum current that can charge the capacitors in the loop filter, which yields a faster settling. Low noise mode is enabled when setting SW_{fast} to logic 0. Both multiplexers then forward f_{REF} and f_{VCO}/N_1 without the extra division. The amplitude of the CP current pulses is at the same time reduced to I_{CP}. The reduced CP current increases the settling time, but the total power consumption is reduced and the decrease in total division ratio improves the in-band phase noise of the PLL. In this work, f_{REF}/N_2 is chosen to be 8, large enough to demonstrate the efficiency of the mode-switching architecture.

It is important to note that for either mode setting, the small signal PLL characteristics remain the same. One CP is switched on or off, but a seamless transition between modes is possible because the steady state value of V_{ctrl} is the same in both modes and no loop filter reconfiguration is needed. The signal SW_{fast} can be easily generated when the current operating frequency is to be changed. As will be demonstrated by measurements in Section IV, the mode transition will indeed be seamless and not generate any sudden transients. Therefore, the mode change back to low-noise mode can be performed simply after a predefined delay, without any need of calibration.

III. PLL IMPLEMENTATION AND CIRCUIT DETAILS

A. The VCO and divider chain

The PLL was implemented in a low power 28-nm CMOS SOI process. The VCO and divider chain is shown in Fig. 4. The phase noise performance of the cross-coupled pair VCO is improved by using the tail current filtering technique [13], which is effective also at 60 GHz [14]. The VCO output is fed differentially to an injection-locked frequency divide-by-3 circuit (ILFD), as well as to two single-ended buffers, for measurement purposes. Simulations show that the full differential VCO voltage swing of 2.7 V peak-to-peak can be preserved, even if the VCO output signal is also required to drive additional, mainly capacitive loads, such as divide-by-two ILFD circuits or a mixer. The differential output of the

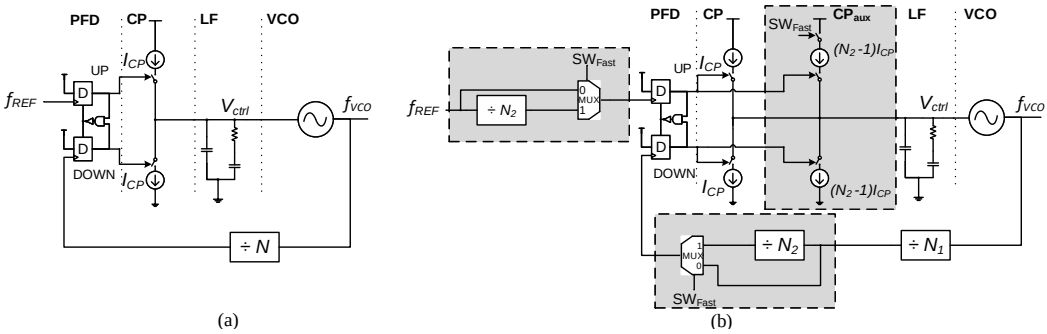


Fig. 3. Schematics of (a) a type II PLL and (b) the proposed PLL architecture, where $\mathrm{SW_{fast}} = 1$ activates fast-locking mode, and $\mathrm{SW_{fast}} = 0$ activates the low-noise mode.

ILFD is fed directly to a differential latch-based divide-by-2 circuit, followed by true single phase clock (TSPC) dividers and a multiplexer [15]. The first stage of the TSPC divider divides the frequency of the input by 4 or 6, depending on if the Sel control signal is set to logic 0 or 1, respectively. This signal is used to perform step response measurements. Based on whether the PLL is to operate in low-noise mode or fast-settling mode, the control signal SW_{fast} is set to either logic 1 or 0. The sinusoidal reference signal is buffered and converted to a square wave on chip, and fed to the PFD though a multiplexer in a similar configuration as in the divider chain path.

For mm-wave PLLs it is preferable to use a division ratio higher than two in the first feedback divider stage after the VCO, if it can be achieved without increasing the power budget. At such frequencies, however, as explored in [16], [17], special architectures suited for mm-wave operation have to be employed. One such architecture that has lately gained increased attention due to its attractive properties, such as low power consumption and small area, is the mm-wave dynamic current mode logic (DCML) divider. The operation at mm-wave frequencies is attributed to that the memory elements in the latches are the parasitic capacitances of the active devices. Unfortunately, this kind of divider is sensitive to process, voltage and temperature (PVT) variations. Injection locking is a more attractive technique in terms of robustness, since LC tanks are then used to tune the divided frequency output, and ILFDs with higher division ratios such as 3 have been demonstrated [18]–[20]. However, current consumption and locking range remain major concerns when increasing the division ratio, due to less effective current injection. The ILFD presented in this work addresses these issues.

Differential ILFD divide-by-two operation is typically based on injecting a current signal at a frequency close to the second harmonic of the ILFD LC resonance (f_0), at the source of the current commutation MOS pair, as shown in Fig. 5(a) [21]. The current signal is then injected by the tail transistor $\mathrm{M_1}$ which acts as a transconductance. Note that $\mathrm{M_2}$ and $\mathrm{M_3}$ act as a single balanced mixer with a maximum conversion gain of $G = \frac{2}{\pi}$, down-converting the injected signal to a frequency close to f_0 at the LC tank. A more general observation is that injection locking division is achieved by injecting a harmonic signal to the circuit that by some mechanism results in a current signal at the drains of $\mathrm{M_2}$ and $\mathrm{M_3}$, with a frequency close to f_0 and a magnitude sufficiently large to pull the oscillator to that frequency. An upper bound of the frequency locking range for the ILFD shown in Fig. 5(a) is expressed by [21], [22]

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}} \tag{1}$$

where Q is the quality factor of the divider's LC tank, I_{inj} the magnitude of the injected current, and I_{osc} the magnitude of the free running oscillator current at f_0. In (1) $G = \frac{2}{\pi}$ is used assuming $\mathrm{M_2}$ and $\mathrm{M_3}$ switch on/off abruptly [22]. Injecting a voltage V_{inj} at the gate of $\mathrm{M_1}$ makes the frequency locking range ω_{range} become

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{G_m \cdot V_{inj}}{I_{osc}} \tag{2}$$

It is important to note that ω_{range} is referred to the output frequency of the divider. Clearly, a way to improve the lock range without compromizing performance, such as reducing Q, is by maximizing I_{inj} (i.e. increasing the injection efficiency).

To make the ILFD to divide by 3, the current can be injected directly to the output using differential back-to-back MOS devices, as shown in Fig. 5(b) [20], [23]. In this work a novel double injection-locked divide-by-3 circuit is proposed, see Fig. 5(c). The proposed divider uses double injection to achieve increased injection efficiency, enabling a wide tuning range at a reduced current consumption. The triode-multiplier constituted by devices $\mathrm{M_4}$ and $\mathrm{M_5}$ multiplies the injected voltage (V_{inj}) at frequency $f \approx 3f_0$ with that of the divider output, tuned to f_0. It was shown in [24] that the output voltage of the triode-multiplier is comprised of even order harmonics. In this case, the multiplier is excited with rail-to-rail signals from the VCO and therefore it acts as an efficient voltage-mode single-balanced mixer with a differential input and a single-ended output. The output of the multiplier is simply the even order inter-modulation terms, which in locked state are at frequencies close to $2f_o, 4f_o$ and higher even order harmonics. These tones are in turn fed to the tail current device, which acts as a transconductance that injects current mainly at $\approx 2f_o$

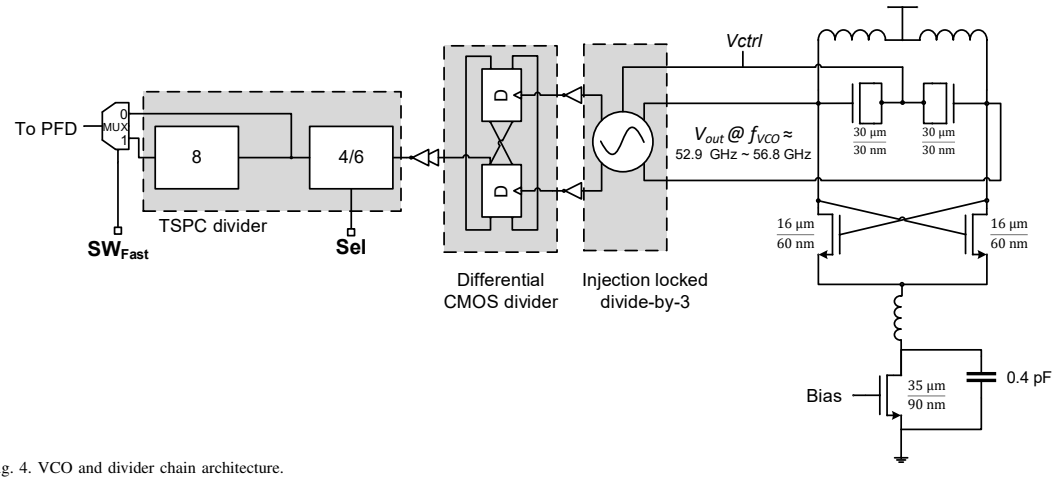


Fig. 4. VCO and divider chain architecture.

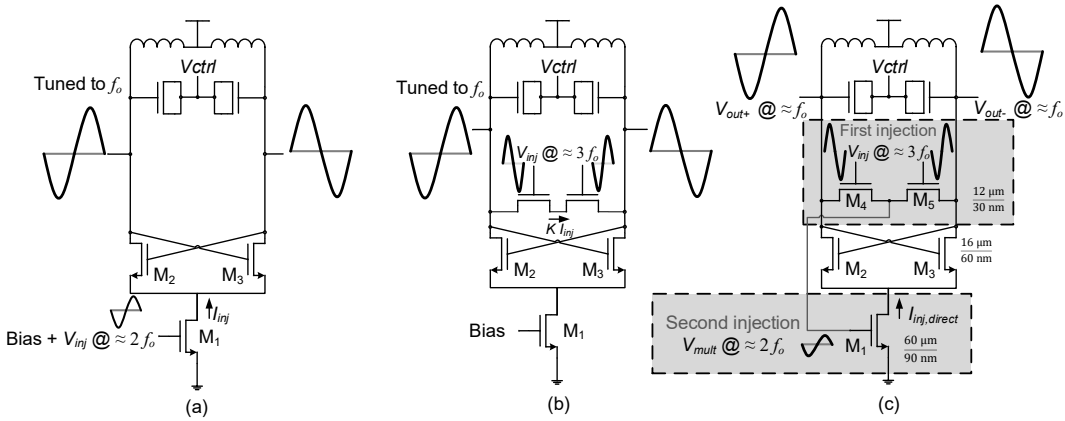


Fig. 5. Injection-locked frequency dividers. (a) Divide-by-2. (b) Divide-by-3. (c) Proposed novel double injection divide-by-3.

to the source of the active pair (M_2 and M_3). This results in an additional injection mechanism similar to that of the divide-by-2 ILFD shown in Fig. 5(a). Higher order harmonics are not significant, as they are suppressed by the circuit. The triode-multiplier also injects a current signal at the first harmonic, $I_{inj,direct}$ directly to the output. Hence, the lock range of the divider is proportional to the sum of lock ranges of the two dividers in Fig. 5(a) and 5(b). Including the transfer of the passive mixer $V_{inj} = \frac{2}{\pi} V_{out}$ in (2) and adding the direct injection gives

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \left(\frac{2}{\pi^2} \cdot \frac{g_m V_{out}}{I_{osc}} + \frac{I_{inj,direct}}{I_{osc}}\right) \qquad (3)$$

Equation (3) presents an upper bound to the lock range of the double injection-locked divider, indicating that the lock range can be increased considerably compared to the direct-injection-only circuit, without any current penalty. The current budget can also be reduced significantly, since with the second injection path established, the first injection devices (M_4 and M_5 in Fig. 5(c)) can be small, increasing the LC resonator impedance. Further efficiency enhancement is also achieved due to the push-push regime that the tail current source M_1 is operated in.

The designed divider covers the frequency range of the VCO with a margin, to account for PVT variations. Simulations of the divider sensitivity with single injection and with the proposed double injection are shown in Fig. 6. At the same power consumption, with an input power of 5 dBm and at a fixed varactor voltage of $VDD/2$, the double injection increases the locking range from 2.5% to 8.5%, i.e. by a factor of 3.4. All possible spurs created by the ILFD are harmonics of the divided signal and, since the output is differential, the odd order harmonics dominate. Directly after the ILFD are inverting buffers that aim to make the signal even more square-wave shaped and thus increase the odd harmonics even further. The spurs of the ILFD are thus of little concern in this case.

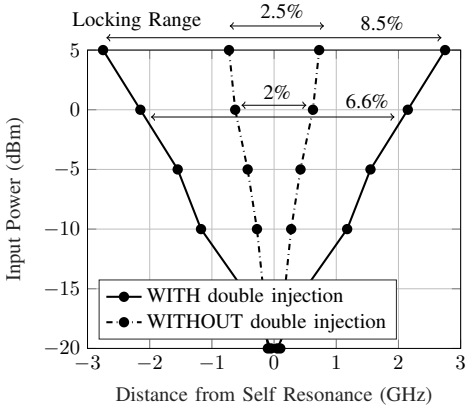


Fig. 6. The simulated sensitivity of the ILFD at a fixed varactor voltage of $VDD/2$, with and without the double injection, at the same power consumption.

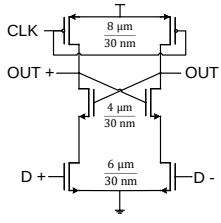


Fig. 7. Differential high speed CMOS latch.

The simulated phase noise of the ILFD at 10 MHz offset from the carrier is below -141 dBc/Hz, with a noise of -146 dBc/Hz close to its self-resonance frequency.

The ILFD is followed by a divide-by-2 circuit as shown in Fig. 5 (a). The latch proposed in [25], shown in Fig. 7, can be used directly after the ILFD thanks to the high speed 28-nm technology, while the last divider stages are implemented in TSPC logic.

B. The PFD-CP

The three-state PFD used in this work is TSPC-based and produces UP/DOWN pulses, which are converted to differential signals by inverters. Transmission gates are used to match the inverter delay, thereby mitigating imbalance between the differential signals.

The CP schematic is shown in Fig. 8, using a differential architecture ($\mathrm{M}_1 - \mathrm{M}_6$) for high speed and reduced charge sharing. The UP/DOWN currents are matched to a first order through a 1:1 current mirror ($\mathrm{M}_1, \mathrm{M}_6, \mathrm{M}_{11} - \mathrm{M}_{13}$). Due to the reduced feature size, however, the channel length modulation causes mismatch between the UP and DOWN currents at high and low values of the output voltage V_{ctrl}. This results in different UP and DOWN pulse widths at steady state, where the pulse with less current must become wider to compensate for the current difference and produce zero net charge to the LF. This issue results in increased spur levels and noise contribution from the CP, as described below.

In [26], [27] it was shown that high frequency noise folding due to CP gain mismatch can result in large PLL in-band phase noise increase, especially in fractional-N PLLs with strong $\Sigma\Delta$-modulation noise. This effect is even more pronounced by charge injection, further increasing gain mismatch in the cross-over region, resulting in more noise folding. To reduce charge injection, an operational amplifier OP1 is therefore used to make the voltage of the dummy node in the differential CP track V_{ctrl} [28]. Furthermore, with increased f_{REF}, the contribution of the CP to the PLL phase noise becomes more significant. This in-band contribution is [29], [30]:

$$\mathcal{L}_{CP} = \frac{2k_B T \gamma g_m n_T}{(I_{CP}/2\pi)^2} \cdot (T_p/T_{REF}) \cdot (1 + \frac{(T_p/T_{REF}) f_c}{f_{offset}}) \cdot N^2 \quad (4)$$

where $T_{REF} = 1/f_{REF}$, k_B is the Boltzmann constant, T the absolute temperature, γ the MOS gamma factor, g_m the transconductance of the devices in the 1:1 current mirror, n_T the number of MOS devices used to copy current to the CP, f_c the $1/f$ noise corner of the MOS devices, and T_p the current pulse width in steady state (in this work $T_p \approx 20$ ps). This relation indicates that the noise contribution of the CP remains constant if I_{CP} is scaled down by the same factor as the PLL division ratio N. However, T_p is dependent on the speed of the latches in the PFD and hence do not scale with f_{REF}. As T_{REF} is reduced the CP phase noise contribution will therefore increase, both thermal noise and even more so $1/f$ noise. A mismatch in UP/DOWN currents will result in wider pulses, as the minimum pulse width is set by the PFD reset delay. The pulses will then contain more charge and contribute more phase noise. There are thus two mechanisms that cause increased phase noise due to CP mismatch, high frequency noise folding and loop filter noise injection, motivating a technique to counteract mismatch.

To reduce the mismatch between UP and DOWN currents, compensation of the channel length modulation effect is required [31]. The schematic of the CP is shown in Fig. 8, where an additional dc current branch ($\mathrm{M}_7 - \mathrm{M}_{10}$) has been introduced, with 1:1 replicas of ($\mathrm{M}_1, \mathrm{M}_3, \mathrm{M}_5, \mathrm{M}_6$). A negative feedback loop, using amplifier OP2 with a push-pull output stage ($\mathrm{M}_{14}, \mathrm{M}_{15}$), controls the UP current so that the dc current branch outputs V_{ctrl}. Since the NMOS and PMOS currents are equal in the dc branch, and it has the same output voltage as the CP, and replicated devices, the UP and DOWN currents must also be equal.

The operational amplifiers used in the CP needs to have high gain as well as capability to handle rail-to-rail common-mode signal levels. This is crucial as the CP output voltage range limits the PLL frequency range. The schematic of a conventional amplifier proposed in [32] is shown in Fig. 9(a). All the devices are biased in weak inversion for low current consumption, keeping in mind that only low frequency signals are processed. The input differential pair limits the minimum common-mode input voltage, and an improved version is shown in Fig. 9(b), where the input stage is a differential pair in parallel with a differential cross-coupled PMOS source follower. As the common mode input voltage drops below

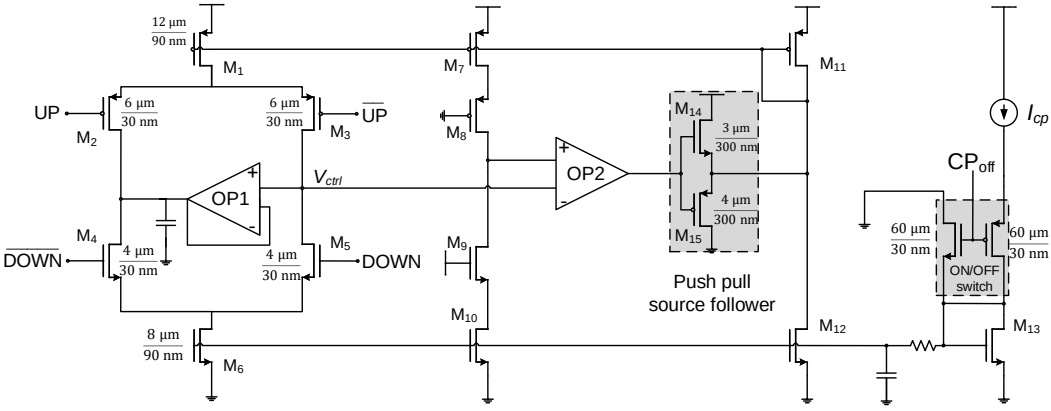


Fig. 8. Schematic of the charge pump with replica-based feedback loop to correct for UP/DOWN current mismatch.

a threshhold voltage, the common source gain is drastically reduced. However, inserting the PMOS source follower in parallell, which turns on under these conditions, preserves some of the gain. Since the differential pair common source amplifiers are loaded with diode connected devices, the voltage gain from the gate to drain is not high, making the gain of the common source an the source follower more similar. This technique has also been used in [24] to improve the linearity of operational transconductance amplifiers. Simulation of the voltage gain with and without the proposed technique is shown in Fig. 10. As can be seen in the figure, using a PMOS source follower helps providing gain even at 0 V common-mode input. Traditionally the amplifier shown in Fig. 9(a) has been used without phase compensation, however, in this case the high gain of the dc loop required compensation, realized by the resistor-capacitor link at the output. The 20 pF capacitor creates a dominant pole, and the resistor a high frequency zero, advancing the phase.

The CP was simulated when driven by two in-phase signals with a frequency of 2 GHz, to resemble the PLL locked state with DIV and REF matched in phase and frequency. The CP output was forced to a fixed voltage and the output current was observed. The net output current then represents the mismatch between UP and DOWN currents. The simulated mismatch versus CP output voltage with/without the proposed CP mismatch correction loop is shown in Fig. 11. As can be seen, the current mismatch is reduced to less than 0.1% in the range from 0.2 V to 0.8 V. The excessive mismatch near supply (1 V) and ground voltage proximity is due to the V_{dsat} drop required over the tail current devices M_1 and M_6 shown in Fig. 8.

IV. Measurement Results

Before designing the complete PLL, a stand-alone ILFD was designed and fabricated. For comparison it shares a chip with an identical ILFD - but without the double injection path. Both the ILFDs and the subsequent PLL were fabricated in the STMicroelectronics 28-nm ultra-thin body and buried oxide (UTBB) fully-depleted (FD) silicon on insulator (SOI) CMOS process with 10 metal layers for interconnect, and with the metal-insulator-metal (MIM) capacitance option. The active area of each divider is 0.05 mm^2 and the total area of the PLL chip is 0.9 x 0.9 mm^2, of which the active area is just 0.17 mm^2. The ILFD die microphotograph is shown in Fig. 12, and that of the PLL chip overlaid with a layout image in Fig. 13. Both chips were mounted on FR-4 printed circuit boards, to which all needed supply, bias and signal pads were wire-bonded. Only the mm-wave signals were probed, using Infinity microprobes from Cascade Microtech. The PLL measurement setup is depicted in Fig. 14. The input reference frequency was generated by an Agilent E4438C signal generator with low-noise option UNJ. For the phase noise measurements, an FSWP phase noise from Rohde & Schwarz with harmonic mixers for the 50 to 75 GHz band was used. The FSWP also provided the setup with low-noise supply voltages. An FSU50 spectrum analyzer with a harmonic mixer, also from Rohde & Schwarz, was used for the output spectrum measurements. The loop control voltage measurements used a 4 GHz 20 GS/s Rohde & Schwarz RTO 1044 digital oscilloscope. Pulses for the mode switch control were generated by a WW2572A 250 MS/s waveform generator from Tabor Electronics. To not introduce noise on the sensitive loop control voltage node, the oscilloscope was disconnected during phase noise measurements.

Measurement results from the the ILFD are shown in Fig. 15, and the two versions are compared in Table I. When utilizing the full range of the varactor, the measured locking range is increased from 13% for the single injection circuit, to 17.5% for the double injection circuit. Even if these ILFD measurements use less than 0 dBm input signal due to measurement setup limitations, which is less than the expected VCO output voltage in the PLL, also the single-injection ILFD demonstrates a wide locking range covering the VCO frequencies. However, using the single injection ILFD in the PLL would allow for almost no drift in tuning due to process and temperature variations between the VCO and

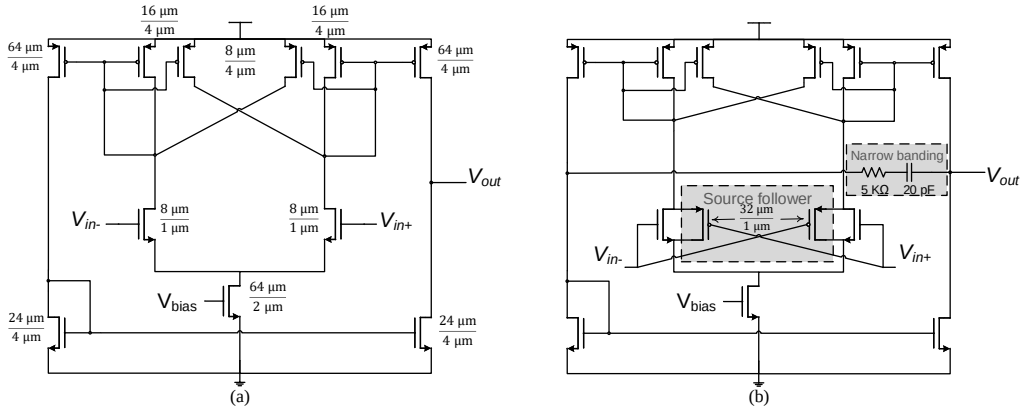


Fig. 9. (a) The amplifier proposed in [32] and (b) improved amplifier with parallel source follower stage for rail-to-rail common-mode operation and RC narrow-banding for loop stability.

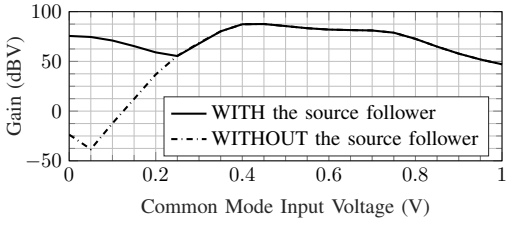


Fig. 10. Simulated low-frequency gain of the amplifier in Fig. 9, with and without the parallel source follower.

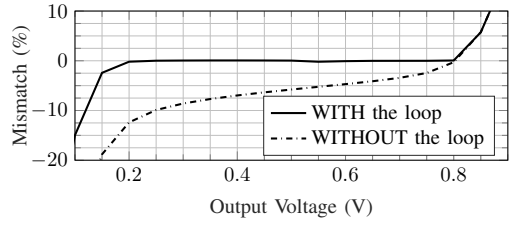


Fig. 11. Simulated CP current mismatch, with and without feedback loop, at 1 V supply.

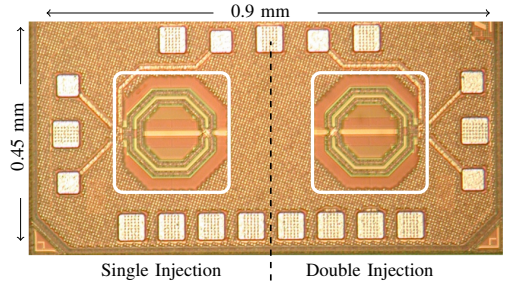


Fig. 12. ILFD chip photo. The active area is inside the white rectangles.

TABLE I
COMPARISON BETWEEN MEASURED RESULTS FOR THE SINGLE AND DOUBLE INJECTION CIRCUITS

At approximately 0 dBm input power	**Single injection**	**Double injection**
Locking range at 2.5 mW	53 - 60.5 GHz (13%)	52.8 - 62.9 GHz (17.5%)
Locking range at 1.5 mW	54 - 60.9 GHz (12%)	53.5 - 62 GHz (15%)
Locking range at 2.5 mW when $V_{varactor} = VDD/2$	54.1 - 55.4 GHz (2.4%)	54.1 - 57 GHz (5.2%)

the ILFD. Since they will be tuned together by the same control voltage, the key concern is how sensitive the mm-wave parts of the PLL are to unforeseen tuning mismatch, and the robustness is dependent on the locking range of the ILFD for a fixed varactor control voltage. At a fixed varactor voltage of $VDD/2$, measurements show that the double injection technique increases the lock range by more than a factor of two, from 2.4% to 5.2%.

When measuring the PLL, deviations from simulated performance were found. One such difference was that the out-of-band noise was worse than anticipated from measurements of earlier stand-alone VCOs in the same CMOS process [14], possibly due to the decision to use a single ended output buffer for the VCO signal, or due to noise coupling to the loop control voltage node. This was addressed by increasing the PLL bandwidth. The in-band noise was also higher than expected from simulations, which was alleviated by the decision to increase the CP current, and to complement the internal loop filter with additional capacitance, connected externally. The choice of external components was a capacitor twice the size of the internal one, in series to ground with a resistor half the size of the internal one. If implemented on chip, the extra loop filter would add approximately 0.02 mm^2 of active area, making the new total active area 0.19 mm^2.

All PLL performance measurements were taken using the same settings applied to a single chip in room temperature. Subsets of the full measurement set were also taken on three additional chips, to investigate variations between samples. The supply voltages for the VCO, ILFD, 20 GHz latch, and

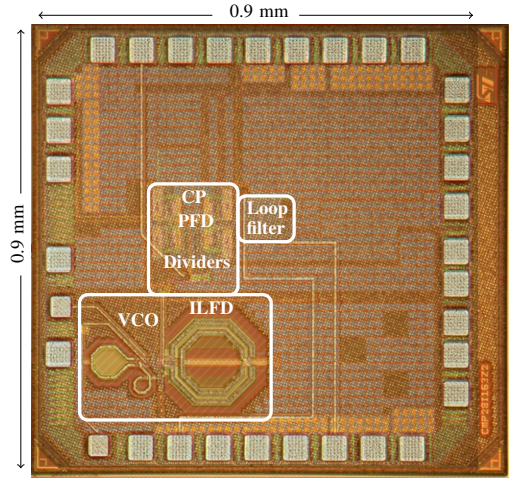


Fig. 13. The chip micrograph with the layout overlayed. The active area of 0.17 mm^2 is inside the white rectangles.

the output buffer were set to 0.8 V, and the supply voltages for the low frequency dividers, PFD, CP and CP amplifiers were set to 1.06 V. The regular and large CP currents were set to 300 μA and 7 x 300 = 2400 μA, respectively. The total power consumption of the PLL was then measured to 15.2 mW in fast-locking mode, and 10.1 mW in low-noise mode. The measured power consumption of each contributor is visualized in Fig. 16. It is apparent that the CP current results in a significant power consumption reduction when the PLL operates in low-noise mode. However, the full effect cannot be clearly seen in the figure since the CP shares supply with the PFD, which in low-noise mode will operate at a frequency 8 times higher, hence consuming more power. Since the PLL will be in low-noise mode nearly all the time, the power in low-noise mode will be presented as the PLL power consumption.

The PLL frequency range, i.e. the range where the PLL is able to acquire lock, was measured to 52.87 to 56.81 GHz. At the edges of this range, however, the reduced CP and VCO gain reduce the PLL bandwidth, which along with increased CP current mismatch result in degraded phase noise performance. Hence, the useful frequency range of the PLL is therefore where the phase noise performance is relatively uniform. This was measured to be between 53.2 and 56.1 GHz, a 5.3% range, in which the jitter deviated by less than 1.6 dB from the minimum value of 176 fs, see Fig. 17. While the measured tuning range, which is 1.45 GHz when divided by two, is wide enough to cover the upcoming 5G band in the USA, that is 0.85 GHz located between 27.5 and 28.35 GHz [5], it still requires some slight tuning. To ensure that the intended bands are covered even in the presence of process variations, the PLL frequency range could be increased. An increased PLL output frequency range will also have the added benefit of making the PLL useful in more applications. The output frequency range of the presented PLL is mainly defined by VCO tuning range. The most straight-forward way to increase this is to increase the VCO varactor size or to include switched capacitor arrays in the VCO tank, resulting in a trade-off between phase-noise and tuning range.

The output spectrum at a PLL output frequency of 54 GHz was measured, see Fig. 18. The PLL was in low-noise mode and the total division ratio of the PLL was set to 24. To access the differential VCO signal outside the chip it was fed to two single-ended on-chip buffers, one of which was accessible by on-chip probing. The buffers were sized down to produce a signal of lower power, to reduce coupling to sensitive parts of the circuit, as well as supply ripple due to high frequency current through bond wires. Because of this, the measured off-chip output signal power was about -27 dBm. Note that this is just for measurement purposes, and that the PLL is intended to deliver its output signal to a transceiver on the same chip. Since the measurement setup lacked external amplifiers and the used external mixer has high signal loss, the measured spectrum has a high noise floor. As can be seen in the PLL output spectrum in Fig. 18, the external harmonic mixer also makes the noise floor itself undulate, and creates spurs. The reference spurs, at a distance of 2.25 GHz from the carrier, are measured to be below -61 dBc.

The PLL phase noise measurements in Fig. 17 show the phase noise and RMS jitter across the PLL frequency range, in low-noise and fast-locking mode. The total division ratio was set to 24, by setting the Sel signal in Fig. 4 to a logic 0. The RMS jitter was calculated from the measurements by integrating phase noise from 1 kHz to 30 MHz offset frequency. The best measured phase noise performance was at an output frequency of 54 GHz, where the RMS jitter was 176 fs and the phase noise at 1 MHz and 10 MHz offset were -95.7 dBc and -103.5 dBc, respectively. The measured in-band phase noise at 1 MHz offset stayed below -93 dBc in all low-noise mode measurements. Since the PLL will be in low-noise mode when used as a clock source, the measured phase noise of this mode will be presented as the overall PLL performance.

The measured noise includes a negligible noise contribution from the frequency reference signal, see Fig. 19. If a CMOS state-of-the-art, low-jitter 2.2 GHz PLL, such as [33], [34], is used as the input reference frequency generator, the integrated jitter is estimated to rise from 176 fs to between approximately 200 and 230 fs.

Separate phase noise measurements were conducted with the current source matching in the CP disabled. They indicate that the technique does help reduce the phase noise, especially at lower offset frequencies, as expected. A measurement showing the impact on the phase noise in low-noise mode is shown in Fig. 20.

To estimate the settling time, and to verify concept of the mode-switching PLL, the loop control voltage was measured during settling with a digital oscilloscope. To introduce a step in the PLL, a pulsed input signal was applied to the Sel signal that controls the division ratio of the divide-by-6-or-4 divider in the feedback path, see Fig. 4, while the reference frequency was kept constant. That means that the PLL goes from an unlocked state, when the division ratio times the reference frequency does not fall inside the VCO tuning range,

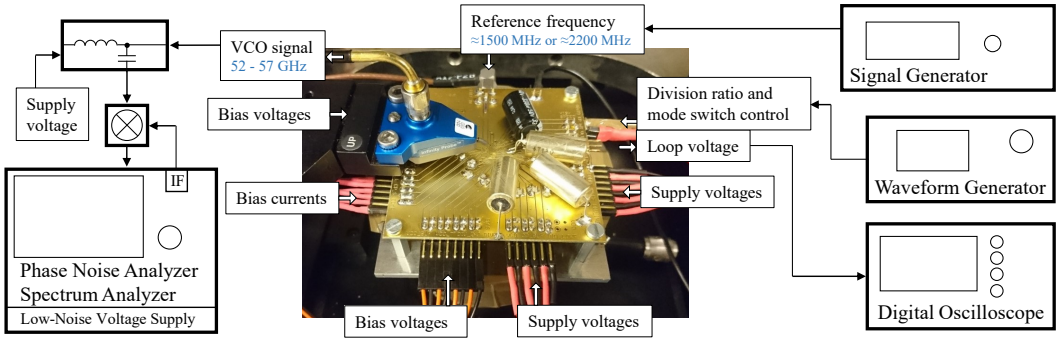


Fig. 14. The PLL measurement setup.

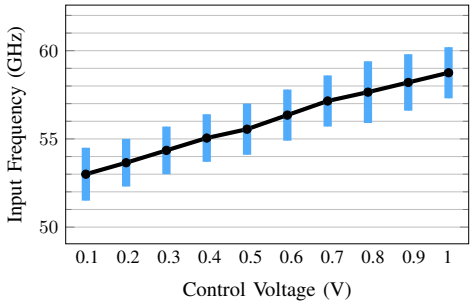


Fig. 15. Measured locking range at a power consumption of 2.5 mW for the double injection version of the ILFD.

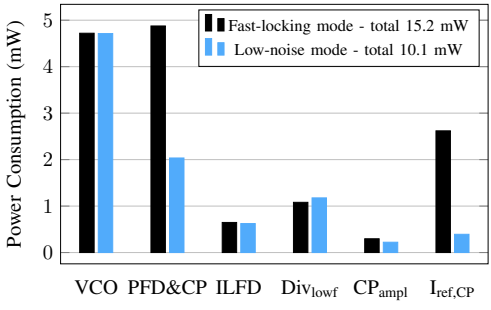


Fig. 16. Measured power consumption of each contributor in low-noise and fast-locking mode.

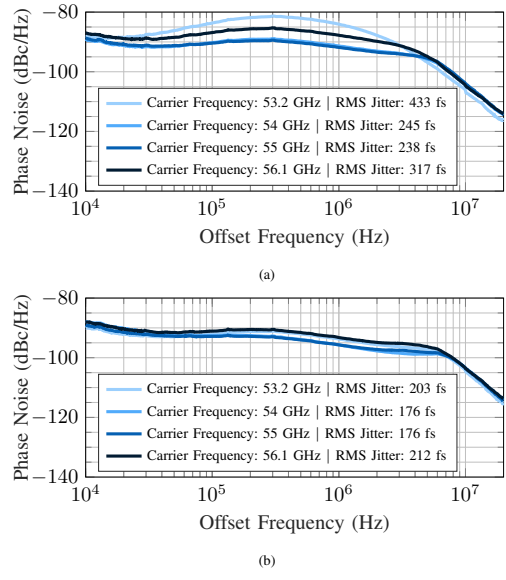


Fig. 17. Measured phase noise of the PLL in (a) fast-locking mode and (b) low-noise mode.

to a locked state. When $Sel = 0$, the total division ratio is equal to 24, and if the loop is then in an unlocked state, the targeted frequency is below the VCO tuning range and the control voltage is at its minimum. When $Sel = 1$, on the other hand, the total division ratio is equal to 36, and if then in the unlocked state the targeted frequency is above the VCO tuning range, and the control voltage is instead at its maximum. Another pulsed signal was used to control the PLL mode switch. In Fig. 21 the settling behaviour with the mode switch activated at different time delays is shown. When both pulsed signals switch at the same time, the settling behaviour will be that of the low-noise mode. When the mode switch signal is delayed, the settling instead starts in fast-locking mode, followed by a switch to low-noise mode. The estimated settling time in low-noise mode is about three times longer than the estimated settling time using fast-locking mode during the first part of the settling. The estimated maximum settling time using fast-locking of 3 μs was determined as the PLL settling time. The figure also shows that the switching between modes has minimal impact on the output frequency, and that the best time to switch from fast-locking to low-noise mode is when the frequency is close to stable. However, the measurements also show that since the switch can safely be made at any time, and that any time operating in fast-locking mode improves the settling time significantly, there is no need for complicated algorithms and feedback to control the mode switch mechanism.

The performance of the PLL is summarized in Table II.

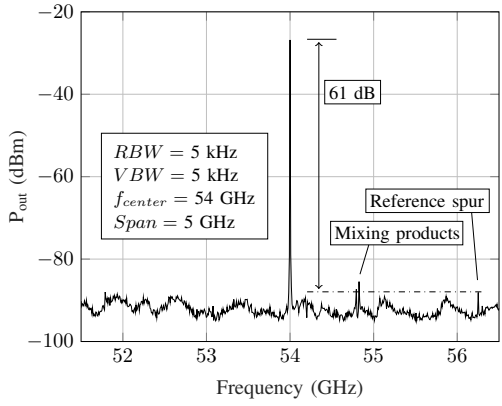


Fig. 18. Measured PLL output spectrum in low-noise mode, with a division ratio of 24. The mixing products and undulating noise floor are due to the harmonic mixer of the spectrum analyzer.

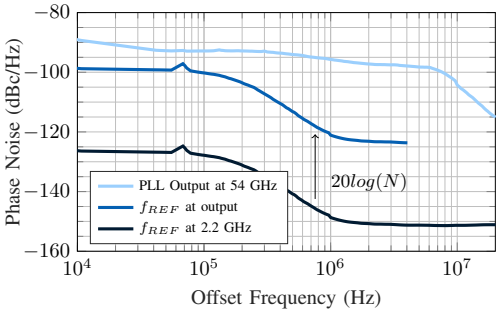


Fig. 19. Measured phase noise of f_{REF}, scaled at output with $20log(N)$, and the best-case measured PLL phase noise.

The PLL figure-of-merit ($\mathrm{FOM_{PLL}}$) is commonly used for wireless communication PLLs, and it is based on the theory in [35], where the phase noise figure-of-merit (FOM) for VCOs is extended to an entire PLL. Compared to state-of-the-art published mm-wave PLLs, the mode-switching PLL reported in this paper achieves comparable settling time, area and phase noise performance, but at much lower power consumption, which results in a state-of-the-art $\mathrm{FOM_{PLL}}$ of -245 dB for this frequency range. Even if the output frequency range is enough to cover the main intended use of the PLL and also enough to demonstrate the architecture, an increased range, attainable with small changes in the VCO, would make it useful for a wider range of applications.

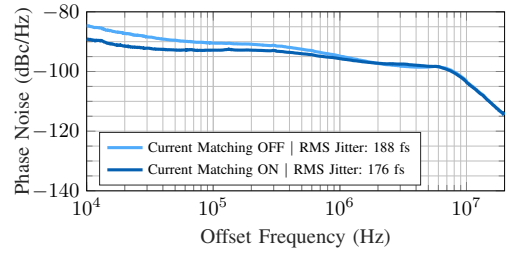
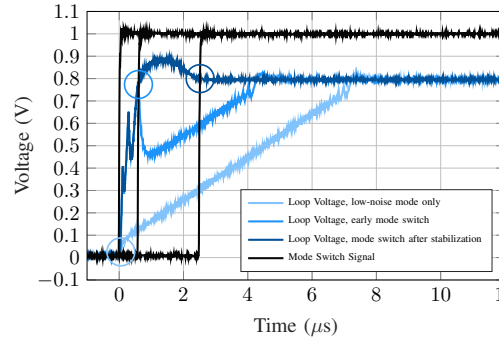
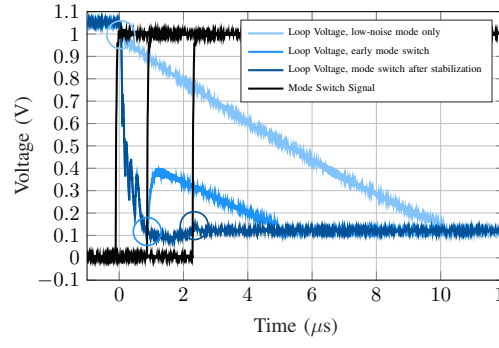


Fig. 20. Measured phase noise of the PLL at 55 GHz in low-noise mode, with the CP current matching ON and OFF.



(a)



(b)

Fig. 21. Measured loop control voltage during settling. Three different cases of timing switching from fast-locking to low-noise mode are shown. (a) Settling to 56.34 GHz. (b) Settling to 53.232 GHz.

V. Conclusion

A novel PLL for mm-wave frequency wireless transceivers is presented, that mitigates the problem of cycle slips during settling by switching between two modes of operation with the same small-signal, but different large-signal properties. Two key building blocks of the PLL include novel circuit techniques. The first is a double injection divide-by-3 circuit which increases the frequency lock range, allowing the power consumption of the mm-wave divider to be robustly scaled down to less than 0.8 mW. The second is the charge pump, which has a replica-based feedback loop to diminish the current mismatch due to channel length modulation, therefore reducing low-frequency PLL phase noise. Measurements show a PLL lock time of about 3 μs using the fast-settling mode during the first part of settling, while then operating in low-noise mode achieves a record low power consumption of 10 mW and a state-of-the-art $\mathrm{FOM_{PLL}}$ of -245 dB for PLLs in the 60 GHz range.

TABLE II
PLL PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART MM-WAVE CMOS PLLS

Ref.	CMOS Tech. (nm)	Type	Ref. Freq. (MHz)	Power (mW)	Phase Noise @1MHz (dBc/Hz)	RMS Jitter (fs)	Lock Time (μs)	Center Freq. (GHz)	Freq. Range (%)	Core Area (mm2)	Ref. Spur (dBc)	$\mathrm{FOM_{PLL}}$[1] (dB)
[36]	65	Fund. LO	135	24.6	-89.9 to -91.5	-	> 5[2]	63.1	16.5	0.192	-54.5	-
[37]	40	Subsampling PLL	40	42	-88 to -92	200 to 350	-	58.5	16.2	0.16	-40	-207.7 to -202.9
[38][3]	65	Time-to-digital converter all digital PLL	100	48	-90	590.2	3	60	11.7	0.48	-74	-228
[39]	28	Fund. LO, frac. N 24 GHz PLL + 60 GHz QILO	27	107	-93.8 to -96.5	900[2]	-	59.4	18.2	0.294	-	-221
[40]	65	All digital PLL	100	46	-88 to -94.5	223 to 302.5	< 1[4]	58	27	0.45	-48.3 /-52.2[5]	-236 to -233
[41]	65	Subsampling 20 GHz PLL + 60 GHz QILO	36 or 40	32	-92[2]	290	-	60.4	16	1.08[6]	-73	-236
This work	28	Fund. LO, integer N	2290	10	-93 to -96	176 to 212	3	54.5	5.3	0.19[7]	-61	-245 to -243

1) $FOM = 10log((\frac{\sigma_{t,PLL}}{1s})^2 \frac{P_{PLL}}{1mW})$, defined in [35] 2) Estimated from graph. 3) Frequency generation part only. 4) Simulated. 5) Fractional spur. 6) Including pads. 7) Including estimated area for implementation if the externally added loop filter is placed on-chip instead.

ACKNOWLEDGMENT

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Paper VI

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A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CM

Therese Forsberg, Henrik Sjöland, and Markus Törmänen, "A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CM," in *2018 IEEE Nordic Circuits and Systems Conference (NORCAS)*, Tallinn, Estonia, Oct 2018, 4 pages.

A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CMOS

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***Abstract* — A mm-wave divide-by-two circuit with high injection efficiency, implemented in a 28-nm fully-depleted silicon-on-insulator (FD-SOI) CMOS process is demonstrated stand-alone, as well as using an on-chip voltage controlled oscillator (VCO) as the input signal source. Measurements show that the divider has a 30.1 % tuning range centered at an output frequency of 24 GHz, at an input signal power of -1.5 dBm, and a power consumption of 4.3 mW from a 0.9 V supply. The VCO and divider combination has a tuning range of 10.2 %, centered at an output frequency of 30.2 GHz, at a total power consumption of 6.3 mW, and an output phase noise of -111 dBc/Hz at 10 MHz offset. The active area of the divider is 0.032 mm^2 and of the divider and VCO combination 0.043 mm^2.**

Index Terms — CMOS analog integrated circuits, mm-wave circuits, frequency dividers, injection-locked frequency dividers.

I. Introduction

To meet an ever-increasing demand for higher data rates in wireless communication, wider bandwidths must be employed. As the spectrum below 6 GHz gets increasingly crowded, the required bandwidths will instead be found at mm-wave frequencies. The unlicensed band at 60 GHz that offers 7 GHz of bandwidth has thus received a lot of interest. Several standards, such as the IEEE 802.11ad for wireless local area networks, are already in place in this band [1]. Another interesting mm-wave band is around 30 GHz where some of the upcoming 5G NR bands will be situated.

Transceivers that target these standards, which are intended for battery-operated consumer electronics, will have to be both low-power and low-cost. To achieve a high integration level and a reduced cost, it is desirable to implement such transceivers using down-scaled CMOS processes.

A key part of any wireless transceiver is the local oscillator signal generation, which usually includes a phase-locked loop (PLL). A common PLL architecture is shown in Fig. 1 [2], where the phase frequency detector (PFD), charge pump (CP), low-pass filter, and most of the divider chain (N) operate at relatively low frequencies, whereas the voltage controlled oscillator (VCO) and the first divider stage in the chain operate at high frequencies. For mm-wave PLLs, the design of the VCO and first frequency divider stage thus requires careful consideration. Divider circuit techniques used at lower frequencies do not suffice, and the most popular solution is to use an injection-locked frequency divider (ILFD). A drawback is that the ILFD free-running frequency must be tuned for lock to occur, and without lock a clean frequency divided output signal will not be provided. Hence, there are strong incentives to try to increase the lock range of the divider, to ensure that the whole VCO frequency tuning range is covered, also in the presence of process variations. Successful efforts to implement divide-by-two ILFDs with wider locking ranges have lately been reported [3]-[8], as well as ILFDs with higher division ratios [9],[10]. However, using a division by two in the first frequency divider stage of a 60 GHz PLL means that signals are also generated at 30 GHz. Local oscillator signals for two important mm-wave frequency bands can thus be generated.

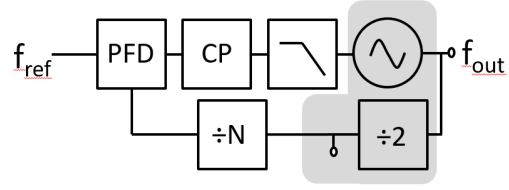

Fig. 1. PLL architecture, where the scope of this work is the mm-wave parts highlighted in gray.

In this work, a CMOS divide-by-two circuit with efficient injection and a wide tuning range is presented, along with a version of the divider that receives its input from an on-chip VCO. The objective has been to create efficient mm-wave circuits for use in a 60 GHz PLL.

II. Theory and Design

An ILFD is a tuned self-oscillating circuit, which is forced by injection locking to oscillate at the desired frequency. A tuned circuit that is well-known for its ease of implementation is a differential oscillator, which consists of cross-coupled transistor pair, with the DC current controlled by a current source, and a self-oscillation frequency determined by the drain inductance and capacitance. The schematic of the VCO together with the injection-locked divide-by-two circuit, which are both based on this architecture, is shown in Fig. 2.

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The efficiency of the injection mechanism directly affects the tuning range. An upper bound of the output-related frequency locking range for an ILFD is expressed by [11],[12] as

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}} \quad (1)$$

where ω_0 is the self-resonance frequency, Q the quality factor of the divider LC tank, I_{osc} is the amplitude of the current going to the tank while free-running, and I_{inj} is the amplitude of the current injected to the tank. A conventional solution is to inject a signal at the second harmonic frequency at the source terminal of the current source transistor, $V_{b,div}$. However, a more efficient method can be used, called direct injection [13],[14], where the signal is injected at the gate of an injection transistor connected between the differential outputs of the ILFD. This method is used, see Fig. 2, and the signal is also differentially fed to the ILFD, hence utilizing the full signal swing of the differential VCO. The injection transistors can be modeled as mixers, and to maximize their conversion gain the DC gate voltages are adjusted to about a threshold voltage above VDD for the NMOS, and about a threshold below VDD for the PMOS transistor. When dimensioning these transistors, the trade-off between locking range and power consumption in direct-injection ILFDs must be considered. There is an optimal size of the devices where they are large enough to provide a substantial injection current, but small enough not to significantly increase the load of the tank and thereby the power consumption [8]. For the stand-alone ILFD, an external differential local oscillator signal is fed to the circuit at point A, defined in Fig. 2.

The ILFD tank consists of a differential inductor, and a varactor, to maximize the frequency locking range, implemented with MOS devices. The inductor was implemented in the top metal layer of the process and simulated in ADS Momentum. The simulated inductance value for the stand-alone ILFD inductor was 450 pH. Due limited available input power to the ILFD at high frequencies in the measurement setup, the frequency range of the stand-alone ILFD was centered at 48 GHz. Also for measurement purposes, the output signals of the ILFD were routed to open drain buffers with approximately 5 dBm of output power.

To further verify the ILFD design, and to get one step closer to a PLL, the ILFD was as previously mentioned also combined with a VCO. The VCO provides the differential input to the ILFD, see Fig. 2, and it has been previously designed and verified [15]. It utilizes current source node filtering at twice the self-resonance frequency for improved phase noise performance, and it has tuning range of about 11 % centered at 64 GHz. Simulations show that when using the differential output of the VCO, the input signal to the ILFD is strong enough to make its lock range cover the VCO tuning range without changing its varactor setting. When combined with the VCO, the ILFD self-resonance is re-tuned to fit with the VCO frequency by reducing its tank inductance from 450 to 300 pH.

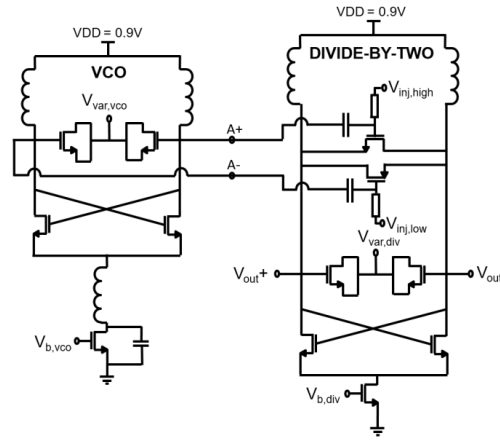

Fig. 2. Schematic of the VCO and divide-by-two circuit. For the stand-alone divider, the external differential signal to be divided is injected at points A+ and A-.

III. Measurement Results

The stand-alone ILFD, as well as the VCO and ILFD combination, were implemented in the STMicroelectronics 28-nm ultra-thin body and buried oxide fully-depleted silicon-on-insulator (UTBB FD-SOI) CMOS technology with 10 metal layers. The chip microphotograph is shown in Fig. 3. The chips were mounted on printed circuit boards, and the bias and supply voltages were provided through bond wires. The mm-wave input signals to the stand-alone divider were provided by a Rohde&Schwarz ZVA 67 network analyzer, through an Infinity i67 SGS microprobe from Cascade Microtech. The single-ended output signals from the divider buffers were also probed on-chip using an Infinity i40 GSG microprobe from Cascade Microtech, and measured using a Rohde&Schwarz FSU50 spectrum analyzer. For the phase noise measurements, the signal was down-converted using an external mixer driven by a Keysight E8257D PSG analog signal generator. It was then amplified and sent to an Aeroflex EuropTest PN9000 phase-noise measurement system.

Both circuits were measured with a 0.9 V supply. The bias was set for a 4.3 mW power consumption of the divider, which yields a wide frequency locking range, see Fig. 4. The divider locking range is 30.1 %, with an input signal power of -1.5 dBm. Even at a reduced power consumption of 1.8 mW, the divider locking range at that input power level is still 13.2 GHz, corresponding to 26.7 %. Fig. 5 shows the frequency locking range of the stand-alone divider at different varactor settings. As can be seen the width of the locking range is maintained when tuning its center frequency. The measured sensitivity of the divider is plotted in Fig. 6. As the maximum input signal power to the divider is limited by the measurement instruments, a higher input power than 0 dBm could only be generated at the lower frequencies of the locking range.

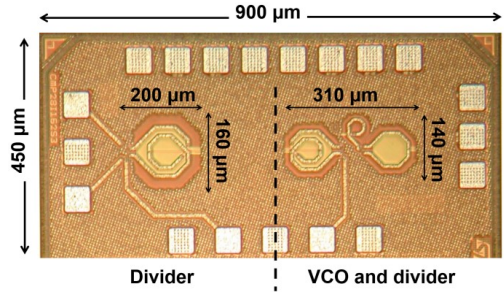

Fig. 3. Chip microphotograph.

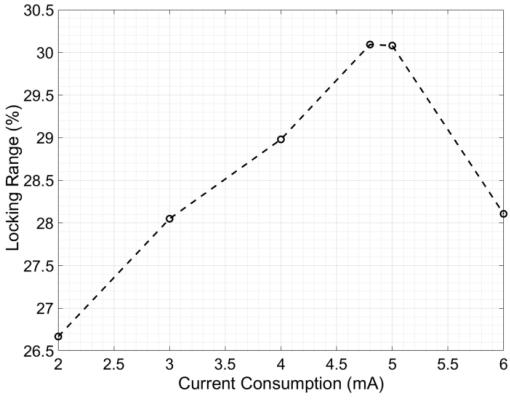

Fig. 4. Measured locking range of the stand-alone ILFD vs. varactor setting, with -1.5 dBm input signal power.

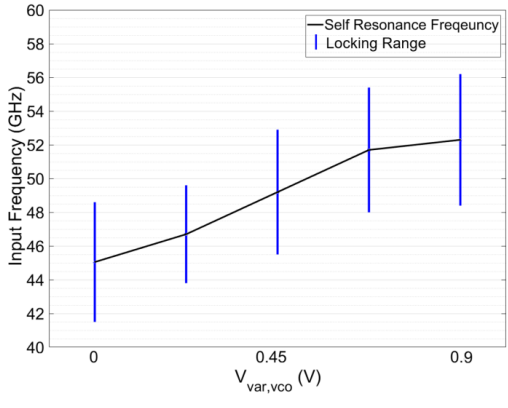

Fig. 5. Measured locking range of the stand-alone ILFD vs. varactor voltage.

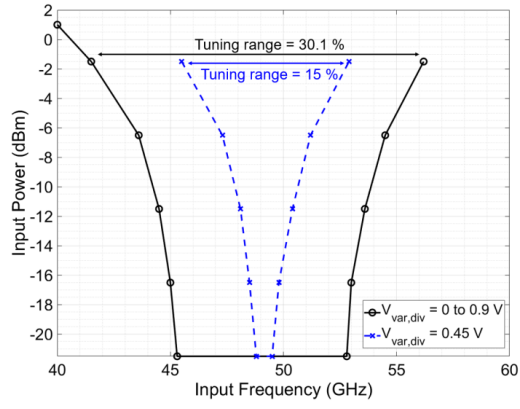

Fig. 6. The measured sensitivity of the divider, using the full divider varactor voltage range, and when it is fixed to VDD/2 (0.45V).

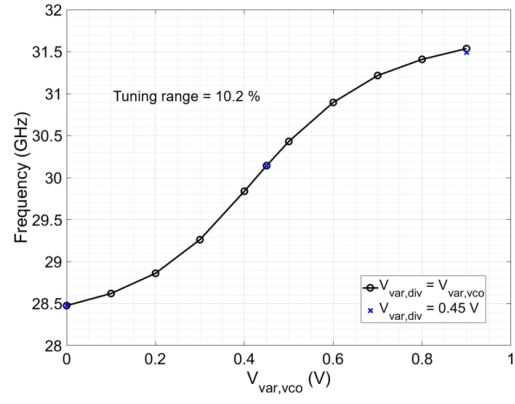

Fig. 7. Measured frequency tuning characteristic of VCO and divider combination.

Assuming that the sensitivity is symmetrical, which is supported by simulations, the estimated locking range at 0 dBm input power can be calculated to 35 %. The locking range for fixed varactor voltage is also shown in Fig. 6, yielding a 15% tuning range at -1.5dBm.

When measuring the VCO and divider combination, the power consumption of the divider was kept at 4.3 mW, and the total power consumption for the combination was 6.3 mW. The frequency tuning characteristics of the VCO and divider combination is shown in Fig. 7. Complying with simulations and measurements of the stand-alone divider, the entire tuning range of the VCO was covered by a single divider varactor setting. The best measured phase noise from the combined

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO RECENTLY PUBLISHED MM-WAVE DIVIDE-BY-TWO ILFDS

Ref.	This work	[3]	[4]	[5]	[6]	[7]	[8]
Tech. (nm CMOS)	28	65	65	65	90	90	65
Supply Voltage (V)	0.9	0.8	0.9	0.75	1.2	0.8	0.8
Pin (dBm)	-1.5	0	0	0	0	5	0
Frequency (GHz)	48.8	62.8	42.25	63.9	58.8	55	66.4
Tuning Range (%)	30.1	29	53.2	9.7	20.5	34.9	39.2
Power Consumption (mW)	4.3	1.9	9	6.3	8.6	0.8	2.9
Area (mm^2)	0.032	0.023	0.2	0.058	0.083	0.385	0.126

circuit was at the lowest varactor setting for both the VCO and the divider, where the phase noise was -111 dBc/Hz at an offset of 10 MHz from the 28.5 GHz carrier.

The measured performance of the divider is compared to other recently published state-of-the-art mm-wave divide-by-two CMOS circuits in Table I. As can be seen the design demonstrated in this work achieves a competitive combination of wide frequency range, low power consumption and input signal power, and small chip area.

IV. CONCLUSION

This paper presents two measured mm-wave designs aimed for PLL integration. The first is a differential direct-injection ILFD circuit dividing by 2, and the other is a re-tuned version of the same ILFD, combined with a 60 GHz VCO. Both designs are implemented on the same die in 28-nm UTBB FD-SOI CMOS technology. At an input signal power of -1.5 dBm the ILFD achieves a wide tuning range of 30.1 %, at a competitive power consumption 4.3 mW, while occupying an active chip area of just 0.032 mm^2. Even using a single varactor setting in the ILFD, it has wide enough locking range to safely cover the full 10.2 % tuning range of the VCO.

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