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Abstract—Two different frequency doubling power amplifiers have been measured, one with differential and one with single-ended input, both with single-ended output at 60 GHz. The amplifiers have been implemented in a 1p8M 130-nm CMOS process. The resonant nodes are tuned to 30 GHz or 60 GHz using on-chip transmission lines, which have been simulated in ADS and Momentum.

The measured input impedance of the single-ended PA is high at 250 Ω, and the differential input is similar, making the PA a suitable load for an oscillator in a fully integrated transmitter. The single-ended and differential input PA delivers 1 dBm and 3 dBm, respectively, of measured saturated output power to 50 Ω, both with a drain efficiency of 8%.

I. INTRODUCTION

The drive for gigabit per second transmission rates in coming WLAN and WPAN applications forces the design of new systems with wider bandwidth. The Federal Communications Commission (FCC) has opened a 7 GHz wide spectrum from 3-10 GHz for UWB communications, and a 7 GHz wide unlicensed band at 57-64 GHz [1] is also available. Both these spectrum allocations will permit communications at several gigabits per second. Also in Japan and Europe [2] frequency bands at 60 GHz are opened for unlicensed WLAN communications, providing a 5 GHz world wide overlap.

To meet the stringent cost requirements of the consumer electronics market, the 60 GHz transceivers must be realized in low cost CMOS technology [3], [4]. To use CMOS at this high frequency is extremely challenging, both in receiver and transmitter. In this work we have therefore realized a frequency doubling Power Amplifier (PA). This will reduce the difficulties in designing the rest of the transmitter, which can then operate at 30 GHz instead of 60 GHz. The power consumption and the losses are then reduced. A harmonic amplifier also makes the frequency planning easier, since the Voltage Controlled Oscillator (VCO) and PA output signal are separated in frequency, reducing the risk of oscillator pulling. Furthermore, at 30 GHz center frequency the achievable tuning range of the VCO increases. The tuning range is limited at high frequencies by the performance of the varactors, and The quality factor of the varactor is approximately doubled at 30 GHz compared to 60 GHz [5].

II. CIRCUIT TOPOLOGIES

To show the concept of 60 GHz CMOS frequency doubling power amplifiers, two different frequency doubling PA topolo-

gies have been investigated, Fig. 1. In cases where higher output power and more gain is needed, more stages can be used [6], [7]. Both amplifiers convert a 30 GHz input signal to a 60 GHz output. The frequency doubling takes place in the first stage, and the drain node of M1 (and M3) is tuned to 60 GHz, passing the second harmonic and suppressing the 30 GHz fundamental. The second stage is a 60 GHz common source amplifier. At the output of the second stage
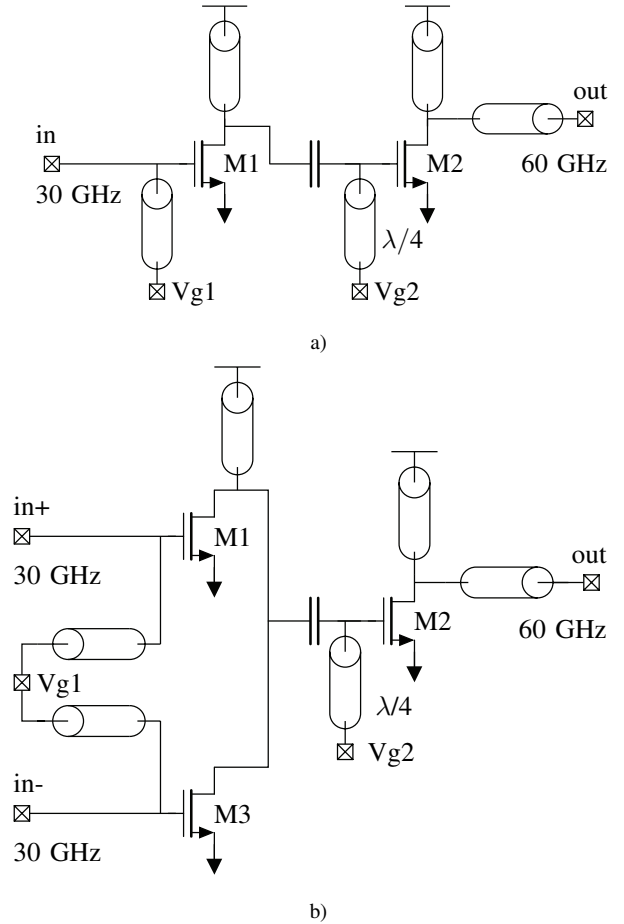

Fig. 1. The frequency doubling power amplifier topologies investigated. a) Single-ended input b) Differential input

an L-match is used to transform the 50 Ω load to a higher impedance seen by the PA. The L-match consists of the drain-

bulk capacitance of M2 and the transmission line from M2 to the output pad. The input of the amplifiers are high-ohmic, making the PAs suitable to proceed the oscillator in a fully integrated transmitter.

The first stage of the differential input amplifier [8] (Fig. 1(b)) conducts at both input polarities, contributing to a larger effective g_m of that stage compared to its single-ended counterpart. The drain-bulk capacitance, however, is correspondingly larger, making the first stage gain approximately equal for the two topologies. The fundamental tone at the drains of M1 and M3 is 180° out of phase, but the second harmonic is in phase. Combining the drains then results in a signal with a suppressed fundamental and a strong tone at twice the frequency of the input. The suppression of the fundamental makes LO leakage through the power amplifier less of a problem, see Table I. Furthermore, not just the fundamental, but all odd harmonics are rejected [8]. The differential input amplifier is also suitable for on-chip implementation, where differential signal schemes dominate thanks to their high common mode noise/interference suppression. In addition to that, the power amplifier produces a single-ended output, eliminating the need of an output balun.

A. Transmission Lines

All the resonant nodes are tuned by Transmission Lines (TLs) terminated by short circuits. A model of the silicon back end of line (metal stack) has been used to simulate the TLs in Advanced Design System (ADS) [9]. The 2.0 μm thick top metal layer was used for the TLs, and metal 1 for ground plane. The width of the TLs was chosen to give a 50 Ω characteristic impedance, which also resulted in a high Q-value, see [10] and [6] for a more thorough investigation of TLs in silicon processes.

The ADS and Momentum simulation results have been compared to the component *tline3* from the library *rfExamples* in Cadence (Fig. 2). The inductance, series resistance, and Q-value have been plotted as a function of TL length at 60 GHz. The Cadence component agrees well with ADS and Momentum for the inductance, but overestimates the losses by 30% for short TLs. Despite this discrepancy *tline3* has been used to simulate the amplifiers, leading to a somewhat pessimistic gain, but still a correct resonance frequency. The Q-values and inductances are in the same range as in [6], [10].

B. Layout Considerations

Metal-Insulator-Metal (MIM) capacitors were used to provide a good AC-ground at the end of each TL. An array of small, high Q-value, capacitors with a total capacitance of 1 pF was placed closest to the TL, and further out larger capacitors were placed. In total more than 11 pF was used for each AC-ground, see the chip microphotographs, Fig. 3 (a) and (b). Under each TL a 20 μm wide metal 1 return path was placed, minimizing current loops in the ground plane. The ground plane was also made in metal 1, and put across the entire chip to provide a low-impedance ground.
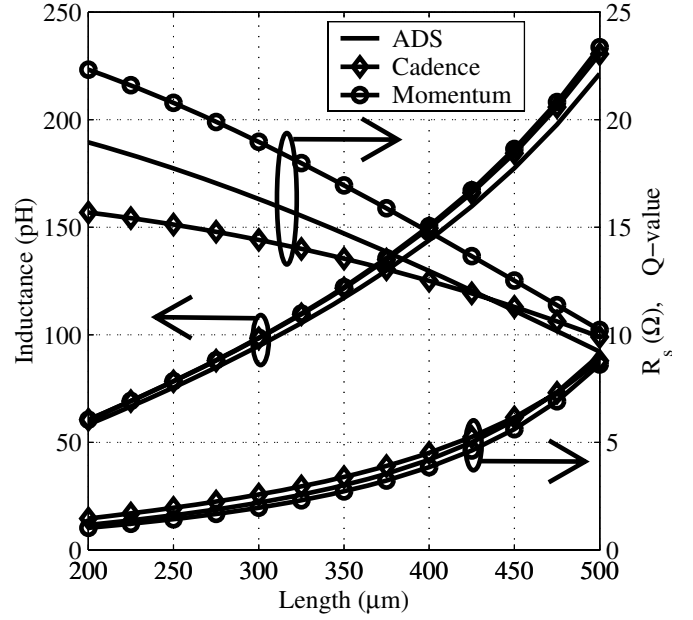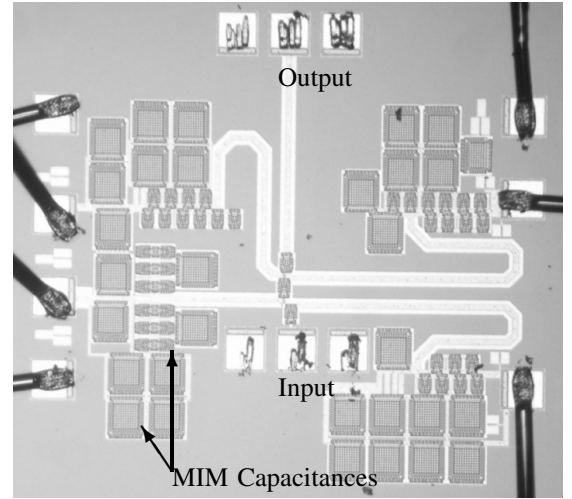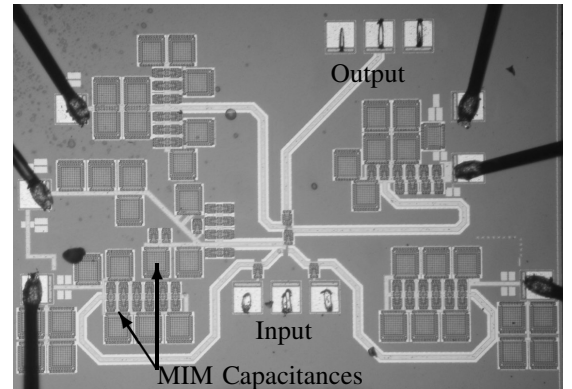

Fig. 2. Comparison of transmission line simulation in ADS, Momentum, and Cadence at 60 GHz, width 10.75 μm

a)

b)

Fig. 3. Chip microphotographs. a) Single-ended input b) Differential input

To verify that the decoupling was sufficient, simulations including parasitics and bond wires were performed. A π-model consisting of 3 nH series inductance with Q=10 and 50 fF shunting capacitances was used for the bond wires. The circuits showed no stability problems, indicating sufficient decoupling.

III. MEASUREMENT RESULTS

The two amplifiers were measured in a probe station using Ground-Signal-Ground (GSG) and Signal-Ground-Signal (SGS) RF probes[1]. The DC pads were bonded to a PCB providing supply and bias voltages.

Using a network analyzer, S11 of the Single-ended Input (SI) PA was measured. It was then converted to Z11, input impedance, shown in Fig. 4 together with simulated impedance for both single-ended and Differential Input (DI). As can be seen the measured input resonates at 32 GHz, with a real valued input impedance of 210 Ω to 250 Ω at resonance. The measured real valued input impedance is 80% of the simulated one. The differential input impedance is therefore estimated to be 275 Ω, also that 80% of the simulated value[2].
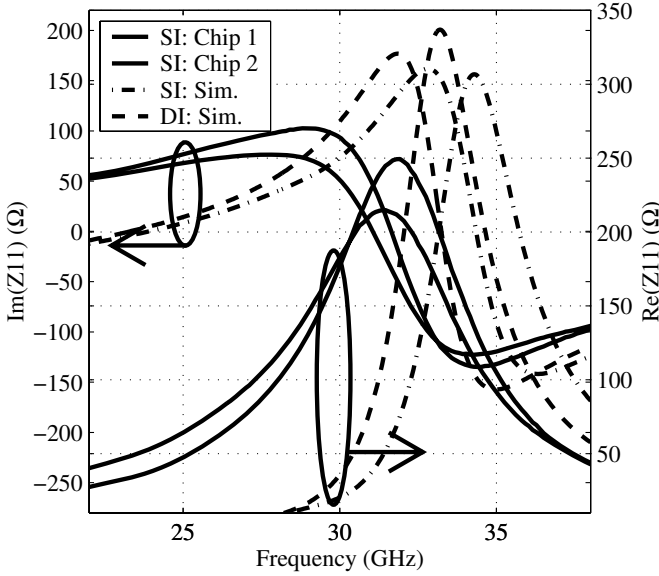

Fig. 4. Input impedance, Z11. SI PA: measured and simulated, DI PA: simulated

The output power versus input voltage was also measured, Fig. 5, achieving 1.2 dBm saturated output power with a drain efficiency of 7.8% for the SI PA. Deriving the input voltage from the above assumption about the input impedance, the output power versus input voltage for the DI PA was also plotted in Fig. 5. It achieves 3.1 dBm saturated output power

with a drain efficiency of 8.2%. As can be seen in the figure, the DI PA reaches its saturated output power for lower input amplitudes, making it easier to drive for an oscillator.
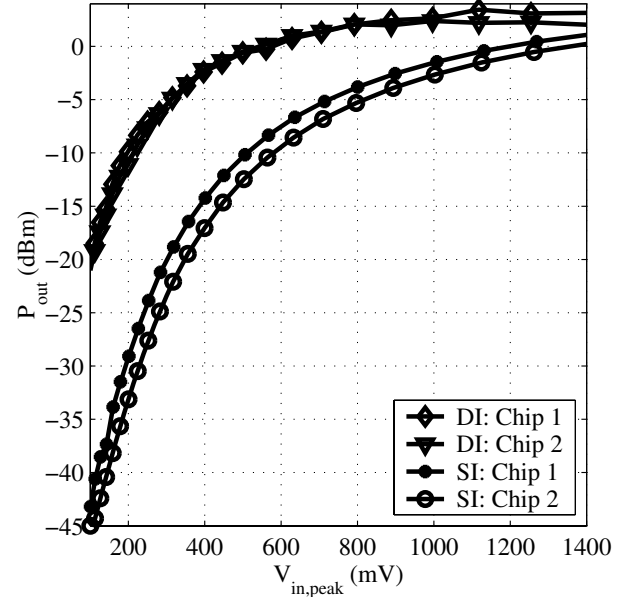

Fig. 5. Output power versus input voltage

The fundamental frequency suppression versus input signal phase difference was measured for the DI PA, using two frequency locked signal generators, showing a good agreement with simulated results, Fig. 6. The measured maximum suppression is 37 dB and it is achieved with differential input. The measured fundamental frequency suppression for the SI PA is larger than 22 dB over the full frequency range.
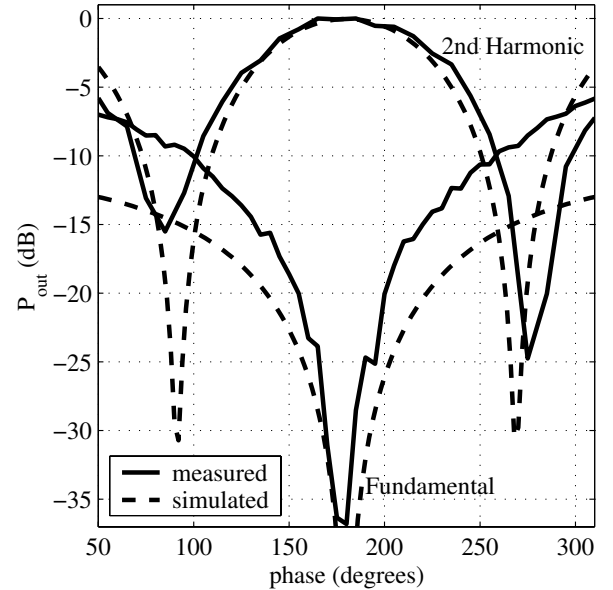
Fig. 6. Fundamental tone suppression for the DI PA

[1]Spectrum analyzer: Rohde&Schwartz FSU 20Hz-50GHz, Harmonic Mixer: Rohde&Schwartz FS-Z75 50-75 GHz, Signal generator: Agilent Technologies E8257D 250kHz-40GHz, Probes: Cascade Infinity and Picoprobe Dual Microwave Probe, VNA: Agilent Technologies E8361A 10MHz-67GHz, Calibration: Cascade Microtech Impedance Standard Substrate and Wincal

[2]The differential input PA could not be measured with the VNA due to calibration difficulties.

TABLE I
COMPARISON BETWEEN THIS WORK AND TWO REFERENCES IN CMOS AT 60 GHz

	SI sim.	SI meas.	DI sim.	DI meas.	[6]	[7]
V_{DD} (V)	1.3	1.3	1.2	1.2	1.5	1.5
I_{DC} (mA)	20.5	13.1	27.7	15.7	36	26.5
Max. P_{out} (dBm)	4.0	1.2	5.0	3.1	—	9.3
Drain efficiency (%)	8.6	7.8	9.5	8.3	3^3	21.4
Power Gain (dB)	-1.1	-3.9	0.4	-0.5	12	5.2
3-dB Bandwidth (GHz)	6.0	12.4	6.8	—	14	13
Fundamental Tone Suppression (dB)	13.8	22.5	—	37	—	—
Number of stages @ 60 GHz	1	1	1	1	3	3
Frequency doubling	yes	yes	yes	yes	no	no
Total Area (mm^2)	—	0.67×0.77	—	0.91×1.38	1.3×1.0	0.35×0.43
Process node (nm)	130	130	130	130	130	90

[3] Authors calculation from P_{DC} and OCP1dB.

A. Summary

Table I is a summary of the simulated and measured results compared to two references [6], [7], both at 60 GHz and in CMOS, but not frequency converting. The authors would like to make a comment about the power gain. In simulations the first stage has a conversion loss of about 4 dB, which should be added to the overall gain when comparing to non frequency converting PAs. Other published 60 GHz power amplifiers in CMOS show about 2-4 dB gain per stage [7], [11], [12], which our amplifiers also have in the last stage. For higher gain one or two more stages at 30 GHz or 60 GHz can be added to the PA.

IV. CONCLUSION

Two 60 GHz frequency doubling power amplifiers in 130-nm CMOS have been presented, one with single-ended and one with differential input. The frequency doubling allows the rest of the transmitter to operate at 30 GHz instead of 60 GHz, which eases the design and lowers its power consumption.

The amplifiers use transistor non-linearity to perform the frequency doubling from 30 GHz to 60 GHz. The differential input amplifier makes use of the fact that the second harmonics at the transistor drains are in phase, thus connecting the drains together (Fig. 1(b)) effectively produces a frequency doubling. A cancellation of the fundamental frequency and the odd harmonics is also achieved by this connection, reducing the feedthrough.

The SI PA shows a 3-dB bandwidth of 12 GHz, well covering the unlicensed frequency band at 57-64 GHz. The SI PA and DI PA reaches 1.2 dBm and 3.1 dBm of saturated output power, respectively, both with a drain efficiency of 8%.

V. ACKNOWLEDGMENT

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