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Semiconductor Nanowires: Epitaxy and Applications

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Semiconductor Nanowires: Epitaxy and Applications

Thomas Mårtensson

Doctoral Thesis

Solid State Physics
Faculty of Engineering
Lund University

Semiconductor Nanowires: Epitaxy and Applications

Doctoral Thesis
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LUND UNIVERSITY

Division of Solid State Physics
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Sweden 2008

Life is too important to be taken seriously.

— Oscar Wilde

Abstract

Semiconductor nanowires are nanoscale objects formed by bottom-up synthesis. In recent years their unique properties have been exploited in fields such as electronics, photonics, sensors and the life sciences.

In this work, the epitaxial growth of nanowires and their applications were studied. Metal-organic vapour phase epitaxy was used for nanowire growth, and both particle-assisted and particle-free nanowire growth were employed.

The first specific contribution of this work to nanowire synthesis is heteroepitaxial growth of III-V nanowires on silicon substrates. This may enable direct band gap materials for optoelectronic devices, as well as high-mobility, low-contact resistance materials for electronics, to be integrated directly on the Si platform. Furthermore, gold-free nanowire synthesis on Si was demonstrated, which offers an advantage in terms of compatibility with established Si processing.

The second specific contribution to nanowire growth is controlled synthesis by employing lithography. This combination of established "top-down" planar processing, and "bottom-up" nanowire growth, enables deterministic synthesis with individual nanowire site control. The process was first demonstrated with electron beam lithography and later extended to nanoimprint lithography, which is a parallel, high-throughput method, suitable for commercial volumes.

Nanowire applications were demonstrated by three examples:

(i) Vertical light-emitting diodes (LEDs) based on GaAs/InGaP core/shell nanowires, epitaxially grown on GaP and Si substrates. LED functionality was established on both kinds of substrates, and the devices were evaluated in terms of temperature-dependent photoluminescence and electroluminescence. This provided a direct demonstration of light-emitting devices on Si made possible by heteroepitaxial III-V nanowire growth on Si.

(ii) A single-electron transistor constructed from a heterostructured nanowire with an InAs island sandwiched between two InP barriers. The narrow diameter of the nanowire provides the lateral confinement, and the tunnel barrier resistances are tunable by varying the InP barrier thickness. The island was ≈ 100 nm long with a

diameter of $\approx$ 55 nm. Coulomb oscillations and Coulomb blockade with a charging energy of approximately 4 meV were observed.

(iii) Sensory nerve cell interactions with nanowires. Substrates covered with 2.5 μm long and 50 nm diameter nanowires supported cell adhesion and axonal outgrowth. The cells interacted closely with the nanostructures, and viable cells penetrated by wires were observed, as well as wire bending due to forces exerted by the cells.

Preface

This thesis is the result of postgraduate studies at the Department of Physics at Lund University during the period $2003 - 2008$. I joined the division of Solid State Physics just after some pioneering work had been done on nanowire growth and nanowire heterostructures. Thus, although I was not among the very first, I still had the privilege to join a leading group early in a in a rapidly expanding field, namely semiconductor nanowires. I have also been privileged to have taken part in some of the first efforts to commercialize nanowire technology. This has been both sobering, as I realised the tremendous amount of work between a scientific discovery and a final product, as well as highly inspiring, as I was able to to see what a focused team can achieve.

The main topic of the thesis is epitaxy. Epitaxy is difficult, and although I and my fellow workers always set up well-thought-out experiments, the results were a mixture of success and (often) total failure. Perhaps this only reflects the beauty of the subject; we try to gain knowledge in order to control and predict, but we are constantly surprised by nature and forced to revise our views.

The second topic of the thesis is nanowire applications. This combination of applications and epitaxy has been thrilling, and it has been important for me to "see the big picture" and to be interdisciplinary. In this sense, nanowires and nanotechnology have been a way of satiating my curiosity in physics.

It is my hope that this work has made a small contribution to the field (there is much left to do indeed). In any event, I enjoyed doing it.

<div align="right">

THOMAS MÅRTENSSON
Lund, August 2008

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Acknowledgements

Conducting research for a doctorate is a fairly lengthy process, and you quickly come to realise that you can achieve very little alone. Teamwork is crucial, and over the years you become indebted to many people. These people are far to many to be listed here, and I can only say — thank you all. Nonetheless, I would like to give my special thanks to a few people.

First, I would like to thank my supervisors, Prof. Lars Samuelson, Prof. emeritus Werner Seifert, Dr. Jonas Ohlsson and Dr. Anders Mikkelsen. Lars Samuelson has been my principal supervisor and a never-ending source of inspiration and scientific ideas. From the very first day he treated me as an equal. At times, it created great stress to reach those standards, but in the end helped me develop tremendously. Werner Seifert taught me epitaxy, and for the first three years, he was an almost daily source of knowledge, practical know-how, valuable discussions and humour. He was also the head of the epitaxy group, and I and many others benefited from his leadership and long experience in epitaxy. Jonas Ohlsson was my Master's dissertation advisor and has continued to play a central role as supervisor and, for the last two years, as a colleague during my industrial endeavours at QuNano AB. Apart from his scientific contribution, I would also like to thank him for being a person of great humanity and passion. Anders Mikkelsen was my supervisor during the later half of my studies. Surface science became a major part of my studies and his contribution was crucial. In the busy world of academia, I admire his ability to always find time for me; I am indebted to him for much good advice and valuable discussions. (Hongqi Xu, I never got around to doing that photonic crystal. If I had, I am confident that I would have enjoyed great support and supervision from you.)

Before I leave my supervisors, I would also like to extend my gratitude the senior PhD students who acted as mentors when I began my PhD studies. Among those I count Ann Persson, Magnus Borgström, Claes Thelander and Mikael Björk.

Most of my time was spent in the lab doing epitaxy, and without the help of talented and friendly colleagues, things would have taken twice the time (or not have been possible at all), and would only have been half as fun. Among the people

I collaborated with in the epitaxy lab are Kimberly Dick Thelander, Philippe Caroff, Niklas Sköld, Brent Wacaser, Linus Fröberg, Patrik Svensson, Bernhard Mandl, Vilma Zela, Jonas Johansson and Prof. Knut Deppert. Being part of this group is what really made this thesis possible. Martin Karlsson and Zsolt Geretovszky are acknowledged for producing the aerosol particles I needed for nanowire growth.

To become really interesting, epitaxy usually has to be married with other disciplines, such as advanced characterization, processing, device design or physics. I had the benefit of collaborating with skilled people: Patric Carlberg is acknowledged for performing the nanoimprint lithography as well as for a enjoyable and fruitful cooperation, Johanna Trägårdh and Christina Larsson are acknowledged for their optical measurements, and Emelie Hilner is acknowledged for her work in scanning tunnelling microscopy. High-quality transmission electron microscopy is hard to come by, and Anders Gustafsson, Magnus Larsson and Jakob Wagner are acknowledged for their work.

I would like to thank Carl Rehnstedt, Claes Thelander and Prof. Lars-Erik Wernersson for allowing me to take (a small) part in the nanowire field effect transistor project.

I also made a short excursion into the bioworld during my studies, and Waldemar Hällström and Christelle Prinz are acknowledged for a good collaboration as well as for teaching me virtually all I know about cells (which is still fairly limited).

I also enjoyed cooperation with other universities, and especially Kristian Mølhave and Christian Kallesøe from the Technical University of Denmark (DTU), and Jiming Bao from Harvad University, are acknowledged for their collaboration.

The technical staff is the backbone of any lab, and I would like to express my gratitude to them. Especially, Ivan Maximov, Lena Timby and Mariusz Graczyk are acknowledged for their direct contributions to this work. I would also like to thank my roommate Sören Jeppesen for technical support, and for many interesting conversations about science and the workings of the world.

I would like to express my gratitude to all the people at QuNano AB, where I have worked part-time during the final two years of my studies, with the aim of commercializing nanowire technology. It has been an interesting ride and it is my hope that it will continue to be so. My special thanks go to my colleagues in the epi-team: Zhaoxia Bi, Patrik Svensson, Giuliano Vescovi and Rafal Ciechonski.

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I would like to thank my parents and brother for their continuous support for whatever I have undertaken in life so far. You have always been a strong foun-

dation. Finally, I would like to thank my love Hanna for her endless support and love during this time. You are my role model.

List of Papers

This thesis is based on the following papers, which will be referred to in the text by their Roman numerals. The papers, together with short summaries and accounts of the author's contributions, are appended at the end of the thesis.

I. **Epitaxial III-V nanowires on silicon**
   T. Mårtensson, C. P. T. Svensson, B. A. Wacaser, M. W. Larsson,
   W. Seifert, K. Deppert, A. Gustafsson, L. R. Wallenberg
   and L. Samuelson
   Nano Letters **4**, 1987-1990 (2004) doi:10.1021/nl0487267

II. **Epitaxial growth of indium arsenide nanowires on silicon using nucleation templates formed by self-assembled organic coatings**
   T. Mårtensson, J. B. Wagner, E. Hilner, A. Mikkelsen, C. Thelander,
   J. Stangl, B. J. Ohlsson, A. Gustafsson, E. Lundgren, L. Samuelson
   and W. Seifert
   Advanced Materials **19**, 1801-1806 (2007) doi:10.1002/adma.200700285

III. **Fabrication of individually seeded nanowire arrays by vapour–liquid–solid growth**
   T. Mårtensson, M. Borgström, W. Seifert, B. J. Ohlsson
   and L. Samuelson
   Nanotechnology **14**, 1255-1258 (2003) doi:10.1088/0957-4484/14/12/004

IV. **Nanowire arrays defined by nanoimprint lithography**
   T. Mårtensson, P. Carlberg, M. Borgström, L. Montelius, W. Seifert
   and L. Samuelson
   Nano Letters **4**, 699-702 (2004) doi:10.1021/nl035100s

V. **Monolithic GaAs/InGaP nanowire light emitting diodes on silicon**
C. P. T. Svensson, T. Mårtensson, J. Trägårdh, C. Larsson, M. Rask, D. Hessman, L. Samuelson and J. Ohlsson
Nanotechnology **19**, 305201 (2008) 10.1088/0957-4484/19/30/305201

VI. **Single-electron transistors in heterostructure nanowires**
C. Thelander, T. Mårtensson, M. T. Björk, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg and L. Samuelson
Applied Physics Letters **83**, 2052-2054 (2003) doi:10.1063/1.1606889

VII. **Gallium phosphide nanowires as a substrate for cultured neurons**
W. Hällström, T. Mårtensson, C. Prinz, P. Gustavsson, L. Montelius, L. Samuelson and M. Kanje
Nano Letters **7**, 2960-2965 (2007) doi:10.1021/nl070728e

Papers Not Included in this Thesis

I contributed to the following papers which are not included due to overlapping contents, or because they are beyond the scope of this thesis. They are listed in chronological order.

viii.
Synthesis of branched 'nanotrees' by controlled seeding of multiple branching events
K. A. Dick, K. Deppert, M. W. Larsson, T. Mårtensson, W. Seifert, L. R. Wallenberg and L. Samuelson
Nature Materials **3**, 380-384 (2004) doi:10.1038/nmat1133

ix.
Growth of GaP nanotree structures by sequential seeding of 1D nanowires
K. A. Dick, K. Deppert, T. Mårtensson, W. Seifert and L. Samuelson
Journal of Crystal Growth **272**, 131-137 (2004)
doi:10.1016/j.jcrysgro.2004.09.004

xvi.

Strain and shape of epitaxial InAs/InP nanowire superlattice measured by grazing incidence X-ray techniques

J. Eymery, F. Rieutord, V. Favre-Nicolin, O. Robach, Y. M. Niquet, L. Fröberg, T. Mårtensson and L. Samuelson

Nano Letters **7**, 2596-2601 (2007) `doi:10.1021/nl070888q`

xvii.

The structure of <111>B oriented GaP nanowires.

J. Johansson, L. S. Karlsson, C. P. T. Svensson, T. Mårtensson, B. A. Wacaser, K. Deppert and L. Samuelson

Journal of Crystal Growth **298**, 635-639 (2007)
`doi:10.1016/j.jcrysgro.2006.10.175`

xviii.

Optical properties of rotationally twinned InP nanowire heterostructures

J. M. Bao, D. C. Bell, F. Capasso, J. B. Wagner, T. Mårtensson, J. Trägårdh and L. Samuelson

Nano Letters **8**, 836-841 (2008) `doi:10.1021/nl072921e`

xix.

Selective etching of III-V nanowires for molecular junctions

C. Kallesøe, K. Mølhave, T. Mårtensson, T. M. Hansen, L. Samuelson and P. Bøggild

Microelectronic Engineering **85**, 1179-1181 (2008)
`doi:10.1016/j.mee.2007.12.023`

xx.

Surface-enhanced Raman scattering of rhodamine 6G on nanowire arrays decorated with gold nanoparticles

J. Chen, T. Mårtensson, K. A. Dick, K. Deppert, H. Q. Xu, L. Samuelson and H. Xu

Nanotechnology **19**, 275712 (2008) `doi:10.1088/0957-4484/19/27/275712`

xxi.

Axonal guidance on patterned free-standing nanowire surfaces

C. Prinz, W. Hällström, T. Mårtensson, L. Samuelson, L. Montelius and M. Kanje

Nanotechnology **19**, 345101 (2008) `doi:10.1088/0957-4484/19/34/345101`

xxii.
Vertical InAs nanowire wrap gate transistors on Si substrates
C. Rehnstedt, T. Mårtensson, C. Thelander, L. Samuelson and L. Wernersson
accepted for publication in IEEE Transactions on Electron Devices (2008)

xxiii.
Development of a vertical wrap-gated InAs FET
C. Thelander, C. Rehnstedt, L. E. Fröberg, E. Lind, T. Mårtensson, P. Caroff,
T. Löwgren, B. J. Ohlsson, L. Samuelson and L. Wernersson
accepted for publication in IEEE Transactions on Electron Devices (2008)

xxiv.
Fabrication of nanogaps using heterostructure III-V-nanowires
C. Kallesøe, K. Mølhave, T. Mårtensson, M. Borgström, T. M. Hansen,
L. Samuelson and P. Bøggild
submitted to Nanotechnology

Patent Applications

The following patent applications were made in combination with the above publications.

Precisely positioned nanowhiskers and nanowhisker arrays and
method for preparing them
L. I. Samuelson, B. J. Ohlsson and T. M. I. Mårtensson
US2005011431 (2005)

Formation of nanowhiskers on a substrate of dissimilar material
L. I. Samuelson and T. M. I. Mårtensson
WO2006000790 (2006)

Method for metal-free synthesis of epitaxial semiconductor nanowires
on Si
L. Samuelson, T. Mårtensson, W. Seifert, B. Mandl and A. Mikkelsen
PCT SE2007/050131 (2007)

Title not yet made public
L. Samuelson, T. Mårtensson and J. Ohlsson
SE 0702402-9 (2007)

Abbreviations and Symbols

1D, 2D, 3D	one-, two-, three-dimensional
a	lattice constant
AFM	atomic force microscopy
APD	anti-phase domain
CMOS	complementary metal oxide semiconductor
EBL	electron beam lithography
E_a	activation energy
E_F	Fermi energy
E_g	energy band gap
EL	electroluminescence
fcc	face-centred cubic
FET	field-effect transistor
hcp	hexagonal close-packed
III-V	compound comprised of one group-III element and one group V-element of the periodic system
LED	light-emitting diode
LOR	lift-off resist
MOVPE	metal-organic vapour phase epitaxy
MBE	molecular beam epitaxy
NIL	nanoimprint lithography
NW	nanowire
PL	photoluminescence
PMMA	poly(methyl methacrylate)
SAE	selective-area epitaxy
SEM	scanning electron microscopy
SET	single-electron transistor
STM	scanning tunnelling microscopy
TEM	transmission electron microscopy
TMGa	trimethyl gallium
TMIn	trimethyl indium
μ	chemical potential
$\Delta\mu$	supersaturation
UHV	ultrahigh vacuum
VLS	vapour–liquid–solid
(hkl)	Miller index notation for a specific plane, e.g., $(1\bar{1}0)$
$\{hkl\}$	a family of equivalent planes, e.g., $\{1\bar{1}0\}$
$[hkl]$	a specific direction, e.g., $[1\bar{1}0]$
$<hkl>$	a family of equivalent directions, e.g., $<1\bar{1}0>$

Contents

Chapter 1

Introduction

This thesis describes the subject of nanowires, which is highly multidisciplinary. Below an introduction to the principal concepts of this thesis is given. A thesis outline is provided at the end of this chapter.

1.1 Materials Science

Materials science has been at the core of many of the technological breakthroughs made by man. Metal working, for example, was considered so important that it was used to describe periods in history (the Bronze Age and the Iron Age), while steel was an important part of the industrial revolution. In the 20th century, the invention and development of semiconductor technology enabled the information technology revolution. Computers, the internet, and mobile phones are now integral parts of daily life.

Today we face new challenges, not least environmental challenges. Efficient and inexpensive materials for clean "combustion" by fuel cells, energy production by solar cells (photovoltaics) and solid state lighting (LEDs) for energy-saving illumination, need to be developed. Just as semiconductors play a central role in computer technology, they are also used for the last two applications, photovoltaics and LEDs. Semiconductor nanostructures are also the materials used in the current work.

1.2 Semiconductors

In Figure 1.1 the elements of the most commonly used semiconductors are shown. Silicon is the most important semiconductor material and is found in nearly all

electronics.

	III	IV	V	VI
	B	C	N	O
II	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

Figure 1.1: Part of the periodic system showing the elements of the III-V and group IV semiconductors. Si and Ge are single-element semiconductors, whereas the III-Vs are binary materials, for example, GaAs and InP.

A semiconductor exhibits a *band gap*, which is an energy interval in which no electron states are allowed. In a semiconductor the states below the gap are fully occupied by electrons, and the states above the gap are empty. Since completely filled bands (or empty bands) carry no net current, these materials are insulators at absolute zero [1]. However, at room temperature these materials have a finite conductance that can be controlled by introducing impurity atoms (doping) and applying electrical fields. The ability to "tune" a material between a conducting- and a non-conducting state forms the basis of a transistor, from which computer logic is constructed. In a semiconductor transistor, doping is introduced during fabrication, and electrical fields are then applied during operation to control the conductance. The so called complimentary metal oxide semiconductor (CMOS) technology is the core of current computer technology.

The so-called III-V semiconductors are compound materials composed of elements from groups III and V of the periodic system (Fig. 1.1), for example, GaAs and InP. These are more expensive than Si, and the degree of perfection of the material is lower. However, these materials have functionality that Si does not posses. The most important difference is perhaps that most of them exhibit a so-called *direct band gap*, meaning that electrons can relax to lower energy states (recombine with holes) with conserved momentum and emit light (photons) in the process. Thus, III-Vs are used in light-emitting applications such as LEDs and lasers.

1.3 Nanotechnology

In recent years, nanotechnology[1] has emerged as a subdiscipline to materials science, or in many cases a discipline of its own. In nanotechnology matter is controlled on the atomic and molecular scale to fabricate features or devices with at least one dimension smaller than 100 nanometres. A central theme in nanotechnology is the so called "bottom-up" [4] approach, meaning that nanostructures are constructed by adding atoms in a controlled way, rather than removing material from a larger piece of starting material, as is done in the so-called "top-down" approach, which currently dominates in industry.

When dimensions shrink to nanoscale dimensions the material properties may change drastically: melting points are depressed [5], magnetic materials may undergo a phase transition from ferromagnetic to superparamagnetic, materials with an indirect band gap in the bulk may change to a direct band gap [6], otherwise inert metals can become highly catalytically active [7], and quantum confinement effects appear [8]. These effects provide new opportunities, as well as challenges.

Today, nanotechnology is a major scientific field with numerous sub-fields. Semiconductor nanostructures comprise a large class of objects, including, for example, quantum dots, carbon nanotubes, nanoribbons and nanowires. The last structure is studied in this work.

1.3.1 Nanowires

Semiconductor nanowires (NWs) have a diameter < 100 nm, whereas the axis is considerably longer, typically in the μm range. The interest in NWs emanates from their, in many regards, unique properties. In recent years substantial effort has been devoted to understanding their synthesis, and electrical and optical and mechanical properties, and how these properties can be exploited in fields such as electronics, photonics, sensing applications and life sciences. A few examples are given here. *(Optoelectronics)* 1D heterostructures can be used to form quantum dots embedded in the NW which function as single-photon sources [9]. NWs can act as laser cavities [10]. Important optical materials, which are difficult to synthesize in their bulk forms without defects, can be fabricated as perfect crystals in the form of NWs, for example, GaN and AlGaN [11]. A further opportunity is the integration of light-emitting materials on Si, as studied in this work in Papers I and V. *(Electronics)* NWs provide an ideal geometry for field-effect transistors (FETs) with a wrap-gate around the NW active channel [12]. Single-electron transistors (Paper VI) and multiple tunnel junction memories [13] have been realized in NWs employing heterostructure technology. NWs may act as 3D interconnects and form networks with new functionality for future generations of

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[1]see e.g. refs [2, 3] for a popular introduction to nanotechnology

ultra-dense electronics [14]. *(Chemical sensors)* The large surface to volume ratio of NWs makes them suitable for chemical sensing applications with ultra-high sensitivity [15]. An overview of NW synthesis, properties and devices was recently given in *Functional Nanowires*, MRS Bulletin [16].

1.4   Thesis Outline

This thesis is organized in seven chapters, which provide background and further discuss the findings of the published papers.

A introduction to epitaxial growth of NWs is provided in Chapters 2 and 3; the general concepts of crystal structures and crystal growth are introduced in Chapter 2 and described in terms of NW growth in Chapter 3.

Chapters 4 and 5 describe the specific contributions made to NW growth in this work: III-V NWs integrated on Si substrates, and site-controlled NW growth.

Chapter 6 describes three examples of NW applications. These were made possible partly by the developments in NW growth described in the previous chapters.

Chapter 7 provides a brief outlook of the field.

The thesis is written in English, but a popular summary, "Populärvetenskaplig sammanfattning", is provided in Swedish at the end.

Chapter 2

Epitaxy and Crystals

This chapter provides the background for Chapters $2-5$ and starts by introducing the thermodynamics of crystal growth. The structures of crystals are also discussed. The atomistic view of epitaxy and the technique of metal-organic vapour phase epitaxy (MOVPE) are then described.

2.1 Thermodynamics of Crystal Growth

The first question is: When is crystal growth energetically possible? A crystal is always in contact with its environment, for example a gas, with which it interacts. At constant pressure and temperature, a system strives to attain minimum Gibbs free energy, G [17]. The energy required to add Δn particles to a system at constant pressure p and constant temperature T is the *chemical potential*,

$$\mu = \left(\frac{\partial G}{\partial n}\right)_{p,T} \tag{2.1}$$

Depending on the chemical potentials of the crystal and its environment, the crystal will either be *(i)* etched, *(ii)* in equilibrium with its environment, or *(iii)* growing (Fig. 2.1). Thus, the difference in chemical potential between two phases, called the *supersaturation*

$$\Delta\mu_{AC} = \mu_E - \mu_C \tag{2.2}$$

is an important quantity. The subscripts E and C denote Environment and Crystal, respectively. For example,
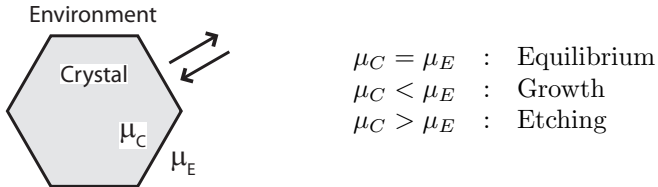
Figure 2.1: Crystal–environment interactions. Depending on the chemical potentials of the different phases, the crystal will either be in equilibrium with its environment, etched, or growing. Figure adapted from reference [21].

the supersaturation for a single-component crystal in contact with an ideal gas of the same component is given by:

$$\Delta\mu = RT \ln \left(\frac{P}{P_0} \right) \tag{2.3}$$

where R is the universal gas constant, P is the pressure of the gas phase, and P_0 is the crystal vapour pressure at the given temperature [18]. Equation 2.3 applies, for example, to molecular beam epitaxy (MBE) growth of Si. It is seen that if the temperature is increased while maintaining the same equivalent beam pressure P, at some point, the growth rate becomes zero, and ultimately becomes negative (the crystal evaporates). The reason is that P_0 increases exponentially with temperature, and $\Delta\mu$ goes through the sequence $P_0 < P \Rightarrow \Delta\mu > 0$: crystal growth, $P_0 = P \Rightarrow \Delta\mu = 0$: cessation of crystal growth, $P_0 > P \Rightarrow \Delta\mu < 0$: evaporation of the crystal (etching). The supersaturation also controls more complex growth behaviour such as the crystalline structure of NWs [19, 20]. The supersaturation is, however, difficult to calculate for many complex systems (such as III-V NWs grown by MOVPE) and is often used conceptually rather that calculated quantitatively.

Besides thermodynamics, an atomistic view of the crystal and its kinetic processes is required for a full understanding of crystal growth.

2.2 Crystal Structures

A *crystal* exhibits long-range ordering of the material. Well-known examples of crystals are diamonds and rock salt, but most metals also have a crystalline structure. This is in contrast to *amorphous* materials, for example, polymers, which do not have long-range ordering. Crystals may be insulators, semiconductors or metals, depending on their energy band structure [1]. The materials studied in this work are semiconductor crystals.
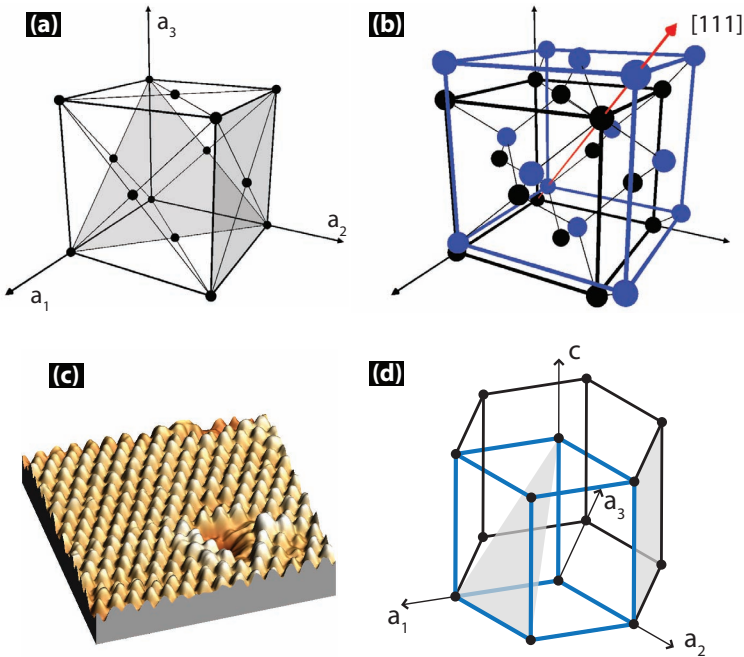
Figure 2.2: Crystal structures. (a) The fcc unit cell. The (111) and (010) planes are shaded grey. (b) The zinc blende crystal structure. The zinc blende crystal structure is constructed from the fcc lattice and a basis at each lattice point. The basis consist of a group III atom at the origin (black) and a group V atom translated $\frac{1}{4}a$ in the [111] direction (blue). If the two basis atoms are the same, for example, silicon, the structure is denoted diamond. (c) Crystal structures can be observed directly with experimental techniques. Here a scanning tunnelling microscopy (STM) image of an InAs(111)B (1x1) surface is shown. Each peak corresponds to an As atom and a triangular defect (hole) is also observed. (Image courtesy of Emelie Hilner and Anders Mikkelsen.) (d) The simple hexagonal unit cell spanned by $\mathbf{a}_1, \mathbf{a}_2$ and $\mathbf{c}$ is shown in blue. The larger cell shown in black is often used for easier viewing. The $(10\bar{1}1)$ and $(\bar{1}100)$ planes are shaded grey.

An ideal crystal is made up of units repeated infinitely and regularly in space. In the simplest case the unit (also called motif or more correctly basis) consists of a single atom. The units are placed at the lattice points of an infinite, regular lattice, a so-called *Bravais lattice*. A Bravais lattice has translational symmetry meaning that the lattice appears exactly the same from whichever point in the lattice it is viewed [1]. In three dimensions there are 14 different Bravais lattices, and in the two lattices most relevant to this thesis are shown in Figure 2.2(a,d): the face-centred cubic (fcc) and the simple hexagonal.

Miller indices are used to denote crystal planes and crystal directions. The Miller indices, (hkl) (note round brackets), of a certain plane can be constructed by noting the plane's intersections with the basis axes, then removing any common factor, and finally taking the reciprocal values. In Figure 2.2(a), the (111) and (001) planes of the cubic system are shown. Crystal directions are given in the basis vectors with the notation (note square brackets):

$$[hkl] = h\mathbf{a}_1 + k\mathbf{a}_2 + l\mathbf{a}_3 \tag{2.4}$$

Many planes and directions are equivalent due to the symmetry of the crystal. A collective notation is then used for equivalent planes, $\{hkl\}$ (curly brackets), and equivalent directions, $< hkl >$ (angle brackets). For example, the eight sides of the fcc cubic unit are equivalent and form the set:

$$\{001\} = \left\{ (001), (00\bar{1}), (010), (0\bar{1}0), (001), (00\bar{1}) \right\} \tag{2.5}$$

For the hexagonal system, *Miller–Bravais* indices $(hkil)$ are commonly used. These are constructed in the same way as described above for the Miller indices, but because four basis axes are used, the first three indices are linearly dependent such that $i = -(k + l)$. The advantage of using four indices is that equivalent planes have similar indices, which is not the case if three indices are used for the hexagonal system [22]. The indices of the six edge planes in Figure 2.2(d) are, for example, constructed by permuting 1 and $\bar{1}$ over the first three indices. To simplify the notation, a letter is often assigned to a certain set of equivalent planes. The six edge planes discussed above are the m planes:

$$m = \{1\bar{1}00\} = \left\{ (10\bar{1}0), (\bar{1}010), (0\bar{1}10), (1\bar{1}00), (10\bar{1}0), (01\bar{1}0) \right\} \tag{2.6}$$

As discussed above, crystal structures are constructed from a Bravais lattice and a basis. The constructions of the crystal structures of interest in this work are described below: the cubic structures diamond and zinc blende, and the hexagonal structure wurtzite.

The cubic structures can be constructed from the Bravais lattice and a basis in the following way. Consider the fcc lattice in Figure 2.2(a). Place a basis, consisting of a group III atom (black) and a group V atom translated $\frac{1}{4}a$ in the [111]-direction (blue), at each lattice point. This is the zinc blende structure (also denoted sphalerite) of the III-V materials (Fig. 2.2(b)). If the two atoms are the same, for example, two Si atoms, the crystal has the diamond structure.

The hexagonal wurtzite structure is based on the hexagonal close-packed structure (hcp), which in turn is constructed from two intersecting simple hexagonal lattices (Fig. 2.2(d)), one being displaced $\frac{2}{3}\mathbf{a}_1 + \frac{1}{3}\mathbf{a}_2 + \frac{1}{2}\mathbf{c}$ from the other. To form the wurtzite structure, a basis consisting of a group III atom at the origin and

a group V atom at $\frac{3}{8}\mathbf{c}$, is placed at each hcp lattice point. Real materials will deviate slightly from the ideal value of $\frac{3}{8}$.

The zinc blende and wurtzite crystal structures described above are closely related. NWs are observed to grow in both crystal structures, for example, zinc blende InP and wurtzite InP [20]. Along certain growth directions, especially the [111]B, a mixture of the two crystal structures is sometimes observed in the same NW, a phenomena denoted polytypism. Polytypism and its effects on the optical properties of nanowires were examined in references [xiv, xvii, xviii], but this large topic is beyond the scope of this thesis.

Some crystal orientations are polar, meaning that the planes are terminated by either group III or group V atoms. The cubic <111> and hexagonal <0001> directions used for NW growth are polar. For zinc blende, the facets terminated by group III atoms are denoted {111}A, and group V terminated facets are denoted {111}B. As described in the next chapter, the most common growth direction for NWs is the [111]B direction. For Si, which has a diamond structure and only contains one atom species, polar surfaces cannot exist, and all <111> directions are equivalent.

2.3 Atomistic View of Epitaxy

Epitaxy[1] can intuitively be understood as building a crystal "block-by-block". The word epitaxy itself originates from the Greek words $\varepsilon\pi\iota$ – "on", and $\tau\alpha\xi\iota\sigma$ – "in order" [18]. Many aspects of epitaxy can be illustrated by the *Terrace-Ledge-Kink model* (also called the Kossel model) [18]. In a *Kossel crystal* (simple cubic crystal) each atom is represented by a cube, and each face of the cube can bind to its nearest neighbour (Fig. 2.3). Growth species are supplied to the growing crystal from the vapour phase or as a molecular beam if high-vacuum conditions are used. Atoms that land on the surface diffuse and are incorporated into the crystal, or desorb again. The so-called adatoms (labelled "1" in the image) are loosely attached and only bind to one nearest neighbour. The adatoms are incorporated into the crystal when they diffuse to a more energetically favourable site, such as the kink position ("3"), or are embedded in the step ("4").

A Kossel crystal can also be used to understand different growth modes. The most commonly used planar growth mode is *step-flow growth*, where atoms are incorporated at a step, which then continuously advances forward (Fig. 2.3(b)). Wafers are often bought "miscut", meaning that they are cut a small angle from the exact crystal plane (a so-called vicinal surface), so as to contain steps and support

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[1]Epitaxy and crystal growth are sometimes used interchangeably, e.g., nanowire growth and nanowire epitaxy. However, strictly speaking, *epitaxy* refers to the method of depositing a monocrystalline film on a monocrystalline substrate, whereas *crystal growth* is the more generic term.
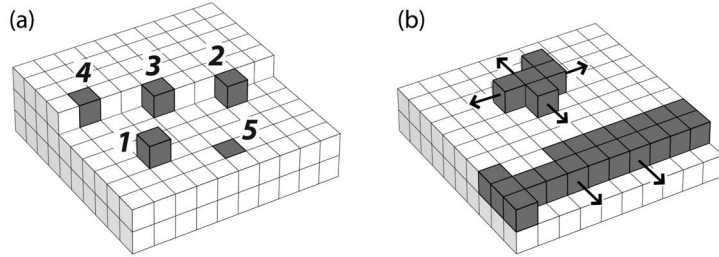
Figure 2.3: Kossel crystals. (a) Five surface atom positions are possible. So-called adatoms ("1") are loosely attached to the surface by only one nearest neighbour and may diffuse across the surface and be incorporated into the crystal at more favourable positions $(3 - 5)$. (b) The most commonly used planar growth mode is step-flow growth where atoms are incorporated at the step, which then advances forwards. Growth can also take place at a smooth facet via nucleation, the so-called birth-and-spread growth mode.

step-flow growth. Vicinal (001) surfaces with a few degrees of miscut are the most commonly used surface for commercial purposes [23]. This enables high-quality epitaxy using step-flow growth mode.

Crystal growth may also take place on an atomically smooth crystal face (terrace) where no steps are present. Adatoms diffusing on the surface may come together to form clusters. If the cluster reaches a certain critical size, it becomes stable and forms a nucleus. The nucleus now provides both steps and kinks for continued growth (Fig. 2.3(b)). This growth mode is often referred to as *birth-and-spread*. Particle-assisted NW growth as described in Section 3.1 is believed to take place by a birth-and-spread mechanism [xvii][19].

Several epitaxial techniques can be used, such as liquid phase epitaxy (LPE), halide vapour phase epitaxy (HVPE), chemical beam epitaxy (CBE), molecular beam epitaxy (MBE) and metal-organic metal vapour phase epitaxy (MOVPE). MOVPE was used in this work.

2.4 MOVPE

Metal-organic vapour phase epitaxy (MOVPE) dates back to the late 1960s and the work of Manasevit and co-workers [24]. It is today the commercially most important epitaxy growth method for III-V semiconductors, and its products range from blue laser diodes (AlGaInN material) to high-speed electric devices (e.g. in the GaInAsP material system).
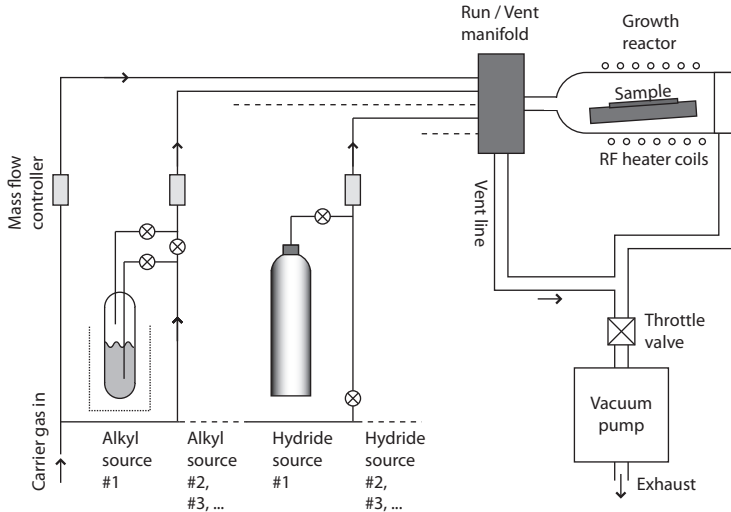
Figure 2.4: Schematics of a MOVPE system.

MOVPE takes place at atmospheric or low pressures (typically 100 mbar). An inert carrier gas is passed over a sample, which rests on a heater. The material for crystal growth is supplied in the form of precursor molecules that flow over the sample together with the carrier gas. For the growth of gallium arsenide, used as an example here, trimethyl gallium (TMGa) and arsine (AsH_3) are commonly used precursors. The precursors decompose at the elevated temperatures used for epitaxy, typically $600 - 700\ °C$ for planar GaAs epitaxy, and the elemental species, Ga and As, are incorporated into the GaAs crystal. Although the detailed chemistry is highly complex, the net reaction for GaAs epitaxy is:

$$Ga(CH_3)_{3_{(gas)}} + AsH_{3_{(gas)}} \longrightarrow GaAs_{(solid)} + 3CH_{4_{(gas)}} \tag{2.7}$$

In the ideal case the methyl groups desorb from the surface, leaving low residual carbon levels in the GaAs crystal. A thorough description of MOVPE processes has been given by Stringfellow [23].

In Figure 2.4 a simplified scheme of a typical MOVPE system is shown. Hydrogen is a commonly used carrier gas because it is available at extremely high purity through palladium diffuser purification, but nitrogen may also be used. The alkyl sources for the group III elements (e.g., TMGa, TMIn, TEGa and TMAl) are in liquid or solid form and are extracted through their vapour pressures by the carrier gas. The hydrides are gaseous and are transported by their own bottle overpressure. The gas flows of the different sources are controlled by mass flow controllers and transported separately to a gas manifold before the growth cell. Here, they are either sent to the growth reactor, "run line" or bypassed to the ex-

haust, "vent line". The sample rests on a susceptor that is heated. In Figure 2.4 a solution that employs RF heating (inductive heating) is shown. Resistive heating and heating by infra-red lamps are also common. A vacuum pump downstream from the growth reactor controls the reactor pressure through a throttle valve. Toxic components are removed from the exhaust by filters or combustion. The epitaxy system is computer-controlled, and a "growth recipe" is executed. Such a recipe contains detailed information on the flows of the different gases, temperature, pressures, and so forth. The duration of a growth run ranges from ~ 30 min to several hours.

Chapter 3

Nanowire Epitaxy

In the present chapter, nanowire epitaxy and its special merits compared with planar epitaxy are described. The two main growth modes, particle-assisted and particle-free, as well as nanowire heterostructures, are briefly reviewed.

Nanowire epitaxy involves quasi-1D growth with a NW diameter < 100 nm. On this scale, many differences compared with bulk start to appear: surface energies make a significant contribution to the total energy of the structure, and strain and defect properties are different to those of bulk. Many NWs are reported to be ideal crystals, free of defects, and may crystallize in a structure different from the stable bulk phase (e.g., wurtzite InAs). Moreover, NW epitaxy offers greater freedom in the design of complex structures compared with planar epitaxy.

(a) Axial hetero-structures

(b) Radial hetero-structure (core-shell)

(c) Branched growth
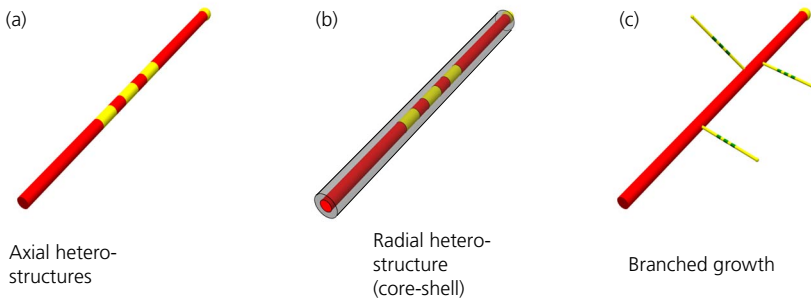
Figure 3.1: NW heterostructures and growth modes.

In Figure 3.1 three different NW structures are shown. Heterostructures, axial (a) and radial (b), are crucial for many devices, and in the axial direction,
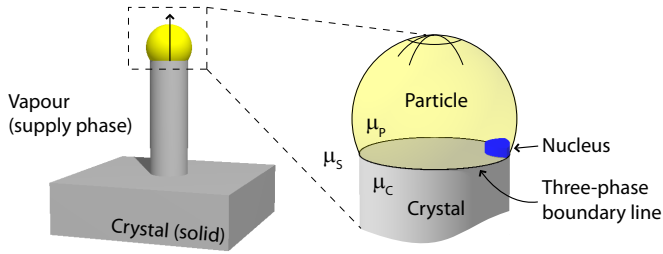
Figure 3.2: Schematic image of particle-assisted NW growth. Crystal growth takes place selectively at the particle/crystal interface.

the NW geometry offers the possibility of new material combinations due to its small cross-section (see Section 3.3). A third type of structure, a branched NW, is shown in panel (c). Branched nanowires can be created by employing particle deposition on NW "stems" and subsequent particle-assisted NW growth to form the branches [viii][25]. A third generation ("leaves") can be formed by further deposition and growth. From these three basic structures, more advanced building blocks can be formed, illustrating the flexibility of NW epitaxy.

3.1 Particle-Assisted Growth

In particle-assisted NW growth, a growth catalyst particle is used to induce 1D growth at the site of the particle. Growth proceeds orders of magnitude faster at the particle/crystal interface than on surrounding surfaces (Fig. 3.2), which results in virtually one-dimensional growth. The size of the particle determines the wire diameter, and reported diameters range from 3 nm [26] up to several 100 μm [27]. The length is controlled by the growth period (at a certain growth rate).

Particle-assisted whisker growth was observed already in the 1950s (see [28] and references therein) and silicon whiskers catalysed by gold particles were systematically studied by Wagner et al. in the 1960s [29]. Together with the group led by Givargizov [30] they pioneered Au-assisted growth of predominantly Si whiskers. Hiruma and co-workers further explored Au-assisted growth of III-V nanowhiskers in the 1990s [31, 32], and at the end of the 1990s and beginning of 2000, several groups initiated work on NW synthesis employing gold particles (see e.g. [33–36]).

In a typical process for NW growth, metal particles (often Au) are deposited on a crystalline semiconductor surface. These particles can, for example, be prepared in the form of aerosols, and filtered to provide a narrow size distribution [37]. The gold-decorated substrate is then transferred to a growth system, for example, a MOVPE system. During heating to the growth temperature, the particles interact

with the substrate, and surface oxides desorb. Growth is then initiated when the source gases are introduced into the chamber.
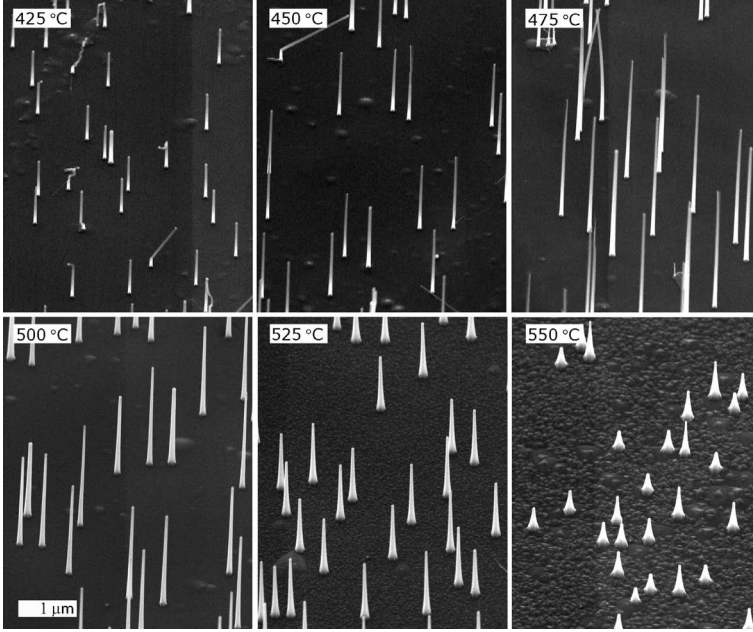
Figure 3.3: Scanning electron microscopy (SEM) images of a growth temperature series of particle-assisted GaP NW. NWs grown on GaP(111)B substrates at a density of $1 \times 10^8 \, \text{cm}^{-2}$. Molar fractions of TMGa and PH$_3$ were 9×10^{-6} and 7×10^{-3}, respectively, i.e. a V/III ratio of ≈ 760. The pressure was 100 mbar in a 6 000 sccm hydrogen carrier gas flow. The growth time was 4 min. Image tilt is $45°$.

Figure 3.3 shows a temperature series of particle-assisted GaP NW growth. The NWs grow epitaxially in the [111]B direction at normal angles to the GaP(111)B substrate. At low temperatures the wires are short and rod-shaped. With increasing temperature, tapering as well as the axial growth rate increase. The length of the NWs peaks at 475 °C and decreases again for higher temperatures.

Figure 3.4 shows the axial growth rate for the GaP NWs displayed in Figure 3.3. The axial growth rate, R, of nanowires is often observed to follow an Arrhenius dependence for low temperatures, that is, $\ln(R)$ depends linearly on $1/T$ with a negative slope (see e.g. refs [xi][30, 36]). Arrhenius behaviour is expected for any process where the rate constant, k, in the rate-limiting step follows a relation of the type $k = Ae^{-\frac{E_a}{k_B T}}$, where E_a is the activation energy, k_B the Boltzmann constant, T the temperature and A the exponential prefactor. This growth regime is referred to as *kinetically limited*. The rate-limiting step has, for example, been reported to
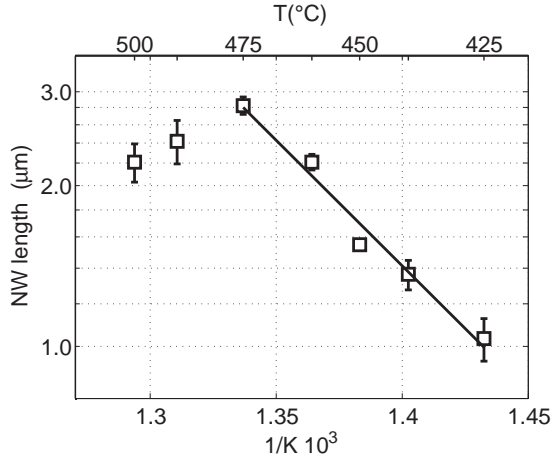
Figure 3.4: Length of GaP NWs after 4 min growth (cf. Fig. 3.3). A linear fit in the temperature interval $425-475$ °C gives an activation energy, E_a, of $89 \text{ J} \cdot \text{mol}^{-1}$.

be the cracking of precursors [36, 38] or the crystal growth at the particle/crystal interface itself [30]. At higher temperatures (here $\gtrsim 475$ °C), the axial NW growth rate decreases due to the onset of competing growth on NW side facets and the substrate surface. These conditions, which also favour radial growth, can be used to grow a shell structure around the NW [39, 40].

The mechanism of particle-assisted NW growth is still an topic of considerable interest. The most often cited growth model is the so-called vapour–liquid–solid (VLS) mechanism, which was first described by Wagner and Ellis in 1964 [27][1] to explain the growth of silicon whiskers employing a gold growth catalyst. The original description of the VLS mechanism was based on the properties of the gold-silicon phase diagram, and the concept of a liquid gold droplet that becomes supersaturated with Si supplied by the gas phase. As the drop becomes supersaturated, Si will precipitate in solid form at the liquid/solid interface, and crystal growth will take place selectively under the Au particle.

Some inconsistencies in the VLS model have recently been pointed out, and the need for a more complete model has become apparent. The particle may, for example, be in the solid form and still support NW growth [xii][41, 42], and surface diffusion of growth species often makes a strong contribution to NW growth [xiii][43], neither of which is accounted for in the original VLS model.

What are the main effects causing NW growth? The particle has been reported to

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[1]This original paper alone had been cited more than 1600 times as of August 2008.

behave as a true chemical catalyst[2] that catalyses precursor decomposition [38, 44] and it could thus support a higher supersaturation in the particle than outside. Although this is an important effect, it cannot be a *necessary* requirement for NW growth, because in many reports, the activation energy for NW growth is the same as for planar epitaxy [36, 45]. Furthermore, NWs can still be grown even if precursor cracking is not involved, for example, using MBE [46].

Also, in the absence of an irreversible step at the particle surface (such as precursor decomposition), the particle cannot sustain a local supersaturation higher than its environment. The chemical potential of the supply phase (e.g., the vapour phase in MOVPE), μ_S, must be higher than the chemical potential of both the particle, μ_P, and the crystal, μ_C, for growth to take place (cf. Fig. 3.2). Furthermore, the growing phase, that is, the crystal, must have the lowest chemical potential, thus:

$$\mu_C < \mu_P < \mu_S \tag{3.1}$$

From this equation it follows that the supply-to-crystal supersaturation, $\Delta\mu_{SC} = \mu_S - \mu_C$, is always higher than the particle-to-crystal supersaturation, $\Delta\mu_{PC} = \mu_P - \mu_C$, that is,

$$\Delta\mu_{PC} < \Delta\mu_{SC} \tag{3.2}$$

Thus, if supersaturation alone determines the growth rate, 2D growth on the substrate should be faster than axial wire growth [47].

Additional effects seem to be needed for a generic model of NW growth, and recent models also focus on a lowering of the nucleation barrier at the particle/crystal interface [19, 47]. The surface under the particle is different from the surrounding crystal/vapour surfaces. It may, for example, have a different surface reconstruction or different step energies. The growth rate may be locally enhanced under the particle if these differences are such that the nucleation barrier is lowered. Nucleation is furthermore believed to take place at the edge of the particle/crystal interface at the three-phase boundary line [xiv][19, 47], where the nucleation barrier is lower [19]. That is, growth proceeds by a birth-and-spread mechanism initiated at the three-phase boundary line. It should be noted that publications providing quantitative calculations on nucleation barriers at the different interfaces are still lacking in the literature.

3.2 Particle-Free Growth

Recently, NW growth without foreign growth catalysts has been reported. Several different types of growth mechanisms exist, and they are fundamentally different from the particle-assisted route. It has, for example, been reported that when

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[2]A chemical catalyst lowers the activation energy, E_a, of a rate-limiting step without being consumed.

certain oxide precursors are used, a passivating oxide shell forms, which promotes 1D NW growth. This is referred to as oxide-assisted NW growth [48]. The catalysing effect of a thin SiO_x film, as well as patterned SiO_x particles, on NW growth has also been reported [xv]. Comprehensive reviews of different synthesis methods and materials systems have been made by Xia [49] and Rao [50].

The formation of one-dimensional objects by controlling the growth rate of different crystal facets is described next. A prerequisite for facet-controlled formation of 1D objects appears to be anisotropy in the crystal structure. Polar materials such as GaN [51–53] and ZnO [54, 55], are often reported to grow in columnar structures. Conversely, covalent materials such as Si have not been reported to grow as 1D structures without the aid of a growth catalyst or passivating shell [48].
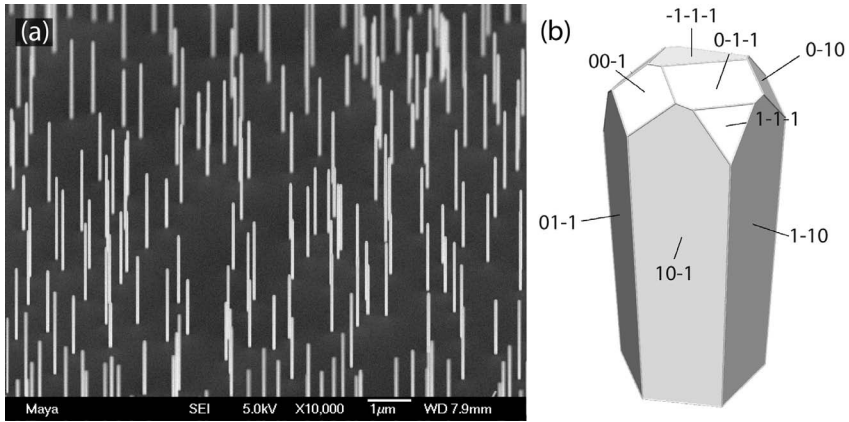
Figure 3.5: Particle-free NW growth. (a) InAs NWs grown on a Si(111) substrate (Paper II). Image tilt 45°. (b) Schematic image of a NW with $\{\bar{1}10\}$ side facets. The tip is bounded by the slow-growing tip facets (most commonly the low-index facets).

How can a one-dimensional crystal shape form? First, it is important to realise that NW growth is a process far from equilibrium, and that Wulff's theorem [56] cannot be used to explain the one-dimensionality of a NW. In the common case for crystal growth of convex shapes, the fast-growing facets "grow out", and the crystal is left bounded by its slow growing facets [57]. However, if the slowest growing facets are all parallel to a crystal axis (e.g., the $\{\bar{1}10\}$ facets parallel to the $(\overline{111})$ axis as shown in Fig. 3.5(b)), they cannot completely bound the crystal. The result is that the fast-growing tip facets can continue to grow without reducing their area. In this way, one-dimensional growth can be sustained and NWs formed. For NW growth with $\{\bar{1}10\}$ side facets (cf. Paper II), the requirement for one-dimensional

growth can be written as:

$$R_{\{\bar{1}10\}} < R_{[\overline{1}\overline{1}\overline{1}]}, R_{\{110\}}, R_{\{\bar{1}00\}}, R_{\{\bar{1}11\}}, R_{higher\ index\ tip\ facets} \qquad (3.3)$$

where R denotes the growth rate of the different facets. For MOVPE growth of III-V materials, this low growth rate of the side facets is usually obtained with a low V/III ratio[3] and a high temperature [58, 59]. The tip shape is determined by the relative growth rates of the different tip facets. Flat tips [xv][58, 59], as well as rounded or pointed tips (Paper II and [54, 55]), have been reported[4].

3.3 Heterostructures

In Figure 3.6 two examples of NW heterostructures are shown, *axial* and *radial*. Axial heterostructures in the InAs/InP material system were essential for the formation of a central InAs island with InP barriers in Paper VI (see Section 6.2), and radial heterostructures were key for forming the light-emitting diode (LED) structure described in Paper V (see Section 6.1).

Axial heterostructures can be fabricated if the growth precursors are alternated during axial NW growth [32, 60–62]. For example, a $GaP/GaAs_{1-x}P_x/GaP$ double heterostructure can be achieved if the group V source is switched from phosphine to arsine and back [63]. A unique feature of the small NW cross-section is the ability to grow axial heterostructures of materials that are normally incompatible due to a large difference in their lattice constants. The lattice mismatch between two materials is defined as:

$$f = \frac{a_u - a_o}{a_u} \qquad (3.4)$$

where a is the lattice constant of the materials, and the indices u and o denote underlayer and overlayer, respectively.[5] In the case of conventional 2D planar layers, interface defects are difficult to avoid even for small mismatches. For a mismatch $f = 2\,\%$, it is expected that defects form already after the growth of a 10 nm thick overlayer ($Ge_{0.5}Si_{0.5}/Si$ [64]). The situation is different for the NW geometry because the small cross-section allows strain to be relaxed also radially. Ertekin et al. used an equilibrium energy minimization approach to determine the critical radius for dislocation formation; it was found that the critical radius for axial heterostructures is approximately one order of magnitude larger than the corresponding critical thickness for planar growth [65]. Experimental observations suggest that the critical radius may be even larger in, for example, the InAs/InP system [60, 66]. A heterostructure similar to the axial forms during growth of

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[3]Flow of group V precursor / flow of group III precursor

[4]It should be noted that these profiles are observed *ex situ* after cooling to room temperature, and that the shape of the tip may have changed from that during growth.

[5]For materials with more dissimilar crystal structures, this expression must be generalized.

NWs on a dissimilar substrate, for example, GaP or InAs on Si (Papers I and II, see Section 4.2).

The second type of heterostructure is the radial, or *core-shell*, heterostructure (Fig. 3.6(b)) [39, 40]. A shell can be grown around the core if the growth parameters are changed to also favour growth on the NW side facets. Such a shell is often important for NW devices; the shell moves detrimental surface states away from the active region where charge transport or radiative recombination take place.
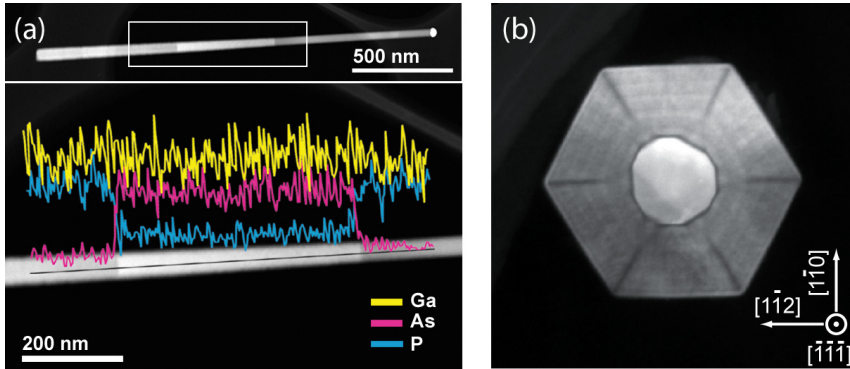
Figure 3.6: TEM images of NW heterostructures. (a) Light-emitting GaAsP segments incorporated into a GaP NW during growth. The sharpness of the interfaces is visible from the X-ray energy dispersive spectroscopy line scan. (b) Cross-section, looking down the axis, of a GaAs/AlGaAs core-shell NW. The GaAs core appears bright with a surrounding AlGaAs shell. The darker regions at the hexagon vertices are Al-rich regions [40].

3.4 Comparison of Particle-Assisted and Particle-Free Growth

Both particle-assisted and particle-free NW growth have their merits and drawbacks. A brief comparison is made here.

☐ *Materials*

Polar materials (III-Vs and II-VIs) can be grown particle-free due to their asymmetry in crystal structure. Covalent materials such as Si and Ge have not been reported in particle-free growth mode. Particle-assisted growth does not suffer from this limitation and has been reported for a wealth of materials, see, for example, Rao et al. [50].

☐ *Growth uniformity*

Both particle-free and particle-assisted NWs can be synthesized with good control of site, diameter and composition (cf. [43, 58]). For lithographic arrays, particle movement may cause distortion in the designed pattern (see Section 5.2), which does not occur for NWs grown by selective-area epitaxy [58]. Moreover, tapered wires are commonly observed with particle-assisted NW growth, whereas untapered wires are usually reported with particle-free growth.

☐ *Scalability*

Some applications require very small NW diameters, which presents a challenge. NWs with diameters as small as 3 nm have been reported [26] with particle-assisted growth. Using particle-free growth via lithographic selected area epitaxy, the minimum size is determined by the hole size [58]. For lithographic particle-assisted arrays, a thin metal disc may reshape upon heating to a more compact shape with smaller diameter, thus enabling wire diameters below the lithography resolution limit.

☐ *Axial heterostructures*

There are a multitude of reports on high-quality axial heterostructures using particle-assisted NW growth (see e.g. [32, 60–62]). For particle-free growth, the number of reports is fewer, and a problem appears to lie in achieving highly selective axial growth with no radial growth.

☐ *Radial heterostructures*

High-quality core-shell structures have been reported for both growth modes (see e.g. [40, 67]). The absence of a particle may, however, be an advantage as the particle is passive during radial growth and may present a complication.

☐ *Growth temperature*

In general, the growth temperature is lower for particle-assisted growth, for example $\sim 100\,°C$ in the InAs system [xii]. A higher growth temperature often result in better crystal quality and less incorporation of carbon impurities. However, a high temperature may be problematic concerning integration with other processes.

☐ *CMOS compatibility*

There are two major concerns regarding compatibility with CMOS: temperature and contamination.
(i) CMOS back-end-of-line processes can only tolerate temperatures $\lesssim 420\,°C$,

which favours the lower temperatures needed for particle-assisted NW growth. NW growth may also be performed front-end-of-line, where much higher temperatures are acceptable. However, contamination problems then become more severe.

(ii) Gold is a deep-level contaminant in Si [68], effectively preventing its introduction into modern CMOS fabrication facilities. This may be resolved by using other catalyst materials, which are CMOS compatible. However, the particle-free method presents a simpler solution.

Chapter 4

III-V Nanowires Integrated on Silicon

Papers I and II describe how III-V nanowires can be grown epitaxially on Si substrates. In this chapter a background is first given to the topic of III-Vs on Si; particle-assisted growth of GaAs/InGaP nanowires on Si, and particle-free growth of InAs nanowires on Si, are then described.

The III-Vs do not have many of the shortcomings of Si (see Table 4.1 for a comparison of properties). For photon-emitting devices, Si is a "dead" material due to its indirect band gap.[1] Most III-Vs have a direct band gap and are the choice for applications such as telecom lasers (GaInAsP), blue laser diodes for optical storage (AlGaInN) and high-brightness light-emitting diodes (AlGaInN or AlGaInP). For electronics, the high electron mobility of, for example, InAs and InSb could enable high-speed, low-power devices; the high mobility allows a low drive voltage with maintained drive current [69]. Moreover, both photonic and electronic devices benefit from the advanced heterostructure technology available for the III-Vs. Heterostructure technology is also the key component for multijunction photovoltaics [70].

Although the III-Vs appear be the preferred choice for many applications, Si will probably remain the preferred platform for many applications for several reasons: it is available as large area wafers of extremely high purity and crystal quality, the material has good mechanical stability, it has a stable SiO_2 oxide, it is an extremely well-characterized material, and simply because immense investments

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[1]Si can be made to emit photons by, for example, introducing rare earth dopants, using very small crystal sizes, or using stimulated Raman emission. However, these technologies yet have to be proven for commercial applications.

Table 4.1: Selected material properties for Si and III-V semiconductors. Values at room temperature.

	Si	**III-Vs**
Band gap (eV)	indirect 1.12	generally direct wide span, InSb 0.163, AlN 6.02
Electron mobility (cm^2/Vs)	1900	InSb: 78 000
Hole mobility (cm^2/Vs)	500	GaAs: 400
Thermal conductivity (mW/cm · K)	1240	GaAs: 560
Wafer cost (111) orient. (EUR/cm^2)	$\approx$ 0.2 (4 inch)	$\approx$ 8 (GaAs 2 inch)
Heterostructure technology	Si/Ge	device-grade lattice-matched technology well-established

have been made in Si-based technology. Opportunities lie instead in the successful combination of the two material systems. However, for reasons discussed below, it has been difficult to achieve monolithic integration of III-Vs on Si. The small footprint of the nanowire/substrate interface may help to overcome many of these difficulties. If III-V NWs could be integrated on Si chips, they could provide standard CMOS with new functionality and could, for example, become a key component in fast on-chip optical communication [71, 72].

4.1 Planar Growth of III-Vs on Si

Much effort has been invested in achieving high-quality planar growth of III-Vs on Si [73, 74], and planar layers with defect densities as low as 10^4 cm^{-2} have been reported for GaAs on Si [75]. However, defect densities of $\sim 10^6 - 10^9$ cm^{-2} are more commonly reported [74]. For comparison, $\sim 10^5$ cm^{-2} is desirable for solar cell applications [74]. The high defect density is due to the difficulties encountered with planar layers in terms of mismatch in lattice parameters and thermal expansion, as well as anti-phase domain (APD) formation, which are described below.

First, if the lattice constant of the epilayer is not the same as that of the underlying substrate, the epilayer will initially try to adapt to the substrate lattice by changing its own natural bond lengths (pseudomorphic growth). However, as the epilayer grows thicker the energy stored in the strained epilayer will increase to a point where it is energetically more favourable to form crystal defects. The thickness at which this occurs is referred to as the *critical layer thickness*, and is of the order of 10 nm for a mismatch of 2 % (50 % Ge) in the Ge_xSi_{1-x}/Si system [64].

Table 4.2: Lattice mismatch of the III-Vs to Si (cf. eq. 3.4) and linear coefficient of thermal expansion. The lattice constant of Si is 5.43 Å. Comparison at 300 K, data from references [76, 77].

	Si	GaP	GaAs	InP	InAs	GaSb	InSb
Lattice mism. (%)	-	0.4	4.1	8.1	11.6	12.2	19.3
Therm. exp. $(10^{-6}/K)$	2.6	4.65	5.73	4.6	4.52	7.75	5.37

Second, mismatch of the thermal expansion coefficients of the substrate material and the epilayer causes problems similar to those of lattice mismatch. Epitaxy often takes place at high temperatures (typically 500 to 1100 °C), and thermal expansion mismatch between substrate and epilayer may cause severe strain upon subsequent cooling to room temperature, resulting in crystal defects and wafer bowing.
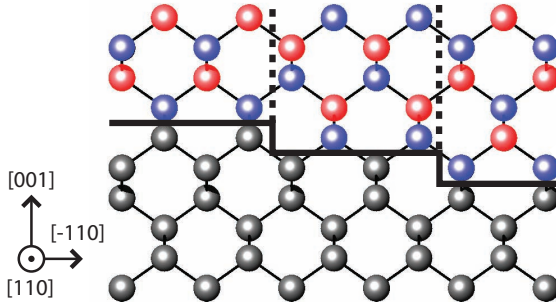
Figure 4.1: Anti-phase domain formation. APDs forming on a Si(001) surface with monoatomic steps. If the first deposited layer of the polar material consist of one species (coloured blue), APDs are created at the steps, as shown by the vertical dashed lines. Adapted from Kroemer et al. [78].

Third, APD defects may arise during the growth of polar materials on non-polar materials. APDs may be explained as follows. The Si diamond crystal structure can be described by two fcc sublattices displaced $\frac{a}{4}[111]$ from one another, where Si atoms occupy both sublattices. This is in contrast to the zinc blende structure

of GaAs (used as an example here), where Ga and As atoms occupy one sublattice each. For the first deposited GaAs layer on the polar Si surface, there is an ambiguity concerning the sublattice on which the Ga atoms should reside. If two domains where the Ga atoms reside in different sublattices grow together, the boundary will be defective with Ga–Ga and As–As bonds (anti-phase) (Fig. 4.1) [73, 79, 80].

As will be discussed below, NWs can partly circumvent the above three problems due to their small footprints.
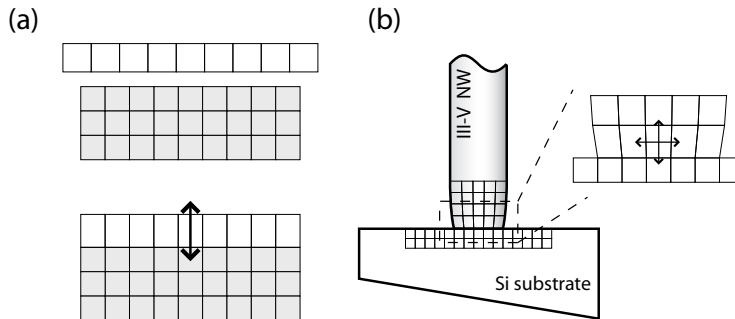
Figure 4.2: Illustration of the Si/III-V interface. (a) For planar growth, strain can only be relaxed along one dimension, normal to the heterointerface. (b) For the NW geometry, strain can also be relaxed laterally, allowing 3D strain relaxation. The III-V compounds are compressively strained at the interface if the growth is pseudomorphic.

4.2 Nanowire Growth of III-Vs on Si

The heterointerface mismatch problem is less serious for nanostructures because the small diameter allows strain to be relaxed laterally (cf. Section 3.3). This is in contrast to planar layer growth, where strain can only be relaxed along one dimension, normal to the heterointerface (Fig. 4.2). The critical thickness for nano-sized growth can thus be considerably larger than for planar growth [81, 82], and the critical thickness is replaced by a *critical diameter* [65, 83]. The strain is also observed to relax quickly along the axial direction. For an InAs/InP heterojunction in a NW with 20 nm diameter, the strained region was found to be confined to 10 nm around the interface [66].

Anti-phase domains form when two nuclei with different sublattice occupation grow together. However, NW growth is believed to proceed layer by layer, with a single nucleation event per layer [xiv]. Thus, there is a single nucleation event for the first deposited III-V layer on the Si crystal, and APDs are not expected

to form. Moreover, since growth takes place on the (111) surface orientation where only steps of double-atomic height exist, APDs cannot form if the first layer contains only one species (i.e., group III-, or group V-rich nucleation conditions).

It should be pointed out that even for nanoscale dimensions, the number of interface atoms is considerable. The Si(111)1x1 surface unit cell has an area $A_{1x1} = a^2\sqrt{3}/4$ and a surface atom density $\rho_{111} = 1/A_{1x1} = 7.83 \times 10^{14}$ cm^{-2}. The footprint of a 40 nm diameter NW thus contains approximately 10 000 Si surface atoms.

4.2.1 The Si(111) Surface

Because <111> are the most common growth directions for NWs, and because NWs normal to the substrate are usually desired, the (111) facet of Si is often used (this is in contrast to standard CMOS processing where the (001) orientation is used).

An oxide-free Si surface is necessary for epitaxial growth. One way of achieving an oxide-free surface is based on the formation of a volatile chemical oxide during wet cleaning, which is then desorbed at ≈ 800 °C. Another method, which is used in this work, is based on wet etching in hydrofluoric acid (HF). The two methods are commonly denoted hydrophilic and hydrophobic, respectively [84].

A Si surface from which the oxide has been stripped in HF is protected from oxidation by hydrogen passivation, meaning that the Si dangling bonds are terminated by hydrogen atoms [85]. A (111) surface from which the oxide has been stripped using HF is atomically rough, with monohydride, dihydride and trihydride groups [86]. However, Higashi et al. demonstrated that the smoothness could be much improved by increasing the pH of the etch solution [87], and proposed the use of pure ammonium fluoride (NH$_4$F) as etchant to achieve an atomically flat surface with monohydride, Si(111)-H, termination. Such a perfect surface is reported to be quite stable, and can even be handled for short times in ambient air without measurable oxidation [88]. However, the resistance to oxidation appears to be dependent on the quality of the termination, and with the simple HF-etch process used in our lab, some oxide formation was always observed when the samples were subjected to ambient air (an oxygen-related peak was observed with X-ray photoelectron spectroscopy and atomic resolution could not be obtained with scanning tunnelling microscopy, results not shown here). In other words, the onset of oxidation seems to be immediate when the Si surface is exposed to ambient air. Paper II describes how such a surface can be oxidized in a templated fashion by organic residues to form an oxide mask, which guides NW nucleation (see Section 4.2.3).

For Au-assisted NW growth on Si, the fact that Au accelerates the formation of SiO$_2$ [89] presents a problem. Si diffuses through Au even at room temperature to

form a SiO_2 layer on top of the Au, which is detrimental to uniform NW growth. This problem can be resolved by either depositing the Au particles on a freshly etched Si surface and grow with as little delay as possible, or etch the sample with the Au particles on in HF just before growth.

4.2.2 Particle-Assisted Growth of GaAs/InGaP Nanowires on Si

Paper I describes how GaP wires can be epitaxially nucleated on Si substrates from Au aerosol nanoparticles. GaP is a preferred material for nucleation of NWs on Si because of its low lattice mismatch to Si. The transition to GaAs, InAs, InP and their alloys from a GaP nucleation segment is then possible [32, 60]. The quaternary III-V compounds are widely used for optical applications, for example, AlGaInP for high-brightness LEDs, and GaInAsP for long-range telecom lasers.
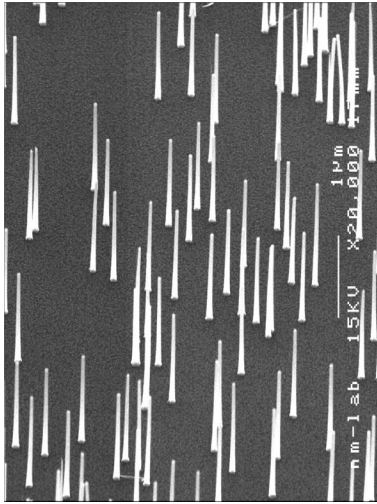
Figure 4.3: SEM micrograph of GaP NWs growing vertically from the Si(111) surface in the vertical [111] direction. The wires were grown using 40 nm seed Au aerosol particles. Tilt angle 45°.

The NWs grow vertically from a (111) substrate in the vertical [111] direction as shown in Figure 4.3. Both Au aerosols and lithographically patterned Au seeds (see Chapter 5) were successfully used for NW growth. The contact to the substrate is monolithic, and if the substrate orientation is changed from (111) to (001), the <111> growth direction is maintained. The wires then grow in the four equivalent <111> directions, separated by 90° azimuthally, with an angle ≈ 35° to the substrate surface (Fig. 4.4(a)).
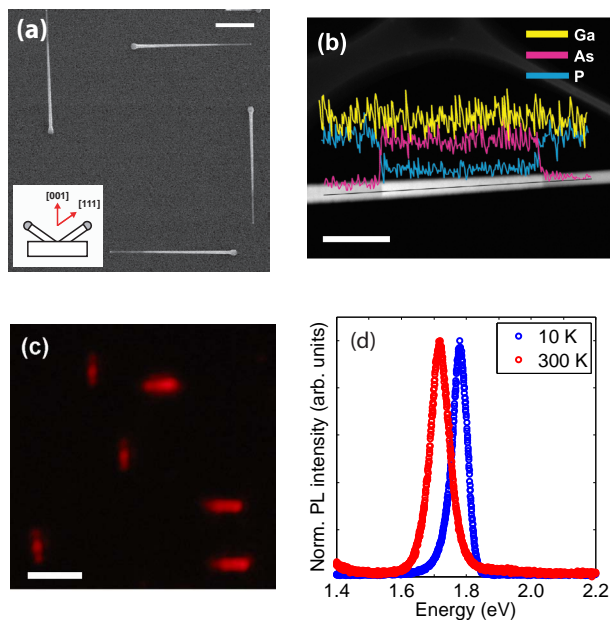
Figure 4.4: (a) Top view of NWs growing in the four inclined <111> directions available from the Si(001) surface; the angle is $\approx 35°$ to the substrate surface (inset). Scale bar 1 μm. (b) Scanning TEM image of a GaP NW with a GaAsP segment. An X-ray energy dispersive spectrometry (XEDS) composition line scan is overlayed. Scale bar 200 nm. (c) Room-temperature top-view photoluminescence (PL) image of as-grown wires on a Si(001) surface. Scale bar 5 μm. (d) Single-wire PL spectra from a wire resting on a SiO$_2$ surface. The FWHM linewidths are approximately 50 and 70 meV for 10 K and room temperature, respectively.

The optical properties of GaP/GaAsP/GaP wires are shown in Figure 4.4. Because pure GaP has an indirect band gap, heterosegments of optically active GaAsP material with a direct band gap were inserted during growth. These GaAs$_{1-x}$P$_x$ segments, where x can be tuned by adjusting the arsenic-to-phosphor precursor ratio during growth [63], can emit from 870 nm (pure GaAs) down towards 600 nm, depending on the P content. The lower limit is determined by the fact that the GaAs$_{1-x}$P$_x$ band gap becomes indirect for x $\gtrsim 0.5$ %.

To achieve high radiative efficiency, it is generally necessary to passivate the surface states or to move the surface away from the free carriers by growing a shell of a high-band-gap material around the active region [40, 90]. GaAs is advantageous as a core material in this respect as both Al$_{1-x}$Ga$_x$As and Ga$_{1-y}$In$_y$P can be grown lattice-matched to GaAs. Due to the similar bond lengths of Ga and Al, x can be chosen over a wide range, whereas y must be ≈ 0.48 to be lattice-matched to

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GaAs. The use of an InGaP shell is described in Paper V; this paper and the radiative efficiency of these structures are discussed further in Section 6.1.

Work on the InGaAsP NW material system on Si has also been carried out elsewhere, for example, at Philips Research Laboratories [91] and NTT Basic Research Laboratories [92, 93].

4.2.3 Particle-Free Growth of InAs Nanowires on Si

InAs is a promising material for high-speed, low-power electronics due to its high electron mobility, high electron saturation velocity and low-resistance contacts. Together with InSb, it is the best candidate for fast and low-power logic [69]. Several NW devices have already been demonstrated in the InAs/InP material system (Paper VI and [13, 94]), and the vertical wrap-gate FET [xxii][12, 95] is especially interesting for integration with Si substrates, and ultimately with CMOS.

The Au seed particles commonly used in NW growth are of concern regarding compatibility with CMOS processing; gold is an impurity in Si that traps electrons and holes by forming deep-level recombination centres [68]. There is a risk that traces of Au will contaminate process equipment or be incorporated into the NW structures themselves. Particle-free NW growth thus offers an attractive alternative to particle-assisted NW growth.

Paper II describes how an organic coating, leaving nanoscale residues, could be employed to oxidize a Si(111) surface in a templated fashion; this oxide mask could then be used to guide NW nucleation. In Figure 4.5 an HF-etched Si(111) surface, and the same surface coated with an organic film of allyl alcohol (C_3H_6O), are shown after InAs growth. The surface prepared with allyl alcohol exhibited approximately 1.5 μm long, untapered NWs, whereas only InAs crystallites were observed on the HF-etched Si reference surface. It was concluded that the organic residues left after the spin-coating process (Fig. 4.6(c)) locally inhibit the oxidation of the Si surface, effectively creating preferred sites for NW nucleation.

The growth of InAs NWs on such oxide-templated surfaces is homogenous over large areas and exhibits comparatively narrow size distributions. In Figure 4.7(a) the length distribution of a sample grown for 2 min is shown. The distribution is Gaussian with a coefficient of variation of 14 %. In panel (b) the mean lengths for a series of samples with increasing growth times are shown. The initial axial growth rate is high: Approximately 140 nm long NWs formed after only 5 s. When the NW length exceeds 1.5 μm, the growth rate approaches a constant value of 5 nms^{-1}. The high initial growth rate and the asymptotic behaviour were interpreted as being the result of a mass-transport phenomenon; initially, there is a mass transport contribution from the substrate surface to the NW growing tip, which then decreases as the tip grows further from the substrate surface.
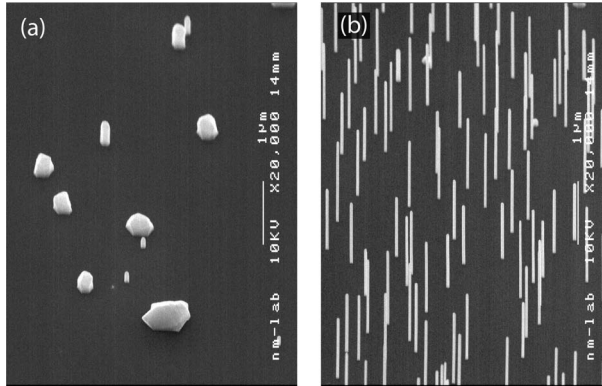
Figure 4.5: InAs NWs grown on Si(111) by the organic micromasking method. (a) Reference sample, growth on a HF-etched Si(111) surface. (b) as panel a but the surface was spun-coated with allyl alcohol after the HF-etch. Image tilt 45°.
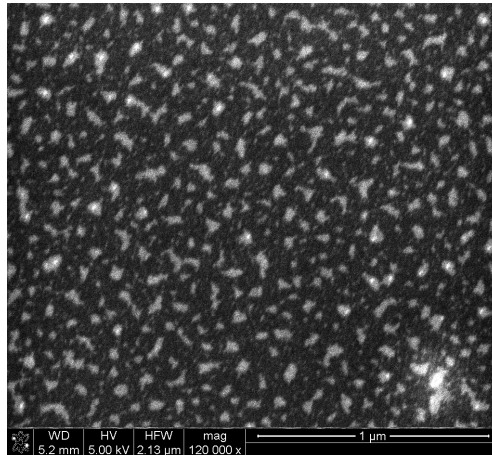
Figure 4.6: SEM image of the Si surface after organic spincoating with allyl alcohol. Nanoscale organic residues are seen as bright spots.

The organic micromasking method described in Paper II has the advantage of simple and inexpensive patterning of large areas; in this respect it resembles the Au aerosol approach. For exact site control, lithographic methods are necessary (see Chapter 5). Initial results are shown in Figure 4.8, where InAs NWs were grown on Si(111) out of the openings in a mask consisting of 30 nm thick SiO_2 thermal oxide. After successful nucleation of InAs on Si, the growth is expected to be similar to selective-area epitaxy (SAE) of InAs NWs on InAs substrates [96].

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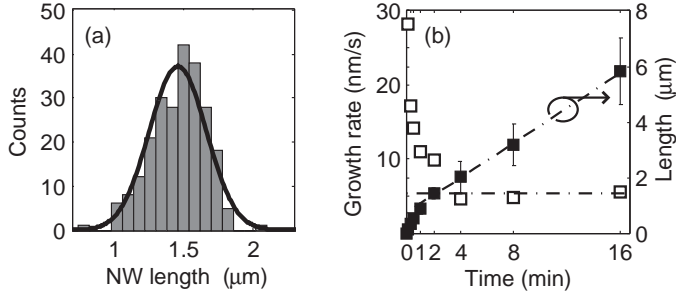
Figure 4.7: Growth data for InAs NWs grown with the organic micromasking method. (a) Length distribution of NWs grown for 2 min at 550 °C. The coefficient of variation for the Gaussian fit is 14 %. (b) NW length (right axis) and differential growth rate (left axis) versus growth time. A growth temperature of 550 °C was used.

4.2.4 Electrical Properties of the Si/III-V Heterointerface

In many possible device geometries, the electrical properties of the Si/III-V interface are of great importance. Unfortunately, little is reported in literature about this type of interface, and it is also beyond the main scope of this thesis. The topic is briefly addressed here due to its importance for the continued development of III-V devices on Si. Preliminary investigations on the Si/InAs interface are presented in Section 4.2.4.

The band alignment of two semiconductors across a heterojunction can be estimated by several methods. A common first approximation of the conduction band offsets is the difference between the electron affinities of the two materials. This is often referred to as the *electron affinity rule* [97]. The band offsets can also be estimated from first principle calculations [98], photoelectron spectroscopy measurements [99], or from electrical transport measurements with thermal or photo-excitation of the carriers [60, 100]. The local band structure is also affected by phenomena at the interface itself. Notably, any charge at the interface will induce band bending.

The Si/III-V heterointerface represents a transition from a non-polar material (Si with the diamond structure) to a polar material (III-Vs with the zinc blende or wurtzite structure) [78]. At an abrupt Si/III-V (111) interface, the first group III or group V monolayer constitutes a δ-charge layer with respect to the non-polar Si crystal. Harrison [101] argued that such an abrupt transition creates unrealistically large electric fields (band bending of the order of a few eV), and that the interface rearranges itself so as to cancel such large dipole shifts. After the rearrangement, the Si/III-V interface is not abrupt but includes several transition planes. To avoid the risk of dipole charges, a non-polar surface orientation can be used and
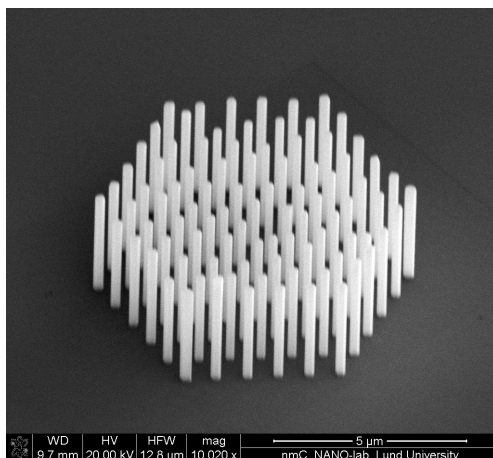
Figure 4.8: InAs NWs nucleated in the openings of a SiO$_2$ growth mask on a Si(111) substrate. Image tilt 45°. Bernhard Mandl et al., unpublished results.

Kroemer proposed the non-polar (211) orientation for growth [78].

Other effects at the interface which may alter the local band structure include: strain, crystal defects, for example, due to lattice mismatch or APDs, and autodoping from the Si/III-V interface mixing, with Si dopants entering the III-V crystal, and vice versa.

The InAs/Si Heterointerface

Figure 4.9 shows a cross-sectional TEM image of the interface between the Si substrate and InAs nanostructure. Crystal information is carried over the interface, and the crystal directions of the Si substrate and the InAs region at the interface align, Si[111] ∥ InAs[0001] and Si[110] ∥ InAs[11$\bar{2}$0]. The base part of the InAs nanostructure is wurtzite whereas the top part is pure zinc blende, in between a zinc blende–wurtzite polytype crystal structure is observed. The interface region itself exhibits a structure which could not be determined from these images. The lattice mismatch between InAs and Si is 11.6 %, and it is improbable that all the strain can be accommodated pseudomorphically. A complex pattern of twin boundaries at the Si/InAs NW interface was reported by Bakkers et al. [72]. The epitaxial relationship between the substrate and the NW was also investigated with high-resolution X-ray diffraction (Paper II). The data indicated a random rotation of the wires around their axes relative to the Si substrate (mosaicity) with a magnitude of only some tenths of a degree.

The conduction band offset of Si relative to InAs given by the electron affinity rule is χ_{InAs}[102] - $\chi_{\text{Si}} = 4.9 - 4.05 = 0.85$ eV. However, Mano et al. [99] estimated a value of 0.44 eV from synchrotron radiation photoelectron spectroscopy, and Van de Walle et al. report ≈ 60 meV from first principle calculations [98]. Clearly, there is a need for a more accurate determination of the band alignment of this type of heterointerface.

Very recently, we have fabricated wrap-gate FETs of InAs NW on Si, showing enhancement-mode operation [xxii]. The NW transistor geometry may also function as a test-structure for investigating the electrical properties of substrate/NW heterointerfaces, and an activation energy of approximately 200 meV for the Si/InAs conduction band off-set was obtained from temperature-dependent measurements. Future experiments will provide a deeper understanding of the electrical properties of the Si/InAs heterointerface, as well as study the feasibility of low-power, high-speed InAs NW FETs directly integrated on Si.
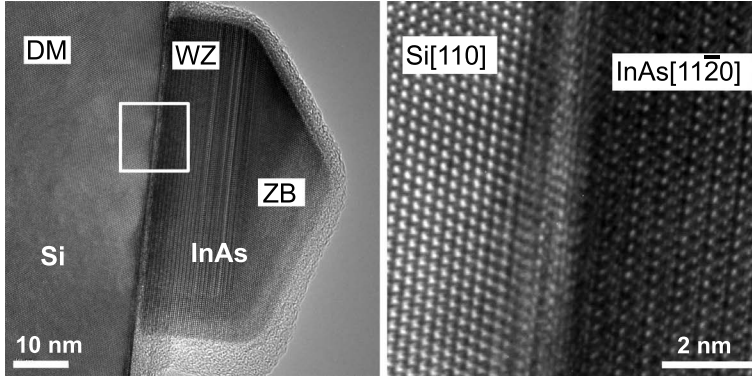
Figure 4.9: High-resolution TEM images of the Si/InAs interface. Si has the diamond (DM) structure. The InAs region closest to the interface is pure wurtzite (WZ), and the top part is pure zinc blende (ZB). The structure shown has a low aspect ratio compared with NWs. Unfortunately, thinner objects on the same sample were broken or bent during sample preparation, preventing observation. The area marked by a white square in the left panel is enlarged in the right panel. TEM images by Jakob Wagner and sample preparation by Anders Gustafsson.

Chapter 5

Lithographically Aided Formation of Nanowires

Papers III and IV describe how the position of individual nanowires on III-V substrates can be controlled by lithography. This technology was later extended to silicon substrates, which is described in Paper V. The current chapter describes why site control is necessary, briefly reviews the two techniques of electron beam and nanoimprint lithography, and discusses process issues and limitations of the technology.

Many applications of NW technology require exact position control of the NWs. There are two major means to achieve this. One option is *post-growth assembly*, where the NWs are removed from their original growth location and transferred for subsequent experiments or device fabrication. Methods of achieving this include, for example, micromanipulation [103], Langmuir-Blodgett assembly [104] and random transfer with subsequent identification by a coordinate grid. Post-growth assembly typically leads to *planar* device geometries (Paper VI and [105, 106]). However, a *vertical* geometry is preferred for many applications such as NW wrap-gate FETs [12], bioprobing (Paper VII and [xxi]) and photonic crystals [107, 108]. For a vertical geometry *as-grown positioning* must be employed. The NWs are grown epitaxially from a substrate at their desired positions; diameter, length and growth direction can also be controlled.

In Figure 5.1 three examples of applications requiring positioning of individual NWs are shown. To the left is shown how rows of free-standing GaP NWs can induce guidance of axons from living cells. The NW rows act like "fences", preventing axons from crossing a line, making it possible to sort and guide large numbers of
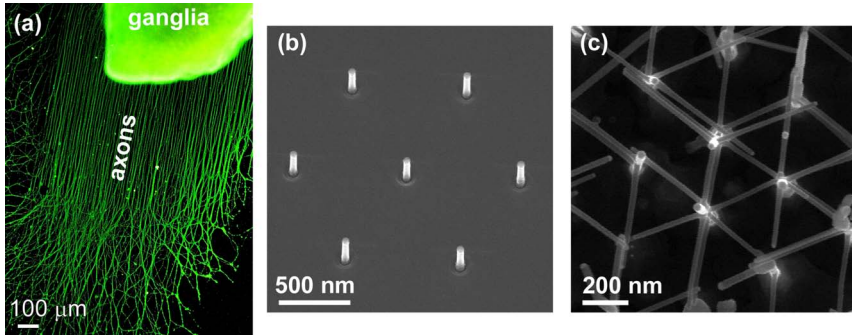
Figure 5.1: (a) Guidance of cellular processes: axons from ganglia on a NW-patterned surface. The axons are guided by rows of NWs. Fluorescence microscopy image [xxi]. (b) An array of vertical wrap-gate InAs NW FETs. The image shows an intermediate processing step. The substrate constitutes the source contact, and a Cr gate has been defined (not clearly visible in the image). Next, a top drain contact will be defined to complete the device [95]. (c) Position-controlled InAs NW network. The branches are seeded by randomly deposited Au aerosol nanoparticles and grow outward at right angles to the trunks in the $< \bar{1}100 >$ directions. Correct positioning of the trunk NWs ensures that branches grow towards neighbouring trunks, connecting them together [14].

axons [xxi] (see Section 6.3). In the centre panel an array of InAs NWs for vertical FETs is shown [95]. The rightmost panel displays "nanotrees" [viii] where the "branches" connect to neighbouring trunks to form arrays of interconnected nanostructures [14].

5.1 Site Control of Seed Particles using Lithography

Lithography is of paramount importance in today's technology [109, 110]. One application is the fine patterns used in the fabrication of integrated circuits found in computer processors, flash memories, camera CCD sensors, and so forth. It is a *top-down* technology, which in this work was used to provide site control for the *bottom-up* technology of NW growth. Lithography can either be used to define the position of the growth seed particles, or to open up areas in a growth mask where the NWs grow particle-free [53, 111]. The former was used in this work.

The generic process scheme for lithographically defined NWs is outlined in Figure 5.2. Both electron beam lithography (EBL) and nanoimprint lithography (NIL) were used, however, most steps are common and the two methods differ
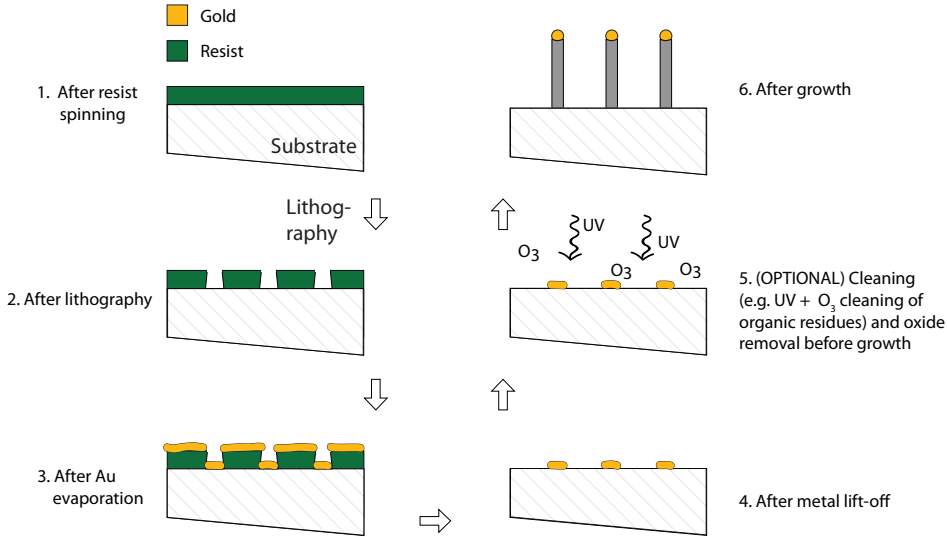
Figure 5.2: Process for site-controlled particle-assisted NWs defined by lithography.

only in the lithography step, which is discussed separately in Sections 5.1.1 and 5.1.2. In the first step the substrate is covered with a electron beam resist (EBL) or imprint polymer (NIL). The polymer layer is patterned by electron beam exposure or a nanoimprint stamp. After nano-sized apertures have been defined in the polymer layer, a thin metal layer (commonly Au, 1-50 nm thick) is thermally evaporated onto the sample (step 3). The resist is then dissolved in an organic solvent lifting the metal on top of the polymer off, leaving only the gold in the apertures. In Figure 5.3 a top view SEM image of a Au seed particle array corresponding to step 4 is shown. An optional cleaning step (step 5) can be inserted before growth; organic residues can be removed with piranha solution, or with UV-light combined with ozone [112], and surface oxides can be removed by wet etching. The sample is then transferred to a growth system where the NWs are grown (step 6).

5.1.1 Electron Beam Lithography

Paper III describes how EBL was used to define Au seeds for NW growth. In EBL, a focused beam of electrons is scanned over a surface covered with a polymer resist sensitive to the electron radiation (Fig. 5.4(a)). The polymer is chemically altered by the electron radiation so that the exposed areas are either selectively dissolved (positive resist), or left intact while surrounding areas are dissolved (negative resist), in a subsequent developer bath.

In theory, extremely high resolution can be obtained with EBL as an electron
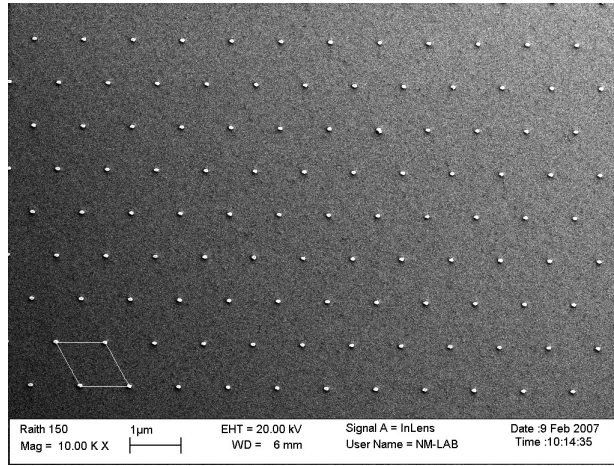
Figure 5.3: Gold seed particle array on a Si substrate produced by EBL. A PMMA/LOR double-layer resist was used. A Raith-150 system was used for exposure (electron energy 20 keV, single pixel dot exposure mode, dose 20 pAs). The pattern pitch is 1 μm, the 1×1 unit cell is indicated in the lower left corner.

accelerated to 50 keV has a de Broglie wavelength of only 5.6 pm. However, the resolution is not limited by diffraction but by aberrations in the electron lenses. Moreover, the resolution when working with polymer resists is limited by forward electron scattering and secondary electrons in the resist [109]. The resolution is still very good; 10 nm wide metal lines have been reported on GaAs [113], and NWs have been grown from 20 nm diameter lithographic Au seed particles in our laboratory. Modern EBL systems can expose 100 nm diameter holes at a rate of $\sim$ 1000 holes/s,[1] which is fully sufficient for academic research and industrial research and development. However, compared with parallel techniques such as photolithography or NIL, EBL is slow due to its serial nature. The long write times are the main disadvantage of EBL as a production technology.

Although a single-layer resist scheme was used for the initial work (Paper III), double-layer resist stacks are more suitable for lift-off processes. The reason is that the resist profile must have a negative slope to create a discontinuity between the gold film on top of the resist and the Au film in the exposed areas (cf. Fig. 5.2, step 3). The pattern displayed in Figure 5.3 was produced using a stack of poly(methyl methacrylate)/lift-off resist (PMMA/LOR$^{\text{TM}}$) [114]. The topmost layer of PMMA is exposed with an electron beam and developed. The LOR is then separately dissolved in a "developer". The amount of undercut is controlled by the LOR developer time. The undercut profile guaranties a discontinuity in the thin Au

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[1] JEOL-JBX9300FS, area exposure mode, dose 120 μC/cm^2
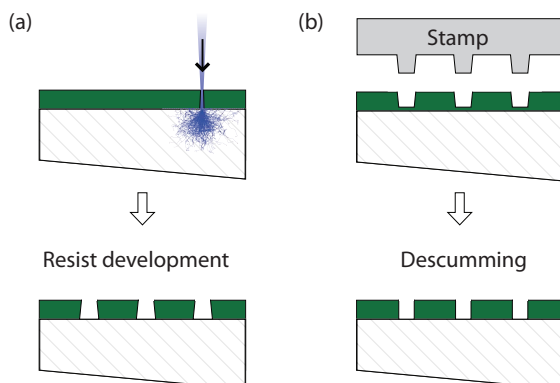
Figure 5.4: The imaging process steps of EBL (a) and NIL (b). In EBL the pattern is "written" by an electron beam, whereas in NIL the features of a stamp are transferred to an image layer. The end results are very similar. Image dimensions not to scale.

film so that the Au dots are readily separated from the rest of the Au film in the lift-off process.

5.1.2 Nanoimprint Lithography

In NIL, a stamp is pressed into a patterning medium for feature replication. The patterning medium is commonly a polymer (Fig. 5.4(b)). In the original process, thermal imprinting, the polymer is heated above its glass transition temperature, and the stamp is pressed into the polymer under high pressure. The viscous polymer reflows to adapt to the stamp. The substrate and stamp are subsequently cooled to a temperature below the polymer glass transition temperature, and the stamp removed, whereupon the polymer retains the imprinted structure. A plasma etch step (descum) is then usually employed to ensure full removal of the resist from uncovered areas.

Paper IV describes how NIL was used to define the Au seeds for NW growth. It was shown that a Si stamp could be used for imprinting on InP(111)B substrates, and that the process was suitable for epitaxy. A resist bilayer scheme, similar to the PMMA/LOR stack discussed above, was used [115][2]. NW growth from NIL-patterned samples was compared with that of EBL-patterned samples, and it was found that the two methods produced virtually equivalent results.

NIL is a parallel process capable of high wafer throughput. The stamp is usually fabricated by serial methods such as EBL, but once the master has been fabricated

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[2]PMMA 50k/LOR2000 resist stack, 3 min imprint at 220 °C, 50 bar imprint pressure
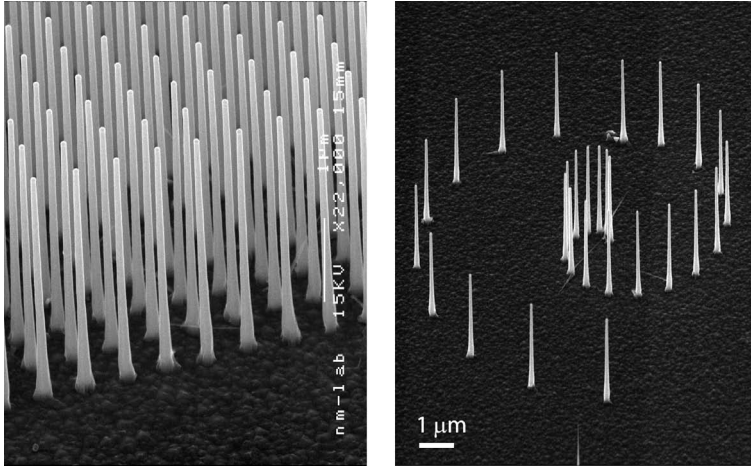
Figure 5.5: InP NWs grown on an InP(111)B substrate. Left: Square lattice with pitch 0.5 μm. The length is $\approx$ 3.5 μm with a tip diameter of $\approx$ 80 nm. Right: Example of design freedom: a hyperbolic spiral defined by NWs. For both panels, Au seeding discs with a nominal diameter of 70 nm and nominal thickness of 23 nm were used. The growth time was 12 min, growth temperature 400 °C and TMIn and PH$_3$ were used as precursors.

it can be used repeatedly. Wafers as large as 8 inches have been imprinted with satisfactory results [116]. Vendors of imprint systems currently promise processing on up to 8 inch wafers at a throughput of 30 wafers per hour [117]. Sub-10 nm Au dots have been defined using NIL and subsequent metal evaporation and lift-off [118].

5.2 Nanowire Growth from Lithographic Gold Patterns

With lithographic design, the position as well as the diameter of each NW can be controlled. In Figure 5.5 two examples of patterned InP NW structures are shown. In the left panel a dense array with 0.5 μm pitch in a square lattice is shown. Compared with wires grown from Au aerosol particles, length and diameter uniformities are much improved. In the right panel a hyperbolic spiral was chosen to illustrate freedom of design. The growth parameters of these structures were similar to those of growth from Au aerosols.

It is important to note that the structures in Figure 5.5 represent results obtained after substantial process optimization. The combination of top-down lithography

and bottom-up epitaxy is challenging and requires great care; a non-ideal process scheme or processing mistakes are often not revealed until after the epitaxy has been carried out. A structure that looks ideal under SEM (cf. Fig. 5.3), may for example, prove to suffer from contamination (Fig 5.6(a)). In this sense, nanowire epitaxy is an extremely sensitive technique for identifying contaminations on the growth surface, often on the monolayer level. These challenges are exemplified by four major problems, which were subsequently solved.

In Figure 5.6(a) a sample with parasitic NW growth covering the surface is shown. Parasitic wire growth was found to result from several contaminants, especially metals. In our process it was, for example, observed that (under certain conditions) the evaporated Au (Fig. 5.2, step 3) could penetrate the resist down to the substrate surface and cause parasitic growth. By optimizing the process steps prior to the Au evaporation, parasitic wires could be practically eliminated (cf. Fig. 5.5).

A second major problem is distortion of the designed NW pattern that may result from particle–substrate interactions prior to axial NW growth. The gold particles have, for example, been observed to spread and form a wetting layer on GaAs substrates [119], and the gold often forms alloys with the substrate. In Figure 5.6(b) a 5×5 square NW array is shown after growth. The white rectangle illustrates the original grid. Distortion of the designed grid was found to be more severe for larger particles, and especially for Ga-containing substrates, GaAs and GaP, compared with InAs and InP. This may be due to the difference in alloying behaviour between Au/Ga(As,P) and Au/In(As,P) [120]. For silicon substrates the pattern retention was excellent (Paper V).

In Figure 5.6(c) multiple wires can be seen to grow from each Au disc. Lithographic seed discs are different from aerosol particles in that they are not spherically symmetric and have lower crystalline perfection. For a thin and wide disc (rightmost structure in panel (c)), the surface tension causes the disc to break up into multiple droplets upon heating, much like growth from thin films [27, 121], failing to produce single wires.

In the fourth and last example, GaP NWs grown on a Si(111) substrate are shown (Fig. 5.6(d)). Multiple wires are observed from each Au dot, growing in one of the four available <111> directions (inset). Similar behaviour was observed by Roest et al. [91]. Under the same growth conditions, Au aerosol particles created well-defined single wires in the vertical growth direction (Paper I). The difference is believed to be the poorer crystallinity or different alloy behaviour of evaporated Au discs compared with Au aerosols. The nucleation from Au discs was much improved by optimizing the *in situ* annealing cycle prior to growth, and well-defined GaAs NW arrays were demonstrated on Si in Paper V.

It is interesting to determine the ultimate limitation in pattern density. For dense patterns the lithography becomes challenging, and movement of the particles prior
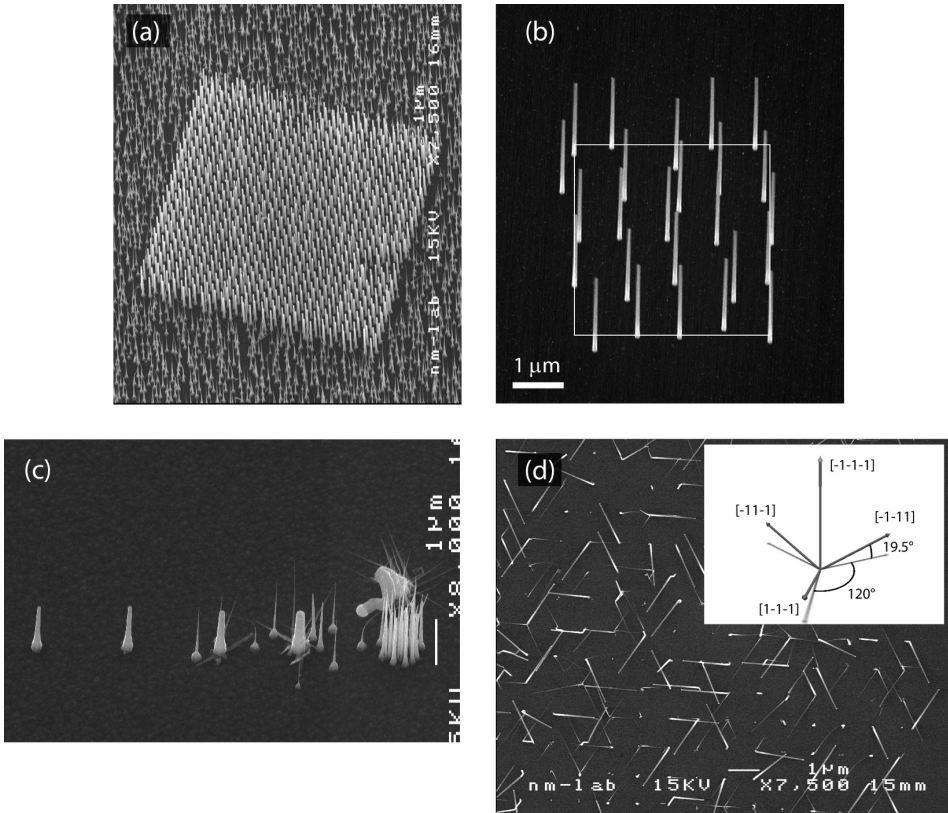
Figure 5.6: Process and growth problems associated with NW growth from lithographic Au particles. (a) Parasitic NW growth due to contamination during processing. (b) Distortion of design grid due to particle movement. GaP NWs on GaP(111)B substrate. The EBL design was a 5×5 grid with 1 μm pitch. (Image courtesy of Patrik Svensson.) (c) Impact of Au disc aspect ratio. Thickness fixed at 17 nm. Height-to-thickness ratios are (left to right) 1/3, 1/6, 1/12, 1/24 and 1/48. The 1/3 ratio is ideally where a disc reshapes to a hemisphere without altering its footprint area. (d) Top view SEM image of GaP NWs growing on a Si(111) surface. Multiple wires and multiple growth directions per lithographic Au particles are observed. The growth directions are the four available <111> directions (inset).

to growth may cause adjacent dots to merge and result in loss of pattern. However, both EBL and NIL have demonstrated features in metal of 10 nm or less [113, 118], and NWs as small as 3 nm in diameter have been reported [26]. A square grid NW array with a 20 nm pitch should in principle be possible, which corresponds to a density of $\sim 10^{11}$ cm^{-2}. This can be compared with the present DRAM (dynamic random access memory) density of $\sim 10^{9}$ bit/cm^{2} [122], and the hard drive density of $\sim 10^{11}$ bit/cm^{2} [123] (no further comparisons implied). For most applications more readily attainable dimensions are sufficient. In Figure 5.7 a double row of NWs with 120 nm pitch, which is the smallest fabricated hitherto in our laboratory, is shown. It was designed to act as a 3D framework with enhanced sensitivity for surface-enhanced Raman scattering [xx].
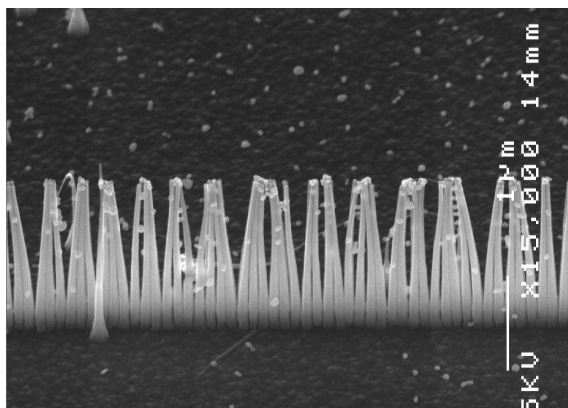
Figure 5.7: SEM image of a double NW row with 120 nm pitch. The wires are decorated with Au nanoparticles and were used for surface-enhanced Raman scattering studies. Molecules were applied from a liquid, and subsequent drying caused the wires to bend due to the capillary force [xx].

Chapter 6

Nanowires in Photonics, Electronics and Life Sciences

Various aspects of NW growth have been described in previous chapters. In most cases the motivation for developing growth techniques was to use them in particular applications, and in the current chapter I describe three different areas of application: photonics, electronics and the life sciences.

In Section 6.1 a NW light-emitting diode is described, and in the following section a NW single-electron transistor is described.

In Section 6.3, the interaction of NWs with living sensory nerve cells is presented. Unlike the previous sections, where the electrical and optical properties of the NW were in focus, the topography and surface chemistry of NWs are the crucial parameters here. The diversity of these three examples demonstrates the versatility of NWs.

6.1 Nanowire Light-Emitting Diodes

In Paper V a vertical nanowire light-emitting diode on Si is reported. In this section a short general introduction to LEDs is given, and the GaAs/InGaP nanowire LED is then described. Lastly, a brief outlook on the second generation of nanowire LEDs, based on nitrides for white-light generation, is included.

A LED converts electrical energy to light. Compared with incandescent light sources, such as the light-bulb, it has the advantages of a considerably longer lifetime and lower energy consumption.

The modern type of LEDs, where light emission takes place at a p–n junction, were demonstrated in the early 1960s [124]. These early LEDs were based on GaAs material and emitted in the infra-red wavelength region. By introducing phosphorus, the wavelength could be moved into the visible, and red GaAsP LEDs for calculators, wrist watches and so forth, were sold in volume at the end of the 1960s. Today, two main materials systems are used for high-brightness, visible light LEDs: AlGaInN for blue and green, and AlGaInP for amber and red. The AlGaInN system is also used for white-light LEDs by using short wavelength blue emission together with a phosphor coating for photon energy down-conversion.
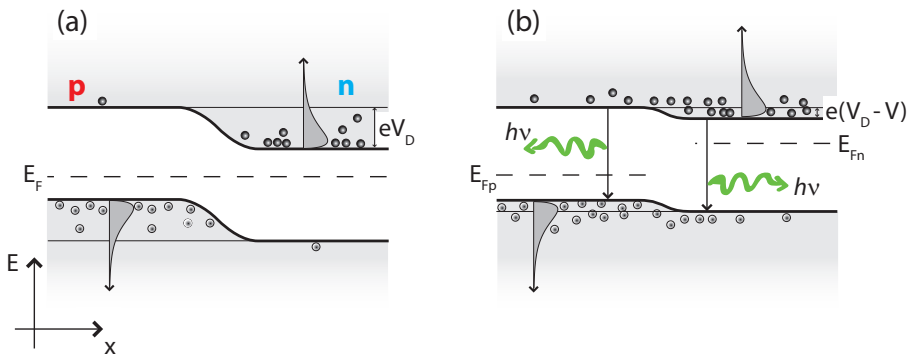
Figure 6.1: Unbiased (a) and forward biased (b) p–n junctions. (a) At zero bias few majority carriers have enough thermal energy to pass the diffusion voltage barrier eV_D (the majority carrier concentrations are illustrated at the conduction and valence band edges). By applying a forward bias V the barrier is lowered to $e(V_D - V)$, and majority carriers are injected over the barrier.

6.1.1 LED principles

At the core of a LED is a p–n junction, the principles of which are shown in Figure 6.1. In a p–n junction, the diffusion of free electrons from the n-side into the p-side, and the diffusion of holes in the opposite direction, create a built-in electric field due to the ionized dopants left behind. This built-in electric field creates an energy barrier for the majority carriers, of height eV_D, where V_D is often denoted the *diffusion voltage*. At thermal equilibrium, few majority carriers have enough energy to pass the diffusion voltage barrier (Fig. 6.1(a)). However, if a forward bias V is applied, it reduces the barrier height to $e(V_D - V)$, and more majority carriers will have enough energy to pass the barrier (Fig. 6.1(b)). Electrons injected into the p-side will recombine with the hole majority carriers and generate photons with an energy corresponding to the band gap of the semiconductor (the opposite applies to holes injected into the n-side). This is known as *radiative recombination*. Virtually all high-brightness LEDs also employ one or several wells of a low band gap material at the p–n junction. The well collects carriers and increases the local concentration of electrons and holes, which enhances the radiative recombination rate.

In practise, there are several loss mechanisms in a LED; not all recombinations are radiative, and non-radiative recombinations generate phonons (heat) rather than light. The ratio of radiative transitions to the total number of transitions is called the *internal quantum efficiency*, denoted η_i. Because many other factors, such as contact resistance and light extraction, also determine the efficiency of the device, other quantities are used to measure the efficiency of a device. For infra-red and UV LEDs, the *power efficiency* (also termed wall-plug efficiency), which is the radiant flux divided by the electrical power, $\eta_p = P/IV$, is commonly used. A typical value for infra-red LEDs marketed in 2008 was $\eta_p \approx 20$ % [125]. For visible wavelength LEDs, the eye's sensitivity to different wavelengths is usually taken into account, and the measure luminous flux (measured in lumens) is used instead of the radiant flux. In 2008 a typical high-power white LED available on the consumer market had a *luminous efficiency* of $50 - 80$ lm/W, depending on the operating current [126]. For comparison, incandescent tungsten light-bulbs typically have an efficiency of $15 - 20$ lm/W. The above values should be compared with the theoretical maximum of approximately 375 lm/W for a white light source [127], which is still far away.

6.1.2 Nanowire LEDs

Nanowire LEDs have been fabricated in a variety of different materials and geometries [9, 62, 105, 106, 121, 128, 129] and are attractive for several reasons. Nanoscale crystals are often free from extended crystal defects such as threading dislocations, which can degrade the optical performance of the material by act-

ing as non-radiative recombination centres. Thus, "nano-LEDs" essentially free of defect-related non-radiative recombination and with high internal quantum efficiency may be feasible. However, with new structures, new challenges are also introduced: especially the large surface-to-volume ratio of nanostructures which pose a problem as interface states often act as non-radiative recombination centres [124].

There is also hope that the light extraction from LEDs can be substantially improved by nanostructuring the surface (for example by placing NWs in regular 2D arrays, cf. Chapter 5 and Paper IV) to make use of photonic crystal effects [107], and thus avoid the light being trapped by total internal reflection [129–131].

Besides application as a highly efficient light source, a second major area of interest is the use of NWs as nanoscale light sources for on-chip integration. A specific example is intra-chip communication that today uses copper interconnects that could be replaced with optical interconnects [132]. Considerable efforts are already being made to develop laser sources integrated with Si for communication [133], and NW LEDs may have an important role to play in this field [71, 72]. Moreover, because the NW geometry lends itself to the incorporation of quantum dots using heterostructures [8, 134], and, importantly, because the quantum dot can be electrically contacted with the NW ends acting as electric leads, a NW LED could also function as a single-photon source [9]. Single-photon sources are highly desirable in quantum cryptography, which enable eavesdropping-safe information transfer by the fundamental laws of quantum mechanics.

6.1.3   Monolithic GaAs/InGaP Nanowire LEDs on silicon

The small footprint of NWs enables them to accommodate strain arising from lattice and thermal expansion mismatch, and to avoid other growth-related problems such as anti-phase domains (see Chapter 4). More specifically, it is possible to nucleate GaAsP NWs on Si from Au aerosols or lithographically patterned Au seeds (see Section 4.2.2 and Chapter 5) for use in NW LEDs. Monolithic integration with Si has the advantage of placing the LED on an inexpensive and stable carrier substrate, as well as providing the opportunity for integration with CMOS technology.

In Figure 6.2 a side view image of NW LEDs is shown. The device is a core-shell LED structure with selective growth of the shell material on the upper part of the NW. To form this structure two growth steps were employed. First, 2 μm long GaAs NWs were grown on p-type GaP(111)B or Si(111) substrates. To protect the active GaAs region, the NWs were capped with an InGaP layer nominally lattice-matched to the core. A SiO$_2$ layer was conformally deposited over the NWs and etched back to cover only the substrate surface and the lower part of the NWs. The samples were then reloaded into the MOVPE reactor, and a radial
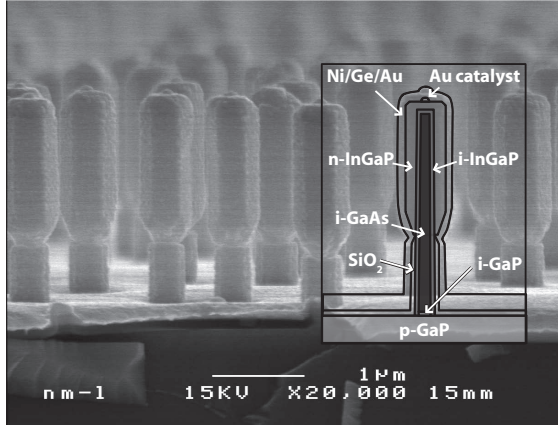
Figure 6.2: Side view SEM image showing functional NW LEDs (Paper V). The structure of the device is shown in the inset. The p-type substrate is used for hole injection, and the n-type cladding is used for electron injection.

Si-doped InGaP layer was selectively grown on the upper part of the GaAs/InGaP core structure. A metal contact was deposited over the n-type InGaP cladding layer for electron injection, and the p-type substrate was used for hole injection. A finished device, mounted for optical and electrical characterization, is shown in Figure 6.3.

In Figure 6.4 the light–curren curve and the electroluminescence spectra for two NW LEDs are shown; a LED on a Si substrate is shown together with a reference device on a GaP substrate. The LED on GaP lights up at lower current than the LED on Si, and at 100 mA, the output power is approximately 13 times higher for the LED on the GaP substrate. The electroluminescence (EL) spectra are shown for 100 mA current load in Figure 6.4(b). Due to the opaque metal contacts used, the external efficiency of the device cannot be correctly measured. However, measuring the light that escapes from under the $200 \times 200 \ \mu m^2$ contacts, the wall plug efficiencies at 80 mA were found to be 8×10^{-4} for devices grown on GaP substrates and 5×10^{-5} for devices grown on Si substrates.

For efficient room temperature operation, thermal quenching must be minimized. Thermal quenching is due to non-radiative recombination centres that are temperature-activated. These centres are defects of some kind in the crystal (e.g., foreign atoms, dislocations and anti-sites), or surface states, which exhibit energy levels inside the band gap of the host crystal. Transitions via these levels usually generate phonons (heat) instead of photons [124].

The fact that non-radiative recombination processes are temperature-activated can be used to assess the internal quantum efficiency at room temperature. The
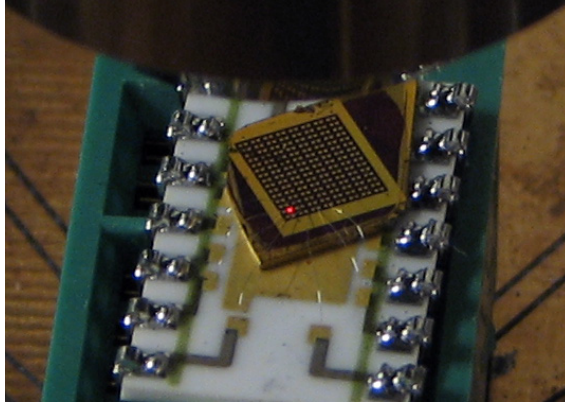
Figure 6.3: NW LED chip mounted for electrical and optical characterization. The underside contact was achieved by mounting the GaP substrate on the chip carrier with conducting silver paste. Device areas of $200 \times 200 \ \mu m^2$ were then contacted by bond threads and are seen to light up upon biasing. (Image courtesy of Patrik Svensson.)

decrease in PL intensity from low temperature (ideally absolute zero) to room temperature is an upper limit of the internal quantum efficiency: $\eta_i \leq \frac{I_{RT}}{I_{LT}}$, where equality occurs if the recombination at low temperature is 100 % radiative, that is, $(\eta_i)_{LT} = 100$ %.

For the best NWs grown on GaP substrates, the decrease in PL intensity was a factor of 20, and thus η_i for these NWs was $\lesssim 5$ %. The corresponding values for NWs grown on Si was $\eta_i \lesssim 0.1$ %. This should be compared with commercial planar GaAs LEDs, which typically have $\eta_i \gtrsim 90$ % [135]. The low efficiency has been attributed to surface effects [40, 90], and GaAs is particularly affected in this respect because of its high surface recombination velocity of 10^6 cm/s (compared with InP: 10^3 cm/s and GaN: 5×10^4 cm/s [124]). A high-quality shell seems to be necessary to achieve a high internal quantum efficiency [40, 90]. Another possible source of non-radiative recombination may be the abundant (111) twin planes in the GaAs core; Joyce et al. reported an increase in radiation efficiency upon the elimination of twin planes [136].

The fact that the NW LEDs on Si displayed lower PL and EL intensity than devices on GaP substrates is intriguing and is not yet understood. The device grown on Si could possibly be doped with Si from the substrate [93, 137], giving rise to other recombination possibilities via defect complexes with emission at lower energies. This could also explain the low energy tail of the EL spectrum (Fig. 6.4(b)). A second explanation of the poor efficiency of the Si devices could be that the shell growth conditions were optimized for growth on GaP substrates. As the PL intensity was observed to depend strongly on the shell composition (see

Paper V, Fig. 3(d)), unoptimized shell growth conditions on Si substrates may have reduced the efficiency considerably.
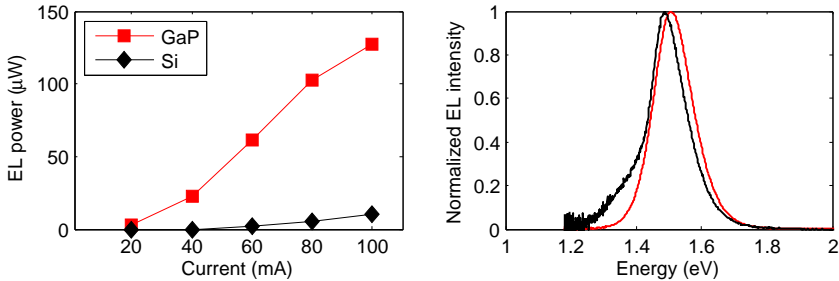
Figure 6.4: Nanowire LED electroluminescence (EL). (a) EL power (radiant flux) as a function of drive current (LI curve) for devices fabricated on GaP and Si substrates. The size of the device was $200 \times 200 \ \mu m^2$ containing approximately 40 000 NWs. (b) EL spectra at 100 mA from GaP and Si-based diodes. The peak wavelengths are blue-shifted compared with the GaAs bulk band gap of 1.42 eV at room temperature, probably due to compressive strain from the shell.

In the continuation of this work several things are of interest. First, we note that both materials for high-brightness visible LEDs (AlGaInP) and telecom applications (GaInAsP) should be attainable on Si with the technology demonstrated here, based either on direct nucleation on Si, or by starting from a GaP nucleation segment on which these materials are grown. Second, an optically active NW device as part of a photonic crystal structure [107, 108] may lead to novel applications.

6.1.4 Outlook — Nitride Nanowire LEDs

The nitride LEDs were made at GLO AB (part of the QuNano group), which is acknowledged for allowing me to show some of the results here.

The nitride material system, AlGaInN, is the prime candidate for general solid state lighting. However, there is no ideal substrate for nitride epitaxy. Bulk GaN crystals only exist in research labs, and it is unclear whether commercial production of GaN wafers will ever be possible. Currently, white-light LEDs are fabricated in a planar geometry, where the nitride LED structure is grown on sapphire, silicon carbide, or recently also silicon substrates. Growth on a lattice-mismatched substrate, such as sapphire or silicon carbide (or worse yet Si), results in material with a high dislocation density of $\sim 10^8 \ cm^{-2}$ [138], and although the optical properties of the nitrides display a remarkable tolerance to these high

dislocation densities, dislocation-free nitride NW LEDs [106, 129] may play a role in further increasing the efficiency.

In Figure 6.5 an array of nitride NWs grown by selective-area MOVPE is shown. This high-quality material forms the basis for a NW nitride LED.
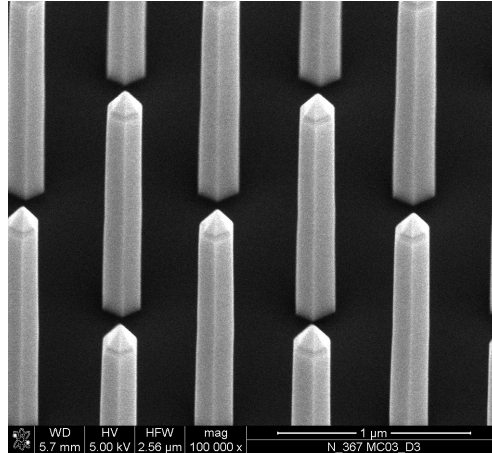
Figure 6.5: GaN NWs grown by selective-area epitaxy. (Image courtesy of GLO AB.)

6.2 Nanowire Single-Electron Transistors

Paper VI reports the fabrication of a nanowire single-electron transistor (SET). In this section, the SET concept is described, and the fundamental equations for charge transport are given. The InAs/InP heterostructure nanowire SET is then described.

A SET belongs to the family of single-electron devices [139], where single charge quanta of $e \approx 1.6 \times 10^{-19}$ coulomb are manipulated. Single-electron devices are expected to have applications in areas such as non-volatile memories, electrometry and current standards. Single-electron transistors have been used, for example, as ultra-sensitive charge detectors [13], and the so-called single-electron turnstile [140] can deliver DC currents of extreme precision with a relative standard deviation $< 10^{-6}$. However, single-electron devices often only function at cryogenic temperatures and their sensitivity to random background charges, introduced during manufacture, has so far limited their commercial use.

The SET [141] consists of a small conducting island that is connected via tunnel junctions to two electrodes, the source and the drain, and capacitively coupled to a third gate electrode (Fig. 6.6). Due to Coulomb repulsion between the negatively charged electrons on the island, work is required to add further electrons to the island. This has important consequences for the electron transport over the island. As discussed below, electrons can only tunnel to the island for specific potentials of the three electrodes and, importantly, for small source–drain biases, *electrons can only pass the island one by one.*
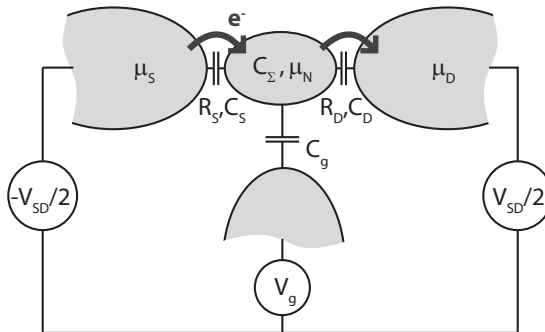
Figure 6.6: The SET. A small island is connected to two electrodes, the source and the drain, via tunnel junctions. A third electrode, the gate, is capacitively coupled to the island.

The first SET was realized by Fulton et al. by employing crossed aluminium metal stripes with an oxide tunnel barrier in between [142]. Since then, SET devices have been fabricated with a variety of different methods, such as electrostatically defined tunnelling barriers [94, 143], tunnel barriers formed by AFM manipulation of metal nanoparticles [144], and tunnel barriers defined by epitaxial heterostructures. With the last-mentioned method, Kouwenhoven et al. etched vertical pillars in a semiconductor substrate containing two epitaxial barrier layers, to create a small central island (quantum dot) connected by tunnel barriers [145]. This structure resembles the NW SET which is shown in Figure 6.7 and discussed in Section 6.2.2. However, an important difference is that the NW SET is epitaxially grown as a one-dimensional structure rather than etched, which avoids crystal damage caused by the etching process.

6.2.1   Energy Structure and Charge Transport in a SET

In the so-called *constant interaction model* [146], the total energy of a semiconductor island with N electrons is the sum of the single-particle levels $\sum_{i=1}^{N} \epsilon_i$, and the electrostatic energy of the island $U(N)$,

$$E(N) = \sum_{i=1}^{N} \epsilon_i + U(N) \tag{6.1}$$

The single-particle levels can be calculated from the Schrödinger equation, and the electrostatic energy can be calculated classically [146], giving:

$$E(N) = \sum_{i=1}^{N} \epsilon_i + \frac{e^2 N^2}{2C_\Sigma} + eN \sum_{j=1}^{n} \frac{C_j}{C_\Sigma} V_j \tag{6.2}$$

where V_j is the voltage of the jth external electrode, C_j is the capacitance between the island and the jth electrode, and C_Σ is the total capacitance of the island. The energy required to add the Nth electron to the island is the chemical potential[1],

$$\mu(N) = E(N) - E(N-1) = \epsilon_N + \frac{e^2}{C_\Sigma} \left(N - \frac{1}{2} \right) + e \sum_{j=1}^{n} \frac{C_j}{C_\Sigma} V_j \tag{6.3}$$

Here, the number of electrodes is limited to three: source, drain and gate. The level spacing,

$$\Delta \mu_N = \mu(N) - \mu(N-1) = \Delta \epsilon_N + \frac{e^2}{C_\Sigma} \tag{6.4}$$

is referred to as the *addition energy*, where $\Delta \epsilon_N$ is the difference between the single-particle levels, $\epsilon_N - \epsilon_{N-1}$. The term that results from electrostatics, $\frac{e^2}{C_\Sigma}$,

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[1]also called Fermi level, these are used interchangeably.

is referred to as the *charging energy*. As discussed below, the charging energy dominates for large islands, whereas for small islands (quantum dots), quantization effects will be important and the single-particle level contribution significant (see e.g. [8, 94, 145]).

To study the charge transport through the island, the gate voltage, V_g, and the source–drain bias, V_{SD}, are varied.[2]

(i) Effect of sweeping V_g. Assume that we start from a blocked state as depicted in Figure 6.8(a). For a small V_{SD}, there are no energy levels available in the island for electrons to tunnel into; a current will only flow if one of the island energy levels lines up with the source and drain electrode Fermi levels, $\mu_S \approx \mu_D$. Because the gate shifts the island energy levels by $e\frac{C_g}{C_\Sigma}V_g$ (Eq. 6.3), a gate sweep will give rise to conductance peaks when the island energy levels pass the source and drain Fermi levels (Fig. 6.8(b)). The spacing of the conductance peaks, $\Delta V_g^{(N)}$, is easily derived from $e\frac{C_g}{C_\Sigma}\Delta V_g^{(N)} = \mu(N) - \mu(N-1)$, giving the expression:

$$e\Delta V_g^{(N)} = \frac{C_\Sigma}{C_g}\Delta\epsilon_N + \frac{e^2}{C_g} \tag{6.5}$$

These oscillations with gate voltage are referred to as *Coulomb oscillations*.

(ii) Effect of sweeping V_{SD}. Increasing the bias, V_{SD}, will raise the chemical potential of the source side μ_S until it eventually reaches the energy level μ_{N+1}, and electrons can tunnel into the island (Fig. 6.8(c)). Increasing the bias further will bring more excited states below μ_S that contribute to tunnelling, and the current increases. Figure 6.8(d) shows the I-V curve for two different gate voltages. The first where V_g is such that μ_{N+1} lines up with μ_S at zero bias, and the I-V curve is close to ohmic, the second where μ_S is approximately mid-gap between μ_N and μ_{N+1} at zero bias, resulting in a current blockade. The latter behaviour is referred to as the *Coulomb blockade*. For symmetric bias conditions, the blockade is lifted when $eV_{SD} = \mu(N) - \mu(N-1)$.

Clearly, for certain combinations of V_g and V_{SD}, current through the island is blocked. A plot of the differential conductance, $\partial I/\partial V_{SD}$, as a function of V_{SD} and V_g is referred to as a *charge stability plot*, and describes the response of the device to V_g and V_{SD}. Such a plot for a NW SET device is shown in Figure 6.8(e). The blocked regions are referred to as *Coulomb diamonds* in which the number of electrons on the island is constant (stable charge).

Lastly, two important criteria must be fulfilled for a device to display single-

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[2]In the following discussion we assume symmetric bias conditions, that is, $\mu_S = \mu_0 + eV_{SD}/2$ and $\mu_D = \mu_0 - eV_{SD}/2$.

electron effects:

$$\frac{e^2}{C_\Sigma} \gg k_B T \tag{6.6}$$

$$R_t \gg \frac{h}{e^2} \tag{6.7}$$

First, the charging energy must be large with respect to the thermal energy, $k_B T$, to avoid thermal smearing effects. Thus, for a SET to function, the island should be sufficiently small to have a low total capacitance. Second, the electrons that tunnel into the island must reside there a sufficiently long time to have a well-defined energy with respect to the charging energy, that is, $\Delta E \ll e^2/C_\Sigma$, where ΔE is the energy uncertainty. The uncertainty in time (or the typical time to charge the island) is $\Delta t = R_t C_\Sigma$, where R_t are the tunnelling resistances of the barriers. Equation 6.7 now follows directly from the Heisenberg uncertainty relation, $\Delta E \Delta t > h$. The tunnel barrier resistances must thus be large with respect to $h/e^2 = 25.813 \text{ k}\Omega$.

6.2.2 Nanowire Heterostructure SET

In the NW SET, the tunnel barriers are formed by heterostructures, and the one-dimensionality of the NW provides the lateral confinement. The schematics of a NW SET is shown in Figure 6.7(a). It is composed of an InAs NW with two InP barriers, nominally 5 nm thick, which separate the $\approx$ 100 nm long InAs island from the InAs leads. The barrier height is determined by the InAs/InP conduction band off-set, which has been calculated to be $\approx$ 400 meV [147] for the geometry considered here. However, experimental results indicate an off-set of $\approx$ 600 meV [60]. Because the barriers are high compared with the thermal energy $\sim k_B T$, tunnelling is the dominating transport mechanism at low temperatures. The tunnel barrier resistance is mainly determined by the barrier thickness, and thus the resistance is tunable by varying the InP segment thickness. A further advantage of the NW SET is that, because the process is parallel and bottom-up, billions of NWs for SETs can be formed in each growth run. To fabricate the SET device, the NW is placed on a degenerately doped Si substrate with a 100 nm thick thermal oxide layer, and the NW ends are contacted using EBL and metal evaporation. The underside of the substrate is contacted electrically to act as a global back-gate. Figure 6.7(b,c) shows electron micrographs of a NW SET device.

In Figure 6.8 the transport characteristics of a NW SET at 4.2 K are shown (Paper VI). The device displayed ideal Coulomb oscillations for a small source–drain bias, as shown in panel (b). Positioning the device on a conductance peak results in an ohmic-like curve, as shown in panel (d) blue line, whereas the device exhibits a clear Coulomb blockade if positioned on a conductance minimum in the V_G sweep, red line.
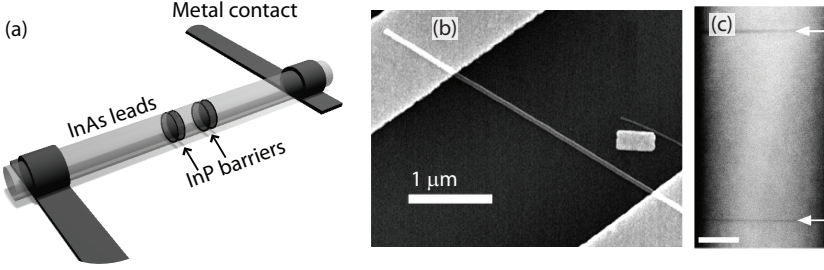
Figure 6.7: (a) Schematics of an InAs NW SET. (b) SEM micrograph of a NW SET. Metal contacts defined with EBL cover the ends of the NW. (c) TEM image of the island region [8]. The barriers are indicated with white arrows and are nominally 5 nm thick. The island is $\approx$ 100 nm long with a diameter of $\approx$ 55 nm. Scale bar is 20 nm.

The addition energy is most easily determined from the charge stability plot (Fig. 6.8(e)). As discussed above, the Coulomb blockade is lifted when $eV_{SD} = \mu(N) - \mu(N - 1)$, and thus the addition energy is half the total height of the Coulomb diamonds. Because an appreciable difference in diamond sizes was not observed, we conclude that the charging energy term dominates, and that the single-particle term in Equations 6.4 and 6.5 can be neglected; thus $e^2/C_\Sigma \approx$ 4 meV, giving $C_\Sigma = 40$ aF.

A value of the gate capacitance, C_g=10 aF, was extracted from the Coulomb oscillation periodicity of 16 meV (Fig. 6.8(b)), using Equation 6.5. The remaining capacitances of the source and drain electrodes can now be determined, $C_S = C_D = 15$ aF.

It is instructive to see if Equations 6.6 and 6.7 are satisfied for the NW SET. First, the charging energy of the device was $\approx$ 4 meV, corresponding to the thermal energy at 10 K, which sets the upper limit on the operation temperature. This agreed well with the observation that the conductance oscillations were visible up to approximately 12 K. Second, the wire resistance was of the order of $1\,\mathrm{M\Omega} \gg h/e^2 \approx 26\,\mathrm{k\Omega}$.

In summary, NWs with epitaxially defined tunnelling barriers can function as building blocks for single-electron devices. The height and width of the epitaxial tunnelling barriers can be controlled by choice of materials and barrier growth time, respectively, which enables tunable barrier resistance. The small diameter provides lateral confinement, making detrimental etching procedures unnecessary. In the future, vertical integration of these devices would enable more complex architectures and devices to be made.
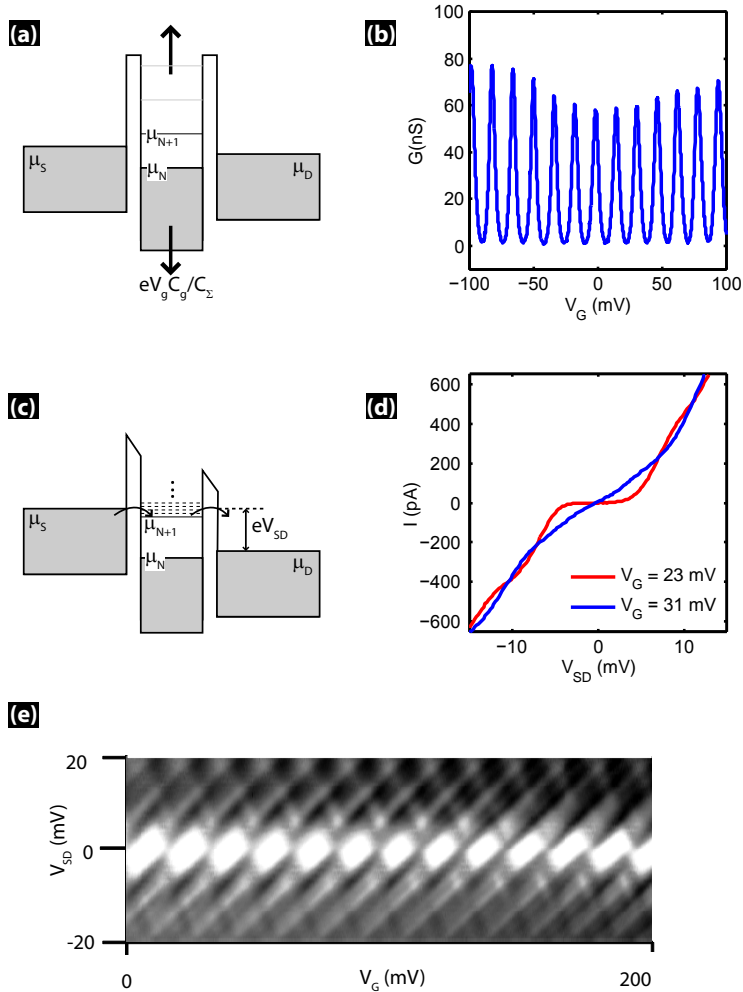
Figure 6.8: Measurements of electron transport over a NW SET. (a) Band diagram for small V_{SD} bias. (b) The current blockade can be periodically lifted by sweeping the gate voltage, resulting in Coulomb oscillations. $V_{SD} = 0.5$ mV. (c) If the device is in a blockade region, the blockade can be lifted by high enough V_{SD} bias. (d) I-V curves for two different gate voltages chosen to illustrate conducting and blockade behaviour, respectively. (e) Plot of the differential conductance, $\partial I / \partial V_{SD}$, in the $V_G - V_{SD}$ plane (charge stability plot). Dark areas correspond to high differential conductance and bright areas to low differential conductance (blockade).

6.3 Nanowires as a Biological Interface

The interaction of sensory peripheral neurons with GaP nanowires is reported in Paper VII. In the current section a brief introduction to nanowires as an interface to living cells is given.

The study of interactions between living cells and nanostructured materials is a recent and vibrant research field [148–150]. Nanoscale structures are smaller than cells (mammalian cells are typically $\sim 10\ \mu m$) and on the same length scale as intracellular features. The risks, as well as biocompatibility, of nanomaterials have attracted substantial attention. The field of nanotoxicology is still young and some partly conflicting results have been presented, for example, concerning carbon nanotubes [151]. However, it is clear that in many cases nanostructured surfaces enhance biocompatibility [148]. Most studies involve *in vitro* experiments, where the natural *in vivo* extracellular matrix is replaced by nanostructured surfaces. The cell response to topography and other artificial stimuli is then studied.

The biocompatibility of freestanding GaP NW arrays with sensory neurons is described in Paper VII. It was shown that cell adherence was enhanced on substrates covered with NWs, and that the cells remained viable and were able to extend processes. After 72 hours of cultivation, $\sim 90\ \%$ of the nerve cells dispersed on the NW surface were still viable. Notably, cells were observed to be penetrated by dozens of NWs while remaining viable (Fig. 6.9(a)). These results agree with those of Kim et al., who reported that cells remain viable if the diameter of the penetrating NWs is small in comparison to the cell body [152]. In our work, cellular processes were found to grow on top of the NWs, in between, or at their base at the substrate surface. The cells growing on top of the NWs and in between were attached to the NW tips and sides, respectively. For the processes growing at the bottom, NWs encountered along their path were internalized. Forces exerted by the cells on NWs are observable as wire bending, which enables the study of mechanotransduction at sub-cellular level. Having established the biocompatibility of NW arrays, several other applications may be feasible, some of which are described below.

Guidance of axonal outgrowth by patterned NW array substrata is interesting because of the extreme aspect ratio and high spatial resolution of the NWs. Detailed knowledge of the motility mechanisms on different substrata is important for several reasons, and necessary to be able to interface the nervous system; guidance of axonal outgrowth by topological cues has been extensively studied [153]. From a medical point of view, better knowledge of, for example, the regeneration of injuries in the peripheral nervous system, would allow better treatment. Artificial substrata, where axons, for example, are "combed" (cf. Fig 6.9(c)), also provide a more controlled environment for experiments, making the results easier to interpret than in the highly complex *in vivo* environment. Guidance may also enable the construction of ordered *in vitro* neural networks.
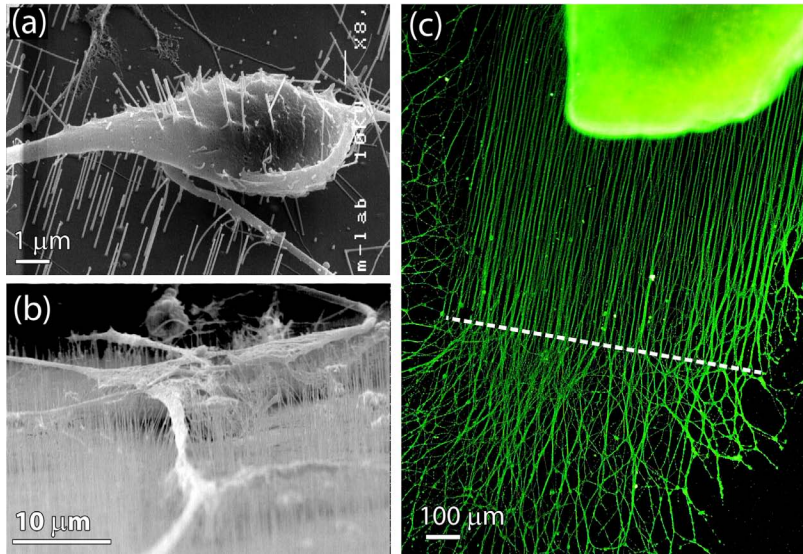
Figure 6.9: Interactions of sensory neurons with NWs. (a) SEM image of the underside of cell body (mechanically flipped over at rinsing) penetrated by NWs (Paper VII). (b) Cellular processes growing on top of randomly positioned NWs. (c) Florescence microscopy image showing guided axons growing from ganglia [xxi]. The axons are guided by parallel rows of NWs with an intra-NW pitch of 400 nm and a row pitch of 10 μm. The white dashed line indicates the edge of the NW row array where guidance ceases.

In Figure 6.9(c) axonal outgrowth from a ganglia guided by rows of NWs [xxi] is shown. The rows of NWs acted as "fences" providing contact points for the growing axons. In contrast to groves on a substrate [153], where the axons can grow at an intermediate angle to climb the continuous wall, the axons cannot cross the rows of NWs because crossing one row would require them to climb individual NWs at a 90° angle. Discrete NWs may thus provide better confinement than the traditionally used grooves.

Nanowires may also act as an "actuator–sensor" system for stimulation and recording of cellular activity. *Electrical* stimulation and probing of nerve cells with NWs in a lateral geometry have already been reported [154]; perhaps even more important would be the use of NWs as intracellular sensors [150]. *Chemically*, NWs can be functionalized to act as highly selective sensors [15, 154], or to introduce elements into the cell by transfection. *Mechanically*, the forces exerted on NWs can be recorded as wire bending, while the rigidity and topography of the NWs constitute mechanical input that affects cell motility.

In summary, NWs provide a substratum that can support cellular processes and

provide guidance. Moreover, they may function as both actuators and sensors with unprecedented spatial accuracy. This multifunctionality makes NWs a powerful tool for many life science studies.

Chapter 7

Outlook

The scientific field of nanowires has experienced a remarkable expansion in the past decade. A plentitude of papers have been published but many questions remain. Nanowires will undoubtedly continue to play a central role in nanoscience as they offer a vast range of phenomena for study, as well as functioning as versatile building blocks for other experiments.

For NWs to be truly established as a technology platform, some key issues must be addressed. A few of those related to this thesis are discussed below.

(i) Complete understanding of growth mechanisms. Detailed understanding and control of NW synthesis are necessary to create the best material possible. Examples of important topics are crystal "defects" such as twin planes, incorporation of impurities and doping, and heterostructures. The mechanism of NW growth is still the subject of lively debate in the scientific community.

(ii) Control of surfaces and interfaces. NWs have a surface-to-volume ratio that is substantially higher than for bulk materials. For certain applications, such as chemical sensors, this is an advantage, however, for many applications in electronics and photonics, a surface can cause problems. For example, a naked GaAs NW without a passivating cladding layer emits almost no light [155]. The surface chemistry and interface states must be understood and controlled.

(iii) Characterization techniques for nanowires. For planar semiconductor technology, there are reliable and (reasonably) fast methods to measure crystal quality, doping levels, carrier mobilities and other material parameters. These methods must be extended, or replaced with new ones, suitable for the nanoscale. The methods should be accurate, reliable and fast. Without good characterization, items *(i)* and *(ii)* above cannot be realized.

(iv) The Si/III-V heterostructure interface. The electrical properties of the Si/III-V

interface are still poorly understood, and many possible device geometries depend on this interface. Further research is thus required.

The above four items constitute a sizeable research challenge for the scientific community interested in NWs.

Another great challenge is the commercialization of NW technology. NWs for applications, such as LEDs, photovoltaics, transistors, field emitters and chemical sensors, have now been reported by several groups. The successful demonstration of a NW-based product will boost the scientific value of NW-related research and spur public interest.

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Populärvetenskaplig Sammanfattning

Nanotrådar är en ny typ av material som rönt stor uppmärksamhet i forskarvärlden under senare år. Nanotrådar är kristaller i form av en tunn tråd och med speciella egenskaper. Forskare har till exempel använt "spikmattor" av nanotrådar för att bättre förstå hur nervceller fungerar, men även använt dem till att framställa extremt små lysdioder. I framtiden skulle nanotrådar till exempel kunna placeras på datorchips för att skicka information med ljus i stället för elektricitet, men även billiga och effektiva lysdioder för att ersätta den energislösande glödlampan står på schemat.
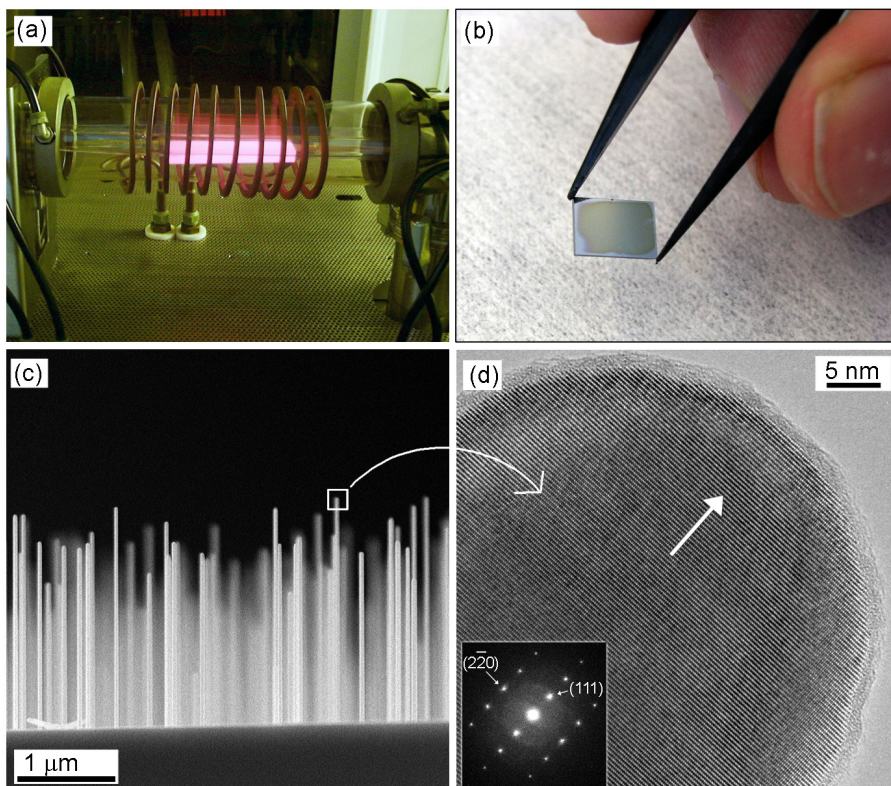
Nanotrådar

Nanotrådar har en diameter på $10-100$ nanometer[1] och är kristaller (precis som diamant eller koksalt). I Figur 1(c) nedan visas nanotrådar stående på en skiva av kisel och till höger visas en elektronmikroskopbild av toppen på en nanotråd (ca. 1 000 000 gångers förstoring). Eftersom tråden är en kristall har varje atom sin exakta position efter ett regelbundet mönster; de mörka prickarna är just rader av enskilda atomer. Kristallerna är av så kallat halvledarmaterial, vilket är samma typ av material som i stort sett all elektronik och fotonik[2] är uppbyggt av.

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[1] En nanometer är en miljardedels meter. Ett mänskligt hårstrå växer ungefär 30 nm i sekunden och har en diameter på 100 000 nm, dvs 10 000 gånger större än en nanotråd.

[2] Fotonik är motsvarigheter till elektronik, där ljus (fotoner) används i stället för elektricitet (elektroner).

1   **Framställning av nanotrådar.** *(a) Reaktor där nanotrådsodling sker. Provet placeras på en värmare i form at ett stycke grafit (glödande i bilden). Genom att flöda gaser (från vänster till höger i bilden) innehållande nanotrådens beståndsdelar, växer nanotråden nedifrån och upp, atom för atom. (Bild från Werner Seifert.) (b) Ett kisel-prov med nanotrådar av indium-arsenid efter växt. Cirka 50 miljoner nanotrådar trängs på provets yta. (c) Bild av indium-arsenid-nanotrådar som växt vertikalt från en kisel-skiva. En 10000 gångers förstoring från panel b. (d) Närbild av nanotråds-topp. Genom att använda elektronmikroskop är det möjligt att se igenom trådarna; varje svart punkt är en atomrad exakt ordnad enligt kristallens mönster.*

"Odling" av nanotrådar

Nanotrådar framställs genom att växa kristaller på ett kontrollerat sätt, atom för atom, i en endimensionell struktur. I Figur 1(a) visas en så kallad epitaxi-maskin för nanotrådsodling. Med epitaxi staplas atomer på varandra på ett kontrollerat sätt och kristallens sammansättning kan styras mycket exakt. Epitaxi används till exempel för att tillverka de lasrar som används för att läsa DVD-skivor. Trådarna odlas vid höga temperaturer, $400 - 1000$ °C beroende på material. Ett prov som

mönstrats för nanotrådsväxt, till exempel belagda med en mask med små öppningar, placeras på värmaren (glödande i figuren). I nästa steg introduceras gaser som innehåller nanotrådens beståndsdelar. Om parametrarna är de rätta under framställningen, det vill säga korrekt temperatur, tryck, gasflöden etc., kommer atomerna att självorganisera i endimensionella strukturer — nanotrådar. Forskning på odling av nanotrådar innebär till stor att finna optimala betingelser för växt och att kontrollera materialets egenskaper så exakt som möjligt.

Nanotrådar — vad kan de användas till?

Nanotrådar har visat sig vara mycket användbara inom vetenskapen och i Lund pågår också verksamhet för att kommersialisera trådar i olika produkter. Vi hoppas till exempel att trådarna ska kunna användas i nästa generations transistorer som ska vara både strömsnålare och snabbare än dagens. Denna avhandling innehåller tre användningsexempel: *(i)* en nanotråds-transistor där enskilda elektroner kan kontrolleras, *(ii)* studier av hur nervceller lever på, och samverkar med, en spikmatta av nano-nålar, *(iii)* extremt små lysdioder på kiselsubstrat.

Varför nano-lysdioder på kisel? Kisel är det absolut dominerande materialet inom elektronik. Kisel har dock en allvarlig brist — det kan inte på ett enkelt sätt användas för att generera ljus. Därför används andra materialtyper, till exempel gallium-arsenid och indium-fosfid, för många optiska tillämpningar. Idealt vore att integrera dessa material med kisel, då skulle det vara möjligt att använda kisels i övrigt utmärkta egenskaper, och dessutom generera ljus vilket är ett krav för många tillämpningar. Problemet är att när t.ex. gallium-arsenid växes på Si blir materialet fullt av defekter, av för låg kvalitet för att användas. Anledningen är att de två lagrens atomstrukturer skiljer sig alltför mycket åt.

> Avhandling är resultatet av doktorandstudier 2003 − 2008 vid Lunds Universitet och beskriver framställning av nanotrådar och deras tillämpningar. Forskningsfältet är tvärvetenskapligt men med tyngdpunkt på materialvetenskap och fasta tillståndets fysik, kombinerat med nanoteknologi.

Finns det då något sätt att växa ljusemitterande material av bra kvalitet på kisel? Här kan nanotrådar vara till hjälp. En struktur i form av en tunn tråd får särskilda egenskaper. En är att material med olika atomstrukturer enklare kan fogas samman i tråden. Eftersom trådarna är så tunna (en 40 nm tjock nanotråd består bara av storleks-ordningen 100 atomer på tvären) är de mycket flexibla och trådarnas atomstrukturer kan töja sig så att de olika materialen passar ihop och bildar en enda lång kristall. Det är bland annat denna egenskap som gör det möjligt att växa ljusutsändande material av hög kvalitet direkt på kisel.

I Figur 2 visas en tvärsnittsbild av en skog av nanotrådar där varje tråd utgör en lysdiod. Effektiviteten av dessa lysdioder är fortfarande låg jämfört med tra-

ditionella lysdioder, men det faktum att de är extremt små, nano-små, och att de kan integreras på kisel, hoppas vi ska öppna upp för helt nya tillämpningar. Till exempel skulle nanotrådar kunna integreras på datorchips för att skicka information med ljus i stället för elektricitet, eller användas till billiga och effektiva lysdioder.
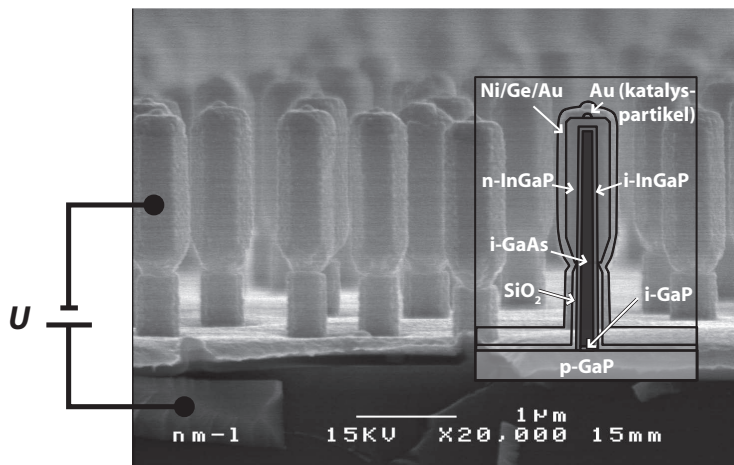
2 **Exempel på tillämpning av nanotrådar.** *Bilden visar nanotråds-lysdioder. När en spänning läggs mellan provets ovansida och dess undersida, kommer varje nanotråd att sända ut ljus. I infällningsbilden visas de olika material som ingår. Från* Papper V *i avhandlingen.*

Mer information

Vår forskning har även beskrivits i allmänpressen. Nedan följer ett par populärvetenskapliga referenser på svenska:

Lagarbete förde forskare till toppen, *Sydsvenskan*, 6 mars, 2005.

Ljusare framtid med nanotrådar, *Ny Teknik*, 20 september, 2006.

Glödlampan ut – lysdioden in, *SVT sydnytt*, 7 november, 2007.

Hetast i Tekniksverige – 33 unika uppstickare, *Ny Teknik*, 12 mars, 2008.

Snabb och snål pyttetransistor, *Ny Teknik*, 30 april, 2008.

Epitaxial III-V nanowires on silicon

T. Mårtensson, C. P. T. Svensson, B. A. Wacaser, M. W. Larsson, W. Seifert, K. Deppert, A. Gustafsson, L. R. Wallenberg and L. Samuelson

Principal achievements
Epitaxial growth of III-V nanowires on Si substrates was demonstrated for the first time. This may enable integration of high-mobility materials for electronics, and direct band gap materials for photonics, with Si. From a crystal growth perspective, successful growth of polar zinc blende material on top of a non-polar diamond substrate was achieved.

A popular account has been published in:
A 'bed of nails' on silicon, Nature **432**, 450 (2004)

My contribution
I managed the project and performed most of the epitaxy.
I wrote the paper.

Note to electronic version

The original papers are not included in the electronic version due to copyright reasons. However, for readers with subscriptions, direct links are provided through the DOI numbers in the list of papers (pages xiii-xvii).

Epitaxial growth of indium arsenide nanowires on silicon using nucleation templates formed by self-assembled organic coatings

T. Mårtensson, J. B. Wagner, E. Hilner, A. Mikkelsen,
C. Thelander, J. Stangl, B. J. Ohlsson, A. Gustafsson, E. Lundgren,
L. Samuelson and W. Seifert

II

Principal achievements
Monolithic integration with Si of a material attractive for electronics was demonstrated. Foreign metal catalysts for nanowire growth were not used, which is advantageous regarding compatibility with silicon technology. The micro-masking patterning method demonstrated may provide a means of large-area and inexpensive patterning.

My contribution
I initiated and led the project. I performed the surface preparation, epitaxy and evaluation of the growth results. I wrote the paper.

Fabrication of individually seeded nanowire arrays by vapour–liquid–solid growth

T. Mårtensson, M. Borgström, W. Seifert, B. J. Ohlsson and L. Samuelson

III

Principal achievements
Individual site-controlled nanowire growth in lithographically designed arrays was demonstrated. Controlled synthesis was achieved by a combination of conventional top-down processing and bottom-up nanowire growth. At the time of publication, nanowire growth from aerosol particles or a thin metal film, that is, without any position control, was usually employed. The method described provides a means of achieving position-controlled growth and has since been employed for a number of projects at our department, some of which are described in this thesis.

My contribution
I planned the project together with my supervisors. I carried out the electron beam lithography and epitaxy. I wrote the paper.

Nanowire arrays defined by nanoimprint lithography

T. Mårtensson, P. Carlberg, M. Borgström, L. Montelius, W. Seifert and L. Samuelson

Principal achievements

It was demonstrated that designed nanowire arrays could be fabricated by a parallel lithography method, namely nano-imprint lithography. The method descibed in paper III using electron beam lithography, which is a high-resolution but serial, slow technique, could thus be transferred to a technology suitable for large-area, high-throughput patterning.

IV

My contribution

I performed the epitaxy and some of the lithography processing. I was the primary author of the paper.

Monolithic GaAs/InGaP nanowire light emitting diodes on silicon

C. P. T. Svensson, T. Mårtensson, J. Trägårdh, C. Larsson, M. Rask, D. Hessman, L. Samuelson and J. Ohlsson

Principal achievements
Nanoscale light sources integrated with Si, which may be controlled on the wafer scale, were demonstrated. For the first time, planar processing of vertical nanowire devices was demonstrated for optoelectronics. Each LED is a vertical nanowire with a core-shell structure. Possible future applications are low-cost LEDs, and on-chip light sources integrated with CMOS technology.

My contribution
I was responsible for the epitaxy on Si and for the optimization of the nanowire shell. I wrote parts of the paper.

V

Single-electron transistors in heterostructure nanowires

C. Thelander, T. Mårtensson, M. T. Björk, B. J. Ohlsson,
M. W. Larsson, L. R. Wallenberg and L. Samuelson

Principal achievements

A single-electron nanowire transistor, with epitaxially grown tunnel barriers, was demonstrated. Prior to this publication, nanowire single-electron transistors had only been fabricated with high-resistance and non-ohmic contacts acting as tunnel barriers. Here, the barrier tunnelling resistance could be tuned by controlling the barrier thickness. The narrow diameter of the nanowire provides the lateral electron confinement and eliminates the needs for etching, which can often damage the device.

My contribution

I fabricated the SET sample and carried out some of the electrical measurements. Claes Thelander provided most of the know-how as I had just began my PhD studies.

VI

Gallium phosphide nanowires as a substrate for cultured neurons

*W. Hällström, T. Mårtensson, C. Prinz, P. Gustavsson,
L. Montelius, L. Samuelson and M. Kanje*

Principal achievements
Sensory nerve cell interactions with nanowires were studied. It was concluded that nanowire arrays provide a substratum that can support cellular processes, and moreover provide information on cellular activity. These results initiated a series of studies. For example, it was later shown how nanowire arrays can be used to provide guidance for axonal growth (Prinz et al. Nanotechnology **19**, 345101 (2008)).

My contribution
I was responsible for the nanowire growth. I took part in writing the article.

VII