LUND UNIVERSITY

Flexible Receivers in CMOS for Wireless Communication

Nejdel, Anders

2015

Flexible Receivers in CMOS for Wireless Communication

Anders Nejdel

LUND INSTITUTE OF TECHNOLOGY
Lund University

Doctoral Dissertation
Lund, October 2015

Department for Electrical and Information Technology
Lund University
P.O. Box 118
SE-221 00 LUND
SWEDEN

ISSN 1654-790X, no.75
ISBN 978-91-7623-415-0 (print)
ISBN 978-91-7623-416-7 (pdf)
Series of licentiate and doctoral dissertations.

Produced using LaTeX Documentation System.
Printed in Sweden by *Tryckeriet i E-huset*, Lund.
October 2015.

Abstract

Consumers are pushing for higher data rates to support more services that are introduced in mobile applications. As an example, a few years ago video-on-demand was only accessed through landlines, but today wireless devices are frequently used to stream video. To support this, more flexible network solutions have merged in 4G, introducing new technical problems to the mobile terminal. New techniques are thus needed, and this dissertation explores five different ideas for receiver front-ends, that are cost-efficient and flexible both in performance and operating frequency. All ideas have been implemented in chips fabricated in 65 nm CMOS technology and verified by measurements.

Paper I explores a voltage-mode receiver front-end where sub-threshold positive feedback transistors are introduced to increase the linearity in combination with a bootstrapped passive mixer. Paper II builds on the idea of 8-phase harmonic rejection, but simplifies it to a 6-phase solution that can reject noise and interferers at the 3$^{\text{rd}}$ order harmonic of the local oscillator frequency. This provides a good trade-off between the traditional quadrature mixer and the 8-phase harmonic rejection mixer. Furthermore, a very compact inductor-less low noise amplifier is introduced. Paper III investigates the use of global negative feedback in a receiver front-end, and also introduces an auxiliary path that can cancel noise from the main path. In paper IV, another global feedback based receiver front-end is designed, but with positive feedback instead of negative. By introducing global positive feedback, the resistance of the transistors in a passive mixer-first receiver front-end can be reduced to achieve a lower noise figure, while still maintaining input matching. Finally, paper V introduces a full receiver chain with a single-ended to differential LNA, current-mode down-conversion mixers, and a baseband circuity that merges the functionalities of the transimpedance amplifier, channel-select filter, and analog-to-digital converter into one single power-efficient block.

Populärvetenskaplig sammanfattning

Tänk dig att du står i en gymnastiksal och ska prata med en person som står på andra sidan rummet. Den andra personen pratar med låg röst och du måste verkligen koncentrera dig för att höra. Låter det svårt? Tänk dig nu att en tredje person står bredvid dig och skriker så mycket den kan samtidigt som du ska försöka höra den andra personen. Detta är vardagen för vad mobiltelefonerna måste klara av för att kunna kommunicera.

I vardagen och i media pratas det mycket om digital kommunikation och analog kommunikation ses som en gammal teknik. Det var till exempel inte många år sedan det analoga TV-nätet stängdes ner och ersattes helt av det digitala. Den analoga tekniken finns dock fortfarande kvar. Även om informationen i moderna kommunikationssystem är digital är själva överföringen och därmed kommunikationen analog. Därför behövs det analoga kretsar som hanterar överföringen och efter dessa så görs signalen om till en digital signal. Vi har idag mängder av olika typer av system för trådlös kommunikation där informationen skickas på olika våglängder eller frekvenser.

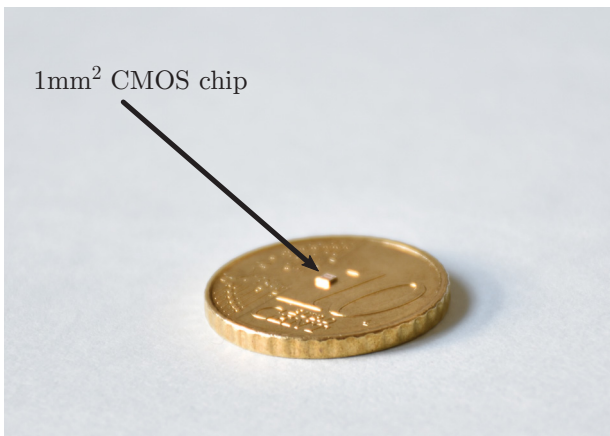
Ett viktigt begrepp inom all kommunikation är bandbredd. Bandbredden beskriver hur mycket information som kan skickas med en viss modulering och optimeras hela tiden för att få plats med så mycket information som möjligt. Människan kan till exempel höra ljud med en frekvens mellan 50 hertz och 20 kilohertz vilket sätter bandbredden för hur mycket information vi kan höra. För att skicka trådlös informationen används en så kallad bärvåg som vanligtvis har mycket högre frekvens än informationen. Ett exempel på detta är FM-radio, där bärvågen är cirka 100 megahertz medan informationen är hörbart ljud, alltså en mycket låg frekvens. För mobil kommunikation är bärvågen mellan 400 megahert och nästan 4 gigahertz. och informationen kan vara 100 megahertz.

Bärvågen med information skickas genom luften från din telefon till en basstation i närheten och skickas vidare till telefonen som signalen ska fram till. Då den kommer fram till slutdestinationen är signalen väldigt svag. Problemet är nu att telefonen som tar emot signalen på samma gång skickar signaler tillbaka till basstationen. Som jämförelse kan skillnaden i styrka mellan den skickade signalen och den mottagna signalen vara lika stor som skillnaden i effekt mellan Ringhals kärnkraftverk och en LED-lampa! Detta gör det svårt för telefonen att ”höra” informationen.

Denna avhandling innehåller fem vetenskapliga artiklar som beskriver konstruktionen av radiomottagare. Eftersom större krav ställs i och med nyare

trådlösa system så som fjärde generationens mobilnät så behövs flexibla lösningar som enkelt kan ändras från en konfiguration till en annan. Ett annat problem är att storleken på transistorerna, som används för att bygga de integrerade kretsarna, hela tiden blir mindre för att optimeras för digitala kretsar. För de analoga funktionerna är detta negativt och tyvärr så skalar inte storleken lika mycket på de passiva komponenterna (spolar och kondensatorer). Fyra av artiklarna innehåller därför lösningar för att ta bort spolar i mottagarkedjan. Alla fem artiklar är baserade på resultat från tillverkade integrerade kretsar, i en 65nm CMOS process, och visar på olika lösningar för flexibla mottagare. De fyra första behandlar den analoga delen som består av en lågbrusförstärkare, blandare som tar ner frekvensen från radiofrekvens till basbandsfrekvens samt basbandskretsar, medan den femte behandlar konstruktionen av en mottagare hela vägen från radiofrekvensingången till den digitala utgången.

Doktorandtjänsten har finansierats av Stiftelsen för strategisk forskning inom ramen för DARE (Digitally-Assisted Radio Evolution) och Marie Curie-projektet ATWC (Adaptive Transceivers for Wireless Communication). Kretstillverkningen har sponsrats av STMicroelectronics.



Jämförelse mellan ett 1mm^2 CMOS chip och ett €0.1 mynt.

Contents

Preface

This dissertation summarizes my academic work for the Ph.D.-degree in Circuit Design at the Analog RF-group, Department of Electrical and Information Technology, Lund University, Sweden. The studies took place from January 2012 until November 2015. The dissertation is divided into two parts, where the first part has six chapters that contains an introduction to the research field whereas the second part consists of five attached research papers.

Included Research Papers

The main contributions are derived from the following publications:

[1] A. Nejdel, M. Törmänen, and H. Sjöland, "A 0.7 to 3 GHz wireless receiver front end in 65-nm CMOS with an LNA linearized by positive feedback," in *Springer Analog Integrated Circuits and Signal Processing*, vol. 74, no. 1, pp. 49–57, Jan. 2013.

[2] A. Nejdel, M. Törmänen, and H. Sjöland, "A 0.7 - 3.7 GHz Six Phase Receiver Front-End With Third Order Harmonic Rejection," in *Proceedings of IEEE European Solid-State Circuits Conference*, Bucharest, Romania, Sep. 16–20 2013, pp. 279–282.

[3] A. Nejdel, H. Sjöland, and M. Törmänen, "A Noise-Cancelling Receiver Front-End With Frequency Selective Input Matching," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1137 –1147, May. 2015.

[4] A. Nejdel, M. Abdulaziz, M. Törmänen, and H. Sjöland, "A Positive Feedback Passive Mixer-First Receiver Front-End," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, Phoenix, USA, May. 16–20 2015, pp. 79–82.

[5] A. Nejdel, X. Liu, M. Palm, L. Sundström, M. Törmänen, H. Sjöland and P. Andreani, "A 0.6—3.0 GHz 65 nm CMOS Radio Receiver with $\Delta\Sigma$-based A/D-Converting Channel-Select Filters," in *Proceedings of IEEE European Solid-State Circuits Conference*, Graz, Austria, Sep. 14–18 2015, pp. 299–302.

The research was funded by the Swedish Foundation for Strategic Research (SSF) under the Digitally Assisted Radio Evolution project (DARE)

Related publications

The publications listed below contain complementary, and overlapping material, but are not considered as a part of this dissertation.

[**6**] A. Nejdel, M. Törmänen, and H. Sjöland, "A Linearized 1.6-5 GHz Low Noise Amplifier Using Positive Feedback in 65 nm CMOS," in *Proceeding of NORCHIP*, Lund, Sweden, Nov. 14–15 2011, pp. 1–4.

[**7**] M. Abdulaziz, A. Nejdel, M. Törmänen, and H. Sjöland, "A 3.4mW 65nm CMOS 5th Order Programmable Active-RC Channel Select Filter for LTE Receivers," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, Seattle, USA, June. 2–4 2013, pp. 217–220.

[**8**] A. Nejdel, M. Törmänen, and H. Sjöland, "A Noise Cancelling 0.7-3.8 GHz Resistive Feedback Receiver Front-End in 65 nm CMOS," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, USA, June. 1–2 2013, pp. 35–38.

[**9**] W. Ahmad A. Nejdel, M. Törmänen, and H. Sjöland, "Fully Integrated Radio over Fiber Downlink for Distributed Multi-antenna Systems in 65nm CMOS," in *Proceedings of IEEE New Circuits And Systems Conference*, Trois-Rivières, Canada, June. 22–25 2014, pp. 353–353.

Acknowledgments

This work would not have been possible without the help and support from many.

First of all, I want to thank my supervisor Henrik Sjöland for his support during these years and for giving me the opportunity to pursue the Ph.D.-degree. You are truly an expert and having a discussion with you always gives me a lot of new insights. Thanks to my co-supervisor Markus Törmänen, especially for all the more practical aspects of circuit design; your valuable knowledge has been very important. Thanks to Johan Wernehag for all our discussions. I am also very grateful for all the advice from Pietro Andreani, especially during the design of the circuit that resulted in the final attached paper.

A special thanks go to all the current and former Ph.D.-students of the analog RF-group, for all the cooperation and company during late tapeout-evenings and also for your friendship and interesting discussions during coffee breaks, travels and lunches. Being a part of the DARE project, headed by Pietro, has been very nice and I am grateful to all my teammates. You have all challenged me to understand other design aspects than only analog RF-design. Another big thanks goes to all other PhD-students, current and former, at EIT for keeping me company during my time here at the department! I am also grateful for all the support from EIT in general, both administrative and technical. To all the people at Ericsson in Lund who have helped me: Thanks; especially to Magnus Nilsson, Sven Mattisson and Lars Sundström.

During my third year, I got the opportunity to do an internship at Marvell in Pavia, Italy. I learned a lot during this time and I am grateful to Paolo Rossi, Giuseppe de Pinto, Marika Tedeschi and Luca Fanori for providing me with some industry experience.

To my family: thank you for your unconditional support! Finally, I am ever grateful to my fiancée Jennie. Without you, this work would not have been possible and I can never express my gratitude for your support, patience and love during the past four years.

This work has been supported by: Swedish Foundation for Strategic Research within the DARE project, Seventh Framework Programme within the ATWC project, traveling to some conferences has been supported by the Ericsson Research Foundation, and chip manufacturing has been supported by STMicroelectronics.

List of Acronyms

2G	Second Generation Mobile Network
3G	Third Generation Mobile Network
4G	Fourth Generation Mobile Network
AC	Alternating Current
ACS	Adjacent Channel Selectivity
ADC	Analog-to-Digital Converter
ADCSF	Analog-to-Digital Converting Channel-Select Filter
AM	Amplitude Modulation
ASW	Antenna Switch
ATWC	Adaptive Transceivers for Wireless Communication
BOM	Bill Of Materials
CCC	Capacitive Cross Coupling
CF	Correction Factor
CG	Common Gate
CIFB	Cascade-of-Integrators-in-Feedback
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
CSF	Channel-Select Filter
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DARE	Digitally Assisted Radio Evolution
DC	Direct Current
Div. RX	Diversity Receiver
DSM or $\Delta\Sigma$M	Delta Sigma Modulator
DSP	Digital Signal Processor
DTV	Digital TV
ENOB	Equivalent Number of Bits

FB LNA	Shunt-Shunt Feedback Low Noise Amplifier
FDD	Frequency Division Duplex
GSM	Global System for Mobile Communications
HRM	Harmonic Rejection Mixer
IC	Integrated Circuit
IDCS	Inductively Degenerated Common Source
IM2	Second Order Intermodulation Distortion
IM3	Third Order Intermodulation Distortion
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
IRR	Image Rejection Ratio
LNA	Low Noise Amplifier
LNTA	Low Noise Transconductance Amplifier
LO	Local Oscillator
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency-Division Multiplexing
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PCB	Printed Circuit Board
PMU	Power Management Unit
PPF	Poly Phase Filter
Prim. RX	Primary Receiver
Q-Factor	Quality Factor
QAM	Quadrature Amplitude Modulation

QVCO	Quadrature Voltage-Controlled Oscillator
QPSK	Quadrature Phase-Shift Keying
REFSENS	Reference Sensitivity
RF	Radio Frequency
RF-ASIC	Radio Frequency Application Specified Integrated Circuit
RSSI	Received Signal Strength Indication
RX	Receiver
SAW	Surface Acoustic Wave
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SSF	Swedish Foundation for Strategic Research
STF	Signal Transfer Function
SX	Frequency Synthesizer
TDD	Time Division Duplex
TD-SCMA	Time Division-Synchronous Code Division Multiple Access
TIA	Transimpedance Amplifier
TSPC	True Single Phase Clocked
TX	Transmitter
UE	User Equipment
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
W-CDMA	Wideband Code Division Multiple Access
XTAL	Crystal

List of Symbols

B	Bandwidth [Hz]
C_{gs}	Gate-to-Source Capacitance [F]
Δf	Offset Frequency [Hz]
ϵ_Q	Quantization Noise
f_{LO}	Local Oscillator Frequency [Hz]
f_{RF}	Frequency of a Radio Frequency tone
f_{RX}	Receiver Frequency [Hz]
f_s	Clock/sampling frequency [Hz]
f_{TX}	Transmitter Frequency [Hz]
γ	Gamma Factor, >2/3 for short-channel MOSFET
g_m	Transconductance [S]
k	Boltzmann's constant, $\approx 1.381 \times 10^{-23}$ [J/K]
$L(\Delta\omega)$	Phase noise at an offset of ω [dBm/Hz]
L_g	Gate Inductor [Ω]
L_s	Source Inductor [Ω]
M_x	Transistor x
N	Number of phases in mixer
ω_0	Self Resonance Frequency [rad/s]
ω_T	Transit Frequency [rad/s]
R_L	Load Resistor [Ω]
R_s	Source Resistance [Ω]
T	Temperature [k]
$\overline{v^2}$	Noise Power
V_{th}	MOS transistor threshold voltage [V]
Z_s	Source Impedance [Ω]
$\text{P}_{1\text{ dB}}$	1 dB Noise Compression Point

Introduction

Chapter 1

Motivation

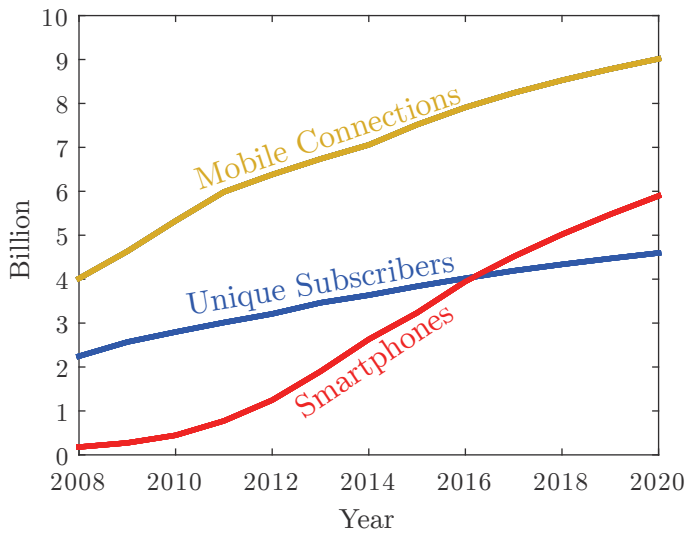


Figure 1: Number of mobile connections, unique subscribers and smartphones from 2008–2014 and estimates from 2015–2020 [10].

Communication and exchange of information is an important part of almost every person's life. Due to the rapid growth of cellular communication, more people communicate through cellular devices and the smartphone is a gadget many people use on a daily basis. It is estimated by GSMA that in 2020 there will be 4.6 billion cellular subscribers, 9 billion cellular connections (excluding machine-to-machine connections) and close to 6 billion smartphones [10], see figure 1. With more smartphones, and more services such as video-on-demand, the wireless internet traffic will also increase. It is estimated by Cisco that the mobile internet traffic will increase from an annual total of 30 exabytes ($30 \cdot 10^{18}$ or 30 trillion bytes) in 2014 to 292 exabytes in 2019 [11]. In the end, cheaper communication devices will be beneficial to both customers and company share holders.

Figure 2: Illustration of wireless communication of digital data from transmitter to receiver.

1.1 Wireless Communication

After a wireless signal reaches the antenna, it passes through the radio frequency (RF) receiver, where the analog radio signal is converted into a digital signal which is then demodulated and decoded and sent to a central processor. This reception of data is called the downlink. The same occurs but in the other direction when information is transmitted (uplink); digital information is coded and converted into a modulated analog signal, which in turn is converted into a radio signal and sent to the antenna, see figure 2.

1.2 The Radio Frequency Application Specific Integrated Circuit

In order to have a cost-effective platform performing these tasks, the functions are implemented on a single integrated circuit or chip, normally called the Radio Frequency Application Specific Integrated Circuit (RF-ASIC). This chip consists of several important blocks, depicted in figure 3. The transceiver is here assumed to be able to operate at three different frequency bands. The signal is received by the antenna and an antenna switch (ASW) is used to steer the signal to one of three duplexers. The duplexers are used to isolate the receiver from the transmitter, where the strong transmitted signal otherwise would desensitize the receiver. After the duplexer the signal enters the RF-ASIC in the primary receiver (Prim. RX). The first task is to amplify the weak received signal while adding as little noise as possible, executed by a low noise amplifier (LNA). After the amplification the signal is down-converted in frequency by a mixer. Lastly, out-of-band interferers that are left after the down-conversion are removed, or heavily attenuated, in a channel-select filter (CSF) and the remaining signal is converted to digital form by an analog-to-digital converter (ADC) and processed by the digital signal processor (DSP).

In order to perform frequency down-conversion the mixer needs a local oscillator (LO) signal which is generated by a frequency synthesizer (SX). This circuit uses a very clean and accurate low-frequency reference, typically provided by an off-chip crystal (XTAL), to generate a high precision frequency

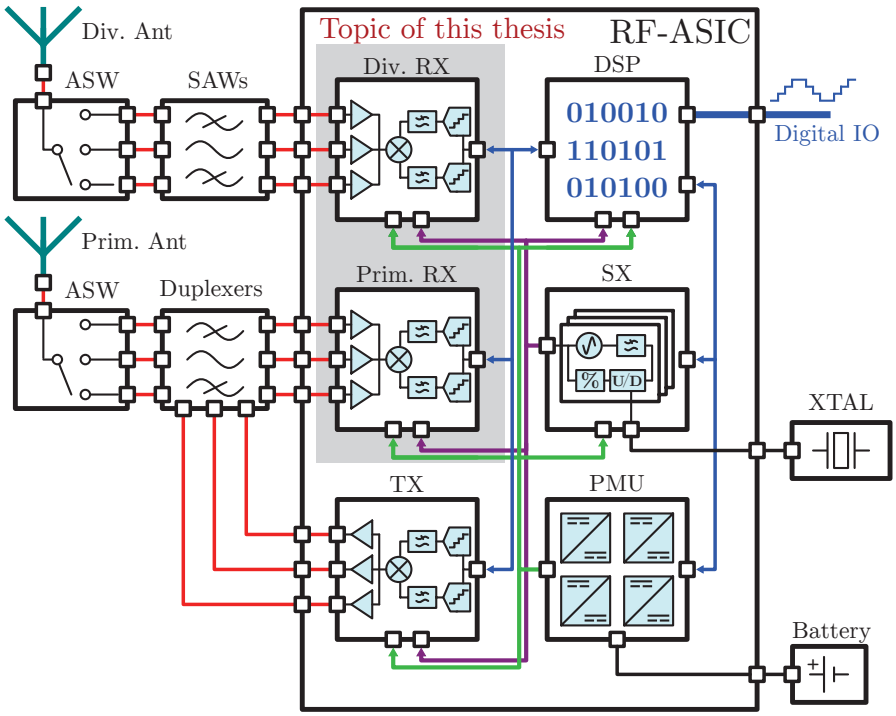


Figure 3: High-level view of a modern transceiver with RF-ASIC and important off-chip components.

LO signal. Supply voltages are provided through a Power Management Unit (PMU) that converts the voltage of the battery to desirable levels for the circuitry.

Parallel to the primary receiver is a diversity receiver (Div. RX). This is connected to a second antenna which can provide reliable communication in environments with fast local fading. For the diversity receiver only SAW filters (very sharp filters to attenuate out-of-band blockers), i.e. no duplexer is used since the transmitter is connected to the primary antenna only. The circuitry of the diversity receiver can, however, be a replica of the primary receiver.

The data to be transmitted is first coded and modulated in the DSP and then fed to the transmitter (TX) circuitry, where digital-to-analog conversion is performed and the analog signal is filtered, frequency up-converted and amplified before being sent to the transmit port of the duplexer, which is connected to the primary antenna. In figure 3 it is assumed that the power amplifier (PA) of the TX is on-chip, but it might also be on a separate chip in a different semiconductor technology.

The fourth generation of mobile communication (4G) called Long Term

Evolution (LTE) is currently the most advanced cellular communication standard and poses new technical challenges. One challenge is the large number of RF bands that are introduced, ranging from 450–3800 MHz. The cellular transceiver depicted in figure 3 can only handle a few bands. At the same time, several of these bands use frequency division duplex (FDD) to be able to transmit and receive information at the same time on different frequencies. This means that there are very strong interferers, i.e. the own transmission, that can cause problems when trying to receive weak signals. This calls for flexible/re-configurable/adaptive circuity. In this dissertation the focus is on the receiver part of the RF-ASIC where papers I-IV present novel RF front-ends and building blocks while paper V presents a full receiver circuit.

1.3 Outline

Chapter 1 presents a motivation and organization for the dissertation.

Chapter 2 introduces the modern radio receiver and presents commonly used performance metrics.

Chapter 3 describes and analyzes the building blocks used in the receiver front-ends.

Chapter 4 presents some architecture-level implementation aspects.

Chapter 5 gives summaries and conclusions of the included papers along with the author's contribution.

Chapter 6 provides a discussion with suggestions for future work.

Paper I presents design and measurements of a wideband receiver with an LNA that uses positive feedback transistors, biased in sub-threshold to improve linearity of the LNA.

Paper II presents a technique to reject third order harmonic down-conversion by using six LO phases. Measurements are also included.

Paper III presents the implementation and measurements of a wideband flexible noise-cancelling receiver front-end based on negative shunt-shunt feedback from baseband to RF input.

Paper IV presents implementation and measurements of a mixers-first receiver front-end where the noise figure is reduced by increasing the switch sizes and introducing positive feedback.

Paper V presents implementation and measurements of a wideband receiver with a noise-cancelling LNA and the complete baseband section including ADC. In order to increase power efficiency, a so called analog-to-digital converting Channel-Select Filter (ADCSF) is used.

Chapter 2

The Radio Receiver

This chapter describes the radio receiver system and introduces common performance metrics that are used to evaluate the analog performance of radio receiver front-ends. In order to understand the importance of the metrics, explanations of problems that can occur due to the imperfections are also explained.

2.1 Standards and Wireless Spectra

There are several wireless standards for cellular communication, where the most common globally used ones are 2G (GSM), 3G (W-CDMA and TD-SCDMA) and 4G (LTE). LTE was introduced to be able to receive a peak data rate of 1 Gbps and has more flexible bandwidth scaling compared to the previous generations. By introducing orthogonal frequency-division multiplexing (OFDM) and using a sub-carrier spacing of 15 kHz, the number of sub-carriers, grouped into resource blocks of 180 kHz, can be chosen to match different bandwidths between 1.4 and 20 MHz, see table I.

Table I: Bandwidths, corresponding number of resource blocks and effective bandwidth for LTE release 12.

Channel BW [MHz]	Number of resource blocks (12 sub-carriers)	Effective BW [MHz]
1.4	6	1.08
3	15	2.7
5	25	4.5
10	50	9
15	75	13.5
20	100	18

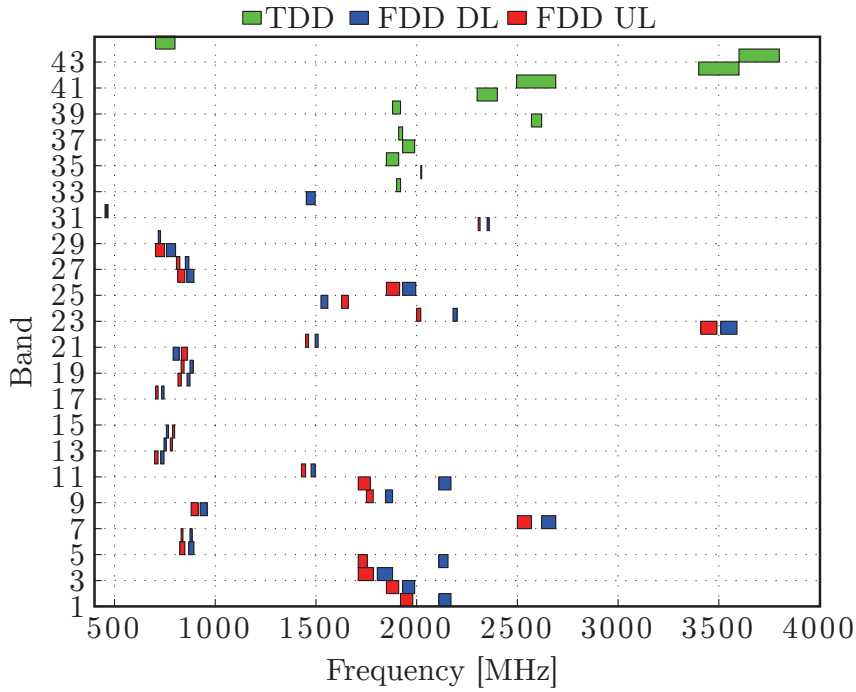


Figure 4: TDD and FDD frequency bands for LTE rel. 12.

Thanks to the flexible bandwidth, there are different configurations used in different RF bands. This creates an efficient way of using all frequency content available in the different bands. As an example, some bands are only a few MHz wide and they can either be configured as a single LTE20 channel or as several more narrow channels.

There are several different bands that are available for LTE, see figure 4, and they are divided into two different groups: time division duplex (TDD) bands and frequency division duplex (FDD) bands. The first bands (band 1–32) use FDD where the user equipment (UE) can receive and transmit signals at the same time, at different frequencies. The downlink can either be at a higher or at a lower frequency compared to that of the uplink. Two current exceptions are band 29 and 32 that are only used for downlink and are assumed to be used in carrier aggregation scenarios[1]. Band 33–44 are used for TDD where transmission and reception takes place at the same frequency but at different time instances. This relaxes some of the compression requirements of

[1]Carrier aggregation introduces even more flexibility to LTE by combining data from different bands (inter-band), or from within the same band (intra-band).

the receiver, since the strong uplink is not active while receiving signals. There are, however, still several blockers, such as adjacent channels and signals from other standards that can desensitize the receiver.

To exemplify this, figure 5 shows a blocker mask with both modulated blockers and continuous wave blockers for an LTE 20 MHz channel with respect to channel center frequency offset. The reference sensitivity (REFSENS), which is the minimum signal the receiver should be able to receive and process with a 95 % throughput, is between -94 dBm and -90 dBm depending on the band. Assuming the effective bandwidth is 18 MHz, according to table I, the in-channel thermal noise power is about -101.5 dBm. Furthermore, according to the standard documentation [12] the target coding rate is 1/3, for a QPSK modulated signal, which requires a signal to noise ratio (SNR) of between -1 dB [13] and -3 dB [14]. This means that the minimum signal at the antenna input can ideally be -102.5 to -104.5 dBm, which gives a margin of about 10 dB for antenna interface losses, and receiver noise figure, assuming no antenna

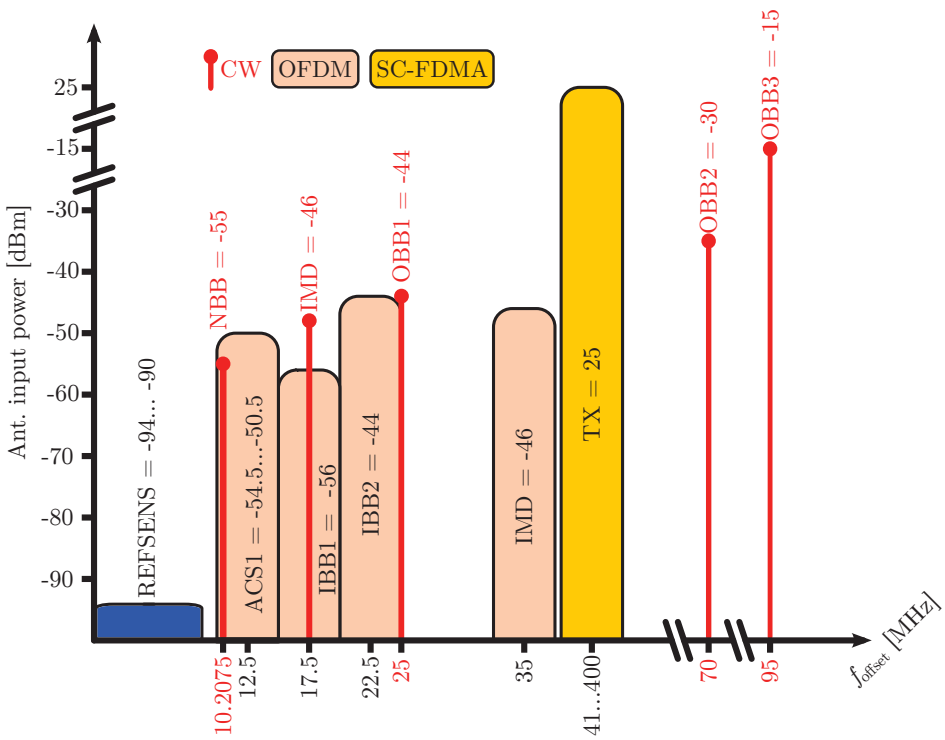


Figure 5: Example of blockers for an LTE20 channel in LTE rel. 12. Wideband signals are 5 MHz wide OFDM signals while the TX is a SC-FDMA signal that has lower peak to average ratio compated to OFDM.

gain. Just next to the receive signal, the adjacent channel can have a power of REFSENS+39.5 dB at 12.5 MHz offset.

The worst case power of the adjacent channel can be as strong as -25 dBm when the signal to be received is -50.5 dBm. The next strong blocker is the in-band blocker that can be -44 dBm at a 22.5 MHz offset. The narrowband IMD signal at 17.5 MHz offset, present at the same time as the wideband IMD at 35 MHz offset, will cause intermodulation distortion due to finite third order linearity as will be described later in this chapter. Another very strong blocker is the device's own transmitter which can supply a signal as strong as +25 dBm to the antenna, resulting in about +27 dBm at the TX output when accounting for losses in the duplexer. Thankfully, this off-chip duplexer attenuates the signal by about 50 dB [15, 16]. These are, however, just a few of the signals that are present at the antenna input that causes problems when designing the receiver. The power of the blockers and frequency offsets depends on RF band and channel bandwidth. There are also some relaxed requirements on the number of resource blocks used, such as in band 20 where the duplex distance is the smallest for an LTE20 bandwidth.

2.2 Architectures for RX

There are two general architectures for receiver front-ends: the homodyne and the superheterodyne. Both of them have benefits and disadvantages which are discussed below.

2.2.1 Superheterodyne

In the superheterodyne receiver [17] the received signal is down-converted to an intermediate frequency (IF). The unwanted image frequency response is suppressed by using a bandpass filter. The advantages of this structure are high image rejection if the bandpass filter has a high Q-factor, immunity to even order intermodulation distortion (primarily IM2) and DC offset, no need for quadrature mixing and LO generation, and low LO leakage to the antenna. Disadvantages are the required high Q-factor image reject and IF filter and

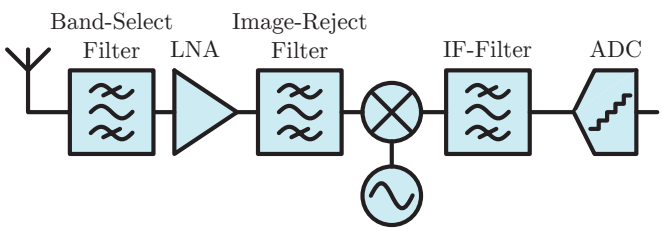


Figure 6: Superheterodyne receiver.

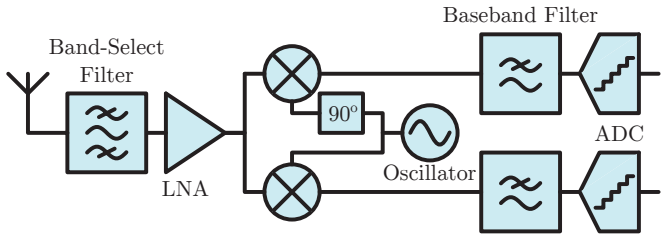


Figure 7: Homodyne receiver.

the associated integration of these components. Using a typical modern integrated process, such as the 65 nm CMOS process used for the circuits in this dissertation, the Q-value of inductors is typically limited to about 10-20 and in order to provide reasonable attenuation of the image frequency the intermediate frequency would have to be very large. There are ways of solving this by introducing active filtering such as high frequency G_m-C filters, but this usually increases the power consumption of the receiver. In even more advanced processes such as 28 nm, where the 1/f noise (flicker) noise is very high, the superhetrodyne architecture has gained new attention since no information is located close to DC.

2.2.2 Homodyne

In the homodyne [18], zero-IF or direct-conversion receiver, the problem with the image frequency is solved by down-converting the channel to a center frequency of zero. Since the image frequency is then the opposite of the receive signal, rejection of the image is simple [19], as unlike the superheterodyne receiver the image is not significantly stronger than the signal to receive. Still some image rejection is necessary to be able to distinguish positive frequencies from negative. For this purpose, to provide orthogonality between two outputs, a 90° phase shift is introduced in the LO signal to one of the down-conversion mixers resulting in a so called complex mixer. Since the output frequencies are centered around zero, the blocks after the mixer such as the CSF and ADC can operate at a minimum frequency, thus power-efficiency is optimized and CSFs can be implemented by using active-RC based architectures where high loop-gain can be exploited for linearity. The architecture has a few drawbacks: DC-offset, sensitivity to second order distortion of the down-conversion stage, and in modern processes sensitivity to 1/f noise [20]. Moreover, since the LO frequency is put in the center of the channel to be received, LO leakage is not attenuated by a image reject filter and becomes critical. LO leakage can cause DC offsets and cross-modulation with other blockers. The architecture, despite its drawbacks, is the most common solution in modern wireless integrated receivers and all included papers are therefore based on this structure.

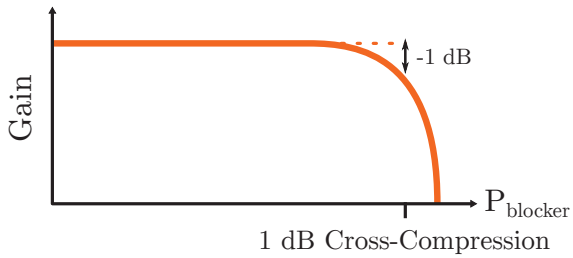


Figure 8: The 1 dB cross-compression point is defined as the power of the blocker when the small signal gain is decreased by 1 dB.

2.3 Sensitivity

Radio communication receivers are basically limited by two things: sensitivity and selectivity. The sensitivity determines how weak signal can be received and selectivity determines how strong signals can be that interfere with the received signal. Sensitivity is determined by the noise figure of the receiver, the required signal to noise ratio needed to demodulate the information and the bandwidth of the signal. Assuming and a temperature of 290 K the equation for the sensitivity in dBm is given by (1).

$$P_{sens} = -174 + NF + SNR_{min} + 10log_{10}(B) \tag{1}$$

The noise of the receiver is limited by the noise figure of the RF-ASIC, but also the insertion losses due to external SAW filters/duplexers and antenna switches. A typical noise figure of a modern RF-ASIC is about 3 dB [21–25].

2.4 Desensitization

At the input of the RF-ASIC there are more signals than the wanted one present. For instance, there are often adjacent channels in the same band and if an FDD system is being used, the device's own transmitted signal will also be present at the input of the receiver. All these interferers can cause desensitization of the receiver and relaxing the requirements of the off-chip filters and duplexers can worsen the situation by further increasing the power of the interferers.

2.4.1 Gain Compression

If a strong enough blocker is present the small signal gain of the receiver will eventually be degraded. A common metric is the 1 dB compression point, defined as the blocker power level where the small signal gain has decreased

by 1 dB, see figure 8. This compression is also sometimes called 1 dB cross-compression point, to distinguish the small signal compression of the in-band signal from the large signal compression of the blockers. There can also be large signal compression if the wanted signal itself is too large. To illustrate this, the input signal in typical wireless standards can be between -100 and -25 dBm. If the gain of the receiver is set to maximum, to minimize the noise figure, a -25 dBm input signal can compress the system. This is solved by introducing a block called the received signal strength indicator (RSSI) that can tune the gain of the receiver for a given scenario; if a strong wanted signal is present the gain can be reduced and even if the noise figure is increased the SNR is still sufficient for demodulation. For cross-compression the wanted signal is at -100 dBm, and a maximum gain is needed to have a minimum noise figure, but the small signal gain is decreased by an out-of-channel blocker. The blocker causing this degradation can be the transmitter in an FDD scenario, but can also be other external blockers originating from other devices, or from other standards in the same terminal. Such an example is the coexistence of WiFi, Bluetooth and LTE that can cause problems [26, 27]. It should be noted that if the small signal gain is decreased the noise will also increase, thus the most accurate way of measuring the desensitization due to a single blocker would be to look at the 1 dB degradation of SNR or signal to noise and distortion ratio (SNDR).

2.4.2 Cross-modulation

Another cause of desensitization is cross-modulation. Consider an amplitude modulated (AM) blocker at f_{mod} together with a continuous wave (CW) signal at f_1. If the signals are amplified by a system that exhibits third order non-linearity, the AM will "move" from the modulated blocker to the pure sinusoidal carrier. This is further explained in (2) where the two signals are amplified by the cubic term of the receiver. The final expression contains two terms where C is signals at frequencies that are not of interest, but the other term is at f_1, with amplitude modulation due to $m(t)$.

$$\begin{aligned} y_3 &= a_3(A_1 cos(2\pi f_1) + A_2(1+m(t))cos(2\pi f_{mod})^3 = \\ &= B + 3a_3A_1A_2^2(1+m(t))^2 cos(2\pi f_1)cos^2(2\pi f_{mod}) \\ &= C + \frac{3}{2}a_3A_1A_2^2(1+m(t))^2 cos(2\pi f_1) \end{aligned} \tag{2}$$

The resulting power of the cross-modulation is then $P_{crossmod} = C_{factor} + 2P_{f_{mod}} + P_{f_1}$–$2IIP3$, where C_{factor} depends on the modulation of the blocker. In [28] C_{factor} is 7.4 dB for the WCDMA TX signal and 2.4 dB for a narrowband blocker.

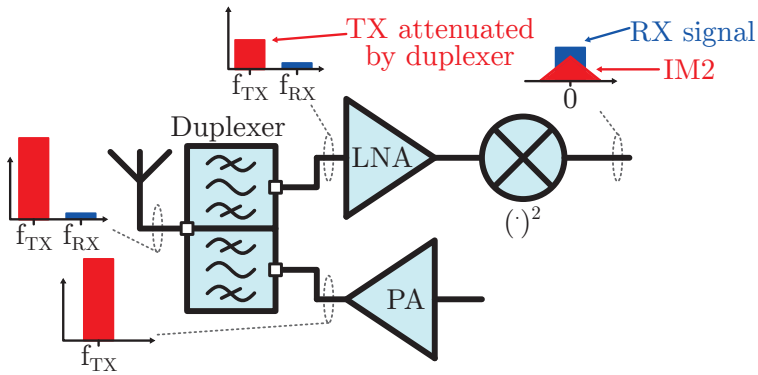


Figure 9: Due to finite IIP2 in the mixer, IM2 from the TX will be present in the receive band and will decrease the sensitivity.

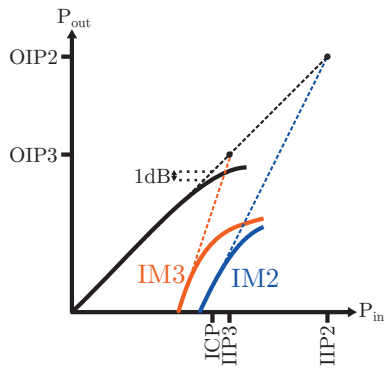


Figure 10: Definitions of both input referred and output referred IP2, IP3 and 1 dB compression point.

2.4.3 2nd Order Non-Linearity

Consider a signal that has some kind of amplitude modulation, this can be either pure AM or a more complex modulation such as QAM, present at the input of the receiver. To simplify the analysis the AM signal is modeled by two tones, f_1 and f_2, closely spaced. If the receiver has second order non-linearity, corresponding distortion will be present at the output. Of special interest is the intermodulation at $|f_1 - f_2|$ as this will be at a baseband frequency, assuming close spacing of the two tones. If this occurs in the LNA, it is less of a problem since the LNA is working at a high frequency and the low frequency distortion can be filtered out by placing a capacitor between the LNA and the mixer. But for the mixer it is a problem since both the wanted information and the second order intermodulation distortion is present at the output at

baseband frequencies [29,30]. After this point, it is hard to distinguish between the information and intermodulation, and the intermodulation can be seen as extra noise which will degrade the sensitivity, see figure 9. There are ways of removing part of the IM2 components in the digital domain [31–33], but these methods will not be further considered in this dissertation.

The most common way of measuring second order intermodulation (IM2) performance of a receiver is to use the second order intercept point (IP2), found by extrapolating the IM2 power and the fundamental power with respect to the input power, all in logarithmic scales, and then see where the extrapolated lines intercept, figure 10. The IP2 can be referred either to the input or to the output of the receiver and in a receiver typically the input referred second order intercept point (IIP2) is used as the performance metric for second order linearity. IIP2 is calculated as (3), where P_{in} is the input power of both the wanted signal (P_{fund} in the baseband) and the two tones that will cause the IM2 product P_{IM2}. A higher IIP2 thus indicates a more linear receiver.

$$IIP2_{2t} = P_{in} + P_{Output\ fund} - P_{OIM2} = 2P_{in} - P_{IIM2} \tag{3}$$

All units must be in logarithmic scale and typically dBm is used. It should be noted that modeling the AM input as two tones as is a worst case condition and realistic scenarios are less severe. A correction factor should thus be added, since the IM2 information is spread beyond the wanted channel's bandwidth. This correction factor depends on several circumstances, such as the standard being used and the channel bandwidth. As an example how the standards can differ is that 3G uses WCDMA for the uplink whereas LTE uses SC-FMDA. Another circumstance that sets the correction factor for LTE is the bandwidth of the downlink. More information about how to derive the correction factors can be found in [34, 35].

According to [34], the most challenging IIP2 requirement for LTE occurs when using band 4 (2110–2155 MHz for the downlink) and the signal bandwidth is 1.4 MHz. In this band the sensitivity defined by the standard is -104.7 dBm [12]. By using (4), where P_{TX} is the transmitted power at the TX output (generally $+23 \pm 2 + IL_{TX}$ dBm [12]), R_{dup} is the duplexer isolation (typically about 50 dB [15, 16]), Δ_M is a margin to the sensitivity, and Δ is a margin to determine how much of the sensitivity level that is determined by IM2.

$$IIP2 = 2(P_{TX} + R_{dup}) - P_{sens} + \Delta_M + SNR + IL_{RX} + \Delta \tag{4}$$

$$IIP2_{2t} = IIP2 - CF \tag{5}$$

The resulting IIP2 is then about 70 dBm for band 4 and 1.4 MHz bandwidth. After correcting for the modulation correction factor (CF) in (5) the required two tone IIP2 is however about 60 dBm. Generally, the correction factor for LTE is between 9 and 11 dB. In a perfectly matched (symmetrical)

differential circuit the even order distortion will be cancelled. An IIP2 of more than 60 dBm is, however, challenging to reach without calibration and thus it is very important to spend great effort in making the LO distribution and mixer layout as symmetrical as possible.

The previous statement that the second order non-linearity of the LNA is neglectable is not true if carrier aggregation is being used. Assume a carrier aggregation scenario with one carrier at f_x and another one at approximately $2f_x$, and the uplink allocated to the uplink frequencies of the second carrier. An example of this can be when using a combination of band 12 (RX of 729–746 MHz) and band 11 (TX of 1427.9–1447.9 MHz). A blocker at $f_{TX,B11} - f_{RX,B12}$ can then modulate with $f_{TX,B11}$ and cause a tone at $f_{TX,B11} - (f_{TX,B11} - f_{RX,B12}) = f_{RX,B12}$.

2.4.4 3rd Order Non-Linearity

Another important scenario where blocking can occur is when a strong signal is located, at a frequency f_1, between the received signal and the transmitted signal, f_2. This blocker will reach the input and generate third order intermodulation at $2f_1 - f_2$, i.e. at the same frequency as the wanted signal, figure 11. The same problem occurs when a blocker at f_3, twice the TX offset frequency, is present. Similar to IIP2, the input referred third order intercept point can be calculated as (6)

$$IIP3 = P_{in} + \frac{P_{Ofund} - P_{OIM3}}{2} = \frac{3P_{in} - P_{IIM3}}{2} \tag{6}$$

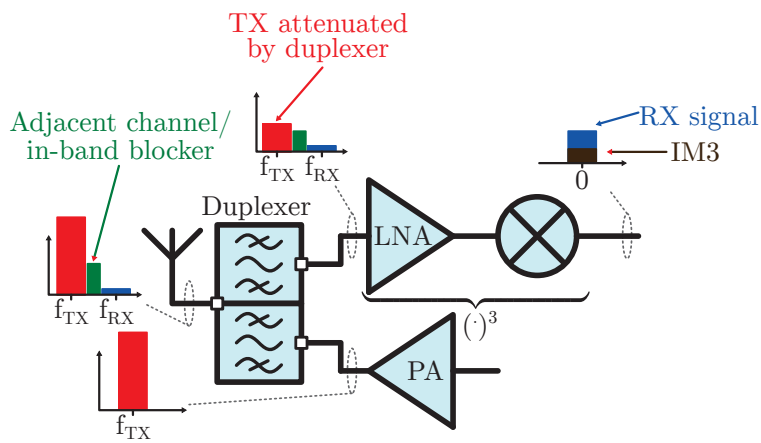


Figure 11: Due to finite IIP3 in the receiver, a blocker at half duplex distance can together with the strong TX signal create an IM3 component that can degrade the sensitivity.

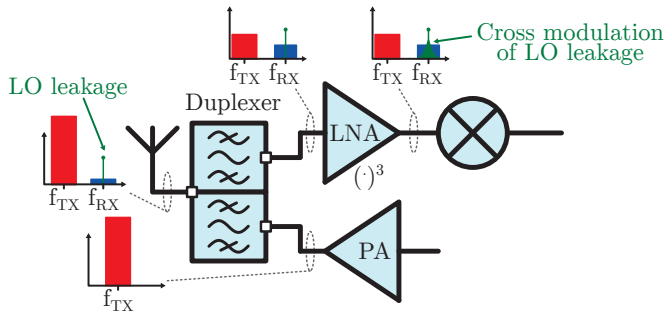


Figure 12: If there is LO leakage at the antenna input, an AM modulation can be cross-modulated in the LO leakage and desensitise the receiver.

2.5 LO Leakage

An important parameter that is becoming critical with the introduction of passive mixer-first receivers is the LO leakage. In more common architectures the LNA is isolating the RF input to the LO. The amount of isolation depends on several parameters such as the type of LNA and LO routing. As an example a common gate LNA has higher isolation than an inductively degenerated common source stage and use of a cascode in the LNA can further reduce the LO leakage. For a passive mixer-first topology or other similar N-path filters, the LNA is removed and the mixer is placed directly at the RF input.

The LO leakage can cause several problems; the first is not to exceed the spurious emission levels allowed by the standard and regulations. For a passive mixer the LO leakage is in the order of -60 to -80 dBm, which can be on the limit of what is tolerated from the spurious emissions point of view, which is -57 to -47 dBm for LTE. Another problem is the DC offset caused by the LO leakage. When a sinusoidal signal is mixed with itself, the resulting output is DC and a second harmonic tone. This DC is then amplified by the subsequent baseband blocks in the receiver and when reaching the ADC the offset can be several 100 mV, which decreases the resolution of the ADC. Thus DC offset calibration loops should be used if a large LO leakage is anticipated [36–38]. The third problem with LO leakage is cross-modulation. As described above and explained in (2), the LO leakage is a sinusoidal blocker that can be cross-modulated by the TX leakage and cause an increased noise floor.

2.6 Reciprocal Mixing

Another problem in cellular receivers is reciprocal mixing. The LO signal that is used to drive the mixer is not a perfect single tone signal, but has some phase noise. As an example, if the phase noise of the LO signal is -160 dBc/Hz at an offset of 100 MHz, a 0 dBm blocker at 100 MHz offset will then not

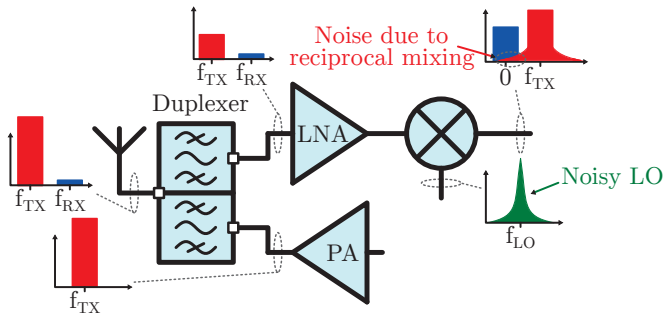


Figure 13: Phase noise of the LO can cause severe desensitisation when a strong blocker is present. Since the mixer will also down-convert the TX to RX baseband frequencies due to the noisy LO, the resulting in band noise is increased.

only produce a strong signal at 100 MHz baseband frequency, but there will also be noise from the TX in the receive band with an input referred power of -160 dBm/Hz, see figure 13. Assuming an LTE20 signal, the total noise due to reciprocal mixing is now -90 dBm which is close to the reference sensitivity level of the receiver, increasing the noise figure. Assuming that a receiver with a sensitivity level of -174dBm/Hz, the additional excess noise factor due to reciprocal mixing, F_{RM}, would be (7), where P_b is the blocker power and $L(\Delta\omega_b)$ is the receiver LO phase noise at the blocker frequency offset.

$$F_{RM} = 10^{(P_b + L(\Delta\omega_b))/10} \tag{7}$$

2.6.1 Harmonic Mixing

Since the use of the passive mixer has become widespread the most common LO signals are square waves. Square waves are easy to generate and distribute on-chip, since digital gates as inverters have a high speed and can work in a power-efficient way in modern CMOS technologies. One problem with square wave signals is, however, the harmonic content. Since a square wave signal contains all odd harmonics of the fundamental frequency, noise and signal at these harmonics can be down-converted, figure 14. When the receiver is wide-band without explicit filtering after amplification, all thermal noise is fed to the down-conversion stage. This will increase the noise figure by close to 1 dB, according to (8).

$$NF_{harm.\ mix.} = 10log_{10}\left(1 + \sum_{k=1}^{\infty} \frac{1}{(2k+1)^2}\right) = 10log_{10}\left(\frac{\pi^2}{8}\right) \approx 0.91 \text{ dB} \tag{8}$$

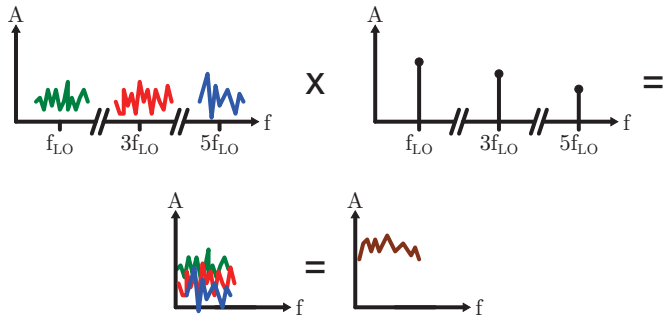


Figure 14: If a square wave signal is used in the mixer, noise and signals at odd harmonics will get down-converted and this will increase the noise floor in the baseband.

Chapter 3

Receiver Building Blocks

This chapter describes radio receiver front-end building blocks and presents some of the design challenges.

3.1 LNA

Usually, the first block at the radio input of an RF-ASIC is the LNA. The LNA is placed at the input of the RF-ASIC and will interface to the off-chip components. To make sure all the power from the antenna and off-chip component with impedance Z_S is transferred into the RF-ASIC, the LNA should provide a real input impedance Z_L. If there is a mismatch between the two impedance levels a reflection factor Γ, equation (9), will determine how much power is reflected back to the antenna. Usually this is presented by the input reflected power ratio S_{11}, which typically should be maintain to below -10 dB.

$$\Gamma = \frac{E^-}{E^+} = \frac{Z_L - Z_S}{Z_L + Z_S}, \quad S_{11} = 20 \cdot log_{10}(|\Gamma|) \tag{9}$$

Furthermore, since the total noise factor of the receiver, equations (10) and (11) where F is the noise and G is the gain, is dominated by the first block, the noise figure of the LNA should be as low as possible.

$$F = \frac{SNR_{\text{input}}}{SNR_{\text{output}}} \tag{10}$$

$$F = F_1 + \sum_{i=2}^{N} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j} = F_{LNA} + \frac{F_{other} - 1}{G_{LNA}} \tag{11}$$

At the same time, the noise from the subsequent blocks is attenuated by the gain of the LNA and the gain should thus be as high as possible without introducing too much distortion. These requirements poses high challenges when designing a high-performing LNA for a cellular receiver. There are mainly three different types of LNAs which are described in this section.

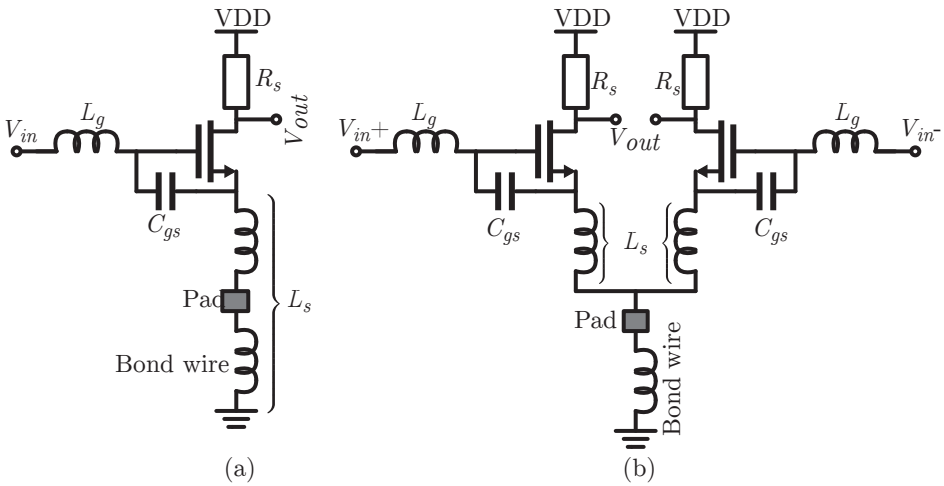


Figure 15: Schematic of the IDCS LNA. (a) The single-ended IDCS is sensitive to added inductance from bond wires. (b) Differential IDCS requires two inputs and twice the current compared to the single-ended version, but is more robust in terms of parasitics and has less even order non-linearities.

3.1.1 Inductively Degenerated Common-Source LNA

The inductively degenerated common-source (IDCS) LNA is a high performance LNA capable of very low noise figure. Since the noise figure is proportional to ω_0/ω_T the performance increases with more advanced process nodes [39–41]. The low noise is achieved using a passive input network that will amplify the signal voltage before reaching the input transistor, thus reducing the noise contribution from the MOSFET. The idea behind the IDCS LNA is to use an inductor between the source of the device and the ground, see figure 15, to create a series resonance circuit and thus a resistive part of the input impedance. By adding an extra inductor at the gate, L_g, the input reactance can be cancelled at the frequency of operation. This gate inductor is providing most of the passive voltage gain before the signal reaches the MOSFET. The input impedance is given by (12), and the resonance frequency by (13).

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{12}$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{13}$$

The main problem with the IDCS LNA is the narrow frequency operation associated with the inductors. A very wide frequency range of operation is required in modern cellular receivers and since the IDCS LNA is tuned to

resonate at a certain frequency, wideband performance is hard to implement. In order to benefit the most from the voltage gain advantage of the input network, the resulting Q-value of the network needs to be high and the input match will thus be narrow. The high Q-value for the series network is limited by the performance of on-chip inductors and since the performance of these might be insufficient, bulky off-chip inductors may be required. There are ways of mitigating the problem of the narrow frequency range by using banks of inductors and by introducing capacitive tuning [21,22], but the area overhead might be very large.

In advanced processes, since the value of the source inductor L_s is inversely proportional to the value of ω_T (12), the source inductor becomes very small. The small value of inductance can cause problems together with the parasitic inductance from bond wires and package. Thus EM simulations and estimation of all parasitics of the ground is important, see figure 15(a). On chip decoupling can also be used, keeping most of the RF current on-chip, but still the inductance may be significant compared to L_s. The problem of parasitic inductors can be alleviated by the use of a differential structure, see figure 15(b), keeping the current in the bond wires constant (DC only).

To decrease the small source inductance and to reach a lower noise figure by reduction of gate induced noise there is often an explicit capacitance placed in parallel with C_{gs} [40]. This increases the effective capacitance, and thus increases the value of L_s, and at the same time decreases the value of L_g making it more suitable for on-chip implementation. Even though, since high-performance inductors are needed, the IDCS LNA was not considered in any of the circuit implementations presented in the attached papers of this dissertation.

3.1.2 Common-Gate LNA

The common-gate (CG) LNA, figure 16(a), can ideally (assuming no capacitance, output impedance, nor any contribution from g_{mb}) provide a pure resistive input match that equals to $Z_{in} = 1/g_m$. The key advantages of this amplifier are the wideband frequency range, high linearity, and low power consumption whereas the main shortcoming is the limited noise performance. Another disadvantage is the matching condition of $Z_{in} = 1/g_m$, i.e. g_m can't be arbitrary chosen to set performance of the LNA. This puts a lower limit on the achievable noise factor of the CG LNA at $\mathrm{F} = 1 + \gamma$ or $\mathrm{NF} \approx 3$ dB, when in matched condition and used in its standard configuration. The thermal noise coefficient, γ, is equal to $2/3$ at low electric field, but can be considerably higher in short-channel devices [42, 43].

To improve the noise performance of the CG LNA a feed-forward gain of $-A$ can be introduced from the input (source node) to the gate, increasing the effective g_m of the amplifier by a factor of $(1 + A)$, see figure 16. To maintain

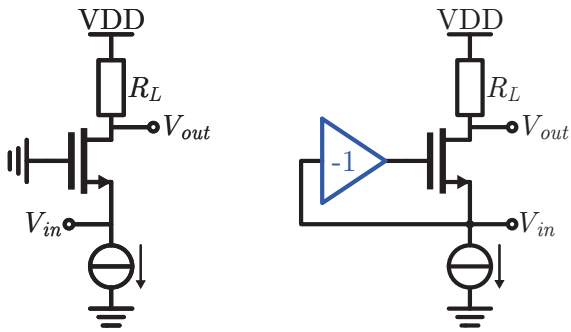


Figure 16: (a) The CG LNA provides a very wideband input match but suffers from restrictions in selection of g_m. (b) By introducing amplification from input to the gate the noise figure can be reduced.

the input match g_m should then be reduced by the factor $(1 + A)$ which will result in a $1 + A$ times less channel noise contribution from the transistor. The minimum noise factor then becomes $F = 1 + \gamma/(1 + A)$ [44, 45].

There are several ways of implementing this feed-forward gain, but if an active device is used as a feed-forward amplifier [46] the noise of that amplifier will also affect the noise performance. An attractive solution is thus passive amplification, either by using capacitive cross coupling (CCC), which will limit the feed forward gain to unity and provide $F = 1 + \gamma/2$, or by using transformers, where the mutual coupling ratio between the inductors can be chosen to obtain more voltage gain and less noise, at the cost of reduced linearity [47].

Another way to increase the freedom in selecting the parameters of the CG LNA is to introduce positive feedback [48, 49]. In a similar way as the feed forward path can increase the effective g_m and decrease the input impedance, the positive feedback can instead increase the effective input impedance. By using both techniques in combination the performance can be set within wider bounds, still ensuring input matching and stability (limited by the positive feedback). The LNAs in papers I and II are based on the CG topology.

3.1.3 Noise-Cancelling CG LNA

One way of reducing the noise of the CG LNA is to use noise-cancellation [50], depicted in figure 17(a). In addition to the CG LNA in figure 16, a CS stage has been introduced in parallel with the same input signal as the CG stage. This enables a single-ended to differential conversion by exploiting the inverting transfer function of the CS amplifier in combination with the non-inverting CG configuration. Channel current noise of the CG stage will introduce a voltage

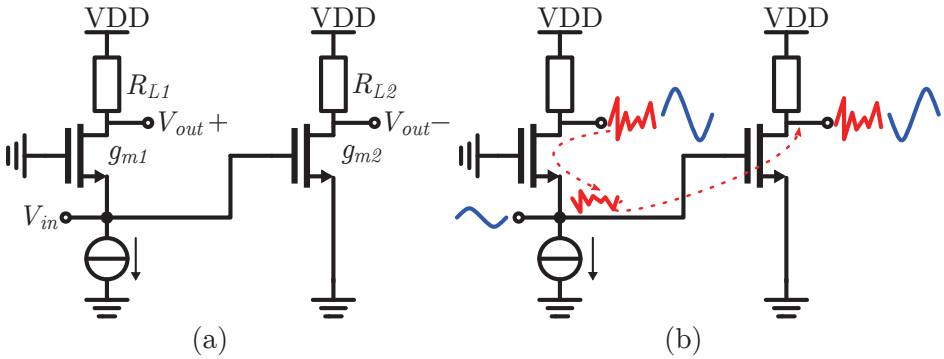


Figure 17: (a) Schematic of a noise-cancelling CG amplifier. (b) Conceptual schematic of how the channel noise of the CG stage is sensed by the CS stage and appears in common-mode at the output.

at the output that is in anti-phase with the corresponding voltage noise at the input, see figure 17(b). The noise at the input is then sensed by the CS stage and amplified to the negative output $V_{out}-$. Now, if the outputs are balanced by $g_{m1}R_{L1} = g_{m2}R_{L2}$, the noise of the CG stage appears in phase and with the same amplitude at both outputs, i.e. it is cancelled at the differential output. This is very beneficial, since g_{m2} can be arbitrarily set, and it can be increased to decrease the remaining transistor noise, the contribution of the CS stage.

3.1.4 Noise Analysis of the CG LNA in Paper II

The schematic of the LNA in paper II can be seen in figure 18(a) and consists of a differential complementary CCC-CG input stage (M_1, M_3) and negative-resistance current sources (M_2, M_4). The effective g_m of M_1 and M_3 is doubled due to the CCC providing $A = -1$. The differential stage can be simplified to the half-circuit in figure 18(b). Due to the complementary structure the circuit can be further simplified by folding to figure 18(c), where the PMOS devices are replaced by NMOS devices. The input resistance of this structure is given by (14), where $g_{mcg} = g_{m1} + g_{m3}$ and $g_{mc} = g_{m2} + g_{m4}$.

$$Z_{in} = \frac{1}{2g_{mcg} - g_{mc}} \tag{14}$$

To calculate the noise performance, the circuit in figure 18(d) can be analyzed where the two noise sources $\overline{i_{ncg}^2}$ and $\overline{i_{nc}^2}$ will be the contributors to the noise factor (15).

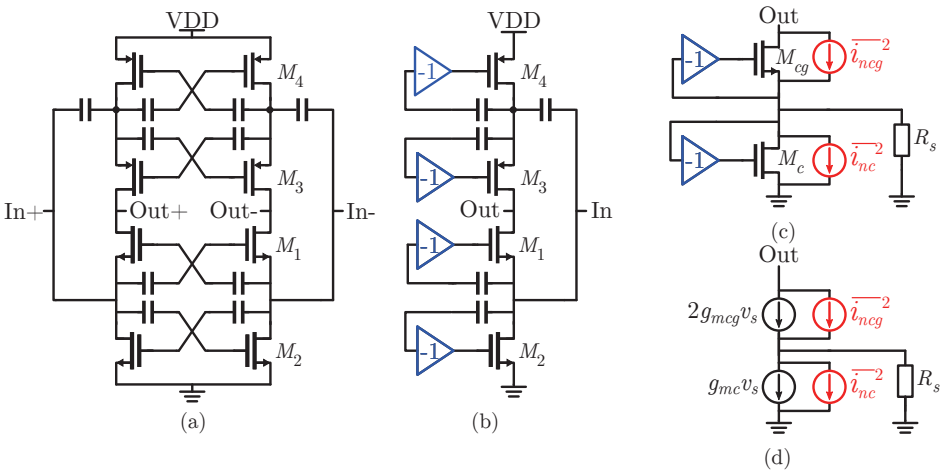


Figure 18: (a) Schematic of the LNA in paper II. (b) Half-circuit simplification. (c) Folded simplification with noise sources. (d) Noise analysis.

$$F = 1 + \frac{\gamma(R_s g_{mc} - 1)^2}{g_{mcg} R_s (2R_s g_{mcg} - R_s g_{mc} + 1)^2} + \gamma g_{mc} R_s = 1 + \frac{\gamma(R_s g_{mc} - 1)^2}{4 g_{mcg} R_s} + \gamma g_{mc} R_s, \text{ if } R_s = Z_{in} \tag{15}$$

An interesting feature of this LNA is that if $g_{mcg} = g_{mb} = 1/R_s$ mS, the noise of the CG transistors will not reach the output, but circulate inside the MOSFETs and will not contribute to the noise figure. The reason for this can be explained by calculating the transfer function from $\overline{i_{ncg}^2}$ to a noise source at the input, $\overline{i_{icg}^2}$, of the CG stage as (16). When $g_{mb} = 1/R_s$ mS the resistance seen by the CG stage is infinite, thus all noise will circulate.

$$\frac{\overline{i_{icg}^2}}{\overline{i_{ncg}^2}} = \left(\frac{1}{1 + \frac{2g_{mcg}}{-g_{mb} + \frac{1}{R_s}}} \right)^2 \tag{16}$$

3.1.5 Shunt-Shunt Feedback LNA

The shunt-shunt feedback LNA (FB LNA), figure 19, uses negative feedback[2] to decrease the input impedance seen from the ideally open gate input of the MOSFET [51]. The equation for the input impedance is given by (17).

[2]In this dissertation only resistive feedback is considered, but capacitive feedback is also possible.

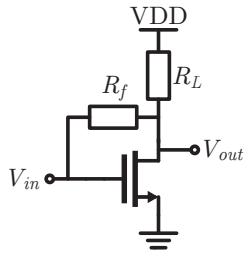


Figure 19: By introducing a resistive feedback, the high open loop input impedance will decrease and matching can be accomplished.

$$Z_{in} = \frac{R_f + R_L}{1 + g_m R_L} \tag{17}$$

Assuming a very high load resistance the input impedance approaches $1/g_m$, the same as for the CG LNA, since the input transistor looks like a diode-connected transistor. However, in real implementations, the load resistance cannot approach infinity, but is at least limited to $1/g_{ds}$ of the transistor, typically in the range of $\sim$ 1 kΩ. The large benefit of the FB LNA is the simple structure and the absence of inductors. A disadvantage is that it relies on a voltage output and requires voltage gain for the feedback to be operational. In order to work as an low noise transconductance amplifier (LNTA), i.e. an amplifier with a current output, either by current steering in a single stage as presented in [52] or using a cascade of a shunt-shunt feedback LNA and a g_m-stage can be used as in the implementation of the LNA in paper V.

3.1.6 Noise-Cancelling Shunt-Shunt Feedback LNA

Noise-cancellation can also be used in the FB LNA to reduce the noise figure. The schematic of one such noise-cancelling LNA is shown in figure 20(a), where a second stage has been introduced with a CS amplifier and a source follower at the top [53]. The transistor channel noise of the FB LNA will be present at the output of the FB LNA, and it will also be fed back to the input through resistive voltage division between R_f and R_s, see figure 20(b). This noise is sensed by the CS stage, consisting of M_2, and the noise is amplified with an inverting transfer function. At the same time, the noise from the FB LNA is also fed to the source follower, M_3, where it is amplified with unity gain and non-inverting transfer to the output. The noise voltages, perfectly correlated since they originate from the same noise source, will cancel at the output if $g_{m3} = g_{m2}/A_{v1}$, where A_{v1} is the voltage gain of the shunt-shunt feedback input stage.

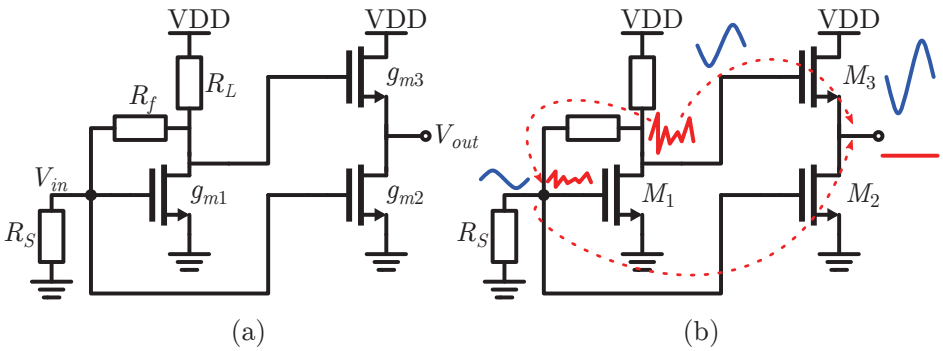


Figure 20: (a) Schematic of a noise-cancelling FB LNA. (b) Conceptual schematic of how the channel noise of the left CS stage is sensed by the right CS stage and then cancelled at the output.

3.1.7 Noise Analysis of the FB LNA in Paper V

Paper V introduces a wideband single-ended to differential noise-cancelling FB LNA, and a simplified schematic is presented in figure 21(a). The amplifier consists of two parallel paths. The first path consists of an shunt-shunt feedback input stage to provide input match, and a second stage provides an output current and signal inversion. The total gain of this path is $g_m = (1 - R_f/R_s)(-g_{m2})$, where g_{m2} is the total transconductance from M_{n2} and M_{p2}. In the parallel second path, a g_m-stage with a total transconductance of $g_{m3} = g_{mMn3} + g_{mMp3}$ is used, and the gain of this path can be selected to match that of the first path for balanced signals. The LNA is further simplified in figure 21(b) where the complementary structure is folded to an equivalent NMOS structure and the parallel output resistance of the devices in the input stage is replaced by R_L.

A nice feature of this LNA is that channel noise from M_1 and noise from R_L can be cancelled. Assuming that these noise sources will cause a voltage at the output of the shunt-shunt feedback stage, this voltage will be amplified to the positive output by g_{m2}, but the voltage is also fed back to the input by the resistive voltage division of $R_s/(R_s + R_f)$ and amplified to the negative output by g_{m2}. If (18) is met, noise is thus cancelled at the differential output.

$$\frac{g_{m3}}{g_{m2}} = 1 + \frac{R_f}{R_s} \tag{18}$$

The full expression of noise factor of the LNA (19) is calculated by analyzing figure 21(c) and assuming perfect common-mode suppression. It is possible to decrease the noise figure further by increasing the value of R_f beyond its optimum value for input matching.

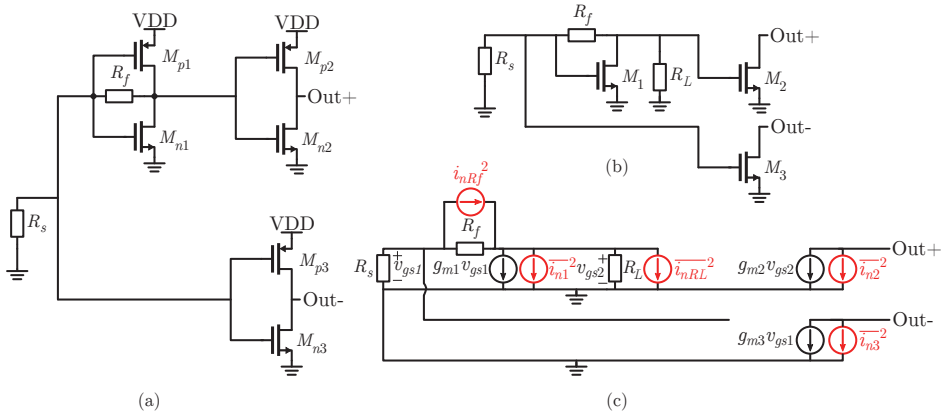


Figure 21: (a) Schematic of the LNA in paper V. (b) Simplified schematic with folding. (c) Schematic for noise analysis.

$$
\begin{aligned}
F =& 1 + \frac{4R_f\left(R_L g_{m2}(R_s g_{m1}+1)+R_s g_{m3}\right)^2}{R_s\left(R_L\,R_s\,g_{m1}+R_L+R_f+R_s\right)^2\left(\left(1-\frac{R_f}{R_s}\right)(-g_{m2})+g_{m3}\right)^2} \\
&+ \frac{4R_L^2\gamma g_{m1}\left((R_f+R_s)g_{m2}-R_s g_{m3}\right)^2}{R_s\left(R_L\,R_s\,g_{m1}+R_L+R_f+R_s\right)^2\left(\left(1-\frac{R_f}{R_s}\right)(-g_{m2})+g_{m3}\right)^2} \\
&+ \frac{4R_L\left((R_f+R_s)g_{m2}-R_s g_{m3}\right)^2}{R_s\left(R_L\,R_s\,g_{m1}+R_L+R_f+R_s\right)^2\left(\left(1-\frac{R_f}{R_s}\right)(-g_{m2})+g_{m3}\right)^2} \\
&+ \frac{4\gamma g_{m2}}{R_s\left(\left(1-\frac{R_f}{R_s}\right)(-g_{m2})+g_{m3}\right)^2} + \frac{4\gamma g_{m3}}{R_s\left(\left(1-\frac{R_f}{R_s}\right)(-g_{m2})+g_{m3}\right)^2}
\end{aligned}
\tag{19}
$$

In paper V the main single noise contributor, accounting for 10 % of the total output noise power (including the noise from the source resistance which accounted for 75 %), was R_f and the total noise figure was simulated to below 1.6 dB.

3.2 Passive Mixer

The passive mixer usually consists of a number of CMOS switches that are controlled by square wave signals at a frequency of f_{LO} [54], figure 22. Usually, the LO signals are divided into N non-overlapping phases where each phase has a frequency of f_{LO} and a duty cycle of $1/N$. Each of the square wave

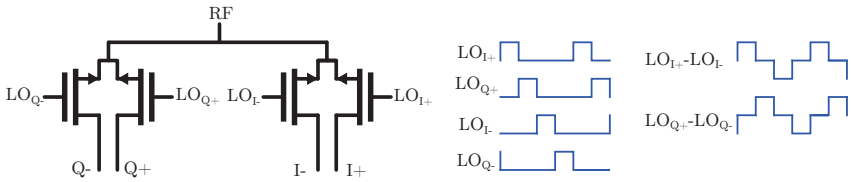


Figure 22: Circuit implementation of a single-balanced passive mixer together with the LO signals.

signals can be seen as a pulse train and can be expanded into a Fourier series equivalent (20), with coefficients according to (21) for the periodic signal.

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n cos(2\pi ftn) + \sum_{n=1}^{\infty} b_n sin(2\pi ftn) \tag{20}$$

$$a_0 = \frac{1}{T}\int_{-T/2}^{T/2} x(t)dt,\ a_n = \frac{2}{T}\int_{-T/2}^{T/2} x(t)cos\left(\frac{2\pi tn}{T}\right)dt$$
$$b_n = \frac{2}{T}\int_{-T/2}^{T/2} x(t)sin\left(\frac{2\pi tn}{T}\right)dt \tag{21}$$

Assuming the signal $x(t)$ is an square wave signal, the coefficients becomes (22).

$$a_0 = 1/M,\ a_n = \frac{1}{M}sinc\left(\frac{\pi n}{M}\right),\ b_n = 0 \tag{22}$$

An input tone at frequency $n \cdot f$ is multiplied with the coefficient a_n (the coefficient at $n \cdot f$) and the resulting output tone resides at the difference, and at the sum, of the two frequencies. This, however, also means that noise at $n \cdot f$ is down-converted to baseband as described in (8). The gain of the mixer of however described by the coefficient of the fundamental harmonic, i.e. a_1.

An important advantage of the passive mixer is the reciprocal impedance translation. This effect is due to the bilateral property of the passive mixer which will down-convert and up-convert and the same time, providing a low-Q filter at the IF side to be up-converted into a high-Q filter centered at the LO frequency, and its harmonics. This technique can be exploited to create a high-Q bandpass filter at the output of an LNA that is assumed to be working in voltage mode as in [55], thereby reducing the interference. The technique can also be used to synthesize N-path filters [56–60] that can create very sharp and tunable bandpass or bandreject filters at RF. By terminating the passive mixer with a low impedance at the IF side, e.g. by using a transimpedance amplifier, the passive mixer will operate in current-mode together with the proceeding

LNTA[3]. This will provide a high linearity by minimizing the voltage swing of both the LNTA and the mixer [61].

3.2.1 Noise in Passive Mixer

The main noise contributor in a passive mixer is the on-resistance. As seen in figure 23(b), each transistor can be modeled as an ideal switch, a resistor and a noise voltage source of $\overline{v_1^2} = \overline{v_2^2} = 4kTR_{sw}$. The noise sources are then moved to the input of the mixer as the source $\overline{v_{sw}^2} = 4kTR_{sw}$, see figure 23(d) assuming non overlapping LO signals such as the 25 % duty cycle LO signals in figure 23(c). To calculate the noise factor (23), the noise is transferred to the output of the circuit as the input noise multiplied with the gain at all harmonics and then related back to the input by the gain of the fundamental harmonic.

$$F = \left(1 + \frac{R_{sw}}{R_s}\right) \frac{\sum_{n=1}^{\infty}(K_n)^2}{(K_1)^2} \tag{23}$$

In (23) K_n are the Fourier coefficients from the effective LO wave. For a standard pulse train, $K_n = a_n$, where a_n are calculated from (22). If the effective LO wave is a differential signal $K_{2n} = 0$, and by introducing more phases other coefficients of K_n become zero. This oversampling of the LO signal to reject down-conversion from harmonics is further described in chapter 4.

[3] An LNA working in current-mode is an LNTA.

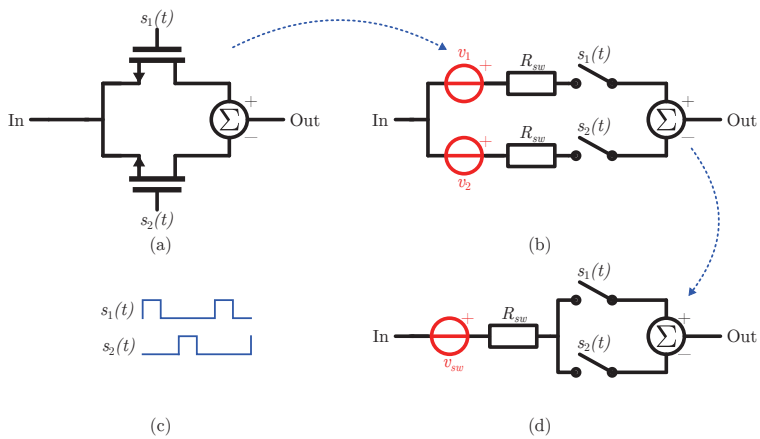


Figure 23: Single balanced passive mixer (a) transistor level implementation. (b) Ideal switches with resistors. (c) 25 % duty cycle LO pulses. (b) Simplified model for noise calculations.

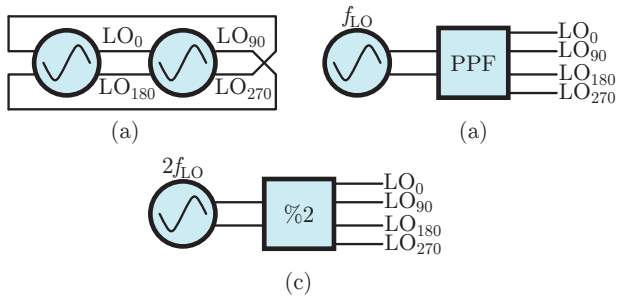


Figure 24: Quadrature LO signal generation can be accomplished by using: (a) A QVCO where two VCO cores are locked in 90° phase shift. (b) Polyphase filter together with a VCO running at f_{LO}. (c) VCO running at $2f_{LO}$ and a frequency divider.

3.3 LO Divider

In a standard quadrature receiver without harmonic rejection (number of phases $N = 4$) the LO signals can be generated from a quadrature voltage-controlled oscillator (QVCO), where two differential voltage-controlled oscillators (VCOs) are injection locked to each other in such that the outputs have a phase difference of 90°, see figure 24(a). The advantage with the QVCO is high Q-value[4], i.e. good phase noise and low power, especially since no frequency divider is needed to generate the quadrature signals. This is especially an advantage at mm-wave frequencies where can be hard to generate a $2f_{LO}$ signal due to limitations of the processing technology. A disadvantage of the QVCO is that a PA in proximity of the QVCO can cause frequency pulling since they operate close in frequency [62] and the QVCO area will also be large due to the two inductors needed. Furthermore, for the direct-conversion receiver, since the oscillation frequency is the same as that of the receive signal, coupling from the QVCO to the RF input can cause a baseband DC offset and LO leakage at the RF port.

Another approach is to use a single VCO running at the LO frequency, combined with a polyphase filter (PPF) to generate the quadrature outputs, figure 24(b). The PPF uses a passive *RC*-filter to generate differential quadrature signals from a single differential input [63]. Since the oscillator is operating at the same frequency as the RF signal, this approach suffers from the same problem as the QVCO: pulling, LO leakage and DC offsets. In order to achieve better quadrature accuracy, multiple stages are usually used in the PPF. The approach of using a PPF is rather narrowband and tuning of the *RC* components to extend the frequency range can decrease the quadrature accuracy.

A third solution, better suited for cellular frequencies, is to use a VCO

[4]It is assumed that the VCOs are based on LC-oscillators.

running at twice the wanted LO frequency and then use a frequency divider to generate the quadrature LO signals. By using a VCO at twice the wanted frequency, the problems with LO leakage are reduced. Furthermore, the area of the inductor will be reduced due to the increased frequency. This solution is assumed in all receiver front-ends described in the included papers of this dissertation, where the frequency divider has been implemented on-chip, while the two times LO signals are supplied from off-chip signal generators.

3.3.1 25 % Duty cycle

Quadrature LO signals were used in papers I, III, IV and V. The divider consists of two cascaded latches where the first latch is triggered on the positive clock slope and the second is triggered on the negative slope, see figure 25. If $2f_{LO}$ is a differential signal instead of single-ended as depicted in the figure, the delay associated by the inverter can be removed by implementing it using simple cross-coupling. Furthermore the quadrature accuracy gets insensitive to duty cycle errors. The divider produces four outputs with 50 % duty cycle, figure 26(a), and by combining these phases with digital logic, 25 % duty cycle signals can be generated. This can be done in different ways, of which two are here briefly described. The first method is to use four 2-input AND-gates where the inputs are connected to the divider outputs. By combining the 50 %

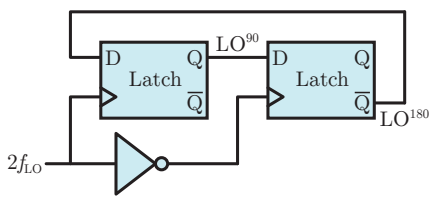


Figure 25: A standard D register, consisting of two latches, with feedback can be used to generate the quadrature outputs.

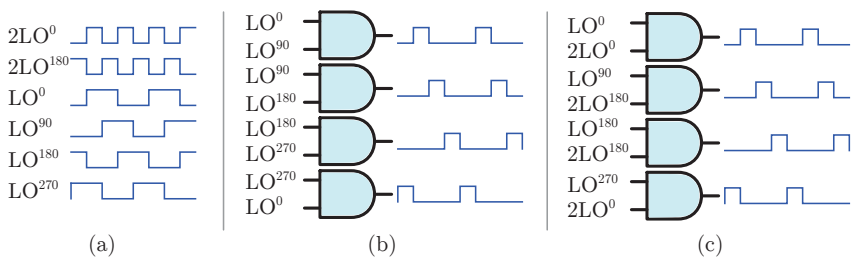


Figure 26: To provide 25 % duty cycle signals, AND gates can be used with either (b) the divider outputs or (c) divider outputs together with 2LO input signals.

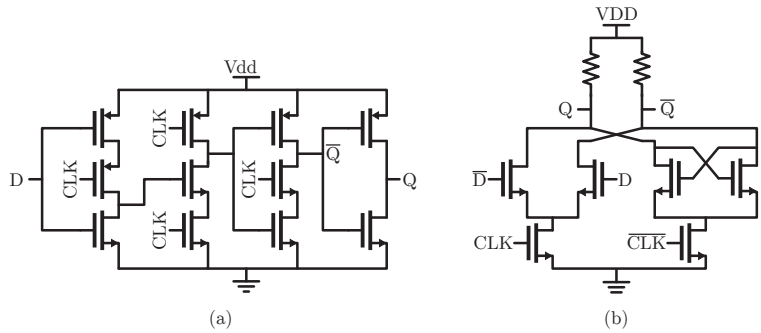


Figure 27: (a) TSPC D register. (b) CML latch.

divider outputs, 25 % signals can be achieved, see figure 26(b). A disadvantage with this technique is however that the phase noise is determined by the divider output, which has more noise than the input signals. By instead using the differential two times LO signal as one input to the AND-gates, and making sure that a small time delay is introduced, so that the 2LO signal is in the center of the LO before combination in the AND-gate, then the edges of the 2LO signals will determine the edges of the output. This typically reduces the phase noise [64].

The two latches can be implemented in different ways. In paper I, a dynamic D register [65] based divider, see figure 27(a), was used and the outputs were generated according to figure 26(b). The D register is very power-efficient, but since it is a dynamic latch low operating frequencies are not possible; the stored energy will be discharged. To create a better latch, current mode logic (CML) was used instead of the CMOS logic-based latch. However, transmission-gate based dividers or static CMOS-based dividers can also be used [66]. The CML divider has a quiescent current, which is not the case for the CMOS latch, but the ripple on the supply node will then also be smaller. The schematic of the CML latch is depicted in figure 27(b), where the left part of the circuit senses the value on the differential D-input and when CLK goes high this value is fed to the output of the circuit Q. The right part of the circuit consists of a cross-coupled stage that will store the differential Q-values when CLK is low. Dividers based in this latch was used in papers III to V.

3.3.2 16 % and 33 % Duty cycle

In paper II, to suppress the down-conversion of noise and signals originating from the third harmonic of the LO frequency, a six phase LO scheme was used instead of the standard quadrature LO scheme. It was assumed that a single VCO, running at three times the LO frequency, was to be used and the divider then needs to provide a frequency division by three. The divider in

figure 28 therefore uses three dual-edge triggered latches based on CML logic to provide six 50 % duty cycle outputs. The dual edge triggered latch, figure 29, consists of two sub-latches; one is triggered with the positive and the other with the negative clock. A multiplexer is then used to select either latch for the corresponding clock (rising or falling edge).

Since the outputs from the six phase divider are 50 % duty cycle signals, figure 30(a), they can be combined into either 33 % or 16 % duty cycle signals. This is done using transmission gates to select the different inputs to an AND-function, figure 30(b). Since a 33 % duty cycle signal contains no third order harmonic, the rejection of this harmonic can be performed already in the down-

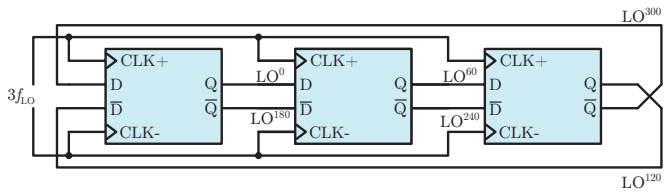


Figure 28: The divider used to generate six phases uses three dual-edge triggered latches.

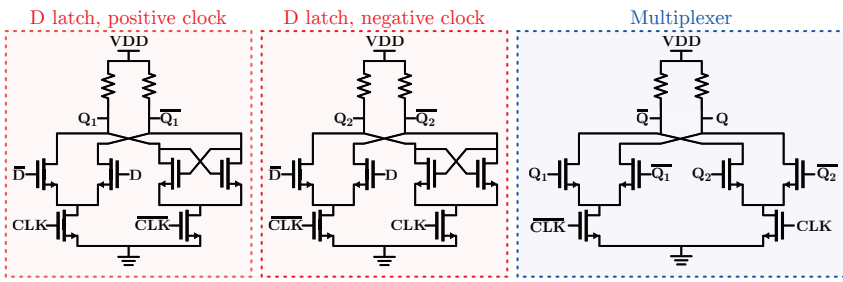


Figure 29: A dual-edge triggered CML latch consisting of two sub-latches and a multiplexer.

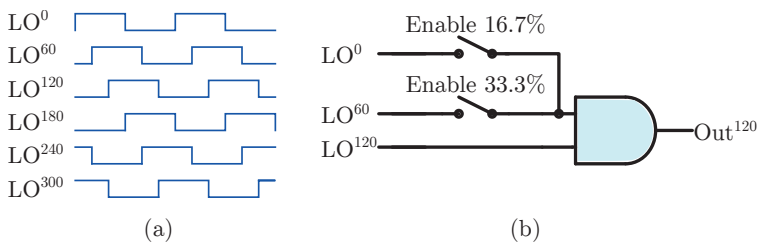


Figure 30: By using transmission gates to select between the LO signals either 33 % or 16 % duty cycle LO signals can be produced.

conversion stage which is beneficial, as explained in chapter 4. The 16 % on the other hand ensures non-overlapping signals and is used in the normal case, together with harmonic rejection in a second baseband stage.

3.4 OPAMP

The OPAMP[5] is the key building block in the baseband, and the same OPAMP structure has been used in papers II to IV. The OPAMP consists of two stages where a complementary input stage is used for reduced noise and increased gain due to the current reuse, and a complementary output stage is used to achieve a high voltage swing at the output, see figure 31. The OPAMP also uses a common-mode sense amplifier to control the common-mode output level of the OPAMP by adjusting the voltage V_{cmc}, ensuring the output voltage is at Vdd/2, i.e. 600 mV in all papers. In order to provide a high 3 dB bandwidth of the OPAMP, a phase-enhancement compensation technique [7, 67–69] is used, where two zeros are introduced by using *RC*-links from the output to the input. The system now has four dominating poles and two zeros. By optimizing the values, the two zeros can be placed at the same frequency as the second and third pole, respectively, and thus only two poles are left uncancelled. The first one of these poles is located at a higher frequency compared to the Miller-compensation case, thus increasing the bandwidth, and the fourth pole is located beyond the unity gain frequency of the OPAMP.

[5]The naming convention of OPAMP is chosen here as a general name for the building block. If the output is a current the block can instead be called an operational transconductance ampifier (OTA) whereas a true operational voltage amplifier should have a voltage buffer before the output.

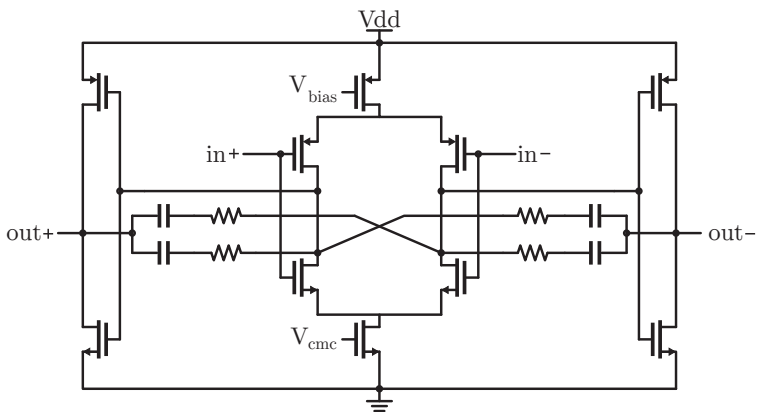


Figure 31: Complementary input and output OPAMP with phase-enhanced compensation.

Chapter 4

System Level Considerations

This chapter provides an introduction to and additional information about some of the system level considerations and techniques of the included papers. Harmonic rejection will be treated first, followed by global negative and positive feedback in receiver front-ends, and finally an introduction to the A/D-converting channel-select filter is provided.

4.1 Harmonic Down-Conversion

As described in chapter 2, one major problem with wideband receivers is down-conversion of noise and signals from harmonics of the LO frequency when using square wave LO signals in the mixer. There are different ways of mitigating this problem, and one is to use a harmonic rejection mixer (HRM). This technique was introduced in [70], and further analyzed in [71], where an 8-phase mixer was used in a wideband transmitter to suppress the up-converted modulated signal at $3f_{LO}$, which can together with the non-linearities of a wideband PA cause distortion close to the f_{LO} carrier. By approximating the wanted sinusoidal

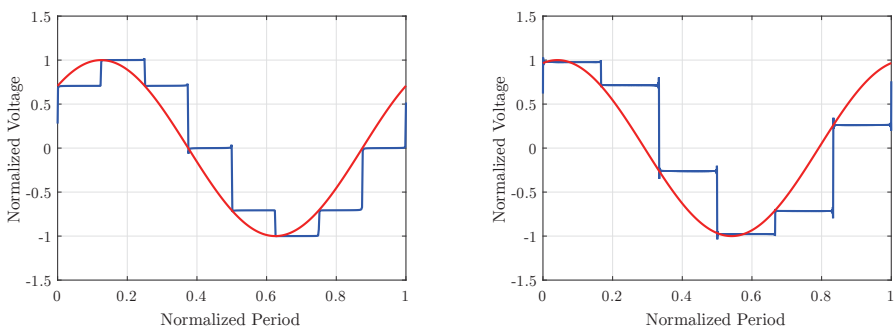


Figure 32: Approximation of sinusoidal signal with: (a) eight scaled 12.5 % duty cycle signals. (b) six scaled 16.7 % duty cycle signals.

wave of the LO using eight phases, see figure 32(a), compared to using only four phases, the oversampling can remove the 3rd and 5th LO harmonics from being up-converted. This technique was later introduced in receivers [61, 72–75]. A similar technique to reject the 3rd order harmonic is to use not balanced signals, but three-phase signals as in [76, 77]. The benefits of harmonic rejection are twofold: rejection of interfering signals and rejection of noise. For applications such as digital TV (DTV) both are important, as the receiver is operating in the VHF and UHF bands, i.e. from 48 to 860 MHz [74, 78]. There is thus a major problem when receiving a low frequency channel and simultaneously facing interference from other channels at higher frequencies.

4.1.1 8-Phase Harmonic Rejection Mixer

A circuit diagram of an 8-phase HRM is shown in figure 33. The passive mixer consists of four differential switch pairs that are driven by non-overlapping 12.5 % LO signals, and each switch pair is terminated by a transimpedance amplifier (TIA), enabling the mixer to operate in current-mode. Following the TIAs, a combination network (shown for one of the two output channels) is used where the signals from three of the TIAs are combined, according to (24), to reject

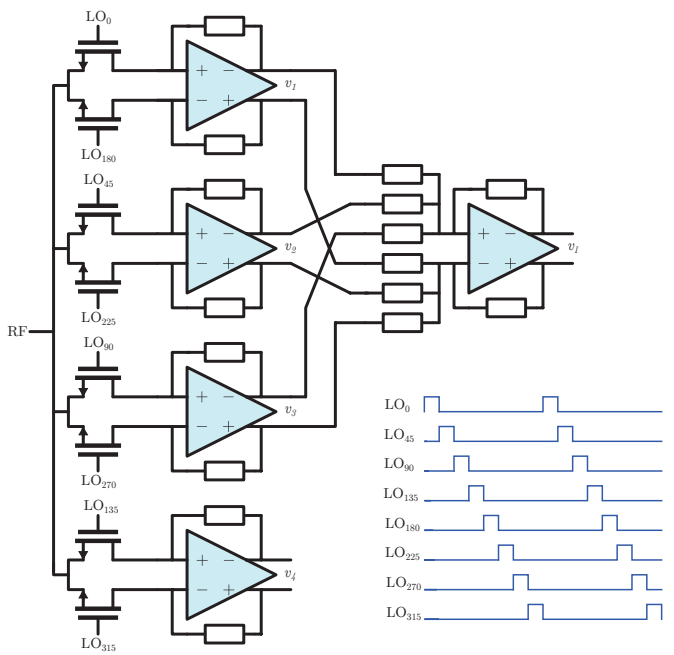


Figure 33: Implementation of an 8-phase HRM where a combination network scales the TIAs outputs to reject 3rd and 5th order harmonics.

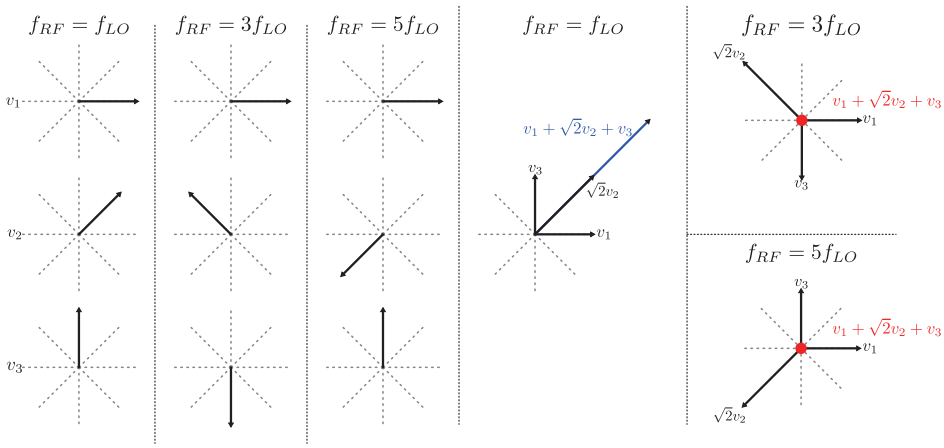


Figure 34: Phasors illustrating the rejection of harmonics when using eight unit length phasors.

the 3rd and 5th order harmonics.

$$v_I = v_1 + \sqrt{2}v_2 + v_3, \quad v_Q = v_3 + \sqrt{2}v_4 - v_1 \tag{24}$$

It is important to note that the down-converted signals from 3rd and 5th harmonics are attenuated first after the combination network, i.e. after the summation resistors at the input of the second stage, and that strong blockers can therefore still saturate the first stage [61, 79]. 2nd order harmonic content is rejected directly at the output of each of the switch pair due to the differential symmetry.

One way of visualizing the harmonic rejection mechanism is to view the signals at the TIA outputs, $v_1 ... v_3$ as phasors, depicted in figure 34. It is worthy to note that the output signal of each TIA is real valued, and is obtained by a projection of the phase to the real axis. However, using the two-dimensional phase representation in this case becomes more intuitive. When the LO frequency is the same as the RF, the RF is sampled at a constant phase in each branch, and since the LO phase is shifted by 45° between branches, the resulting phasor will rotate in steps of 45° between v_1, v_2 and v_3. When f_{RF} is instead three times f_{LO}, each phasor will rotate three times as fast, and the phase between v_1, v_3 and v_3 will then be 135°. Similarly, when f_{RF} is equal to five times as fast as f_{LO}, the phase difference will be 225°.

When combining the three signals according to (24) the fundamental signal will be one 45° phasor with the length of $2\sqrt{2}$, assuming v_1 is normalized to zero phase and unit length. For the 3rd order harmonic, v_1 and v_3 will create a 315° phasor with phase length $\sqrt{2}$, which is cancelled by the phasor $\sqrt{2}v_2$; similar happens for the 5th harmonic. An alternative way is to calculate the

Fourier series expansion of the effective LO signal in (25).

$$f(t+nT) = \begin{cases} 1, & 0 < t < \frac{T}{8} \\ \sqrt{2}, & \frac{T}{8} < t < \frac{T}{4} \\ 1, & \frac{T}{4} < t < \frac{3T}{8} \\ 0, & \frac{3T}{8} < t < \frac{T}{2} \\ -1, & \frac{T}{2} < t < \frac{5T}{8} \\ -\sqrt{2}, & \frac{5T}{8} < t < \frac{3T}{4} \\ -1, & \frac{3T}{4} < t < \frac{7T}{8} \\ 0, & \frac{7T}{8} < t < T \end{cases} \tag{25}$$

The Fourier coefficients are then provided by (26)

$$\begin{aligned} a_n = &\frac{1}{\pi n}\left((1-\sqrt{2})sin\left(\frac{\pi n}{2}\right) - sin\left(\frac{\pi n}{4}\right) + (\sqrt{2}-1)sin\left(\frac{3\pi n}{4}\right) + \right. \\ &\left. (\sqrt{2}-1)sin\left(\frac{3\pi n}{2}\right) + sin\left(\frac{5\pi n}{4}\right) + (1-\sqrt{2})sin\left(\frac{7\pi n}{4}\right)\right) \end{aligned} \tag{26}$$

$$\begin{aligned} b_n = &\frac{1}{\pi n}\left((\sqrt{2}-1)cos\left(\frac{\pi n}{2}\right) + cos\left(\frac{\pi n}{4}\right) + (1-\sqrt{2})cos\left(\frac{3\pi n}{4}\right) - cos\left(\pi n\right) + \right. \\ &\left. (1-\sqrt{2})cos\left(\frac{3\pi n}{2}\right) - cos\left(\frac{5\pi n}{4}\right) + (\sqrt{2}-1)cos\left(\frac{7\pi n}{8}\right) + 1\right) \end{aligned} \tag{27}$$

After calculating these coefficients, the transfer function magnitude of each harmonic can be calculated, and the result is presented in figure 35. As can be seen, the only LO harmonics below order 10 that are still present after the combination stage are the 7^{th} and 9^{th}, whereas the 3^{rd} and 5^{th} are cancelled.

It should be noted that the cancellation is only perfect when the phase shift between the LO signals is exactly 45°, and the ratio $1:\sqrt{2}:1$ can be exactly implemented. In real implementations, with analog imperfections both in the LO signal generation and in the irrational ratio baseband combination network, the amount of rejection of the 3^{rd} and 5^{th} harmonic is limited to about 40 dB. If a larger harmonic rejection is required, either tuning of the analog components as in [80] or post-processing in the digital domain by using more ADCs [81,82].

4.1.2 6-Phase Harmonic Rejection Mixer

For cellular systems like LTE, where the frequency range spans between 700–2800 MHz for most bands, it is mainly the 3^{rd} order harmonic that poses problems.

This can be seen in figure 36, where all LTE TDD and FDD bands in figure 4 are shown together with the 3^{rd} and 5^{th} order harmonic up to 4 GHz. The

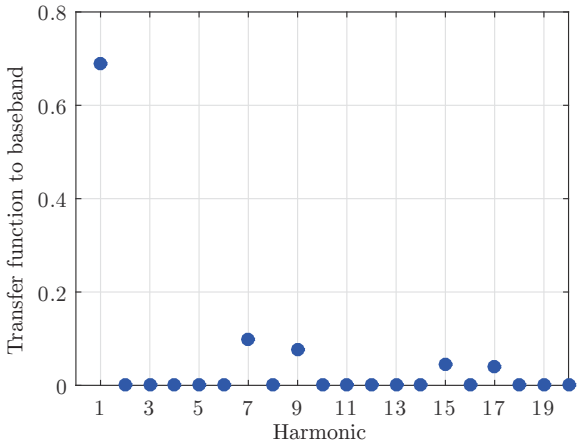


Figure 35: Gain from LO harmonics to baseband for an eight phase mixer.

3rd order harmonics for the low frequency bands are located around 2500 MHz whereas the 5th order harmonics are located around 3750 MHz. The rejection of the 3rd order harmonics is thus more important in LTE. Furthermore, the 3rd harmonic contributes more to the degradation of noise figure due to harmonic folding, and at the 5th order harmonic the LNA gain is usually already has reduced by limited bandwidth. This bandwidth reduction can also be accomplished by introducing explicit capacitance in the LNA.

To address this situation a HRM with six phases is proposed in paper II, which relaxes the requirements of the VCO and divider. Also, one less double or single-balanced mixer is used compared to the 8-phase technique, and the 6-phase HRM is a good trade-off between the quadrature (4-phase) and the 8-phase HRM.

For the 6-phase HRM only three differential mixers, implemented as single-balanced passive mixers in figure 37, are used together with 3 TIAs. The TIA outputs $v_1 ... v_3$ are combined in the second stage, shown for one output. Since six phases are used, the LO duty cycle is set to 16.7 % for non-overlapping signals, generated from a $3f_{LO}$ VCO and divided by 3 as described in chapter 3. At the baseband output signals, v_I and v_Q, all even harmonics and the 3rd harmonic are rejected. The problem of rejecting the 3rd order harmonic and generating the orthogonal baseband signals can be divided into two subproblems. In order to address the former problem the phasors in figure 38(a) can be used. In this figure, similar to the case of an 8-phase system, the 3rd harmonic phasor will rotate three times as fast as the fundamental phasor. Now a new set of phasors are introduced, $v'_1 ... v'_3$, calculated according to (28), where the properties of the first corresponding phasor is depicted in figure 38(b).

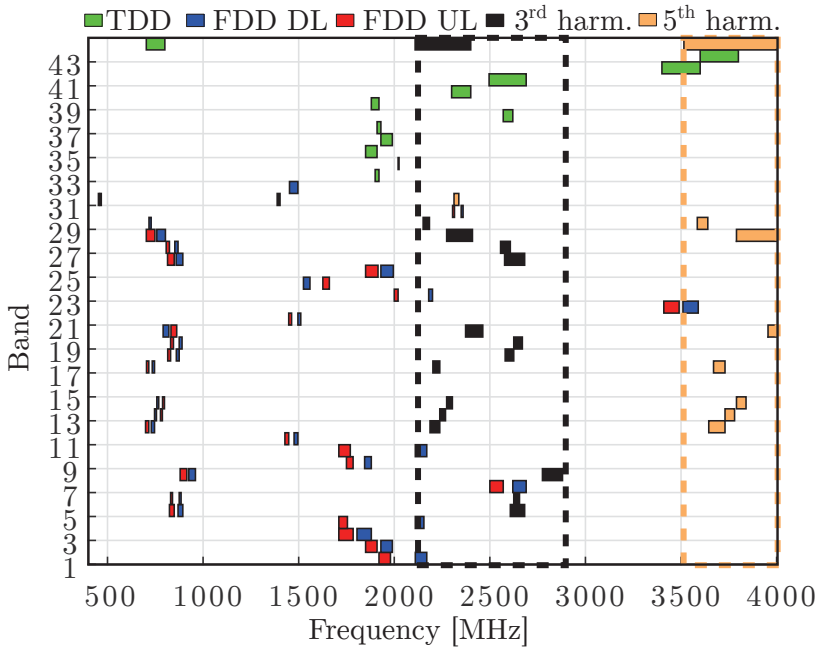


Figure 36: Frequency bands for LTE including 3rd and 5th order harmonics.

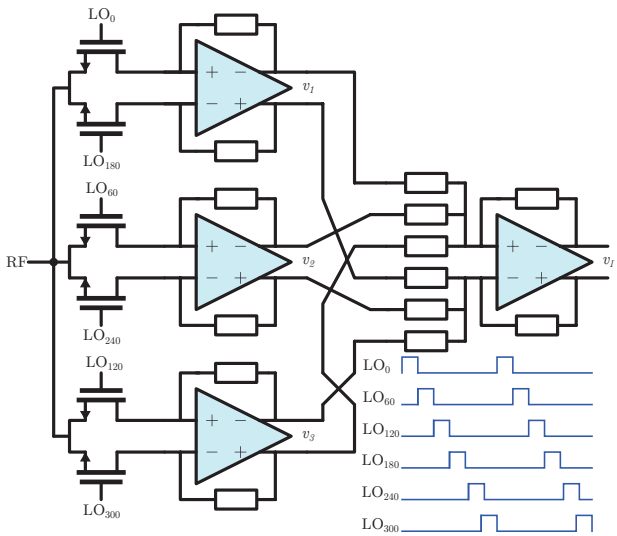


Figure 37: Implementation of a 6-phase HRM where a combination network scales the TIAs outputs to reject 3rd order harmonic.

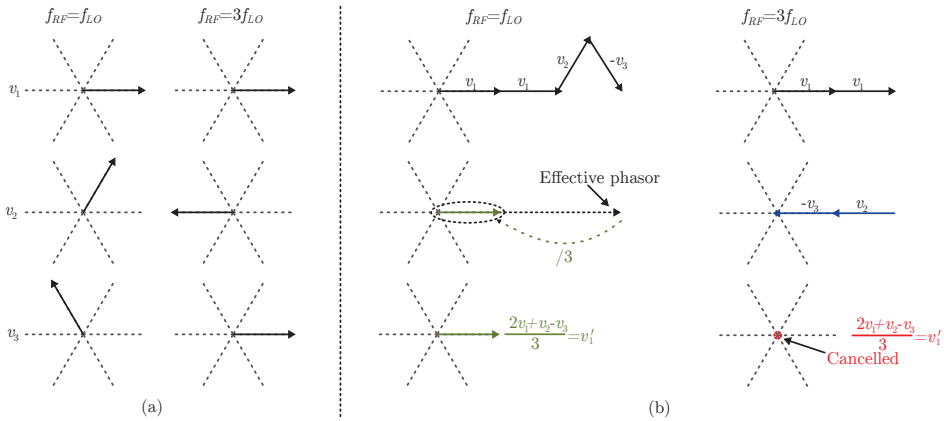


Figure 38: (a) Phasors for the fundamental and 3rd order harmonic. (b) by introducing a new set of phasors the 3rd order harmonic can be rejected.

$$\begin{aligned} v_1' &= (2v_1 + v_2 - v_3)/3 \\ v_2' &= (2v_2 + v_1 + v_3)/3 \\ v_3' &= (2v_3 - v_1 + v_2)/3 \end{aligned} \tag{28}$$

It is clear that the properties of the fundamental signal has not changed, i.e. $v_1 = v_1'$, but the 3rd order harmonic is rejected in v_1'.

The second sub-problem addresses generation of the v_I and v_Q signals. The fundamental property of these vectors is orthogonality, and since three vectors with 60° phase difference are used to create the 90° signals, combining the three signals in a symmetrical way there will be $-15°$ between v_I and v_1' and 15° between v_Q and v_3', see figure 39. One possible set of equations to generate

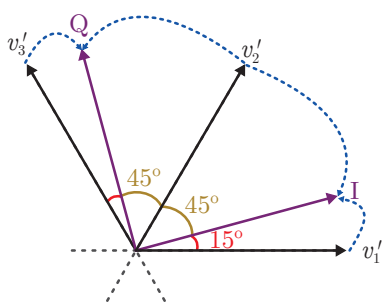


Figure 39: Illustration of how in-phase (I) and quadrature-phase (Q) signals can be generated from the three vectors with 60° phase difference.

the I and Q vectors is given by (29).

$$\begin{aligned} v_i &= (1+\sqrt{3})v_1' + v_2' \\ v_q &= (1+\sqrt{3})v_3' + v_2' \end{aligned} \tag{29}$$

By combining (28) and (29), equations (30) and (31) can be calculated. Both 3rd harmonic rejection and symmetrical I and Q generation is then achieved in one stage.

$$v_i = 1/\sqrt{3}((\sqrt{3}+2)v_1 + (\sqrt{3}+1)v_2 - v_3) \tag{30}$$

$$v_q = 1/\sqrt{3}(-v_1 + (\sqrt{3}+1)v_2 + (\sqrt{3}+2)v_3) \tag{31}$$

The Fourier series coefficients of the effective LO wave of (30) can be calculated as (32) and (33).

$$\begin{aligned} a_n = &\frac{1}{\pi n\sqrt{3}}\left(sin\left(\frac{\pi n}{3}\right) + (2+\sqrt{3})sin\left(\frac{2\pi n}{3}\right) - sin\left(\frac{4\pi n}{3}\right) + \right. \\ &\left. (-2-\sqrt{3})sin\left(\frac{5\pi n}{3}\right)\right) \end{aligned} \tag{32}$$

$$\begin{aligned} b_n = &\frac{1}{\pi n\sqrt{3}}\left(-cos\left(\frac{\pi n}{3}\right) + (-2-\sqrt{3})cos\left(\frac{2\pi n}{3}\right) + (-1)^n(-1-\sqrt{3}) + \right. \\ &\left. cos\left(\frac{5\pi n}{3}\right) + (2+\sqrt{3})cos\left(\frac{4\pi n}{3}\right) + 1 + \sqrt{3}\right) \end{aligned} \tag{33}$$

Based on the Fourier coefficients, the magnitude of the transfer function for the first 20 LO harmonics to baseband is presented in figure 40, and as expected the 3rd harmonic is rejected.

Another property of the 6-phase system is the integer ratio needed to reject the third harmonic in (28), compared to the irrational $\sqrt{2}$ ratio needed in the 8-phase system (24). This can be exploited in a receiver where strong blockers, present at harmonics, should be rejected already before the first voltage amplification. This idea of rejecting the harmonic already before the first TIA output was presented in [79] for an 8-phase system, based on the idea in [61] where the irrational ratio is partly implemented at the RF side instead of in the baseband. Matching is, however, hard to accomplish at RF. By using the 6-phase system, three LNTAs with a ratio of 1:2:1 can instead be used; this ratio is easier to implement and simplifies matching. Another advantage of the 6-phase system is that the LO generation can easily be re-configured to provide 33 % duty cycle signals, which will also reject harmonic down-conversion of the third harmonic, already in the mixer, at the expense of increased noise figure due to cross-talk between the mixers due to overlapping LO signals.

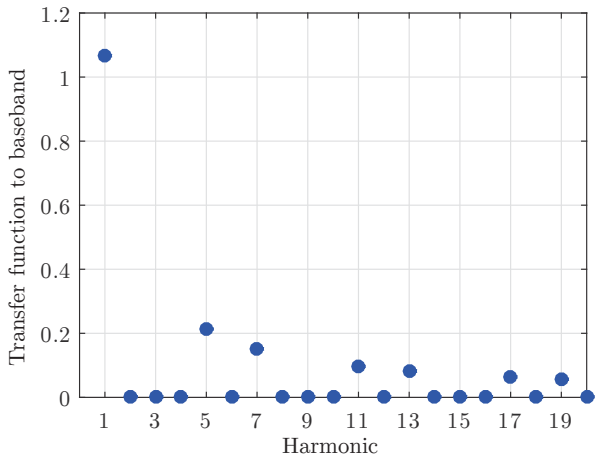


Figure 40: Gain from LO harmonics to baseband for a 6-phase HRM.

4.2 Global Negative Feedback

The FB-LNA, described in chapter 3, uses shunt-shunt negative feedback with a loop gain close to unity to match the input impedance to the off-chip interface. This shunt-shunt feedback technique can also be used in a receiver front-end, with a frequency translational feedback path [83–85]. The baseband voltage signal, after the TIA, is converted into a current, frequency up-converted by a feedback mixer, and fed back to the input of the LNA, see figure 41. The feedback resistors, R_f, can be placed at the RF side of the feedback mixer to decrease LO leakage by the resistive voltage division, or at the low frequency side of the mixer to decrease the associated parasitic capacitance of digital tuning and decrease the signal voltage level in the mixer. Paper III is based on this technique, using the basic block level schematic shown in figure 41.

The stability of the system is ensured by two things: the low loop gain and the dominant pole in the baseband. This is in contrast to most traditional feedback systems, where the loop gain is often very high in-band, and ensuring stability then becomes more of a challange. As mentioned previously, the in-band loop gain of this system is close to unity, and decreases to less than unity out-of-band. The stability of the receiver with respect to source impedance is simulated in figure 42, where 15 different source impedances are selected in all quadrants. According to the simulations, the real part of the input impedance, presented in figure 42(b), is always positive, which indicates unconditional stability with respect to source impedance.

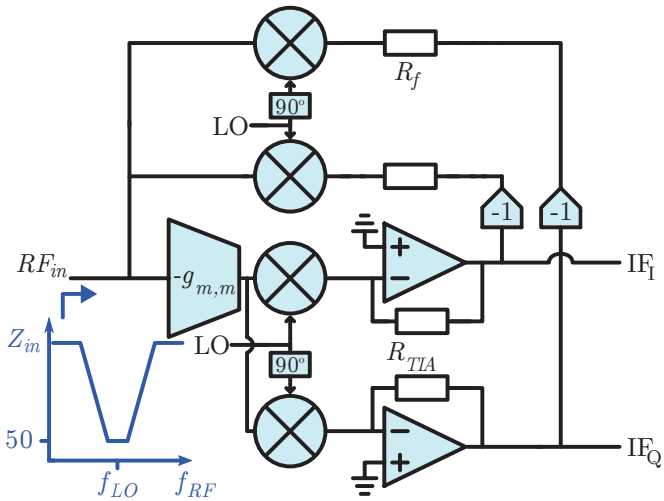


Figure 41: Shunt-shunt resistive feedback from baseband can be used to match the receiver front-end.

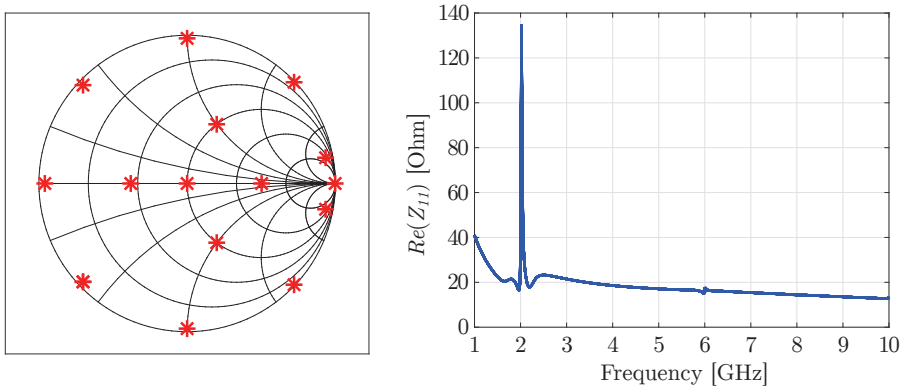


Figure 42: (a) 15 different source impedances were chosen to (b) Simulated real part of the input impedance for all Z_s to investigate stability.

4.2.1 Noise-Cancelling Receiver Front-End

Similar to the idea of introducing an auxiliary path for the FB LNA to cancel the noise of the main path, an auxiliary receiver front-end can be introduced in parallel with the FB receiver front-end, see figure 43. This was exploited in paper III, where the auxiliary path can cancel some noise from the main path. Even though, in paper III, the gain of the auxiliary path was selected to be lower than that of the main path some noise and non-linearity is still

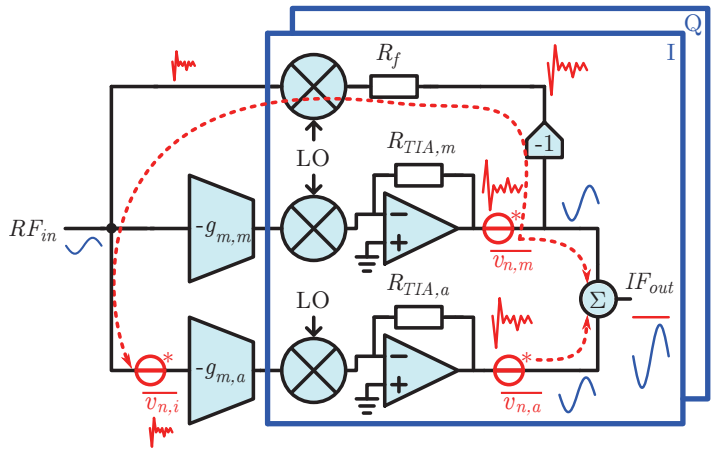


Figure 43: Conceptual schematic of noise cancellation for a shunt-shunt feedback receiver front-end.

cancelled. As mentioned in the paper, but not implemented in the measured chip, an additional feature of the FB receiver front-end is that in the presence of a source reactance, such as parasitic inductance from a bondwire, a phase shift between the two paths can be introduced to further optimize the noise figure. Since all processing can be performed at baseband, compared to using tuning at RF, parasitic capacitance is less of an issue and finer tuning steps can then be implemented in combination with digital tuning. Another advantage by introducing the auxiliary path is that when a large blocker is present the gain of the main path can be decreased while the gain of the auxiliary path is increased, as described in [23] for an LNTA, to provide a low noise figure in the presence of the blocker.

4.3 Global Positive feedback

The passive mixer-first receiver front-end [86–88] has excellent linearity and is a good candidate for a wideband reconfigurable and flexible receiver. The main drawback is the noise figure, equal to (34) for a 4-phase LO scheme. Assuming that the noise and input impedance of the baseband TIA is low the minimum noise figure is about 4 dB, if the mixer should providing matching to the source resistance (35) [88].

$$F = \left(1 + \frac{\overline{v_{R_{SW}}^2}}{\overline{v_{R_s}^2}} + \frac{\overline{v_{BB}^2}}{4\overline{v_{R_s}^2}}\right)\gamma, \quad \gamma = \frac{\pi^2}{8} \tag{34}$$

$$Z_{in} \approx R_{SW} + \alpha Z_{BB}(\Delta\omega), \quad \alpha = \frac{4}{\pi^2} \tag{35}$$

A possible way to reduce the noise figure was introduced in [88] where the idea of noise-cancellation of the CG LNA is used, and the passive mixer is replacing the CG stage. In parallel with the passive mixer-first main path, an auxiliary path is then introduced, consisting of a g_m stage, down-conversion mixers and baseband TIAs. Now, if the gain of the auxiliary path is set close to that of the main path, the noise of the main path is cancelled. The advantage is here that the added auxiliary path can have high g_m, independent of input match, and thus low noise figure.

Another way of decreasing the noise figure, proposed in paper IV, is to use large input devices with an on-resistance far less than 50 Ω. This will, however, decrease the input impedance of the circuit, see figure 44(a). A possible way of increasing the input resistance is to use positive feedback [89, 90]; just as negative shunt feedback decreases the input impedance, positive shunt feedback increases it. The feedback technique is similar to the negative feedback receiver front-end, where the baseband voltage signal is converted into a current and then fed back through up-conversion mixers and connected to the input, but with positive feedback. The feedback loop has most gain (but always less than

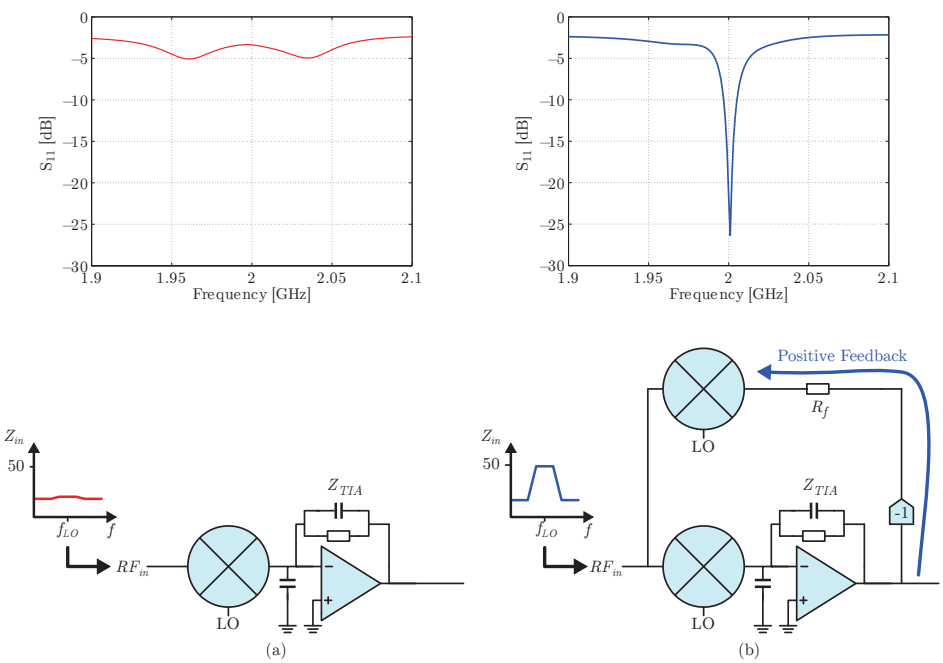


Figure 44: (a) Passive mixer-first receiver front-end with low input impedance and corresponding input reflection. (b) By introducing poisitive feedback the input impedance can be increased.

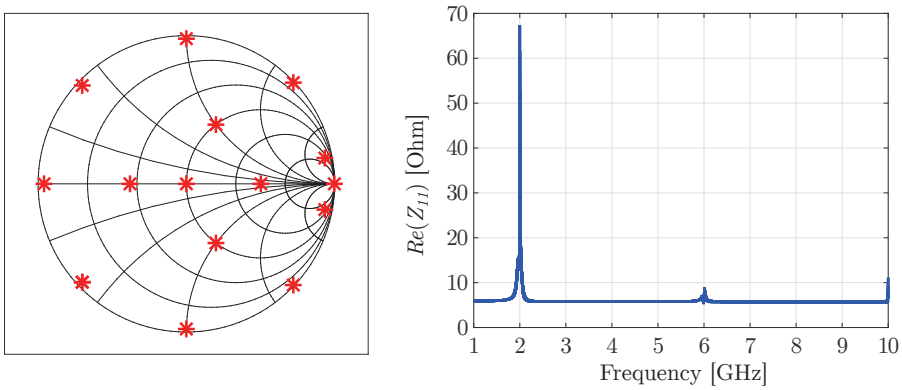


Figure 45: (a) 15 different source impedances were chosen to (b) simulate the real part of the input impedance, to investigate stability of the positive feedback receiver front-end.

unity) around the LO frequency, determined by the bandwidth of the baseband circuitry, and it then decreases out-of-band. Similar to the negative feedback receiver front-end, this enables a narrowband input match which is tunable with the LO frequency, see figure 44(b). A main difference is that the far out-of-band impedance of the positive feedback system will be small whereas the impedance is high for the negative feedback system.

With positive feedback, the loop-gain must always be less than unity to ensure stability of the system. The stability of the positive feedback passive mixer-first receiver, with respect to source impedance, is therefore analyzed by simulating the input impedance for 15 different source impedances. The points for these source impedances are depicted in the Smith chart in figure 45(a). The real part of the input impedance was then extracted for all points and presented for all the different cases, figure 45(b), and it is always positive indicating stability. In paper IV, the implemented main mixer has an on-resistance of about 8 Ω, which would lead to a minimum noise figure of $10log_{10}(1+8/50)+0.9 = 1.55$ dB if the baseband was noiseless and the feedback resistor much larger than Z_s. This equation also assumed 25 % duty-cycle non-overlapping LO phases, which results an harmonic down-conversion which adds the 0.9 dB.

4.4 Analog-to-Digital Converting Channel-Select Filter

This section introduces the oversampled ADC based on the continuous-time Delta Sigma Modulator (ΔΣM). It then also explains the re-arrangement of the loop filter poles to synthesize a CSF with embedded ADC functionality.

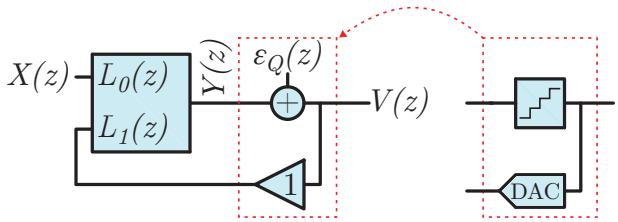


Figure 46: Simplified linear model of a ΔΣM.

4.4.1 Continuous Time ΔΣM

The basic structure of a ΔΣM can be modeled as a linear discrete time system as portrayed in figure 46. It consists of an input, $X(z)$, that is fed to a loop filter, L, with two transfer functions: $L_0(z)$ and $L_1(z)$. The output of the filter, $Y(z)$, is then fed to an n-bit ADC, usually a low resolution flash ADC. The sampled output, $V(z)$, is then converted back into an analog signal and fed back to the loop filter. A quantization error, $\varepsilon_Q(z)$, is introduced by the ADC, and it can be modeled as additive white noise at the input of the ADC. Furthermore, it is assumed that the gain of the quantizer and DAC is equal to unity. The output of the system is described by (36), where $NTF(z)$ denotes the noise transfer function of $\varepsilon_Q(z)$ and $STF(z)$ is the signal transfer function of $X(z)$ to $V(z)$.

$$\begin{aligned} V(z) &= STF(z)X(z) + NTF(z)\varepsilon_Q(z) \\ NTF(z) &= \frac{V(z)}{\varepsilon_Q(z)} = \frac{1}{1+L_1(z)} \\ STF(z) &= \frac{V(z)}{X(z)} = \frac{L_0(z)}{1+L_1(z)} \end{aligned} \tag{36}$$

As can be seen from (36), there is a strong connection between NTF and STF since $STF(z) = L_0(z)NTF(z)$. The selection of NTF thus affects STF. If $NTF(z)$ can be chosen to have a high pass characteristic, the in-band quantization error is suppressed. The analysis of the discrete time system can also be translated into a continuous time system, which is a mixture of the continuous time loop filter and the sampled digital output signal. Today's cellular receivers with ΔΣM-based ADCs typically use low oversampling, in combination with multibit flash ADCs and a high order loop filter, to achieve a reasonable clock frequency for the ADC.

4.4.2 Co-Design with Channel Select Filter

Traditionally, the design of the loop filter of the ΔΣM is optimized for NTF, and the STF can even be peaking out-of-band [91]. At the same time, a lot of effort is spent on designing a CSF that attenuates out-of-band interferers. This traditional approach where the two blocks are cascaded is shown in figure 47(a). Assuming $STF_{\Delta\Sigma M} = 1$, the modulator can instead be placed inside the filter loop as depicted in figure 47(b). The filter now consists of two parts: the CSF and the ΔΣM loop filter, with a feedback loop from the digital output to the CSF input. Similar to the analysis in figure 46 the noise from the ΔΣM can be modeled as a noise source $\varepsilon_{\Delta\Sigma M}$, which will be suppressed by the CSF [92–95] thanks to the global feedback. This additional suppression can be used to provide either an increased SNR performance, or a reduction in power dissipation for the same SNR.

Another way of viewing the integration of the two blocks is to consider a single N^{th}-order ΔΣM, with N integrators, where P integrators are optimized for STF and $O = N - P$ integrators are optimized for NTF. The system can then be noted as a P+O system, where P is the order of the filter and O is order of the ΔΣM. This is exemplified by a 2+2 system in [92], a 2+3 system in [93], a 3 + 2 system in [94], and a 4 + 1 system is presented in paper V. When the majority of the integrators are optimized for STF, the ΔΣM can instead be called an Analog-to-Digital converting Channel-Select Filter (ADCSF). One additional block to incorporate into this ADCSF is the TIA, and a receiver based on this structure, together with RF circuitry, is presented in paper V.

The selection of a 4 + 1 system was based on a number of considerations. The first one was the required SNDR of the system. Assuming a voltage gain of about 280 (49 dB), the thermal noise at the receiver output for a 18.5 MHz wide baseband signal (2xLTE20 channels or 37 MHz RF bandwidth) from a 50 Ω source at the input will be $\overline{v_o^2} = 4kTRB \cdot (1/2)^2 \cdot 282^2 = 6.1272 \cdot 10^{-7}$ V^2. At the same time, if the system should be able to handle a signal of 0.5 V$_p$ (0.125 V^2) at the output, the SNR requirement becomes about 56 dB. Given that the RF circuity, in particular the LNTA, should dominate the noise floor,

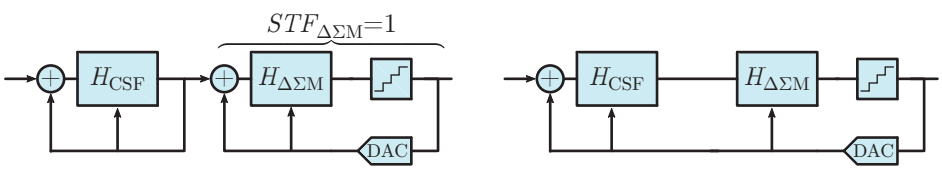


Figure 47: When co-designing the CSF and ΔΣM, the CSF becomes an additional loop filter that can further suppress the noise of the ADC. (a) Cascade of CSF and ADC. (b) ADCSF.

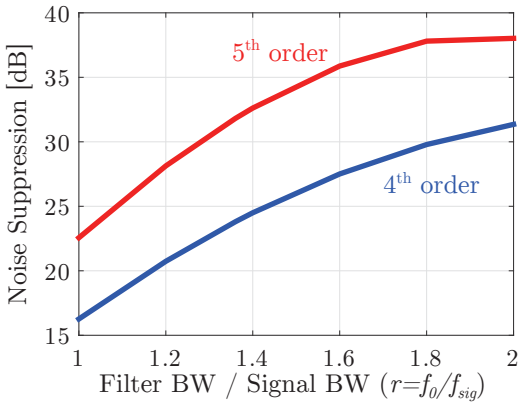


Figure 48: The noise suppression by the CSF part of the ADCSF depends both on the order, but also of the ratio between f_0 and f_s.

the noise of the baseband should be about 9 dB lower, also assuming a 2 dB noise figure of the RF part, to limit the noise figure increment due to the baseband contribution to about 0.5 dB, yielding an SNR requirement of 63 dB. Furthermore, in a power-efficient ADC design the quantization noise is about 10 dB lower than the thermal noise [96, 97], leading to a SQNR requirement of 73 dB for the ADC. With this SQNR requirements, further choices in the design were to use a 3-bit flash ADC, 5 integrators in total for each channel, and an oversampling ratio (OSR) of 16. The oversampled 3-bit flash ADC has an equivalent number of bits of $ENOB = n + 0.5log_2(OSR) = 5$, resulting in an SQNR of ≈ 32 dB.

The next selection was on the type of filter signal transfer function characteristic where the Butterworth filter was chosen. The reason for this choice is the lower Q-value of the filter poles, which reduces the noise peaking close to the the filter passband edge, compared to a Chebyshev filter.

Next, the ratio between the filter bandwidth f_0 and the signal bandwidth f_{sig} was decided. The smaller this ratio the higher selectivity but also reduced noise suppression [98, 99]. Figure 48 illustrates the trade-off for a fourth order system, taking the considerations of the loop delay into account as described in [94]. In order to have a good trade-off between selectivity and noise suppression the ratio was chosen to 1.36. This also limits the in-band droop to about 0.2 dB. For a 5^{th} order Butterworth this ratio would lead to a noise suppression of about 32 dB, figure 48, yielding a total SQNR of 64 dB which is about 10 dB too low from the specification of 73 dB. Instead a 4+1 system was analyzed and according to [96] the SQNR of a first order modulator is 50 dB. The 4th order Butterworth filter will then provide an additional noise suppression of 23 dB which leads to a total SQNR of 73 dB, matching the specifications of SQNR.

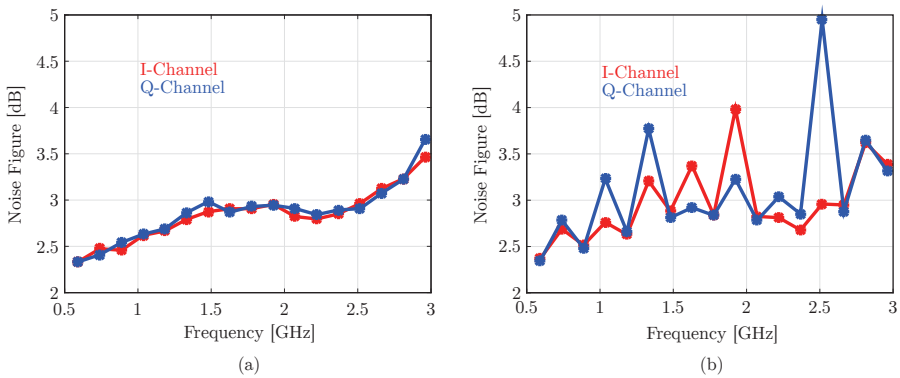


Figure 49: (a) Noise figure versus RF for the ADCSF based receiver when programmed to receive an LTE10 channel (b) Noise figure when programmed to receive an LTE20 channel with the same step size in RF.

One problem that was encountered in the measurements was a strong noise figure dependence on the ratio between the sampling frequency, f_s, and the LO frequency, f_{LO}. To exemplify this, the noise figure for the two output channels with the receiver programmed in LTE10 mode is presented in figure 49(a). At this setting, the sampling frequency f_s is equal to 148 MHz and f_{LO} is increased in steps of 148 MHz. Thus the ratio f_{LO}/f_s is always an integer. In figure 49(b) the noise figure was measured when the receiver was instead programmed to receive an LTE20 channel. As can be seen, for some values of f_{LO} the noise figure is about 1-2dB higher. The reason for this can be explained by investigating the ratio f_{LO}/f_s. When increasing the bandwith from LTE10 to LTE20, the sampling frequency of the ADCSF was doubled (296 MHz) to maintain the same OSR (selected to 16). However, f_{LO} was still increased in steps of 148 MHz. The high noise figure occurs at points where the ratio is $f_{LO} = Mf_s + 0.5f_s$, i.e. a non-integer number.

A possible explanation for this problem can be found by analyzing the frequency content of the ADCSF output. Due to the noise shaping by the loop filter, the noise density reaches a maximum value at $0.5f_s$. After this frequency, the noise decreases again and has a minimum at f_s, see figure 50(a). Assume that there is a coupling of this noise to the input of the mixer[6], as depicted in figure 50(b). If the ratio $f_{LO}/f_s = M$, the low-power noise is down-converted which will not significantly affect the total noise floor. But if the ratio is a non-integer number, e.g. $f_{LO}/f_s = M + 0.5f_s$, as depicted in figure 50(c), the high-power noise is instead down-converted, which will increase the noise figure.

[6]Coupling can either be on-chip or off-chip from the high frequency ADC outputs.

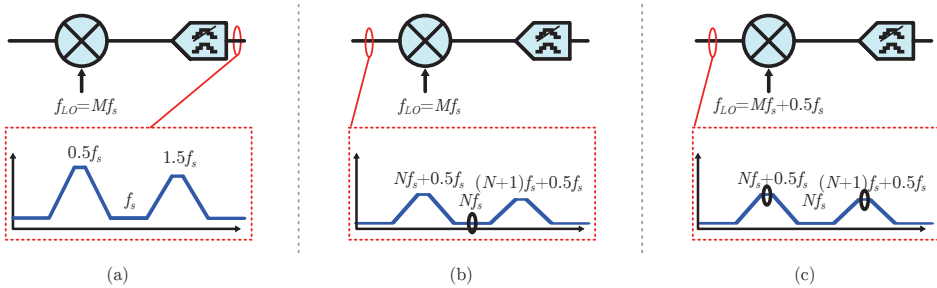


Figure 50: (a) The output of the $\Delta\Sigma$M has a high power content at $0.5f_s$. (b) Noise from the output couples to the input and is down converted. (c) If $f_{LO} = Mf_s + 0.5f_s$ the high power noise is down-converted, increasing the noise figure.

This problem could not be observed in simulations with the same settings as measurements. Non-idealities such as mismatch of mixer devices and feedback DACs were simulated but showed no increase of the noise figure. However, since the difference is significant between the I-channel and the Q-channel on several samples the problem is most likely not a first order effect. To further address the question of the increased noise figure at certain ratios of f_{LO}/f_s, a second design of the receiver has been designed and fabricated.

Chapter 5

Paper Summary and Conclusions

This chapter presents a summary and conclusion of the results obtained in the included papers. The author's contributions to each paper are also stated.

Paper I presents a receiver front-end based on an CCC CG amplifier. In order to increase the linearity of the amplifier, positive feedback transistors biased in sub-threshold are used. By operating the LNA in voltage-mode with a passive mixer, a low frequency single baseband pole becomes a bandpass-shaped high-Q filter at the LNA output, which increases the out-of-band IIP3 and selectivity. In order to reduce the noise figure, capacitive cross coupling is used in the LNA to boost the transconductance. A complementary current re-use structure is also used. Custom-made on-chip inductors are used, both at the NMOS and PMOS input devices as bias sources.

Furthermore, bootstrapped passive mixers were exploited to increase the linearity of the frequency down-conversion stage. By feeding back signal from the output to the gate node of the mixer devices, the voltage swing between gate and channel is reduced, thus improving linearity.

The design was implemented in 65 nm CMOS, taped-out in October 2011, and successfully measured. By using the positive feedback devices, the linearity can be improved without significantly increasing the power consumption. The bias voltage achieving maximum linearity was close to identical for the three samples measured, yielding an IIP3 improvement of approximately 3 dB both in and out-of-band. If linearity is of less concern, in situations with less interference, the bias current of the feedback transistors can be increased, resulting in increased gain and improved noise performance. The amount of feedback is, however, limited by the level where the input impedance and stability will be degraded. The front-end can operate from 700 MHz to 3 GHz, and thereby covers most important cellular bands.

Contribution: I did the simulations, implementation, layout, measurements and wrote the manuscript under supervision of the second and third authors.

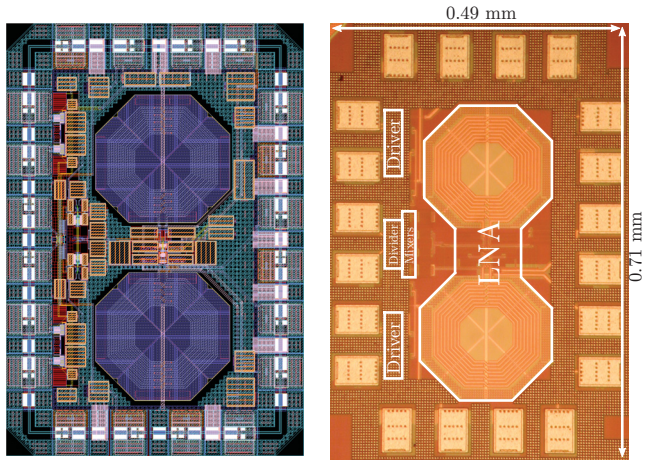


Figure 51: Layout and chip micrograph of the circuit in paper I.

Paper II presents a receiver front-end with a mixer arrangement that can suppress down-conversion from the third harmonic of f_{LO}. The input device is an area-compact complementary CCC-CG LNTA obtaining a high linearity and low noise figure without using inductors. The architecture uses an LNTA instead of an LNA, like in paper I, to reduce the RF voltage swing. This is achieved by operating in current-mode. Three differential mixers are used, and their outputs are combined in a combination stage, where the third order harmonic is cancelled. An on-chip solution to create the two quadrature phase signals was implemented, and harmonic rejection was measured by using an off-chip combiner for the I and Q signals. In order to compare the technique of using six phases with 16 % duty cycle to using 33 % duty cycle LO phases, that will reject the third order harmonic already in the down-conversion stage, the LO divider can be programmed to support both cases. Gain tuning was also implemented in the baseband by programming the feedback resistors of the TIAs.

The receiver front-end covers the LTE bands from 700MHz to 3700 MHz with a third order harmonic rejection of about 40 dB. By using six phases the complexity is reduced, compared to the more traditional approach of using eight phases. The circuit was taped out in 65 nm CMOS in June 2012, dissipated 18.2 to 37.5 mW in measurements, and provided a maximum gain of 52 dB with a noise figure of $3-4.5$ dB. The IIP3 is above +5 dBm and IIP2 exceeds +55 dBm. Additionally, analysis of the six phase harmonic rejection system is presented.

Contribution: I did the simulations, implementation, layout, measurements and wrote the manuscript under the supervision of the second and third authors.

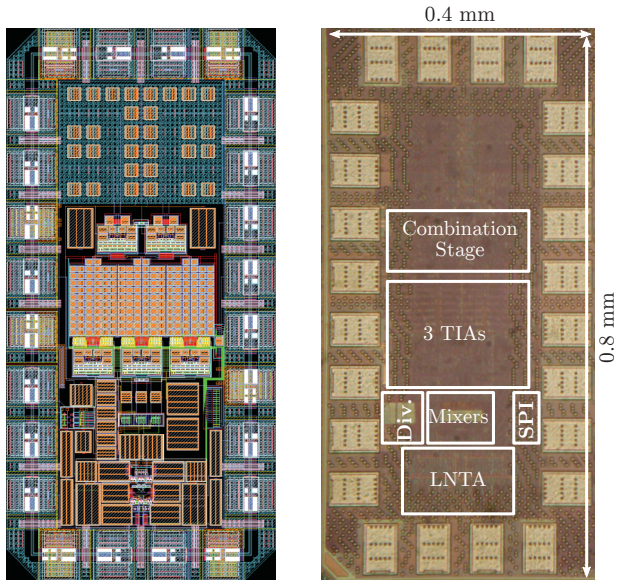


Figure 52: Layout and chip micrograph of the circuit in paper II.

Paper III describes a flexible receiver front-end based on shunt-shunt global feedback. The LNTA is simplified to an inverted-based stage with no local feedback except a large resistor for self-biasing. By using the down-converted baseband voltage and feeding this signal, converted into a current, back to the input via an up-converting mixer, the input can be matched. In parallel to this impedance matching path, a second path is introduced that can partially cancel the noise from the input stage. By using the auxiliary path, the transconductance of the main path can be reduced and the total linearity can be increased.

The receiver front-end was designed and taped-out in a 65 nm CMOS process in April 2013. By using complex feedback, mentioned in the manuscript but not implemented in the presented circuit, the feedback can also be used to counter reactive components at the input. The measured circuit has a frequency range of 700-3800 MHz, while maintaining a noise figure of 1.6 dB to 3.2 dB in the standard mode of operation with an IIP3 of 0 dBm. By reprogramming the circuit into a low noise mode, the noise figure decreases to a minimum of 1.2 dB. The receiver front-end consumes 23-35 mW from a 1.2 V and the IIP2 exceeds +80 dBm for almost all settings.
Contribution: I did the simulations, implementation, layout, measurements and wrote the manuscript under the supervision of the second and third authors.

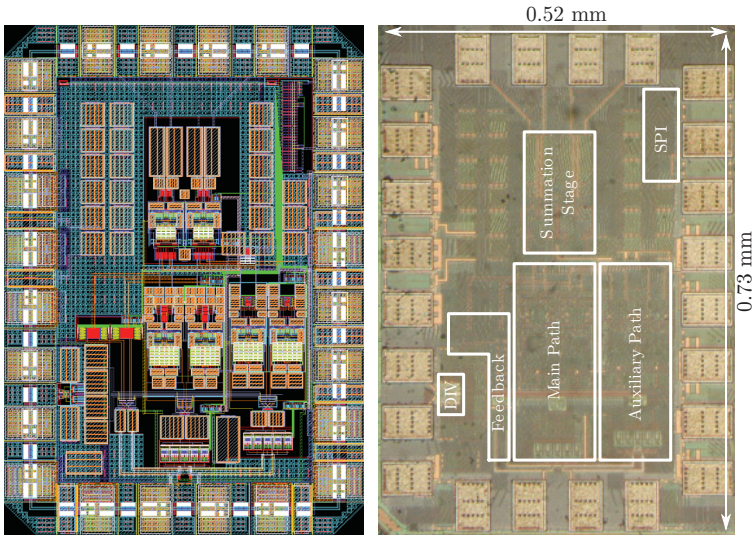


Figure 53: Layout and chip micrograph of the circuit in paper III.

Paper IV presents a passive mixer-first receiver front end. It is well known that the passive mixer-first receiver provides excellent linearity but is limited by the noise figure. Assuming a standard four phase down-conversion, the noise figure is limited to about 4 dB for a perfect input match. Even if more phases are introduced for harmonic rejection, which will reduce the down-converted noise from LO harmonics, the noise figure is limited to about 3 dB. One way to reduce the noise is to decrease the on-reistance of the mixer, but this will also change the input impedance of the receiver. To re-obtain correct input match a positive feedback was therefore introduced from the baseband output, up-converting the baseband signal to RF and feeding it to the mixer input. By tuning the loop gain of this feedback, the input can be matched to 50 Ω.

The circuit was taped-out in 65 nm CMOS technology in October 2013 and it can operate from 700 MHz to 3.8 GHz. The noise figure is less than 4 dB over the entire frequency range, with a minimum value figure of 2.5 dB. Out-of-band linearity is excellent due to the passive mixer-first architecture. The 1 dB cross-compression point, with an OOB blocker at 100 MHz offset, is +3 dBm. The power consumption is 27.4–75.4 mW and the circuit was supplied by 1.2 V.

Contribution: I did the simulations, implementation, layout and wrote the paper under the supervision of the third and fourth authors. Some measurements were performed in cooperation with the second author.

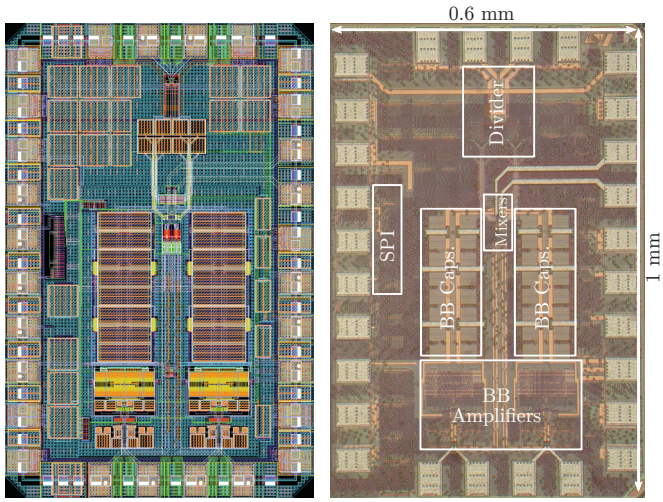


Figure 54: Layout and chip micrograph of the circuit in paper IV.

Paper V presents a full receiver chain from RF input to digital output (to be fed to a decimator). The LNTA performs single-ended to differential signal conversion to reduce the complexity of the PCB routing and minimize the number of required pads. This is crucial when more frequency bands are introduced. In order boost the performance of the inductorless LNTA, noise-cancelling performed by exploiting the properties of the differential output. The output current of the LNTA is fed to quadrature passive mixers, and the down-converted output is directly fed to a baseband ADCSF. This single component replaces the TIA, CSF and ADC, combining their functionalities into one power-efficient block.

The receiver was implemented in a 65 nm process and taped-out in March 2014. Configurable to receive either a single LTE10, an LTE20 channel, or two contiguously aggregated LTE20 channels, the receiver consumes between 35.5 to 53 mW and can operate between 600 MHz and 3 GHz at a noise figure of 2.5 to 3.5 dB.

Contribution: I was responsible for the RF part where I did the simulations, implementation, and layout. The second author was responsible for the baseband section. I also contributed to defining the system and baseband requirements and simulating the full system. I did most of the top level layout, including some part of the baseband section and the output drivers. Several baseband blocks provided by the third author was used. I performed all measurements in cooperation with the second author, and the project was supervised by the fourth to seventh authors.

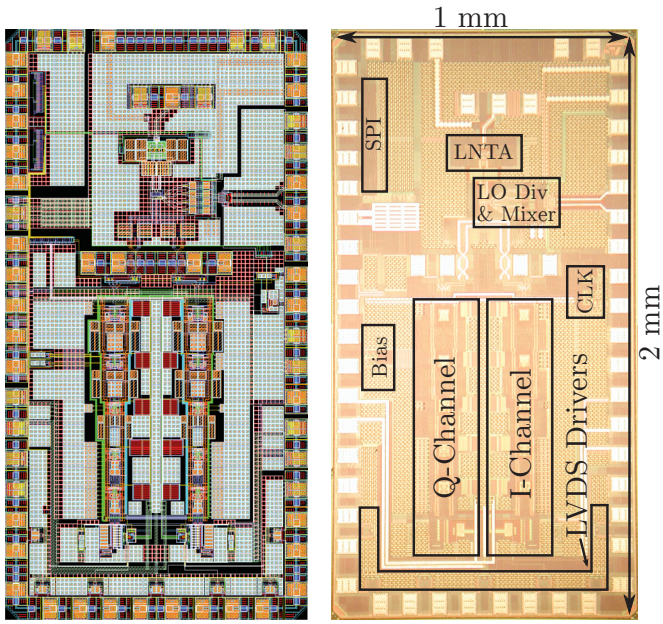


Figure 55: Layout and chip micrograph of the circuit in paper V.

Chapter 6

Discussion and Future Work

This dissertation presents five different receiver front-end circuits. They have high performance despite the absence of inductors in papers II to V. The key goal has been to design flexible and high-performing receiver front-ends, and this chapter presents some of the author's thoughts on improvements of the presented techniques.

One of the major problems with voltage-mode receiver circuits is synthesizing the high-Q bandpass or bandreject filters since they rely on the bilateral frequency translation of the passive mixer and thus also relies on a high spectral purity LO signal. This requires a high performance VCO and divider circuitry with low phase noise, which is also needed for highly linear current-mode receiver circuits such as the passive-mixer first architecture. Solutions to solve this problem have merged but more research is required.

The harmonic rejection presented in paper II can suppress down-conversion from the third order harmonic, but suppression is accomplished first after the combination network of the second TIA. Future work for this receiver front-end is therefore to investigate if the RF part can be designed in such a way that the harmonic rejection is achieved already in the down-conversion stage. A nice property of the six-phase system is that an integer ratio between the LNTAs can be used, compared to the irrational ratio ($\sqrt{2}$) for the eight-phase solution, to reject the harmonic in the down-conversion stage.

For the two feedback-based receiver front-ends, signals from the baseband will, as described in paper III, be up-converted by the feedback to the LO harmonics. Thus, harmonic rejection should be implemented in the feedback path to attenuate the spurious emissions at LO harmonics. Moreover, the receiver circuits (positive and negative global feedback) should be measured together with SAW-filters or duplexers, to make sure that the out-of-band rejection of the filters still sufficient, and single-ended to differential conversion at duplex distance is intact if the receiver has a differential input, when using a non-50 Ω out-of-band impedance. For aggregation of two carriers located far apart in the same band, such as in band 42 or 43, where the RF bandwidth is 200 MHz, non-contigous carrier aggregation with two separate LO frequencies

may be more power-efficient than using a single wideband IF receiver. This could also be investigated with the feedback architectures where two different feedback paths with different LO frequencies are used. The idea to use a blocker power detector, and in case of very strong blockers decrease the gain of the main path while using the auxiliary path for reception can also analyzed.

In paper IV the baseband uses OPAMP based TIAs, but the baseband can also be implemented using wideband CG stages with high g_m to achieve low input impedance. The loop gain of the baseband amplifiers, affected by the low source impedance i.e. the mixer switch resistance and the off-chip impedance, could also be increased in order to reduce the input impedance and further boost the linearity. Another interesting topic would be to use a single-balanced mixer to remore the off-chip balun. This will, however, lead to an increased down-conversion of flicker noise from the LO generation network, and increased challenges in accommodating IIP2 requirements.

The increased noise figure in paper V when using a non-integer ratio between the LO frequency and sampling frequency of the ADCSF should be further investigated. To increase the understanding this issue, a new receiver has been implemented and sent for fabrication. One way to reduce the problem may be to use a fully-differential LNA, and on-chip decimation filters to reduce the digital data rate of the chip interface.

References

[1] A. Nejdel, M. Törmänen, and H. Sjöland, "A 0.7 to 3 GHz wireless receiver front end in 65-nm CMOS with an LNA linearized by positive feedback," *Analog Integrated Circuits and Signal Processing*, vol. 74, no. 1, pp. 49–57, 2013.

[2] A. Nejdel, M. Törmänen, and H. Sjöland, "A 0.7-3.7 GHz six phase receiver front-end with third order harmonic rejection," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2013, pp. 279–282.

[3] A. Nejdel, H. Sjöland, and M. Törmänen, "A noise-cancelling receiver front-end with frequency selective input matching," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 1137–1147, May 2015.

[4] A. Nejdel, M. Törmänen, and H. Sjöland, "A positive feedback passive mixer-first receiver front-end," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2015, pp. 79–82.

[5] A. Nejdel *et al.*, "A 0.6—3.0 GHz 65 nm CMOS radio receiver with $\Delta\Sigma$-based A/D-converting channel-select filters," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2015, pp. 229–302.

[6] A. Nejdel, M. Törmänen, and H. Sjöland, "A linearized 1.6-5 GHz low noise amplifier using positive feedback in 65 nm CMOS," in *NORCHIP, 2011*, 2011, pp. 1–4.

[7] M. Abdulaziz, A. Nejdel, M. Törmänen, and H. Sjöland, "A 3.4mW 65nm CMOS 5th order programmable active-RC channel select filter for LTE receivers," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2013, pp. 217–220.

[8] A. Nejdel, M. Törmänen, and H. Sjöland, "A noise cancelling 0.7-3.8 GHz resistive feedback receiver front-end in 65 nm CMOS," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 35–38.

[9] W. Ahmad, A. Nejdel, M. Törmänen, and H. Sjöland, "Fully integrated radio over fiber downlink for distributed multi-antenna systems in 65 nm CMOS," in *Proceedings of IEEE New Circuits And Systems Conference*, 2014, pp. 353–356.

[10] GSMA. (2015) Global mobile economy report 2015, *accessed 2015-10-12*. [Online]. Available: http://www.gsmamobileeconomy.com/GSMA_Global_Mobile_Economy_Report_2015.pdf

[11] CISCO. (2015) Cisco visual networking index: Forecast and methodology, 2014–2019, , *accessed 2015-10-12*. [Online]. Available: http://www.cisco.com/c/en/us/solutions/collateral/service-provider/ip-ngn-ip-next-generation-network/white_paper_c11-481360.pdf

[12] 3GPP TS 36.101 V12.5.0 (2014-11), "User Equipment (UE) radio transmission and reception (Release 12)."

[13] H. Holma and A. Toskala, *LTE for UMTS: Evolution to LTE-Advanced*, 2nd ed. John Wiley & sons, ltd.Academic Press, 3 2011.

[14] S. Ahmadi, *LTE-Advanced, A Practical Systems Approach to Understanding 3GPP LTE Releases 10 and 11 Radio Access Technologies*, 1st ed. Academic Press, 12 2013.

[15] (TDK), "SAW Duplexer LTE Band 20, B8633."

[16] (TriQuint), "856979 806/847 MHz Duplexer."

[17] E. Armstrong, "A new system of short wave amplification," *Proceedings of the Institute of Radio Engineers*, vol. 9, pp. 3–11, Feb 1921.

[18] F. M. Colebrook, "Homodyne," *Wireless World and Radio Rev.*, vol. 16, pp. 645–648, Jun 1924.

[19] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1399–1410, Dec 1995.

[20] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, pp. 428–435, Jun 1997.

[21] M. Nilsson *et al.*, "A 9-band WCDMA/EDGE transceiver supporting HSPA evolution," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2011, pp. 366–368.

[22] T. Sowlati *et al.*, "Single-chip multiband WCDMA/HSDPA/HSUPA/EGPRS transceiver with diversity receiver and 3G DigRF interface without SAW filters in transmitter / 3G receiver paths," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 116–117,117a.

[23] M.-D. Tsai *et al.*, "A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 354–355.

[24] M. Mikhemar *et al.*, "A rel-12 2G/3G/LTE-advanced 3CC receiver," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2015, pp. 143–146.

[25] S. a. o. Tadjpour, "A multi-band rel9 WCDMA/HSDPA/TDD LTE and FDD LTE transceiver with envelope tracking," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2014, pp. 383–386.

[26] A. Cavalcante *et al.*, "Performance evaluation of LTE and Wi-Fi coexistence in unlicensed bands," in *Proceedings of IEEE Vehicular Technology Conference*, 2013, pp. 1–6.

[27] X. Yang, H.-Y. Liu, and X. Guo, "Bluetooth coexistence with 4G broadband wireless networks," in *Proceedings of IEEE Conference on Sensor, Mesh and Ad Hoc Communications and Networks*, 2010, pp. 1–9.

[28] C. W. Liu and M. Damgaard, ""IP2 and IP3 nonlinearity specifications for 3G/WCDMA receivers," *High Frequency Electronics*, vol. 8, pp. 16–29, June 2009.

[29] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, 2003.

[30] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A +78 dBm IIP2 CMOS direct downconversion mixer for fully integrated UMTS receivers," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 552–559, March 2006.

[31] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, and P. Kinget, "Digitally assisted IIP2 calibration for CMOS direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2253–2267, Oct 2011.

[32] K. Dufrene, Z. Boos, and R. Weigel, "Digital adaptive IIP2 calibration scheme for CMOS downconversion mixers," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2434–2445, Nov 2008.

[33] V. Aparin, G. Ballantyne, C. Persico, and A. Cicalini, "An integrated LMS adaptive filter of TX leakage for CDMA receiver front ends," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1171–1182, May 2006.

[34] E. Atalla, A. Bellaouar, and P. Balsara, "IIP2 requirements in 4G LTE handset receivers," in *Proceedings of IEEE Midwest Symposium on Circuits and Systems*, 2013, pp. 1132–1135.

[35] O. Jensen *et al.*, "Rf receiver requirements for 3G W-CDMA mobile equipment," *Microwave Journal*, vol. 43, pp. 22–46, Feb 2000.

[36] H.-Y. Shih, C.-N. Kuo, W.-H. Chen, T.-Y. Yang, and K.-C. Juang, "A 250 MHz 14 dB-NF 73 dB-gain 82 dB-DR analog baseband chain with digital-assisted DC-offset calibration for ultra-wideband," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 338–350, Feb 2010.

[37] D. Kaczman *et al.*, "A single-chip tri-band (2100, 1900, 850/800 MHz) WCDMA/HSDPA cellular transceiver," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1122–1132, May 2006.

[38] D. Kaczman *et al.*, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and + 90 dbm iip2," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 718–739, March 2009.

[39] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[40] P. Andreani and H. Sjöland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Transactions Circuits Systems II, Analog and Digital Signal Processing*, vol. 48, pp. 835–841, Sep 2001.

[41] D. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2004, pp. 97–100.

[42] A. Abidi, "High-frequency noise measurements on FET's with small dimensions," *IEEE Transactions on Electron Devices*, vol. 33, pp. 1801–1805, Nov 1986.

[43] A. Scholten *et al.*, "Noise modeling for RF CMOS circuit simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 618–632, March 2003.

[44] X. Li, S. Shekhar, and D. Allstot, "Gm-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2609–2619, Dec 2005.

[45] W. Zhuo *et al.*, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 52, pp. 875–879, Dec 2005.

[46] I. Chamas and S. Raman, "Analysis, design, and X -band implementation of a self-biased active feedback G_m -boosted common-gate CMOS LNA," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 542–551, March 2009.

[47] X. Li, S. Shekhar, and D. Allstot, "Low-power gm-boosted LNA and VCO circuits in 0.18 μm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2005, pp. 534–615.

[48] A. Liscidini, G. Martini, D. Mastantuono, and R. Castello, "Analysis and design of configurable LNAs in feedback common-gate topologies," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 55, pp. 733–737, Aug 2008.

[49] S. Woo, W. Kim, C.-H. Lee, K. Lim, and J. Laskar, "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 218–219,219a.

[50] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1341–1350, June 2008.

[51] S. Andersson, C. Svenson, and O. Drugge, "Wideband LNA for a multistandard wireless receiver in 0.18 μm CMOS," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2003, pp. 655–658.

[52] C. G. Tan *et al.*, "A universal GNSS (GPS/galileo/glonass/beidou) SoC with a 0.25mm^2 radio in 40nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2013, pp. 334–335.

[53] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 275–282, Feb 2004.

[54] A. Shahani, D. Shaeffer, and T. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 2061–2070, Dec 1997.

[55] J. Borremans *et al.*, "A 40 nm CMOS 0.4-6 GHz receiver resilient to out-of-band blockers," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1659–1671, July 2011.

[56] L. Franks and I. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *The Bell System Technical Journal*, vol. 39, pp. 1321–1350, Sept 1960.

[57] A. El Oualkadi, M. El Kaamouchi, J.-M. Paillot, D. Vanhoenacker-Janvier, and D. Flandre, "Fully integrated high-Q switched capacitor bandpass filter with center frequency and bandwidth tuning," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2007, pp. 681–684.

[58] C. Toumazou *et al.*, "400 MHz switching rate GaAs switched capacitor filter," *Electronics Letters*, vol. 26, pp. 460–461, March 1990.

[59] A. Ghaffari, E. Klumperink, M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 998–1010, May 2011.

[60] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 2962–2976, Dec 2013.

[61] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3359–3375, Dec 2009.

[62] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1415–1424, Sept 2004.

[63] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 873–887, Jun 2001.

[64] X. He and J. van Sinderen, "A low-power, low-EVM, SAW-less WCDMA transmitter using direct quadrature voltage modulation," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3448–3458, Dec 2009.

[65] Y. Ji-Ren, I. Karlsson, and C. Svensson, "A true single-phase-clock dynamic CMOS circuit technique," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 899–901, Oct 1987.

[66] R. Dutta *et al.*, "Flip-flops for accurate multiphase clocking: Transmission gate versus current mode logic," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, pp. 422–426, July 2013.

[67] M. Abdulaziz, M. Törmänen, and H. Sjöland, "A compensation technique for two-stage differential OTAs," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 61, pp. 594–598, Aug 2014.

[68] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, and Y. Papananos, "A low-power wideband reconfigurable integrated active-RC filter with 73 dB SFDR," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1997–2008, Sept 2006.

[69] M. Vadipour, "Capacitive feedback technique for wide-band amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 90–92, Jan 1993.

[70] J. Weldon *et al.*, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 2003–2015, Dec 2001.

[71] E. Mensink, E. Klumperink, and B. Nauta, "Distortion cancellation by polyphase multipath circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, pp. 1785–1794, Sept 2005.

[72] K. Lee *et al.*, "A single-chip 2.4-GHz direct-conversion CMOS receiver for wireless local loop using multiphase reduced frequency conversion technique," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 800–809, May 2001.

[73] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 2004, pp. 401–404.

[74] S. Lerstaveesin, M. Gupta, D. Kang, and B.-S. Song, "A 48–860 MHz CMOS low-IF direct-conversion DTV tuner," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2013–2024, Sept 2008.

[75] H.-K. Cha, S.-S. Song, H.-T. Kim, and K. Lee, "A CMOS harmonic rejection mixer with mismatch calibration circuitry for digital TV tuner applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, pp. 617–619, Sept 2008.

[76] T. Yamaji, T. Itakura, R. Ito, T. Ueno, and H. Okuni, "Balanced 3-phase analog signal processing for radio communications," in *Proceedings of IEEE International Symposium on Circuits and Systems*, 2006, pp. 2386–3789.

[77] T. Yamaji *et al.*, "A 6-phase harmonic rejection down-converter with digital assist," in *Proceedings of IEEE Symposium on VLSI Circuits*, 2010, pp. 181–182.

[78] J. Greenberg *et al.*, "A 40-MHz-to-1-GHz fully integrated multistandard silicon tuner in 80-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 2746–2761, Nov 2013.

[79] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver resilient to large harmonic blockers," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 1336–1350, June 2015.

[80] H.-K. Cha, S.-S. Song, H.-T. Kim, and K. Lee, "A CMOS harmonic rejection mixer with mismatch calibration circuitry for digital TV tuner applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, pp. 617–619, Sept 2008.

[81] N. Moseley, E. Klumperink, and B. Nauta, "A two-stage approach to harmonic rejection mixing using blind interference cancellation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, pp. 966–970, Oct 2008.

[82] N. Moseley, Z. Ru, E. Klumperink, and B. Nauta, "A 400-to-900 MHz receiver with dual-domain harmonic rejection exploiting adaptive interference cancellation," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 232–233,233a.

[83] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2011, pp. 372–374.

[84] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1097–1111, May 2014.

[85] R. Chen and H. Hashemi, "Reconfigurable SDR receiver with enhanced front-end frequency selectivity suitable for intra-band and inter-band carrier aggregation," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2015, pp. 1–3.

[86] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2696–2708, Dec 2010.

[87] M. Soer, E. Klumperink, Z. Ru, F. van Vliet, and B. Nauta, "A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving >11dbm IIP3 and <6.5 db NF," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 222–223.

[88] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec 2012.

[89] C. Izquierdo, A. Kaiser, F. Montaudon, and P. Cathelin, "Reconfigurable wide-band receiver with positive feed-back translational loop," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2011, pp. 1–4.

[90] F. Lin, P.-I. Mak, and R. Martins, "An RF-to-BB current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 74–75.

[91] K. Philips *et al.*, "A continuous-time ΔΣ ADC with increased immunity to interferers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2170–2178, Dec 2004.

[92] M. Sosio, A. Liscidini, R. Castello, and F. De Bernardinis, "A complete DVB-T/ATSC tuner analog base-band implemented with a single filtering ADC," in *Proceedings of IEEE European Solid-State Circuits Conference*, Sept 2011, pp. 391–394.

[93] M. Andersson, M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A 9MHz filtering ADC with additional 2nd-order ΔΣ modulator noise suppression," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2013, pp. 323–326.

[94] M. Andersson, , M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A filtering ΔΣ ADC for LTE and beyond," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1535–1547, July 2014.

[95] R. Rajan and S. Pavan, "Design techniques for continuous-time ΔΣ modulators with embedded active filtering," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 2187–2198, Oct 2014.

[96] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 1st ed. John Wiley & sons, ltd.Academic Press, 2005.

[97] R. Rajan and S. Pavan, "Device noise in continuous-time oversampling converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, pp. 1829–1840, Sept 2012.

[98] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1770–1780, Sept 2010.

[99] M. Sosio, A. Liscidini, and R. Castello, "A 2G/3G cellular analog base-band based on a filtering ADC," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 59, pp. 214–218, April 2012.

Paper I

A 0.7 to 3 GHz Wireless Receiver Front End in 65-nm CMOS with an LNA Linearized by Positive Feedback

Abstract

This paper presents a wireless receiver front-end intended for cellular applications implemented in a 65 nm CMOS technology. The circuit features a low noise amplifier (LNA), quadrature passive mixers, and a frequency divider generating 25 % duty cycle quadrature local oscillator (LO) signals. A complementary common-gate LNA is used, and to meet the stringent linearity requirements it employs positive feedback with transistors biased in the subthreshold region, resulting in cancellation of the third order non-linearity. The mixers are also linearized, using a baseband to LO bootstrap circuit.

Measurements of the front-end show about 3.5 dB improvement in out-of-band IIP3 at optimum bias of the positive feedback devices in the LNA, resulting in an out-of-band IIP3 of 10 dBm. With a frequency range from 0.7 to 3 GHz the receiver front-end covers most important cellular bands, with an input return loss above 9 dB and a voltage gain exceeding 16 dB for all bias settings. The circuit consumes 4.38 mA from a 1.5 V supply.

Anders Nejdel, Markus Törmänen, and Henrik Sjöland, "A 0.7 to 3 GHz wireless receiver front end in 65-nm CMOS with an LNA linearized by positive feedback,"
 from *Analog Integrated Circuits and Signal Processing*, Vol. 74, No. 1, pp. 49-57, 2013.

I Introduction

Cellular communication systems evolve quickly towards ever increasing data-rates and traffic volumes. As a consequence the number of radio frequency bands and communication standards to support in cellular devices increase. To further add to the growing complexity multiple antennas are needed to support the increasing data-rates using multiple input multiple output (MIMO) techniques. Using traditional narrowband receivers will soon become unattractive, resulting in both larger chip area due to the several parallel receiver front ends and increasing number of off-chip components. To reduce the cost and size it is therefore important to find receiver topologies that offer both wide operating frequency range and high linearity, while maintaining high performance in other key parameters.

For lowest cost in mass-production the transceiver should be implemented in standard CMOS technology, which is optimized for dense digital circuits rather than analog performance. Using such technology allows the analog and digital parts of the wireless transceiver to be realized on the same silicon die. This facilitates schemes where the digital parts sense errors of the analog parts, and generate control signals that can adjust the analog circuitry so that the errors are minimized. Such schemes become more and more attractive, as the scaling of CMOS technology reduces the cost of digital functions such as implementing advanced algorithms, while at the same time raw analog performance decreases and analog circuits will become more prone to malfunction due to mismatches of the small devices available in modern CMOS technologies. [1]

The linearity is a crucial parameter of the receiver, and it will most likely become even more important as the traffic volumes increase in cellular networks resulting in more interference due to strong signals from other transceivers. Highly selective surface acoustic wave (SAW) filters are typically used in cellular receivers to suppress out-of-band interference by their sharp transition from pass band to stop band. These SAW filters are implemented by off-chip components that increases the bill of material (BOM) significantly, especially with the growing number of frequency bands to support, each band requiring a separate filter. As the number of frequency bands increase it would therefore be desirable to relax the filter specifications to reduce cost, which requires increased receiver linearity. It would be especially valuable to reduce the requirements of duplex filters. Such filters are used in full duplex systems, where large signals can be transmitted at the same time as the receiver must be able to receive a weak signal, using the same antenna. The frequency distance between the transmitted and received signal can be quite small, and the only isolation from the transmitter output signal to the receiver input is provided by a duplex filter. High performance is thus needed in the duplex filter, resulting in a high cost. Increased linearity, allowing the receiver to handle more interference, would thus be very valuable. In this paper a technique to increase the linearity, by

positive feedback, of the common-gate (CG) LNA is presented. The paper is an extended version of [2], presented at the Norchip conference 2011. Section II presents an overview of the radio receiver front end. Section III introduces the low noise amplifier with a positive feedback technique to increase linearity, and section IV presents the bootstrapped passive mixer used in the front-end. The results are given in section V and finally the conclusions in section VI.

II Receiver front end overview

The front-end is intended for a direct conversion receiver. It consists of an LNA followed by two frequency down-conversion mixers, fed by quadrature local oscillator (LO) signals from a digital frequency divider, see Fig. 1. The LNA is linearized using a positive feedback technique. The feedback transistors are biased in the sub-threshold region, providing an expanding third order non-linearity that cancels the compressing non-linearity of the main devices. The frequency conversion from RF to baseband is performed by quadrature voltage commutating passive mixers. To avoid harmful interaction between the quadrature mixers and to achieve high linearity, the mixers are fed by 25 % duty cycle signals from a digital frequency divider [3]. The fast rise-time of the digital waveforms reduces the signal dependence of the switching instants in the mixers, resulting in high linearity. To further increase the linearity, a bootstrap from baseband to LO is used [4]. In addition to performing the necessary frequency down-conversion of the received signal, the passive mixers, thanks to their bi-directional property, frequency translate the baseband load impedance to the RF side. This creates a second order high-Q bandpass filter at the output of the LNA [5], reducing the risk of interferers saturating the LNA output. This filter, however, does not attenuate interference at the input of the LNA. It is thus of key importance to achieve high LNA input linearity, and to investigate new techniques for further improving the linearity [6].

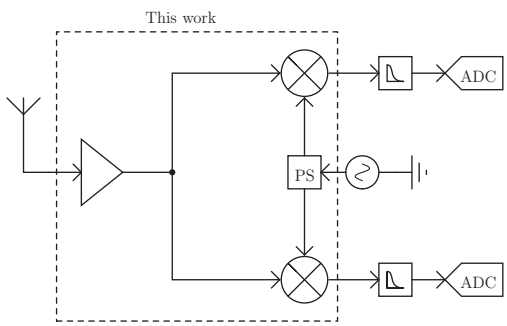


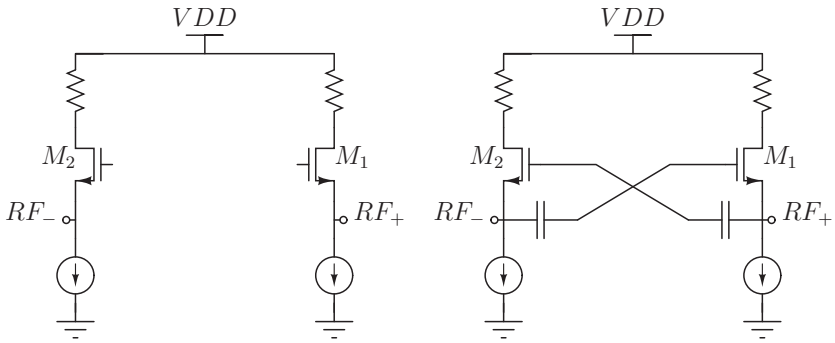
Figure 1: A typical receiver front end.

III Low Noise Amplifier

The LNA is critical to the receiver sensitivity and it must therefore have low noise figure. Since the LNA is the first stage of the receiver front-end, all signals from the SAW band select filter or duplex filter will be present at its input. This means that the LNA must have sufficient linearity to handle all in-band interferers, out-of-band interferers attenuated by the filter, and in an frequency division duplex (FDD) device also the transmitted uplink signal attenuated by the duplex filter. Especially signals present halfway between the received signal and transmitted signal can cause severe degradation of the received signal quality due to the third order non-linearity of the system. At the same time the LNA must provide low noise and sufficient gain for the signal to receive, not to degrade the receiver sensitivity, and this must be achieved at low power consumption. Designing the LNA in modern CMOS technology furthers adds to the challenge, due to the low supply voltage resulting in limited voltage headroom of the transistors, causing compression. To reduce the problems we suggest to employ linearization circuitry in the LNA, and use the digital baseband to control it so that the third order non-linearity is cancelled.

Traditionally the inductively degenerated common source topology has been used when implementing LNAs in CMOS technology, because of the excellent noise performance that can be achieved. The disadvantage of that topology, however, is the inherently narrow band input match. This is the result of the reactive part of the input impedance being determined by a series resonance circuit consisting of the gate-source capacitance of the input transistor and the inductors at gate and source. The resonance frequency, which is also the frequency of the input match, is mainly set by the gate inductor. Substantial gate inductance is often needed, and at the same time the series resistance of the inductor must be kept low to maintain high noise performance. The gate inductor is therefore often implemented off-chip, due to higher available quality factor (Q) product for discrete inductors, thus increasing the BOM. [7].

The common gate (CG) amplifier, seen in Fig. 2a has an input impedance that, ideally, is frequency independent and equal to the inverse of the transconductance (g_m) of the input transistor. Due to parasitic capacitances, however, the input impedance is not that ideal in reality, but the CG topology is still an attractive choice for wideband systems that must cover several frequency bands. In Fig. 2a there are current sources at the amplifier inputs. Their function is to provide a bias current path without loading the RF signal. This can be implemented with an inductor, which has the advantage of minimum DC voltage drop, thus providing maximum voltage headroom for signals. The inductor can be designed to resonate with the parasitic capacitances at the input node, improving the input match at the frequency of operation. The highest bandwidth is achieved when the parasitic capacitances are low, and the inductance is large, as this results in a low Q of the parallel resonance



(a) Common gate amplifier. (b) Capacitive cross coupled CG amplifier.

Figure 2: Common gate amplifier with and without capacitive cross coupling.

circuit consisting of the inductor, parasitic capacitances, and the input resistance. To minimize the noise contribution of the inductor it should have a large equivalent parallel resistance, corresponding to a large inductance and quality factor, i.e. a large LQ product. Fortunately the noise contribution of this inductor is in general less severe compared to that of the gate inductor in the CS topology, and it can therefore typically be implemented on-chip.

The major drawback of the CG amplifier is its noise performance, with the noise factor excluding noise from the load impedance and input inductor given by (1). As can be seen the noise factor can be reduced by increasing the transconductance, but doing so will unfortunately also degrade the input match. When the input is matched the noise factor can be simplified to the final expression in (1), which for input device channel lengths compatible with wideband operation at GHz frequencies results in noise figures of about 3 to 4 dB.

$$\begin{aligned} F &\approx \frac{\bar{i}_{nd}^2}{\bar{i}_{nR_s}^2}\left(\frac{1}{g_m R_s}\right)^2 \\ &= 1+\frac{4kT\gamma g_{d0}\Delta f}{4kTR_s^{-1}\Delta f}\left(\frac{1}{g_m R_s}\right)^2 \\ &= 1+\frac{\gamma}{\alpha}\bigg|_{g_m R_s=1} \end{aligned} \tag{1}$$

One way to improve the noise performance of the common gate topology is to provide negative voltage gain $-A$ from the input to the gate terminal, no longer keeping the gate at signal ground [8]. The significant improvement of

the noise factor is clear from equation (2). Note, however, that this equation assumes that the amplifier providing the voltage gain is noiseless.

$$\begin{aligned} F &\approx \frac{\bar{i}_{nd}^2}{\bar{i}_{nR_s}^2}\left(\frac{1}{g_m R_s}\right)^2 \\ &= 1+\frac{4kT\gamma g_{d0}\Delta f}{4kTR_s^{-1}\Delta f}\left(\frac{1}{(1+A)g_m R_s}\right)^2 \\ &= 1+\frac{\gamma}{(1+A)\alpha}\Big|_{(1+A)g_m R_s=1} \end{aligned} \tag{2}$$

One way of implementing a negative unity voltage gain ($A = -1$) is by using cross-coupled capacitors (CCC) in a differential LNA [9]. These capacitors feed each differential input signal to the gate of the opposite side input transistor, see Fig. 2b. Each transistor then receives signals of opposite polarity at the gate and source, doubling the effective input signal. Using capacitors, the negative voltage gain can be implemented without introducing additional noise. However, it should be noted that the increased drive of the input transistors result in a doubling of effective transconductance, halving the input impedance, affecting the input match. The most common way to restore the input match is to reduce the transconductance of the input devices to half the original value. The noise figure is improved compared to a standard common-gate amplifier thanks to the halved current noise power of the input devices.

Another way of increasing the input impedance is to use positive feedback [10] [11]. The feedback will change the impedance according to (3).

$$Z_{in,fb} = \frac{Z_{in,ol}}{1-A_{fb}} \tag{3}$$

A feedback loop gain equal to 0.5 will accomplish the desired doubling of the input impedance. Another benefit of using positive feedback is the extra degree of freedom that is introduced. This can be used to counter non-linearities, by using feedback transistors biased in the sub threshold region. The feedback transistors will then exhibit an expanding non-linearity that when used in positive feedback will counteract the compressing behaviour of the main transistors. By using transistors biased in the sub-threshold region, the extra current consumption of the feedback path also becomes negligible. For best linearity the bias point of the feedback transistors should be tuned. In practice their gate bias voltage can be set by a DAC controlled by the digital baseband. The powerful and low power baseband circuits that can be implemented in modern CMOS technology make this type of tuning scheme attractive, as it can improve the linearity versus power consumption trade-off.

A LNA Design

The circuit schematic of the LNA can be seed in Fig. 3. It is a CCC-CG-LNA, using the positive feedback linearization technique described above. The bias current of the cross-coupled input transistors M_1, M_2 is supplied by a differential on-chip inductor. The positive feedback is realized by transistors M_3, M_4, having their gates connected to the CG-stage outputs and their drains to the inputs. They thereby feed a signal current to the inputs that is controlled by the output voltages, that is a feedback signal. In order to increase isolation from the output to the input of the LNA, cascode devices M_5, M_6 are used. The dimensions of the transistors of the LNA, as well as their gate bias voltages, are provided in Table 1.

In order to obtain a flat gain over a large RF bandwidth, a resistive load was chosen. The bias current of the input stage would, however, cause a large DC

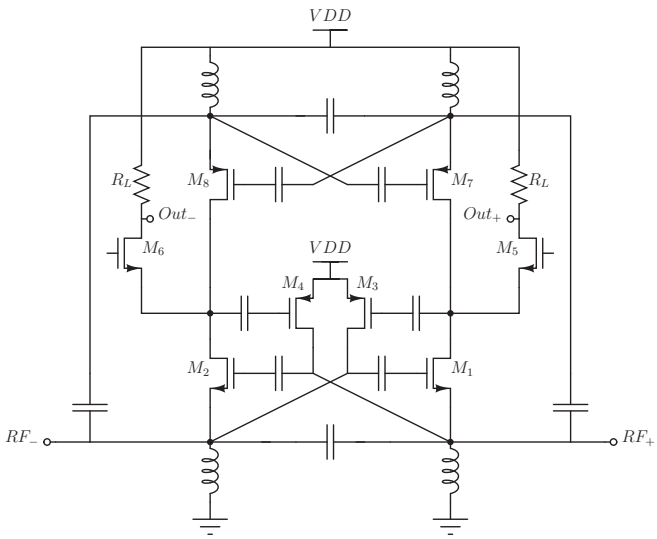


Figure 3: Simplified schematic of the LNA, omitting bias sources.

Table I: Sizes and bias voltages of the devices in the LNA.

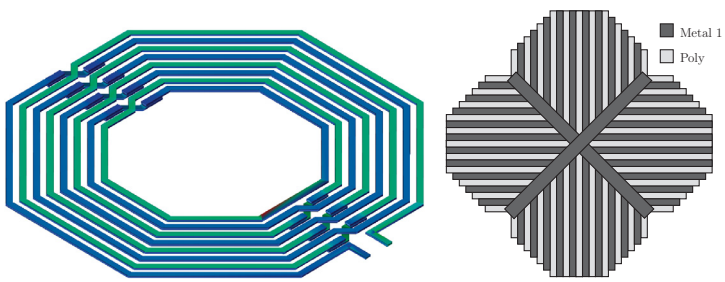
Device	W / L / μm	Bias voltage / V
M_1, M_2	25.3 / 0.06	0.600
M_3, M_4	17.18 / 0.1	-
M_5, M_6	10.4 / 0.1	1.350
M_7, M_8	30.9 / 0.1	0.900

voltage drop across the load resistors unless current bleeding was introduced. To ensure sufficient voltage headroom, a complementary cross-coupled PMOS input stage M_7, M_8 is therefore used, providing an alternative path for the bias current, and also adding to the input stage transconductance. Effectively the PMOS and NMOS cross-coupled input stages are connected in parallel. The total gain is then determined by $A_v = (g_{m2} + g_{m8})Z_L$. In this design g_{m8} is less than g_{m2}, since the bias current is less in the PMOS input stage. It is approximately 50 % of that in the NMOS stage, resulting in a 50 % reduction of the DC voltage drop across the load resistors and thus increasing the linearity by the higher available voltage headroom. The resistors were chosen to 480 Ω each, which according to simulations results in 22.8 dB voltage gain of the LNA, at 2 GHz. The voltage drop is 630 mV, corresponding to 1.31 mA in each resistor. The total LNA bias current is 4.33 mA.

Current bleeding devices will introduce more noise to the circuit, but by connecting them to the input signal in a CCC-CG topology, they become a part of the input stage This is similar to [12] and together with noise cancelling, the noise performance is not degraded.

Since the NMOS and PMOS cross-coupled stages are connected in parallel, the LNA input conductance is equal to the sum of the input conductance of the two stages. If the NMOS and PMOS transistors were designed to have equal transconductance, the resulting input resistance of the LNA would thus be halved compared to an NMOS-only design. By keeping the transconductance of current bleeding devices low, however, the input resistance of the LNA will still be dominated by the NMOS stage.

B RFC



(a) Differential inductor. (b) Patterned ground shield.

Figure 4: Inductors, used both in the NMOS and PMOS input stages.

The circuit is fully integrated, including the inductors used in the LNA, see figure 4a. In order to achieve good symmetry and to simplify the layout, the two

differential inductors used for the NMOS and the PMOS stages are identical. The inductors were simulated in Agilent ADS Momentum and designed to have large inductance and at the same time occupy small area. This led to a multi-turn design with a relatively narrow trace. By using the top copper layer for main routing and realizing crossings in a lower copper layer, see figure 4a, a fully symmetrical geometry was achieved, fitting the differential structure of the LNA. On the chip the two inductors are in close proximity of each other, but coupling is not an issue since the same signal, the LNA input signal, will be present in both inductors. A custom made patterned ground shield was used to electrically isolate the inductors from the substrate, thereby increasing Q-value [13]. The patterned ground plane, see figure 4b, was designed in both the first metal layer, width = 0.3 μm, and the poly layer, width = 1 μm, to minimize the electrical coupling to the substrate. The inductance was simulated to 6.9 nH per side, the Q value to 4.6 at 3 GHz, and the self resonance frequency to 5.42 GHz. This was accomplished by using 8 turns, an outer radius of 90 μm, a spacing of 2.65 μm and a width of 3.2 μm.

IV Passive Mixer

Passive mixers have several benefits, compared to active ones. One of the main ones is the frequency translation of impedance from the IF side to the RF side. If the baseband load is a standard RC low pass impedance, this will be up-translated to the RF side of the mixer providing high-Q bandpass filtering centred at the LO frequency. The filter is not perfect, but it can still attenuate out-of-band and even in-band interferers by up to about 15 dB at the LNA output [14]. In this circuit, a capacitor of 3 pF was used to create the pole at the

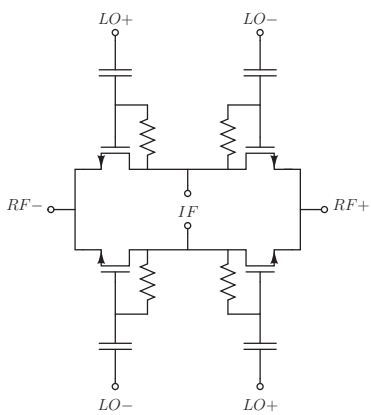


Figure 5: Schematic of bootstapped passive mixer.

baseband side of the passive mixer. In direct conversion and low-IF receivers, the passive mixer also has the benefit of having very low flicker noise due to the absence of DC current through the mixer transistors [15]. When modeling the switching of a passive mixer, the switches should ideally switch abruptly between zero conductance and a high constant conductance. But in practice, this is only possible if the gate of the transistor is fed by a perfect square wave, and all the other transistor terminals have the same potential. When a signal is received, there will be RF and baseband signal present at drain and source. The baseband signal will cause a low frequency modulation of the potential, which results in distortion. The distortion will be due to conductance modulation of the transistor, and due to modulation of the switching instants, the latter since the gate signal has finite rise and fall times. One way of reducing the distortion is to feed some of the low frequency information to the gate of the switching transistor, making the gate bias track the baseband voltage. This is accomplished by a low pass filter from the baseband to the LO [4]. This bootstrapping technique results in a 4 dB increase of IIP3. In order to have low loss, high linearity and to minimize harmful interaction between the I and Q mixer, the mixer is driven by 25 % duty cycle LO signals. The signals are generated on chip by a digital frequency divider. To improve matching the length of the transistors were chosen longer than the minimum length. This is especially important to second order linearity performance, since this can easily be ruined by transistor mismatch. The width and length of the transistors in the passive mixer was 20.5 and 0.12 μm respectively, and the resistors and capacitors, used in the bootstrap, were 2 kΩ and 630 fF, respectively.

A LO signal generation

The LO generation is crucial to obtain high mixer performance. Rapid transitions are beneficial as they reduce mixer non-linearity. The waveform should

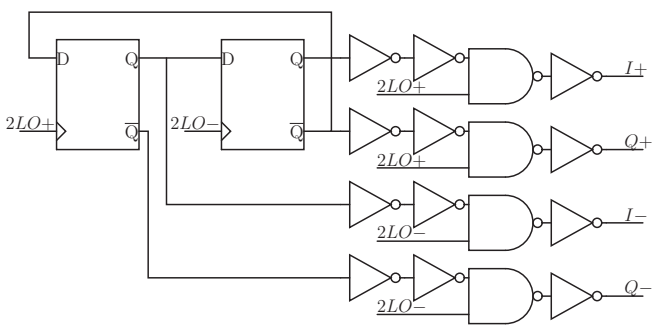


Figure 6: Frequency divider, generating 25 % duty cycle LO signals.

thus resemble a square-wave, making digital implementations attractive. By ensuring that the generated signals are non-overlapping, harmful interaction between the I and Q mixer is minimized. The duty cycle of the four LO waveforms should thus not exceed 25 %. LO generation is realized by a standard divide by 2 circuit, implemented using two true single phase clock (TSPC) D-registers clocked by positive and negative edges to accomplish phase shift [16] [17]. By combining the signals generated by the divide by 2 circuit and the differential input signals, four non overlapping signals can be generated. These are buffered with wide inverters and used as LO signals to the mixer. The LO phase generation schematic can be seen in figure 6.

V Results

The circuit was fabricated in 65-nm CMOS technology, and the chip photo can be seen in figure 7. The dies were wire-bonded to printed circuit boards (PCBs), featuring SMA connectors, decoupling capacitors and 100 Ω to 50 Ω differential matching. To drive the 50 Ω measurement instruments on-chip open drain buffers were used at the mixer output. The buffers were designed to provide unity voltage gain magnitude for a 50 Ω load. The current consumption of these buffers is omitted from the total chip current consumption, which was 4.38 mA with the feedback path turned off, 5.01 mA with a bias voltage of 1 V, and 6.15 mA with a bias voltage of 0.850 V. The main supply voltage was equal to 1.5 V.

In order to cover a large number of cellular communication bands, the input match needs to be wide, which can be seen in figure 8 for three different bias

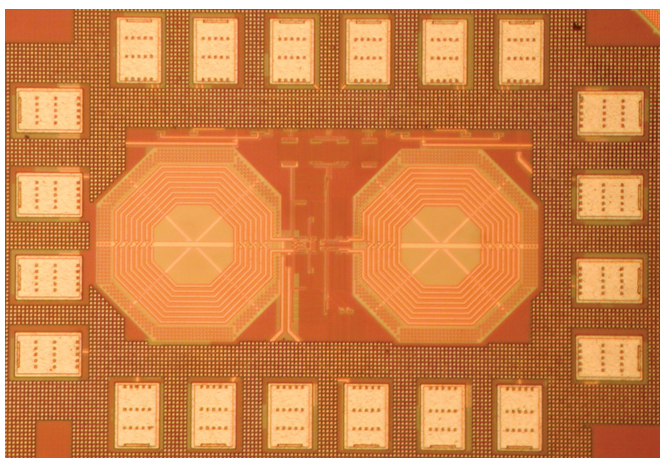


Figure 7: Photo of the chip, measuring 710μm by 490μm.

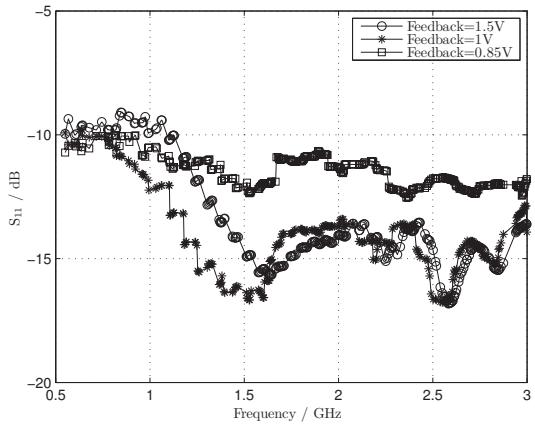


Figure 8: Input impedance match vs. frequency.

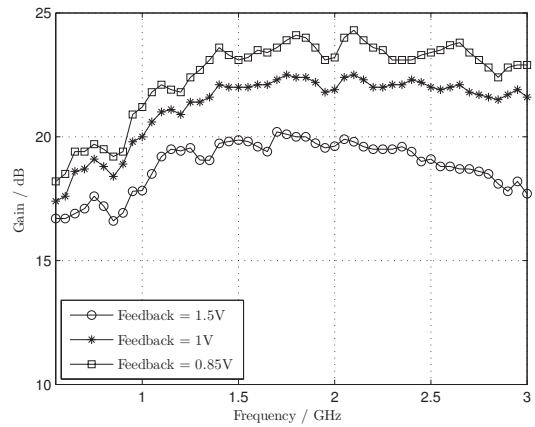


Figure 9: Voltage gain vs. frequency and bias voltage of the positive feedback.

voltages of the feedback transistors. The input match is below -10 dB for all frequencies from 0.5 to 3 GHz, except for some frequencies in the lower range, where the input match is below -9 dB.

The gain, see figure 9, depends on the bias voltage of the feedback transistors; if the feedback transistors are used in the active region, they will increase the gain due to the positive feedback. The amount of feedback must, however, be limited to ensure stability and maintain good input match.

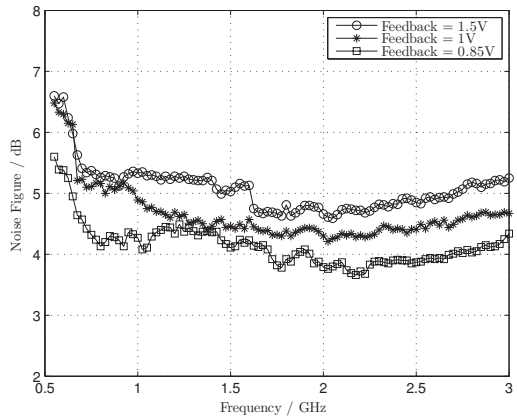


Figure 10: Noise figure vs. radio frequency and bias voltage of the feedback transistors.

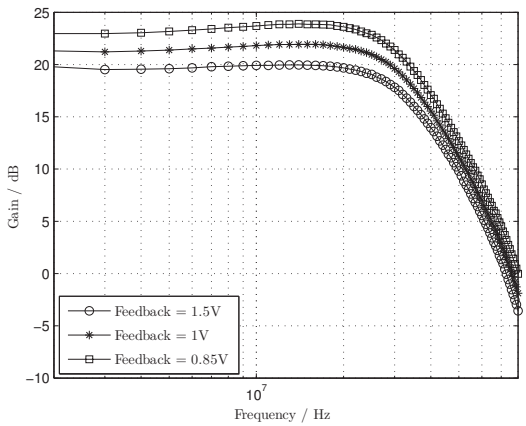


Figure 11: Gain vs. baseband frequency.

The noise figure was measured using a fixed baseband frequency of 10 MHz while sweeping the LO frequency. The noise can be decreased by increasing the bias current in the feedback transistors, as can be seen in figure 10. The gain, versus baseband frequency, for a 2 GHz RF input signal can be seen in figure 11. The baseband bandwidth is 20 MHz due to the capacitor at the output of the passive mixer. This filtering will also be present at the RF output of the LNA and help to suppress the of-band-blockers and interferers.

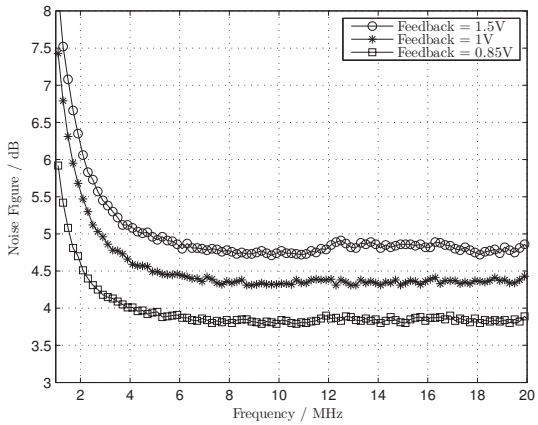


Figure 12: Noise figure vs. baseband frequency.

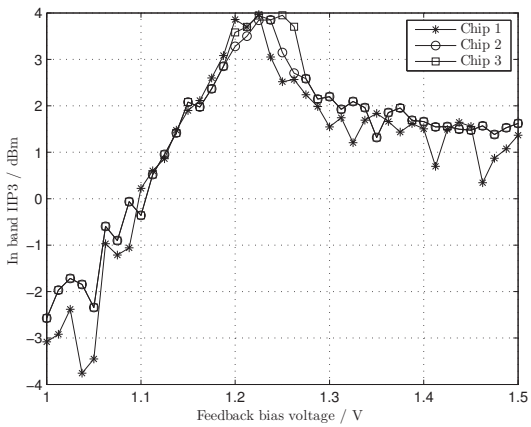


Figure 13: In band IIP3 vs. bias voltage of the feedback path.

Baseband noise, see figure 12, increases at low frequencies, due to the $\frac{1}{f}$ noise of the open drain buffers to drive the 50 Ω measurement equipment. The passive mixers are not expected to contribute any 1/f-noise.

As seen in figure 13, measured for three different chips, the in band IIP3 can be increased by about 2.5 dB by changing the bias voltage of the feedback transistors in the LNA compared to having the feedback transistors turned off; feedback voltage set to 1.5 V. The optimum value is approximately the same

for all three chips: 1.2 - 1.25 V. The in band IIP3 was measured by using two tones at 1.988 GHz and 1.99 GHz, and an LO frequency of 2 GHz.

The out-of-band IIP3 can be seen in figure 14 for the same three chips as the in band IIP3. Here the two test tones were 1.948 GHz and 1.9 GHz with an LO of 2 GHz. Here there is about 3.4 dB improvement at the optimum bias voltage, which is between 1.15 and 1.3, similar to the in band results.

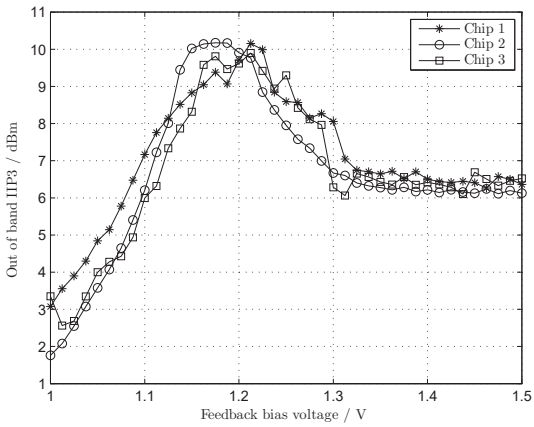


Figure 14: Out of band IIP3 vs. bias voltage of the feedback path.

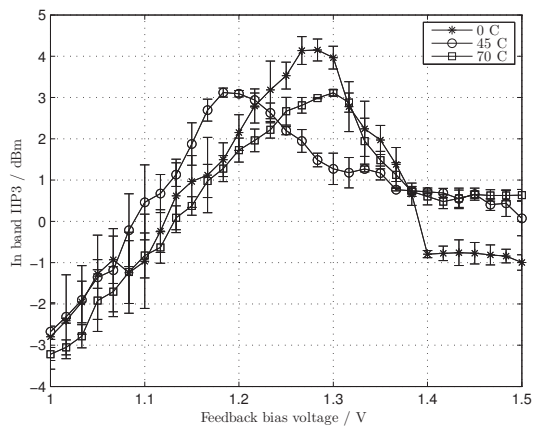


Figure 15: In band IIP3 vs. bias voltage of the feedback path versus temperature, median value and standard deviation for three samples.

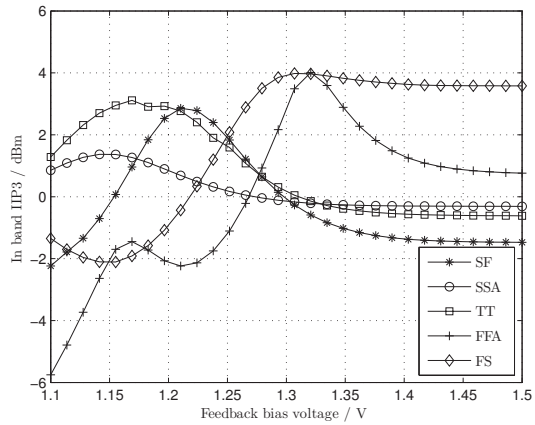


Figure 16: Simulated in band IIP3 vs. bias voltage of the feedback path for different corners.

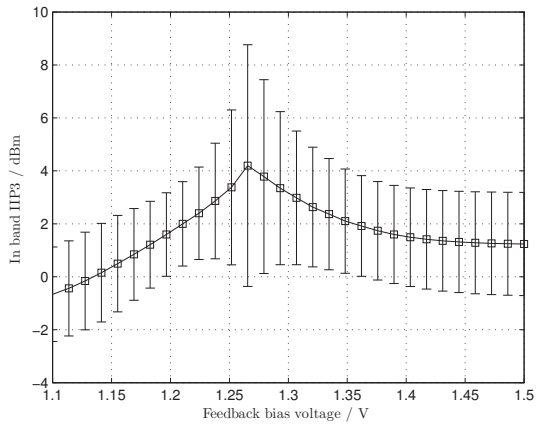


Figure 17: Simulated mean in band IIP3 with standard deviation for supply variations from -10 % to +10%.

The in band IIP3 was also measured for three different temperatures; 0° C, 45° C and 70° C, as seen in figure 15. In this figure, the median IIP3 value with standard deviation for three samples is presented. The optimum feedback voltage is between 1.15 and 1.35 V, depending on the temperature, and the largest IIP3 improvement was measured at 0° C.

The IIP3 improvement by the feedback was also simulated for different process corners, shown in figure 16. The improvement of the positive feedback depends on the corner but the in band IIP3 is always higher than +1 dBm. IIP2 was also measured to be above 35 dBm with an improvement of up to 10 dB depending on the bias voltage.

The simulated effect of supply variation can be seen in figure 17, where the supply has been swept 90 % - 110 % from the nominal voltage of 1.5 V. The trace of the mean value shows that there is an improvement of linearity over this supply voltage range.

VI Conclusion

A wideband receiver front-end in 65-nm CMOS has been designed and measured. The linearity can be increased by using positive feedback transistors in the LNA, biased in sub-threshold. By using the feedback devices, the linearity can be improved without significantly increasing the power consumption. The bias voltage achieving maximum linearity was close to identical for the three samples measured, causing an IIP3 increase of approximately 3 dB both in and out of band. If linearity is of less concern in situations with less interference, the bias current of the feedback transistors can be increased, resulting in increased gain and reduced noise. The amount of feedback is, however, limited by the level where the input impedance and stability will be degraded. Also, the linearity of the mixer is increased using a bootstrap circuit. The front-end can operate from 700 MHz to 3 GHz, and thereby covers most important cellular bands.

Acknowledgements

The authors would like to thank the Swedish Foundation for Strategic Research for funding the Digitally Assisted Radio Evolution project, and the other researchers in the Analog RF group at Lund University for fruitful discussions.

References

[1] R. Brederlow *et al.*, "A mixed-signal design roadmap," *IEEE Design Test of Computers*, vol. 18, pp. 34–46, Nov 2001.

[2] A. Nejdel, M. Törmänen, and H. Sjöland, "A linearized 1.6-5 GHz low noise amplifier using positive feedback in 65 nm CMOS," in *NORCHIP, 2011*, 2011, pp. 1–4.

[3] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, pp. 2353–2366, Sept 2010.

[4] F. Tillman and H. Sjoland, "A bootstrapping technique to improve the linearity of CMOS passive mixers," in *Proceedings of IEEE Symposium on VLSI Circuits*, 2003, pp. 221–222.

[5] A. Mirzaei *et al.*, "A frequency translation technique for SAW-less 3G receivers," in *Proceedings of IEEE Symposium on VLSI Circuits*, 2009, pp. 280–281.

[6] H. Zhang and E. Sanchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, pp. 22–36, Jan 2011.

[7] D. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2004, pp. 97–100.

[8] X. Li, S. Shekhar, and D. Allstot, "Gm-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2609–2619, Dec 2005.

[9] W. Zhuo *et al.*, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 52, pp. 875–879, Dec 2005.

[10] A. Liscidini, G. Martini, D. Mastantuono, and R. Castello, "Analysis and design of configurable LNAs in feedback common-gate topologies," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 55, pp. 733–737, Aug 2008.

[11] S. Woo, W. Kim, C.-H. Lee, K. Lim, and J. Laskar, "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 218–219,219a.

[12] G. Zare Fatin, Z. Koozehkanani, and H. Sjöland, "A technique for improving gain and noise figure of common-gate wideband LNAs," *Analog Integrated Circuits and Signal Processing*, vol. 65, pp. 239–244, 2010.

[13] C. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 743–752, May 1998.

[14] J. Borremans, G. Mandal, B. Debaillie, V. Giannini, and J. Craninckx, "A sub-3dB NF voltage-sampling front-end with +18dBm IIP3 and +2dBm blocker compression point," in *Proceedings of IEEE European Solid-State Circuits Conference*, 2010, pp. 402–405.

[15] M. Voltti, T. Koivi, and E. Tiiliharju, "Comparison of active and passive mixers," in *Proceedings of European Conference onCircuit Theory and Design*, 2007, pp. 890–893.

[16] Y. Ji-Ren, I. Karlsson, and C. Svensson, "A true single-phase-clock dynamic CMOS circuit technique," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 899–901, Oct 1987.

[17] L. F. Fei, "Frequency divider design strategies," *RF Design*, vol. 28, pp. 18–26, Mar 2005.

Paper II

A 0.7 - 3.7 GHz Six Phase Receiver Front-End With Third Order Harmonic Rejection

Abstract

This paper presents a highly linear receiver front-end operating from 700 MHz to 3.7 GHz with 3rd order harmonic rejection. It consists of a complementary low noise transconductance amplifier with capacitive cross coupling and negative g_m current sources, a six phase current-mode passive mixer, and baseband transimpedance amplifiers providing programmable gain. The circuit has been fabricated in 65 nm CMOS technology with an active area of just 0.09 mm^2. It consumes 7.2 mA, excluding the six phase local oscillator generation, from a 1.2 V supply, achieving a third order harmonic rejection of 40 dB, and a noise figure of 3 to 4.5 dB at 52 dB gain. The out of band IIP2 and IIP3 at full gain is +55 dBm and +5 dBm, respectively.

Compared to the published paper, an error in equation (7) has been corrected.

Anders Nejdel, Markus Törmänen, and Henrik Sjöland, "A 0.7 - 3.7 GHz Six Phase Receiver Front-End With Third Order Harmonic Rejection," © 2013 IEEE, reprinted from *Proceedings of IEEE European Solid-State Circuits Conference*, Bucharest, Romania, Sep. 16–20 2013, pp. 279–282.

I Introduction

The large growth of cellular communications has increased the need for high performance, low cost, and low power receivers. To reduce the price of cellphones, manufacturers want to use as few and low-cost components as possible. Substantial cost could be saved by complete removal or reduced performance of radio-frequency (RF) band-select filters. However, as these are used to suppress out of band interferers, the performance requirements of the receiver front-end increases. Especially if the low noise amplifier (LNA) is wideband, thus amplifying out-of-band interferers with low selectivity, the linearity becomes critical. To handle all important frequency bands of modern cellular systems, the receiver front-end needs to cover frequencies ranging from 700 MHz to 3.7 GHz [1]. Further adding to the problem, in some frequency bands the downlink is located at three times the frequency of another band, causing problems with the third harmonics down-conversion. Due to the square wave signals of the mixer, both bands will be down-converted to baseband. The problem can occur between e.g. band 20 (791-821 MHz) and the 2.4-2.5 GHz ISM-band where interference from the ISM band is down-converted to baseband. It is thus important to suppress the 3rd order harmonic down-converted harmonic. In this system the third order harmonic, which is the most critical harmonic to remove, is rejected by a current mode six phase harmonic rejection mixer, using either 16.7 % or 33.4 % duty cycle signals, which uses less power and less area compared to a conversational 8-phase system.

Voltage mode front-ends [2] have been published that use the bilateral property of the passive mixer to translate a low-pass impedance at the mixer output into a high Q bandpass impedance at the mixer input, centred at the LO-frequency. This can suppress out of band signals by approximately 15 dB, but since the LNA is operating in voltage mode the output node will still have a significant voltage swing. Because of the limitation with voltage mode front-ends, in this work we use a current mode low noise transconductance amplifier (LNTA), combined with a passive mixer, followed by a transimpedance amplifier (TIA) with a low input impedance. This will force the voltage swing at the output of the LNTA to a low level, and thereby its linearity will be increased [3, 4]. Since the voltage swing of the passive mixer will also be small due to the low impedance termination, i.e. it will operate in current-mode, its linearity is also improved.

II Receiver Front End Design

The proposed receiver front-end is seen in Fig. 1. It consists of an LNTA, followed by three passive mixers using a six phase LO-signal, connected to three TIAs. A combination stage is finally used to sum the outputs of the TIAs so that third order harmonic down-conversion is rejected, and a quadrature output is created to interface conventional baseband circuitry.

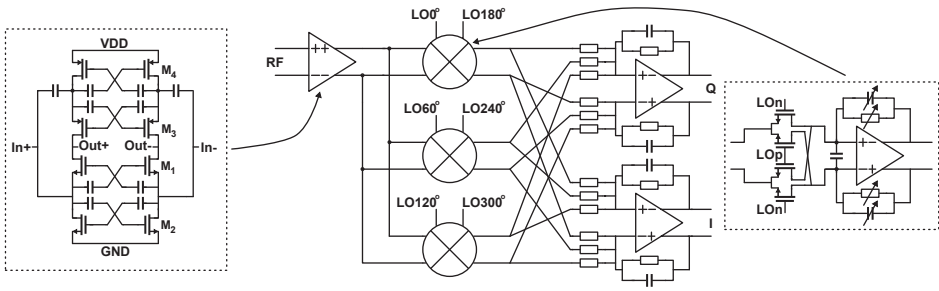


Fig. 1: Architecture of the receiver front-end, using three mixers to reject third order harmonic down-conversion and a schematic of the LNTA.

A LNTA

A major issue when using nanometer CMOS technologies is the low voltage headroom. This is the key reason for using an LNTA instead of a voltage mode LNA. When it comes to input matched amplifier topologies, largely the same options are available for an LNTA as for a voltage mode LNA.

The common gate (CG) amplifier has the advantage of a simple input match, where the input impedance is ideally equal to the inverse of the transconductance g_m. The input match can also be very wideband and provide simultaneous matching for all the frequency bands of interest. Additionally, the CG stage provides good isolation from drain to source, reducing LO leakage from mixer to antenna. The main disadvantage is the relatively high noise figure, typically exceeding 3 dB. One way to reduce noise is to use cross-coupled capacitors, connecting the inputs to the gates of the opposite side input transistors in a differential CG stage [5] effectively doubling the transconductance. Since the effective transconductance is twice as high, the transconductance of the devices can be halved, producing less noise.

In this design a complementary CG stage is used, consisting of both NMOS and PMOS devices, see Fig. 1. The use of both NMOS and PMOS devices increases the large signal linearity due to the complementary structure and also increases power efficiency due to the current reuse and eliminates the need of separate load devices. Both stages use cross-coupled capacitors to improve noise performance. The transistors acting as current sources, at the source terminals of the input devices, are also cross-coupled, improving both linearity and noise figure [6]. The simulated noise figure of the LNTA is 2–2.5 dB. The effective input impedance can be approximated using (1) and in this work, all g_m are equal.

$$Z_{in} = \frac{1}{2g_{m_{M1}} - g_{m_{M2}} + 2g_{m_{M3}} - g_{m_{M4}}} \tag{1}$$

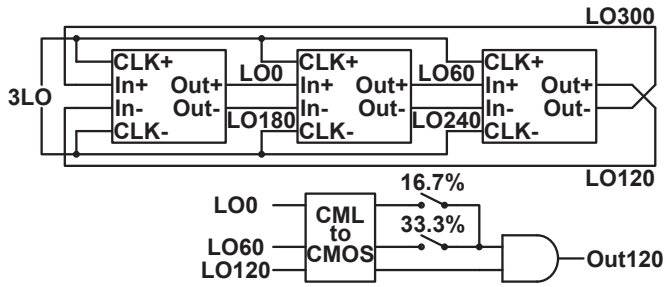


Fig. 2: Schematic of LO divider, generating the six 16.7 % or 33.3 % duty cycle signals that control the three passive mixers.

B Mixer and LO-Generation

In a current mode system there is still reason to put a pole after a passive mixer, since due to the limited loop gain of the TIA its input impedance increases with frequencies, increasing the voltage swing at the input. If a pole (shunt capacitor) is inserted, the impedance seen by the LNA and mixer will still be low also for high offset frequencies, enabling a high out-of-band linearity. Three passive mixers are implemented with NMOS transistors due to the smaller capacitive load for the same on resistance, compared to PMOS devices, and are controlled by either 16.7 % or 33.3 % duty cycle LO signals. The on-chip LO generation circuitry is clocked by a differential external signal at three times the desired LO frequency. These signals are divided by three double-edge triggered D flip-flops, implemented in current mode logic (CML) to achieve low phase noise. The output signals of the divider are six 50 % duty cycle LO signals, phase shifted by 60° with respect to one another. These are fed to a CML-to-CMOS logic level converter, and then CMOS logic is used to generate either 16.7 % or 33.3 % duty cycle signals, see Fig. 2.

III Harmonic Rejection

A major problem in wideband systems is LO harmonic down-conversion. Since the signals controlling the mixer are square waves to maximize linearity, gain and noise performance, interference at odd harmonics of the LO signal will be down-converted to baseband. Receiver architectures able to suppress 3rd and 5th order harmonic down-conversion have been published [7], but for cellular applications the 5th harmonic is typically outside the frequency range of the system, whereas the 3rd harmonic is still a major issue. The 3rd and 5th harmonic can be rejected by using a harmonic rejection mixer, implemented by using an eight phase mixer and four differential TIAs but this will increase power consumption. Not having to suppress the fifth harmonic, the capacitive load of the LO buffers can be reduced and one TIA can be removed by using six phases. A six phase mixer also simplifies the LO divider due to the decrease of

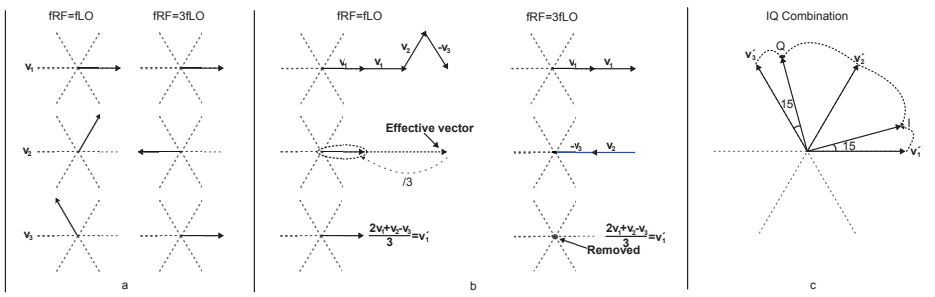


Fig. 3: Vector diagram, illustrating third order cancellation and quadrature generation. a) Three phases at both $fRF = fLO$ and fRF=3fLO b) New coordinate system introduced and shown for v_1', that will not affect $fRF = fLO$, but reject $fRF = 3fLO$ c) Combination to generate I and Q vectors.

dividing factor from 4 to 3. The task of obtaining quadrature signals (I and Q) from the outputs of three TIAs while removing the third order down-converted signal can be divided into two parts. The first part addresses the harmonic rejection. Consider three LO signals that are 60° phase shifted, v_1, v_2 and v_2, see Fig. 3a. When $fRF = 3fLO$ the phase rotation is three times as fast. If a new coordinate system is introduced according to (2) the third order harmonic will be cancelled while the first order is unaffected. This is shown for v_1' in Fig. 3b, where the fundamental vector is constructed by first creating an effective vector, three times as large as v_1 by adding and subtracting, and then diving by three, to make $v_1' = v_1$. When considering the third harmonic down-conversion the resulting vector will be zero and the content is removed.

$$\begin{aligned} v_1' &= (2v_1 + v_2 - v_3)/3 \\ v_2' &= (2v_2 + v_1 + v_3)/3 \\ v_3' &= (2v_3 - v_1 + v_2)/3 \end{aligned} \tag{2}$$

The second part addresses the generation of IQ signals. In order to get a symmetric combination circuit, two new vectors, v_i and v_q, that are 90° phase shifted to one another, are introduced into the coordinate system with an angle of 15° to both v_1' and v_3', see Fig. 3c. These vectors can be constructed by (3).

$$\begin{aligned} v_i &= (1 + \sqrt{3})v_1' + v_2' \\ v_q &= (1 + \sqrt{3})v_3' + v_2' \end{aligned} \tag{3}$$

By solving the equations, the combinations of the signals will be according to (4) and (5).

$$v_i = 1/\sqrt{3}((\sqrt{3} + 2)v_1 + (\sqrt{3} + 1)v_2 - v_3) \tag{4}$$

$$v_q = 1/\sqrt{3}(-v_1 + (\sqrt{3} + 1)v_2 + (\sqrt{3} + 2)v_3) \tag{5}$$

A Fourier series analysis of the effective LO-signals, resulting from (4), (5), can also be calculated (6), (7) to prove the harmonic rejection.

$$f(t+nT) = \frac{1}{\sqrt{3}} \begin{cases} 2+\sqrt{3}, & 0 < t < \frac{T}{6} \\ 1+\sqrt{3}, & \frac{T}{6} < t < \frac{T}{3} \\ -1, & \frac{T}{3} < t < \frac{T}{2} \\ -2-\sqrt{3}, & \frac{T}{2} < t < \frac{2T}{3} \\ -1-\sqrt{3}, & \frac{2T}{3} < t < \frac{5T}{6} \\ 1, & \frac{5T}{6} < t < T \end{cases} \tag{6}$$

$$\begin{aligned} f(t) =& \frac{1}{\pi\sqrt{3}} \sum_{k=1}^{\infty} a_k \cos\left(\frac{2\pi k t}{T}\right) + b_k \sin\left(\frac{2\pi k t}{T}\right) \\ a_k =& \frac{1}{k}\left(sin\left(\frac{\pi k}{3}\right) + (2+\sqrt{3})sin\left(\frac{2\pi k}{3}\right) - sin\left(\frac{4\pi k}{3}\right) + \right. \\ & \left. (-2-\sqrt{3})sin\left(\frac{5\pi k}{3}\right)\right) \\ b_k =& \frac{1}{k}\left(-cos\left(\frac{\pi k}{3}\right) + (-2-\sqrt{3})cos\left(\frac{2\pi k}{3}\right) + (-1-\sqrt{3})(-1)^k + \right. \\ & \left. cos\left(\frac{5\pi k}{3}\right) + (2+\sqrt{3})cos\left(\frac{4\pi k}{3}\right) + 1 + \sqrt{3}\right) \end{aligned} \tag{7}$$

As expected, using $k = 3$ in (7) results in a third harmonic coefficient is equal to zero. In the test chip the full signal combination network has not been implemented, but just the second part of implementing quadrature signals. This means that third order harmonic down-converted signals will appear with equal magnitude and phase in I and Q and that harmonic rejection can be accomplished by using an external combiner to subtract the signals. This will give a good approximation of the achievable harmonic rejection and IQ imbalance of a full implementation due to the irrational $\sqrt{3}$ terms in (3). The LO generation circuitry can generate LO signals with either 16.7 % or 33.3 % duty cycles. The 33.3 % signal will cancel the third order harmonic directly in the mixer, since there is no third order harmonic content in a 33 % signal. This can be used if the interference at the third order harmonic is so strong that it might compress the TIAs when using a 16.7 % duty cycle. Due to the overlapping LO-signals when using an LO of 33.3 % the noise figure will, however, be increased.

IV Measurement Results

The receiver front-end has been manufactured in an ST Microelectronics 65-nm CMOS process, see Fig. 4. The total area including pads is 800 μm x 400 μm,

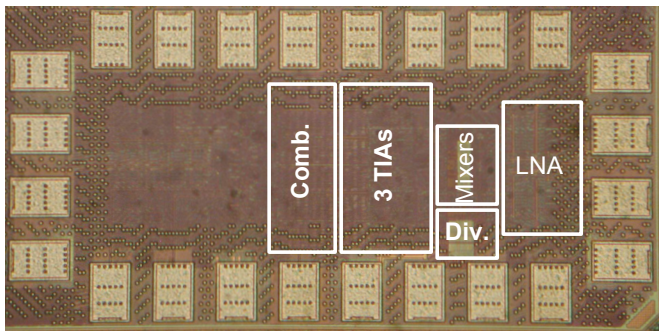


Fig. 4: Photograph of the chip, measuring 800 μm x 400 μm with pads.

Fig. 5: S_{11} of the receiver front end is below -10 dB due to the complementary CG input stage.

while the active area is just 450 μm x 200 μm. The receiver core, including LNA and TIA:s, consumes 7.2 mA from a 1.2 V supply and the LO-generation and buffering consumes between 8 mA and 24 mA, depending on operation frequency.

The silicon dies were wire-bonded to an FR-4-substrate printed circuit board (PCB). The input match (S_{11}) was better than -10 dB from 700 MHz to 3.7 GHz, see Fig. 5. This is due to the wideband input impedance of the complementary CG amplifier.

Gain versus RF, at a fixed baseband frequency of 1 MHz, is shown in Fig. 6, as well as the noise figure. The gain is tunable in 6 dB steps from 22 to

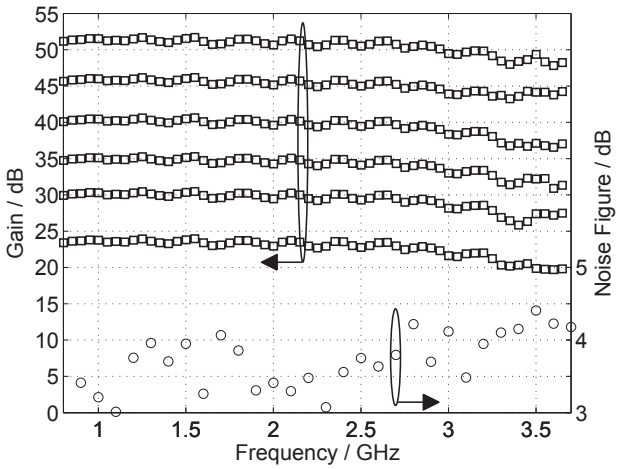


Fig. 6: Gain, with different settings, ranging from 22 to 52 dB and noise figure at maximum gain.

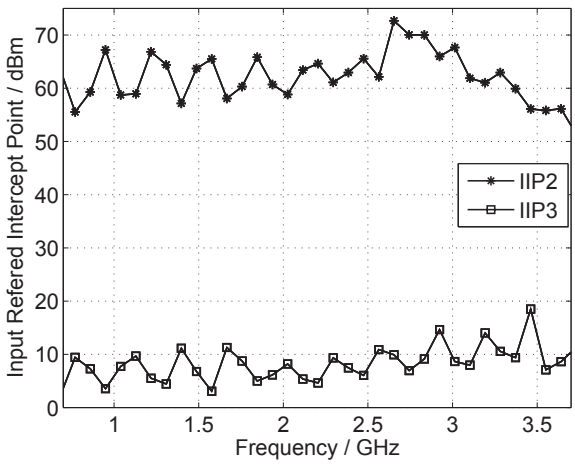


Fig. 7: The IIP3 and IIP2 are above +5 and +55 dBm, respectively.

52 dB, controlled by changing the value of the feedback resistors in the TIAs. The baseband bandwidth can also be tuned, by changing the TIA feedback capacitance. The noise figure is between 3 and 4.5 dB at maximum gain.

The IIP2 is above +55 dBm in the range between 700 MHz and 3 GHz without any calibration, see Fig. 7. This IIP2 was measured with two tones closely spaced at an offset of 50 MHz. IIP3 is above +5 dBm across the entire

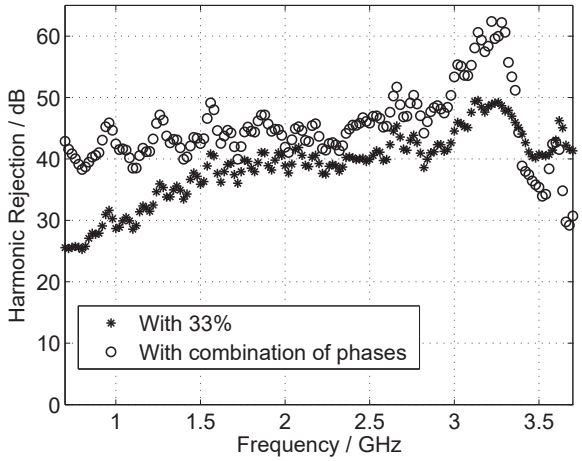


Fig. 8: Harmonic rejection for both 33 % duty cycle LO and combination of the six phases.

frequency range, measured with one tone at 26 MHz offset, and one at 50 MHz offset. Both IIP2 and IIP3 was measured at full gain, and the 3 dB baseband bandwidth of the system was set to 10 MHz.

Third order harmonic rejection is measured by using an external 180°-combiner to subtract the I from the Q signal, see Fig. 8. The harmonic rejection is between 40 and 50 dB up to 3.5 GHz and decreases at higher frequencies, most probably due to imbalance of the baluns used to generate the differential RF and LO signals. For comparison, the harmonic rejection was also measured with the LO divider set to generate LO signals with 33.3 % duty cycle. The LO leakage at the antenna was also measured, and it was below -76 dBm over the entire frequency range. The quadrature accuracy was measured, with a phase error of 1.2° and a gain error of 1.75 %, at 2 GHz. The receiver is compared with recently published receiver front-ends in Table I providing similar performance with lower area and power due to the reduced architecture complexity.

V Conclusion

In this paper we have presented a receiver front-end covering all the LTE bands (700–3700 MHz) with a third order harmonic rejection exceeding 40 dB. The harmonic rejection is accomplished by using six phases, simplifying the system and reducing power compared to an eight phase system. The circuit consumes 18.2 to 37.5 mW from a 1.2 V supply and provides a maximum gain of 52 dB with a noise figure of $3-4.5$ dB. The linearity is high with an out-of-band IIP3 above +5 dBm and a corresponding IIP2 of more than +55 dBm. Additionally,

Table I: Comparison with recently published receiver front-ends.

Parameter	**This work**	**[8]**	**[9]**
Architecture	Current-Mode	Noise Cancelling	Mixer First
Technology / nm	65	40	65
Area / mm^2	0.09	1.1	0.75
Frequency / MHz	700–3700	300–2900	100–2400
Gain / dB	52	58	70
NF / dB	3-4.5	∼2 dB	4±1
Supply Voltage / V	1.2	1.2/1.3/1.5	1.2/2.5
Power Con. / mW	18.2–37.5	49.4–99.8	37–70
IIP2 / dBm	+55	+68	+56
IIP3 / dBm	+5	+12	+25
3'rd Har. Rej. / dB	40	43	35.5

we have presented some analysis of harmonic rejection in a six-phase system.

Acknowledgement

The authors are grateful to ST Microelectronics for donation of silicon for manufacturing. This work is funded by the Swedish Foundation for Strategic Research (SSF).

References

[1] (3GPP TR 36.912 version 9.1.0 Release 9), "Feasibility study for Further Advancements for E-UTRA (LTE-Advanced) ."

[2] J. Borremans *et al.*, "A 40 nm CMOS 0.4-6 GHz receiver resilient to out-of-band blockers," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1659–1671, July 2011.

[3] D. Kaczman *et al.*, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and + 90 dBm IIP2," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 718–739, March 2009.

[4] C.-Y. Yu *et al.*, "A SAW-less GSM/GPRS/EDGE receiver embedded in 65-nm SoC," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 3047–3060, Dec 2011.

[5] W. Zhuo, X. Li, S. Shekhar, S. Embabi, J. de Gyvez, D. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 52, pp. 875–879, Dec 2005.

[6] J. Yoon, H. Seo, I. Choi, and B. Kim, "Wideband LNA using a negative gm cell for improvement of linearity and noise figure," *Journal of Electromagnetic Waves and Applications*, vol. 24, no. 5-6, pp. 619–630, 2010.

[7] H.-K. Cha, K. Kwon, J. Choi, H.-T. Kim, and K. Lee, "A CMOS wideband RF front-end with mismatch calibrated harmonic rejection mixer for terrestrial digital TV tuner applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, pp. 2143–2151, Aug 2010.

[8] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec 2012.

[9] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2696–2708, Dec 2010.

Paper III

A Noise-Cancelling Receiver Front-End With Frequency Selective Input Matching

Abstract

This paper presents an inductor-less frequency selective input match wireless receiver front-end utilizing noise cancellation, operational from 0.7 to 3.8 GHz. The main path of the receiver consists of a high input impedance transconductance stage where the output is down-converted to baseband by current mode passive mixers, and then amplified to voltage by a transimpedance amplifier. The output voltage is converted into a current and frequency up-converted by a second set of transconductance stage and mixer. This current is then fed back to the input of the main path, reducing the input impedance, providing input match by means of negative feedback. An auxiliary path with digitally controllable gain is also introduced to cancel the noise of the main path while maintaining high linearity. The chip prototype is fabricated in a 65 nm CMOS process and occupies an active area of 0.15 mm^2. It achieves a noise figure between 1.6 dB and 3.2 dB depending on the frequency of operation, and an out-of-band IIP2 and IIP3 better than +75 dBm and +1 dBm, respectively. The chip is supplied by 1.2 V and consumes 22.8–34.9 mA.

Anders Nejdel, Henrik Sjöland, and Markus Törmänen "A Noise-Cancelling Receiver Front-End With Frequency Selective Input Matching," © 2015 IEEE, reprinted from *IEEE Journal of Solid-State Circuits* Vol. 50, No. 5, pp. 1137-1147, 2015.

I Introduction

A modern wireless receiver front-end for cellular applications needs to operate over a wide range of frequencies, ranging from 450 MHz up to 3800 MHz [1]. Thus, traditional techniques, such as the rather narrowband inductively degenerated Common Source (CS) Low Noise Amplifiers (LNA) [2, 3] will become unattractive, since they require a minimum of two inductors per LNA. Even if some of these inductors can be shared between the LNAs [4, 5], by grouping the LNAs into low, mid and high frequency bands, the addition of carrier aggregation will require that several LNAs within the same band are enabled simultaneously, increasing the number of inductors. Furthermore, adding to the problem of increased number of RF inputs, are the requirements for receiver diversity and multiple input multiple output (MIMO) systems, which dramatically increase the number of LNAs needed. The introduction of carrier aggregation will also increase the demand for more flexible RFICs to support different band combinations from different operators. In order to decrease the cost of the growing complexity receiver front-ends, advanced digital nanometer process nodes are nowadays used. However, with these downscaled digital processes the analog performance has decreased, with e.g. a lower intrinsic voltage gain in the active devices and reduced voltage supply headroom.

Due to these aforementioned issues associated with the use of narrowband inductor-based LNAs, there is a need for flexible circuits which can be used over a wide frequency range and adapted for different requirements depending on operating conditions.

In this paper, which is an extended version of [6], we propose a flexible receiver front-end intended for generic FDD or TDD single carrier reception, requiring either an off-chip SAW filter for TDD or duplexer for FDD. The input of the circuit is differential, relying on the off-chip filters to provide balun functionality. The receiver front-end is based on frequency translated feedback [7, 8] from the baseband to obtain a wide frequency range of operation and frequency selective input match. The bandwidth of the input match is limited by the baseband channel bandwidth, but the center frequency can be retuned by changing the LO. The flexibility of the receiver front-end is exemplified in figure 1 where to the left a traditional RFIC intended for four different bands has narrowband receiver front-ends tuned to different bands with matching duplexers. The proposed receiver front-end, shown to the right, is more flexible and can be used not only for the same frequency bands as the traditional RFIC, but also for other customer demands as the receiver paths can be used for different bands by changing duplexers and LO frequencies. By introducing an auxiliary path to this receiver front-end, we present a way of reducing the noise of the main path by means of noise cancellation. Furthermore, the linearity of the receiver front-end is increased by introducing the auxiliary path compared to only using the main path, thus relaxing the noise-linearity trade-off.

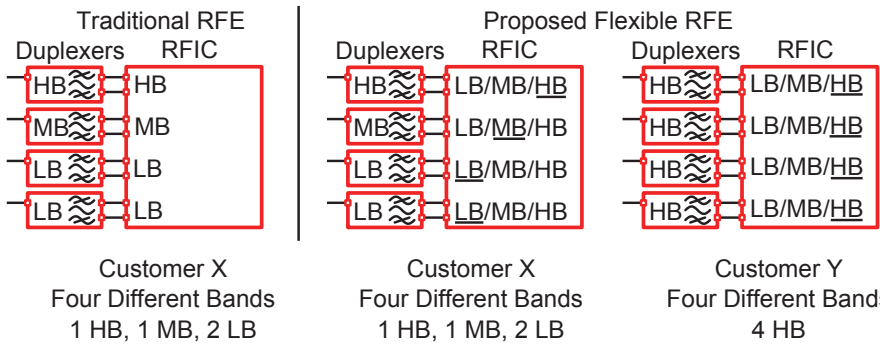


Figure 1: In order to satisfy different customer demands, flexible RFICs are needed.

By employing the auxiliary path flexibility is introduced not only in frequency of operation, but also in noise and linearity versus power consumption. The paper is organized as follows. Section II presents the wideband receiver front-end with frequency translating feedback input match, and Section III explains the noise cancellation. Section IV covers the implementation of the receiver front-end prototype, and experimental results are presented in Section V. Conclusions are given in Section VI.

II Wideband Receiver front-end

For a wideband input matched LNA, two techniques are widely used, the common gate (CG) LNA and the shunt-shunt negative feedback LNA. The input match of the CG LNA sets the transconductance of the input transistor, which also ultimately limits the noise performance [9, 10]. Even if there exist ways to break the noise-input match trade-off [11], the performance of the CG LNA alone is often insufficient to meet high sensitivity requirements in cellular applications without the use of inductors.

The other well-known technique used to provide a wideband input match is the use of shunt-shunt negative feedback [12,13]. The input match is accomplished by using a high input impedance of the first stage of the system, and feeding back a current to the input that is proportional to the output signal and in opposite polarity, i.e. negative feedback. Often the feedback is realized by a resistor between the output and input. If the loop gain of the system is set properly, matching to 50 Ohm can be accomplished. When applied in an LNA, shunt-shunt feedback negative feedback can result in excellent wideband performance and noise figure. However, there is an issue with the shunt-shunt feedback LNA when using it as a low noise transconductance amplifier (LNTA), i.e. when the LNA is connected to low impedance of a current mode passive

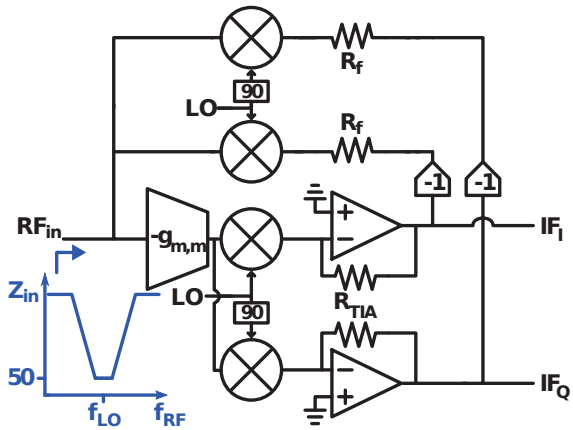


Figure 2: Using global feedback from the baseband, a frequency selective input matching can be obtained at f_{LO}.

mixer feeding a baseband transimpedance amplifier. The reduced LNA output voltage swing that is beneficial for front-end linearity prevents proper function of the feedback, since there is too little voltage signal at the output to convert to current through the feedback resistor. There are ways of solving this by introducing high impedance nodes within the LNA and still using an isolated output node connected to the low impedance mixer [14] [15], however, high impedance nodes can have large voltage swing that can counteract the linearity benefits of using the current mode passive mixer.

In order to solve these issues we propose a direct conversion receiver front-end where the input matching is set by a global feedback from the baseband output to the RF input [6,16,17], see figure 2. While solving the LNA output swing problem, it should be noted that the input matching for out-of-band signals is sacrificed. The input impedance far from f_{LO} is high, approximately equal to the gate input impedance of the g_m cell, and thus the voltage swing is twice as large resulting in an approximate 6 dB increase of LO phase noise requirements at these frequencies, compared to a 50 Ohm wideband input matched receiver front-end. Modelling the receiver front-end with an ideal transconductance stage with transconductance $g_{m,m}$, ideal baseband with transimpedance $Z_{BB,m}$, and mixers with 25% duty cycle yielding a conversion gain of $\frac{\sqrt{2}}{\pi}$, the input matching becomes (1).

$$Z_{in}(\omega_{LO} + \Delta\omega) \approx \frac{\pi}{2\sqrt{2}} \cdot \frac{R_f}{1 + g_{m,m}\frac{\sqrt{2}}{\pi} Z_{BB,m}(\Delta\omega)} \tag{1}$$

The input impedance is thus narrowband but tunable over a wide frequency range by the LO frequency, and by determining the LNTA $g_{m,m}$ and the base-

band transimpedance the value of the feedback resistor can be selected to match the required 50 Ohm to interface to an off-chip antenna interface. The value of the feedback resistor will also set the gain of the receiver front-end according to (2).

$$A_v \approx 1 - \frac{\pi R_f}{2\sqrt{2}Z_s} \approx g_{m,m}\frac{\sqrt{2}}{\pi}R_{TIA,m} \tag{2}$$

The input match dependence of the feedback resistor R_f will set the loop gain of the feedback receiver front-end to approximately unity at f_{LO}, whereas it decreases far from the LO frequency due to poles in the baseband. Thus the feedback will not increase the linearity of the receiver front-end, but is instead intended to match the input to an off-chip interface. The loop will also feed undesired signals back to the input, but the SAW filter or duplexer attenuates the up-converted frequency content present at odd harmonics of the LO frequency if no harmonic rejection mixer is used. Since global feedback is used to set the input match where the first large voltage swing of the feed forward path is at baseband, the RF nodes will have a low voltage swing, enabling high linearity. According to equation (1) the input will only be matched around the LO frequency, while the input impedance is high at large offsets from the LO frequency due to the decreased loop gain. If the baseband transimpedance is changed to adapt the gain for handling different scenarios, i.e. decreased when a strong receive signal is present, the input impedance will be changed. Thus the global feedback resistance R_f should be reprogrammed to restore input matching from the loop. If R_{TIA} is changed, so should R_f be.

A Phase adjustment of frequency translational negative feedback.

When packaging the chip and connecting to external components, the source impedance may deviate from 50 Ohm. If the impedance seen from the external components differs too much from the input impedance of the chip, power is reflected and the sensitivity of the receiver will be decreased. This can be solved in the proposed architecture by tuning the resistance of R_f to change the magnitude of the input matching, and by changing the phase to tune for reactive variations of the source impedance. The phase can be changed either by changing the phase of f_{LO} connected to the feedback mixer with respect to the phase of f_{LO} of the forward down-converting mixer, see figure 3a, or by combining cross-coupled currents from the quadrature outputs to yield a phase rotated baseband current, which is up-converted by the feedback mixer, figure 3b, illustrated by phasors in figure 3c. One of the paths needs to be inverted, which can be accomplished by cross coupling the differential baseband signals. If a negative phase shift is required, another set of resistors can be used for the negative phase rotation. The effect of this phase shift can be seen in figure 4 where a parallel source inductance of $j50$ Ohm at 2 GHz has been added to represent a reactive component in the source. As can be seen in figure 4a,

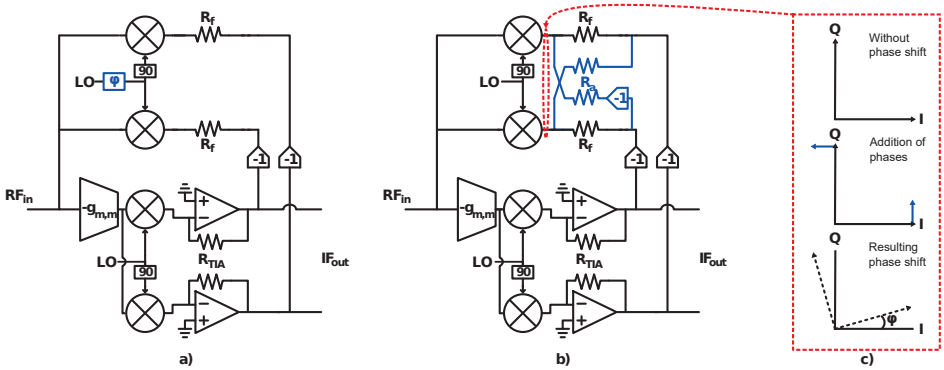


Figure 3: By using a phase shift in the feedback, reactive source components can be matched. This can be accomplished by an LO signal phase shift relative to main path. (a) Phase adjustment by directly introducing a phase shift of f_{LO}. (b) Phase adjustment by scaling resistors in the baseband. (c) Phasors illustrating the resulting phase shift by using baseband signals.

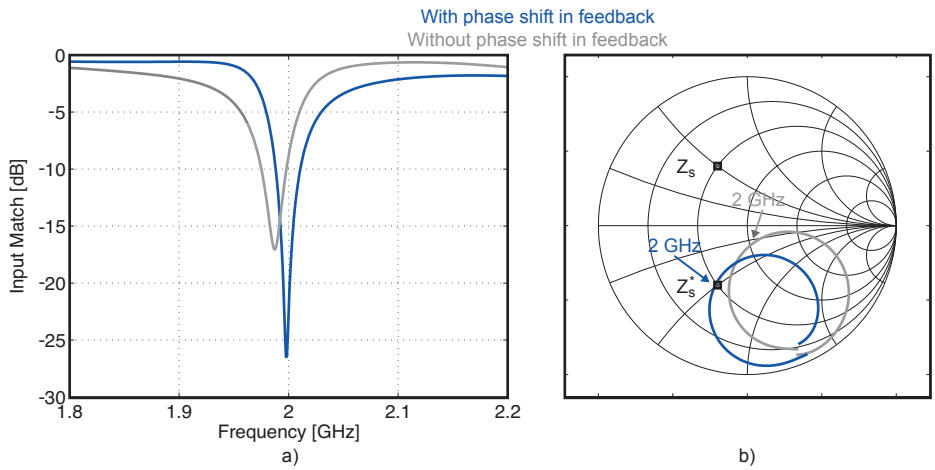


Figure 4: (a) S_{11} input match when the source port has reactive components, with and without phase adjustment. (b) Smith chart for the same conditions.

the minimum S_{11} is slightly below 2 GHz, but by changing the phase of the feedback, simulated in this case to -30 degrees, the input matching can once again be accomplished at f_{LO}. The input impedance of the receiver front-end is simulated and the result is presented in a Smith chart in figure 4b. As seen at 2 GHz, the receiver front-end match the complex conjugate to the source impedance of 50 Ohm shunted by $j50$ Ohm when a phase shift is introduced in the feedback path.

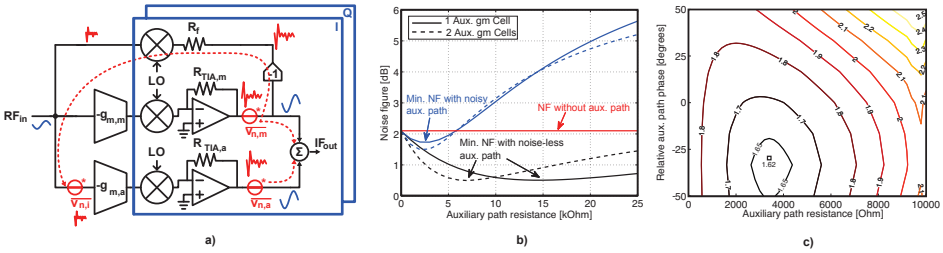


Figure 5: a) Conceptual schematic of the noise cancellation. b) Noise cancellation optimum for noisy and noiseless auxiliary path. c) Noise figure versus gain and phase of auxiliary path with an added source reactance.

Being able to correct for non-ideal input impedance is very attractive allowing the receiver to partly act as an impedance tuner. By the use of global feedback, the resistors controlling the feedback magnitude can be located at the baseband where the associated parasitic capacitance of the switches required for digital control can be neglected. If the resistors were placed at the RF side of the passive up-conversion mixer, careful planning would be needed to reduce the parasitic effects of these switches.

III Noise Cancellation

Several noise cancellation techniques have previously been presented [18, 19]. In this section we will focus on the two most known implementations; the common gate-common source (CG-CS) noise cancelling LNA, and the shunt-shunt feedback noise cancelling LNA. The CG-CS LNA, also known as the active balun LNA, was proposed to reduce the high noise of the CG LNA [18]. By using an auxiliary path composed of a CS amplifying stage, the noise of the CG stage providing the wideband input match can be cancelled. This implementation is of particular use when a voltage mode LNA is used, since the transconductance of the CS stage can then be increased compared to that of the CG stage, while the load resistors are properly scaled to balance the outputs. The noise of the CS stage, which is not cancelled, will then be much lower than of the CG stage. However, for a current mode approach the transconductance of the CG and CS stages must be equal, which limits the benefit of the noise cancellation. The noise-cancelling blocker-tolerant receiver front-end [20] can be derived from the implementation of the active balun noise-cancelling LNA, where the CG stage has been substituted by a passive mixer-first receiver. The passive mixer first solution has a high noise figure, but an excellent linearity [21]. By introducing a CS stage in the form of an inverter-based LNTA, the noise of the passive mixer first receiver can be sensed, amplified and processed. Finally, the outputs are combined and the noise figure can be decreased due

to cancellation. Another way to achieve a noise cancellation LNA is to use a shunt-shunt feedback stage to provide the input match. An auxiliary path is then used to sense and amplify the noise of the input matching stage. The correlated noise at the outputs can then be cancelled by combining the two outputs [19].

In this paper we will focus on the shunt-shunt feedback noise-cancelling LNA and show that its principle can be used to reduce the noise of a shunt-shunt feedback receiver front-end. The main path discussed in Section II is used to provide the wide frequency selective input match and the auxiliary path consists of an inverter-based LNTA, see figure 5a. The noise $\overline{v_{n,m}}$ at the baseband I signal output of the main path is transferred to the RF input of the receiver front-end by the I-channel feedback mixer driven by 25% duty cycle LO signals. The corresponding transfer takes place from the Q-channel baseband signal noise to the RF input. The noise at the input, $\overline{v_{n,i}}$, is sensed by the auxiliary path and amplified to $\overline{v_{n,a}}$. If the amplification of the auxiliary path is set according to (3), the correlated noise is cancelled. The absolute gain of the auxiliary path should thus be approximately equal to that of the main path in equation (2) for optimum noise cancellation of the noise source $\overline{v_{n,m}}$.

$$g_{m,a}\frac{\sqrt{2}}{\pi}R_{TIA,a} \approx 1 + \frac{\pi R_f}{2\sqrt{2}Z_s} \tag{3}$$

Even if the main path noise contribution is minimum when the auxiliary path gain is set according to equation (3) it does not necessarily result in minimum total noise. The reason is that there is noise also in the auxiliary path which will then dominate. Depending on design, the auxiliary path can have even more noise than the main path. This can be seen in figure 5b, where the receiver front-end was simulated, at an LO frequency of 2 GHz, first with a noise-less auxiliary path where the g_m of the LNTA was set to 5.5 mS. The optimum noise figure occurs when the feedback resistance of the auxiliary TIA, $R_{TIA,a}$ is about 15 kOhm. At this setting, the gain of the auxiliary path approximately equals that of the main path. The ideal LNTA is then replaced by an inverter-based LNTA with the same transconductance. The TIA feedback resistance yielding optimum noise figure is now lower. At higher $R_{TIA,a}$ settings, the noise from the auxiliary path dominates, which degrades the total noise figure. If the transconductance is increased by a factor of two, i.e. to 11 mS, the minimum noise figure for the noise-less auxiliary path occurs at a TIA gain that is half compared to the previous case, as predicted by equation (3). For the noisy LNTA case, the minimum noise figure occurs at almost the same $R_{TIA,a}$ setting, but the noise figure is decreased. It should be noted that even if the auxiliary path was noiseless, the minimum noise figure could still not reach 0 dB, due to noise sources such as the global feedback resistor, summation amplifiers, and due to harmonic noise folding.

It should be noted that the transfer function of the noise to the input

depends on the source impedance Z_s. Due to parasitic effects, such as bond wires and PCB traces, the impedance will not be completely resistive. This will introduce a phase difference between the main and auxiliary path, which should be corrected to obtain the optimum noise cancellation. The unwanted phase shift can be neutralized in two different ways, either a phase shift is applied to the LO signal of the auxiliary path mixer or corrections can be made in the summation stage of the quadrature baseband signals to realize a phase rotation. The latter alternative has the advantage of being easily controlled by programming resistors [22] with digital switches, while the former technique can affect the phase noise performance of the LO. The effect of changing the phase and gain of the auxiliary path is illustrated in figure 5c, simulated at 2 GHz. In this figure, a parallel source inductance, corresponding to $j50$ Ohm has been added to represent a source reactance. Just as in Section II where the same impedance was added to show the effect on the input match, the optimum noise figure is at a phase shift of -30 degrees.

Having to control both magnitude and phase it is difficult to optimize noise cancellation in a noise-cancelling LNA, but it is feasible in a noise-cancelling receiver front-end due to the access of the baseband representation of the signal. In the prototype we have implemented the magnitude control for optimizing noise cancellation of the main path. This can be done by varying two different settings, namely the $g_{m,a}$ of the auxiliary path and the gain of the auxiliary TIA, $R_{TIA,a}$. The noise could also be decreased by increasing the transconductance of the main path, however, increasing the gain of the main path also decreases the linearity. By introducing the auxiliary path, the linearity is maintained or even increased, while the noise is reduced, thus relaxing the linearity-noise trade-off. This is accomplished while the input match is minimally affected, only the extra capacitance of the auxiliary LNTA cells will slightly degrade the input match, and as has been shown in Section II, this can be tuned by changing the phase of the global feedback.

IV Circuit Implementation

The proposed quadrature receiver front-end circuit uses inverter-based LNTA cells in both the main and auxiliary path, see figure 6. The benefits of using inverter-based LNTA cells are easy implementation of digital control and compact layout. The width ratio of the PMOS/NMOS transistors is designed to set a common mode level which approximately equals VDD/2 when self-biasing is employed. To be able to digitally turn on and off different LNTA cells, a large PMOS transistor acts as a low voltage drop switch between each LNTA cell and supply. Transmission gates are used at the output of each LNTA cell in order to be able to isolate disabled cells from enabled ones. In the main path, five equally sized LNTA cells are used. The output of the LNTA bank is connected to the two quadrature paths. In the implemented prototype, the

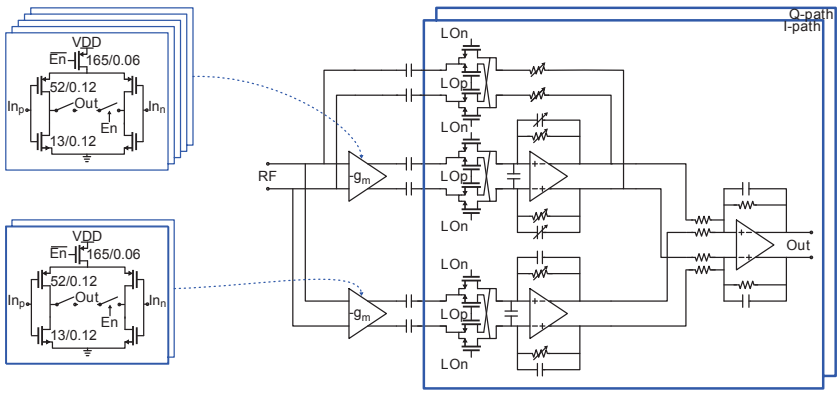


Figure 6: Schematic of the noise-cancelling shunt-shunt feedback receiver front-end. Each LNTA bank consists of inverter-based amplifier cells.

RF input is fully differential and thus the LNTA cells are pseudo-differential to enable a high second order linearity of the front-end. In order to reduce the thermal noise coefficient of the LNTA, decrease noise and improve matching, the channel length of these transistors was chosen to $2L_{min}$, and the g_m of each LNTA cell is 13 mS. The LNTA banks are self-biased by large resistors, setting the common mode level at the LNTA input and output. The amplified RF signal current from the LNTA, AC coupled to support self-biasing and to remove the low frequency components due to finite IIP2 of the LNTA, is down-converted by a double balanced passive mixer, with switch device sizes of 20/0.1 μm, driven by 25% duty cycle LO signals with baseband signals biased a common mode level of 600 mV. By the use of non-minimum switch device length, the mismatch of the mixer transistors is reduced, which is beneficial for cancellation of even order non-linearity. In order to terminate the LNTA with low impedance, a TIA based on an OPAMP, with R_{TIA}=8 kΩ and C_{TIA}=1 pF is used at the mixer output with a fixed pole at 20 MHz. The output of the TIAs are then converted into current through a digitally controllable resistor and the current is further up-converted by a double balanced passive mixer, with transistor sizes of 5/0.1 μm, and fed to the RF input to set the input impedance. The negative unity gain before the resistor indicated in figure 5 is implemented by cross-coupling the differential signals. By placing the programmable feedback resistor at the baseband instead of at the RF side [16] of the up-conversion mixer, the effect of the parasitic capacitance associated with the digital switches is minimized. Furthermore, due to the large ratio between the feedback resistor R_f and the source impedance Z_s, the voltage swing across the feedback mixer is reduced and the mixer will operate more in current mode than in voltage mode. Since the feedback is connected to the input of the receiver front-end, the LO leakage of this mixer will dominate the

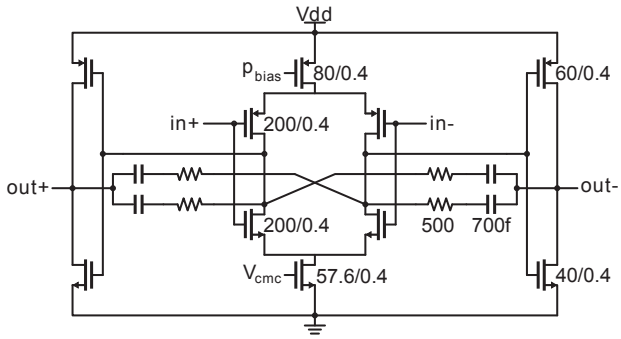


Figure 7: OPAMP with complementary input stage, push-pull output stage and the use of phase enhanced compensation technique.

total LO leakage. The LO leakage can, however, be reduced by minimizing the size of the mixer, and by using careful layout to ensure symmetry and matching or by digital calibration [23, 24]. The use of LNTA cells isolates main path and auxiliary path mixers from the RF input and thus reduce LO leakage

The auxiliary path uses two controllable LNTA cells with the same structure and size as those used in the main path. Passive mixers are used also in the auxiliary path, with transistor size of 10/0.1 μm, and the TIA has digitally programmable feedback resistance of about 4 kΩ, in order to control the gain of the auxiliary path to optimize noise cancellation.

The outputs of the different paths are combined in a summation stage with unity gain and a bandwidth of 15 MHz, which uses the same OPAMP design as in the TIAs of the main and auxiliary paths. The schematic of the OPAMP, omitting the common mode feedback amplifier, is shown in figure 7. In order to reduce the noise for a given current, the input stage is complementary, and the input is biased at a common mode level of VDD/2. The impact of flicker noise is reduced by the use of long channel input transistors. The output is amplified by a second stage, a class AB complementary output stage, in order to increase the gain and output swing of the OPAMP. The OPAMP is compensated using the phase enhanced compensation technique which achieves a higher GBWP, and 3 dB bandwidth, with maintained stability, for an equal current consumption compared to traditional Miller compensation [25]. For the main path TIA, the unity gain frequency of the loop gain was simulated to 320 MHz, with a phase margin of 70 degrees and a low frequency loop gain of 30 dB. In order to prevent common-mode latch-up, transistors biased in sub-threshold are added in parallel with the input transistors. Together with the common mode feedback, these transistors force the common mode to 600 mV at the input of the OPAMP, and thus also at the input and output of the mixer. The quiescent point of the OPAMPs is set by an off-chip 100 μA current source.

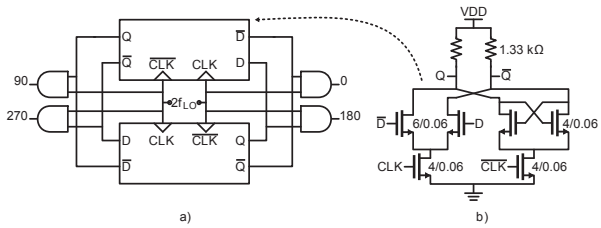


Figure 8: CML divider and CMOS AND gates used for quadrature LO signal generation.

Current Mode Logic (CML) based dividers are used to generate quadrature LO signals to the passive mixers, see figure 8. The outputs of the CML divider are combined with the $2f_{LO}$ input signals in AND gates to generate 25% duty cycle LO signals. By combining the divider input and outputs, the phase noise is lower, compared to combining only the outputs for quadrature generation [26]. With proper timing between divider input and output, both the positive and negative flanks of the 25% duty cycle output signal are determined by the $2f_{LO}$ rather than the divide-by-2 output and thus the noise contribution of the divide-by-2 cell is reduced. This is achieved by using inverters to delay the the outputs of the divide-by-2 cell and ensure non-overlapping LO signals of 25% duty cycle. The simulated LO phase noise was below -165dBc/Hz for offsets larger than 10 MHz from a 2.25 GHz carrier, which is low enough to not desensitize the receiver front-end due to reciprocal mixing. The out-of-band phase noise requirements are 6 dB more stringent than for a traditional receiver front-end, due to the increased out-of-band input impedance. All three passive mixers, feed forward, feedback and auxiliary path, use the same LO signals and no controllable phase shift was implemented in the prototype.

V Experimental Results

The prototype chip, manufactured in a standard 65 nm CMOS process, see figure 9, was wirebonded to an FR-4 substrate for measurement purposes. The dimensions of the chip including bond pads is 0.52 mm by 0.73 mm, with an active area of 0.15 mm^2. All external component losses, including the wideband baluns used at the RF input (Marki BAL-0006 used for linearity measurements and Krytar 4005040 used for noise measurements), have been de-embedded. An off-chip wideband video amplifier (AD830) with unity gain was used to drive the 50 Ohm measurement equipment (R&S FSEB). The system was controlled through a USB to SPI device (NI USB-6008) to enable global digital control with MATLAB^{TM} on a computer. The chip was supplied by 1.2 V in all measurements. Each LNTA cell, used both in the main and auxiliary receiver,

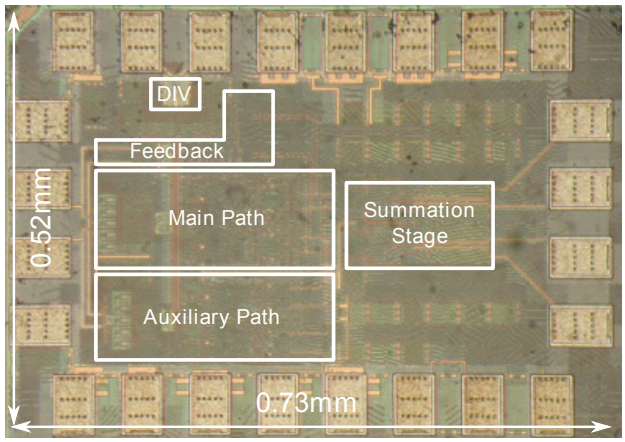


Figure 9: Chip photo. The circuit measures 0.730 mm times 0.520 mm including padframe and has an active area of 0.15mm^2.

consumes 1.4 mA. The measured DC voltage at the chip output, set by the common mode reference voltage, is 600 mV. Each of the total six OPAMPs used consumes 1.2 mA. The receiver front-end thus consumes a static current of between 6.2 mA, when only one LNTA cell in the main path is used and 17 mA when all LNTA cells in the main and auxiliary path are enabled. The quadrature LO divider and buffering for the passive mixers consume between 10 and 22 mA depending on operation frequency, see figure 10a, and are functional from 700 MHz to 4000 MHz output frequency. In this figure, the simulated current consumption is also presented, and it agrees well with measurements.

In the following measurements the receiver front-end was configured with three out of five LNTA cells enabled in the main path, and one of two LNTA cells enabled in the auxiliary path, to represent a trade-off between minimum noise and maximum linearity, as will be shown below. This setting results in a current consumption of 22.8 mA at 700 MHz, and 34.9 mA at 3.8 GHz LO frequency. The measurements were performed by sweeping the LO frequency while programming the global feedback resistor for each frequency to find a minimum and maximum setting, programming word, such that the input matching below -10 dB was achieved. The saved resistor programming word was then used to find the optimum noise figure and the corresponding input match, shown in figure 10b, is below -10 dB. The noise figure, see figure 10c, was measured by changing the programming word for the transimpedance gain of the auxiliary path until optimum noise performance was obtained. It should be noted that this optimization will not change the input match due to the isolation of the auxiliary path LNTA cells. Depending on operation frequency, the noise figure is between 1.6 and 3.2 dB, but less than 2 dB up to 2.5 GHz.

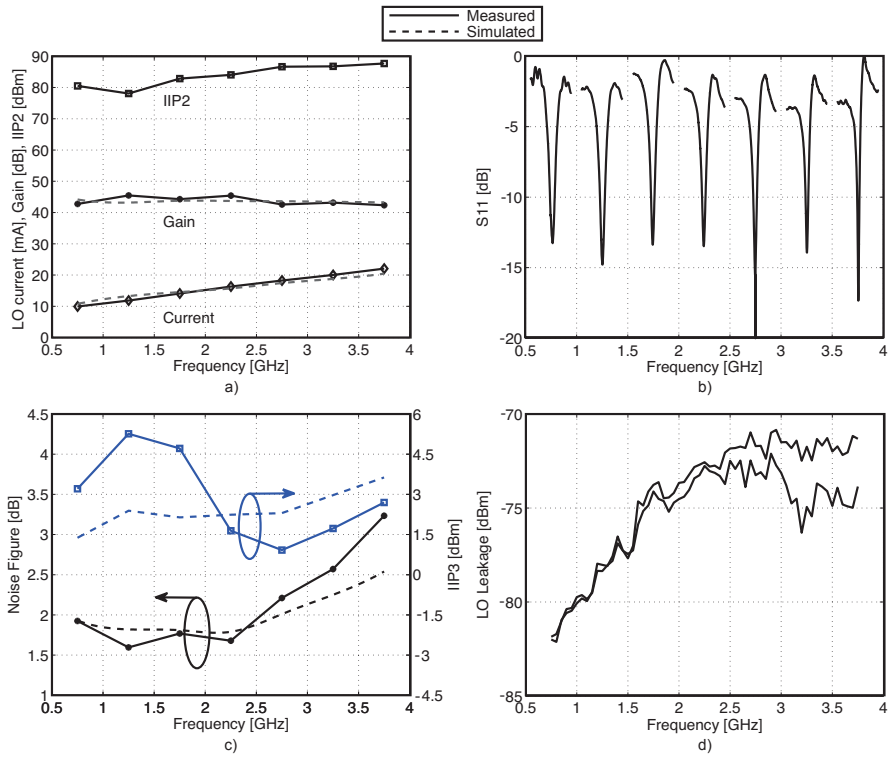


Figure 10: Measured performance versus operating frequency. (a) IIP2, Gain and LO Current. (b) Input match. (c) IIP3 and noise figure. (d) LO leakage.

Due to the wideband nature of the LNTA cells and non-presence of harmonic rejection techniques, this also includes down-conversion of noise from odd LO harmonics, and the noise figure could thus be further reduced by introducing harmonic rejection [27]. The increased noise figure above 2.5 GHz is due to reduced gain from the LNTA cells, and to a larger degree due to the parasitics at the LNTA input altering the phase and preventing optimum noise cancellation. By optimizing the phase both of the feedback and the auxiliary path as described previously, the noise figure can be decreased at higher frequencies. The simulated noise figure is also presented in figure 10c where the simulated noise figure was about 0.5 dB lower at high frequencies.

The conversion gain at a baseband frequency of 1 MHz, shown in figure 10a, exceeds 40 dB for the entire frequency range and agrees well with simulations. The third order intercept point (IIP3) was measured by applying two tones at f_1=f_{LO}+50.5 MHz and f_1=f_{LO}+100 MHz, resulting in a baseband IM3 component at 1 MHz. The IIP3, figure 10c, was then extracted to between +1 and +5 dBm, depending on operating frequency. Simulated IIP3 is

also presented and corresponds well with measurements, however, with slightly lower measured than simulated IIP3 at high LO frequencies. Similarly, the second order linearity was measured by using two tones at f_1=f_{LO}+99 MHz and f_2=f_{LO}+100 MHz, resulting in an IM2 component at 1 MHz. The IIP2 for two samples was measured and the minimum IIP2, figure 10a, exceeds +78 dBm for all operation frequencies.

Furthermore, the LO leakage at the RF port was measured to be below -70 dBm for two samples, figure 10d. There are three main problems that can occur due to this high level of LO leakage: DC self-mixing, cross-modulation with TX signal and exceeding the allowed spurious emission level. The receiver front end is intended to be used in a system where the DC sub-carrier is removed, and thus the problem of DC self-mixing is mitigated. Assuming a 20 MHz RF bandwidth and a standard 50 dB isolation duplexer, the transmission signal will be on average -25 dBm at the RX input, for a +25 dBm TX. This together with the measured IIP3 gives a cross modulation product [28] of -110 dBm, well below the noise floor of the receiver. Finally, modern cellular standards [1] require spurious emission in the RX band to be below -57 dBm for the low frequency bands, and -47 dBm for the high frequency bands which is higher than the measured LO leakage. To conclude, the LO leakage is high, but still acceptable with some margin. The quadrature accuracy was measured at 1 MHz baseband frequency with an oscilloscope (Tektronix TDS7404) for three samples. Gain and amplitude mismatch was extracted from the sampled data and the calculated image rejection is presented in figure 11 with a minimum IRR of 36 dB at the highest LO frequency.

By digitally changing the setting of the receiver front-end, the performance can be selected to be either low noise or low power, depending on the current system requirements, while maintaining input matching. This flexibility of the digital programming is illustrated in figure 12 for an LO frequency of 2.25 GHz, in the middle of the receiver's operation range. In the figure different regions with the same total current consumption of the LNTA cells are indicated, where each box represents an LNTA cell, enabled in either the main or auxiliary path. Within such a region the noise figure is in some cases lower by using less current in the main path and enabling the auxiliary path, compared to using all the current in the main path. Interestingly, the IIP3 is always larger with the auxiliary path enabled, thus relaxing the trade-off between low noise and high linearity. If a noise figure of 3.7 dB, at 2.25 GHz, can be accepted, the receiver front-end can be configured to a low power mode where the IIP3 is +6 dBm. Similarly if a low noise figure is required, the receiver front-end can be programmed to reach a noise figure of 1.2 dB with an IIP3 of -2 dBm.

Similarly, the maximum and minimum noise figure, IIP3, and gain versus the LO frequency are presented in figure 13. In the low power mode one LNTA is used in the main path and one in the auxiliary path, whereas in the low noise mode five LNTA cells are used in the main path and two cells in the

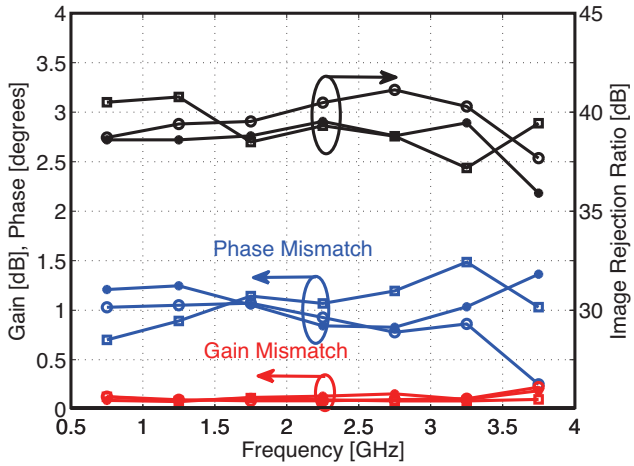


Figure 11: Gain mismatch, phase mismatch and image rejection ratio for three samples at 1 MHz baseband frequency versus LO frequency.

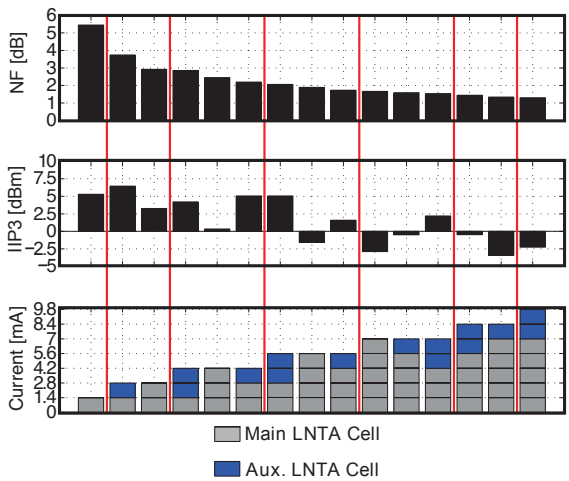


Figure 12: Noise figure and IIP3 versus different combinations of LNTA cells in the main and auxiliary paths at 2.25 GHz.

auxiliary path. The minimum achieved noise figure is 1.1 dB at 1.75 GHz with a corresponding IIP3 of 0 dBm. Also visible in this figure is the increased noise figure at higher LO frequencies.

Measurements of IIP2, 1 dB compression point and IIP2 versus the upper LO tone offset is presented in figure 14 where the receiver was programmed

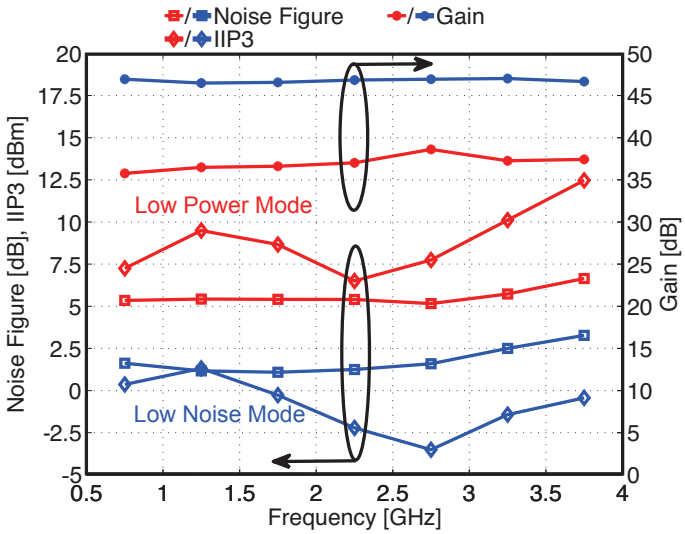


Figure 13: Maximum and minimum noise figure, IIP3 and gain versus LO frequency.

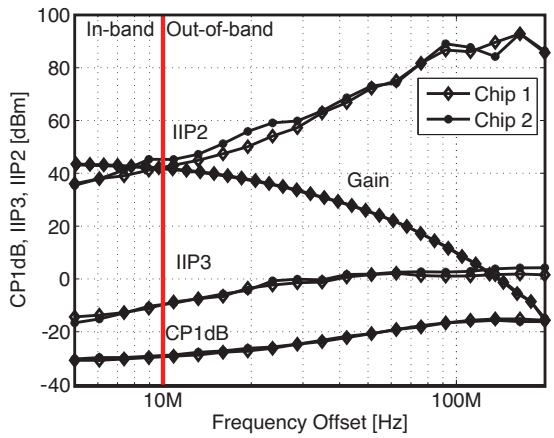


Figure 14: IIP2 and IIP3 versus two tone baseband output frequency at 2.25 GHz LO. For IIP3 the frequency is that of the upper tone. 1dB compression point and gain versus the baseband frequency is also presented.

for 10 MHz signal bandwidth. The settings of the receiver front-end were the same in this measurement as for figure 10, three LNTA cells in the main path were active and one in the auxiliary path. The frequencies were chosen to obtain the resulting output IM2 and IM3 components were in-band at 1 MHz,

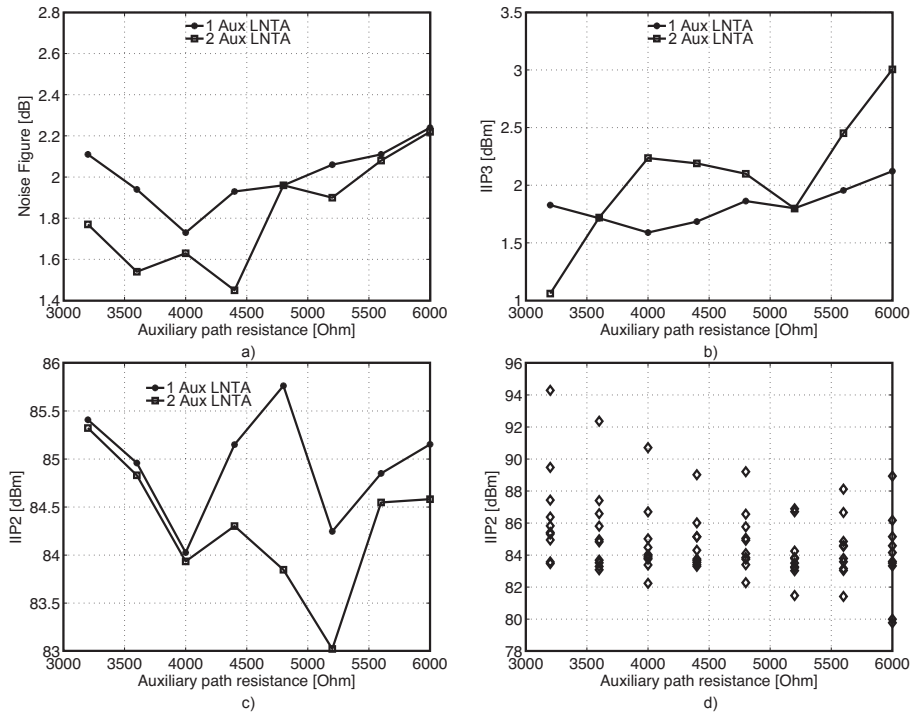


Figure 15: Measurements versus auxiliary path transimpedance at 2.25 GHz LO. (a) Noise figure (b) IIP3. (c) IIP2. (d) IIP2 for all LNTA cell combinations.

and the corresponding IIP2 and IIP3 versus tone frequency is then calculated. Close to the LO frequency, at low baseband frequencies, the gain of the TIAs is high. They will thus determine the IIP3 and compression at these frequencies. The high loop gain of the TIAs at low frequencies will help maintain a high performance but cannot fully compensate for the effect of increased gain on the linearity. Further away from the LO, where the baseband filtering attenuates the signal, the compression and linearity is instead set by the RF parts of the circuit.

The effect of the auxiliary path gain on the noise figure, IIP3 and IIP2 at 2.25 GHz is shown in figure 15, with three LNTA cells enabled in the main path. As can be seen the auxiliary path gain has a significant effect on the noise figure. In figure 15d, the IIP2 at 2.25 GHz for all cases of the five main path LNTA cells and two auxiliy path LNTAs is presented, with the IIP2 always above +80 dBm.

Finally, the performance of the receiver front-end is summarized and compared with published state-of-the-art wideband inductor-less receiver front-ends

Table I: Comparison with previously published inductor-less receiver front-ends.

	JSSC'12 [20]	ISSCC'11 [16]	JSSC'14 [17]	**This Work**
Type	Noise Cancelling	Resistive Feedback	Sampling	**Noise Cancelling**
Freq. / GHz	0.01–2.7	0.7-2.1	0.5–3	**0.7-3.8**
Input type	Single-Ended	Single-Ended	Differential	**Differential**
NF / dB	1.9	2.2-2.7	5.5–8.8	**1.6-3.2**
Gain / dB	70	37	35	**42**
Current / mA	35.1–78**	7.3*	208–500**,†	**22.8–34.9**
Supply / V	1.3	1.3	1.2	**1.2**
IIP3 / dBm	+13.5	-3.5	+11.7	**+1**
IIP2 / dBm	>54	>40	>58	**>75**
Area / mm^2	1.2	0.2	5.9#	**0.15**
Process / nm	40	45	65	**65**

*Excl. Quadrature LO generation and mixer buffering.
**Incl. Harmonic Rejection. † Incl. Freq. Synthesizer.
Incl. Pads

in table I. This work provides an attractive combination of low area, low noise figure, and high linearity while having a large upper frequency of operation. The settings used in the comparison were three LNTA cells active in the main path and one in the auxiliary. It should be noted that lower noise or higher linearity can be achieved by other settings if required, but this reported setting represents a good performance trade-off. By introducing the auxiliary path to offload the main path, the achieved IIP3 is higher and the noise figure lower than in [16]. Compared to [8], the noise figure is lower for the same frequencies and the differential input yields higher second order linearity.

VI Conclusion

We have presented a receiver front-end based on global shunt feedback to realize a wideband frequency selective input match, and introduced an auxiliary path to cancel noise from the main path. By introducing the auxiliary path, the linearity of the receiver front-end can be increased for a fixed noise figure, compared to only using the main path. By using shunt feedback, no inductors are required in the receiver front-end and thus the occupied chip area is small while the circuit can operate over a wide frequency range. Even if the large signal handling of the proposed technique is not enough to support operation without a SAW-filter or duplexer, the number of off-chip components can be reduced due to the absence of gate inductors. The demonstrated chip achieves

low noise figure, chip area, and power consumption.

Acknowledgement

This work was supported by the Digitally Assisted Radio Evolution (DARE) project, funded by the Swedish Foundation for Strategic Research (SSF). The authors would like to thank STMicroelectronics for silicon manufacturing.

References

[1] 3GPP TS 36.101 V11.6.0 (2013-09), "User Equipment (UE) radio transmission and reception (Release 11)."

[2] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[3] P. Andreani and H. Sjöland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Transactions Circuits Systems II, Analog and Digital Signal Processing*, vol. 48, pp. 835–841, Sep 2001.

[4] M. Nilsson *et al.*, "A 9-band WCDMA/EDGE transceiver supporting HSPA evolution," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2011, pp. 366–368.

[5] T. Sowlati *et al.*, "Single-chip multiband WCDMA/HSDPA/HSUPA/EGPRS transceiver with diversity receiver and 3G DigRF interface without SAW filters in transmitter / 3G receiver paths," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 116–117,117a.

[6] A. Nejdel, M. Törmänen, and H. Sjöland, "A noise cancelling 0.7-3.8 GHz resistive feedback receiver front-end in 65 nm CMOS," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 35–38.

[7] L. Franks and I. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *The Bell System Technical Journal*, vol. 39, pp. 1321–1350, Sept 1960.

[8] A. Mirzaei *et al.*, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 950–964, April 2011.

[9] A. Rofougaran, J.-C. Chang, M. Rofougaran, and A. Abidi, "A 1 GHz CMOS RF front-end ic for a direct-conversion wireless receiver," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 880–889, Jul 1996.

[10] W. Zhuo *et al.*, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 52, pp. 875–879, Dec 2005.

[11] A. Liscidini, G. Martini, D. Mastantuono, and R. Castello, "Analysis and design of configurable LNAs in feedback common-gate topologies," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 55, pp. 733–737, Aug 2008.

[12] J.-H. Zhan and S. Taylor, "A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2006, pp. 721–730.

[13] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2422–2433, Nov 2008.

[14] C. G. Tan *et al.*, "A universal GNSS (GPS/galileo/glonass/beidou) SoC with a 0.25mm2 radio in 40nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2013, pp. 334–335.

[15] M.-D. Tsai *et al.*, "A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 354–355.

[16] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2011, pp. 372–374.

[17] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1097–1111, May 2014.

[18] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1341–1350, June 2008.

[19] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 275–282, Feb 2004.

[20] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec 2012.

[21] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2696–2708, Dec 2010.

[22] D. Murphy, M. Mikhemar, A. Mirzaei, and H. Darabi, "Advances in the design of wideband receivers," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 2013, pp. 1–8.

[23] S. Jayasuriya, D. Yang, and A. Molnar, "A baseband technique for automated LO leakage suppression achieving <; -80dBm in wideband passive mixer-first receivers," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 2014, pp. 1–4.

[24] Y. Shuhei, O. Boric-Lubecke, and V. Lubecke, "Cancellation techniques for LO leakage and dc offset in direct conversion systems," in *Proceedings of IEEE International Microwave Symposium*, 2008, pp. 1191–1194.

[25] M. Abdulaziz, M. Törmänen, and H. Sjöland, "A compensation technique for two-stage differential OTAs," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 61, pp. 594–598, Aug 2014.

[26] X. He and J. van Sinderen, "A low-power, low-EVM, SAW-less WCDMA transmitter using direct quadrature voltage modulation," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3448–3458, Dec 2009.

[27] J. Weldon *et al.*, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 2003–2015, Dec 2001.

[28] C. W. Liu and M. Damgaard, ""IP2 and IP3 nonlinearity specifications for 3G/WCDMA receivers," *High Frequency Electronics*, vol. 8, pp. 16–29, June 2009.

Paper IV

A Positive Feedback Passive Mixer-First Receiver Front-End

Abstract

This paper presents a technique to reduce the noise figure of a passive mixer-first receiver front-end. By using lower than 50Ω switch resistance in the current-mode passive mixer and introducing a positive feedback from base-band to the RF-input, it can be well matched close to f_{LO} while achieving a noise figure below 3dB, which is otherwise a fundamental limit. A quadrature front-end prototype for a direct conversion receiver has been implemented in 65nm CMOS, occupying an active area of 0.23mm^2 with a frequency operation ranging from 0.7 to 3.8GHz. The prototype achieves a minimum noise figure of 2.5dB, an out-of-band 1dB compression point of +3dBm, with IIP3 and IIP2 exceeding +26 and +65dBm, respectively. The current consumption from a 1.2V supply is between 22.8 and 62.8mA, depending on frequency operation.

Anders Nejdel, Mohammed Abdulaziz, Markus Törmänen, and Henrik Sjöland,, "A Positive Feedback Passive Mixer-First Receiver Front-End," © 2015 IEEE, reprinted from *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, Phoenix, USA, May. 16–20 2015, pp. 79–82.

I Introduction

The dramatic increase of wireless traffic resulting in ever more frequency bands and channel bandwidths calls for more reconfigurable hardware which can be configured for specific standards and operating conditions. The increased traffic also results in more interference, both in-band and out-of-band. High linearity is thus critical, especially if operating in an FDD system, where also interference from the own transmitter can de-sensitize the receiver. If the large signal capability of the receiver can be increased the requirements on the off-chip duplexer isolation can be relaxed, and thus the cost can be reduced.

TDD cellular operation does not require any duplexer since there is no transmitter signal present at the time of reception. However, there is still a need to filter out large out-of-band blockers that can compress the receiver. If the large signal capability of the receiver can be increased, the off-chip SAW-filter typically used in TDD systems can be removed or heavily reduced in complexity to further reduce cost.

In this paper, to improve out-of-band interference handling we propose a current-mode passive mixer-first based receiver front-end with low mixer switch resistance and positive feedback to increase the impedance at f_{LO}. Thus, the receiver front-end is matched close to f_{LO}, whereas the impedance is low out-of-band. The low impedance input reflects the out-of-band interferers and minimizes the voltage swing they cause. Furthermore, the reduced switch resistance yields a lower noise figure.

II Passive mixer first receiver

The passive mixer-first receiver is a good candidate for software defined radio [1–3]. It consists of a current-mode mixer followed by a TIA, see figure 1a. The received bandwidth can easily be selected by tuning the pole of the TIA. The shunt capacitor at the TIA input enables attenuation of out-of-band blockers before the TIA. The main issue, however, with the passive mixer-first receiver front-end is its fairly high noise figure. The noise figure of the passive mixer, assumed to be driven by standard quadrature 25% duty cycle LO signals without any harmonic rejection, is given by (1) [3].

$$F = \left(1 + \frac{\overline{v_{R_{SW}}^2}}{\overline{v_{R_s}^2}} + \frac{\overline{v_{BB}^2}}{4\overline{v_{R_s}^2}}\right)\gamma, \quad \gamma = \frac{\pi^2}{8} \tag{1}$$

As seen in (1) there are two main noise contributors, namely the baseband and the mixer on-resistance, R_{SW}. This would lead to the assumption that the noise figure can be decreased by either spending more current in the baseband TIA or decreasing the on-resistance of the mixer. Spending more current in the TIA will not only reduce its noise but also increase the loop gain and thereby decrease its input impedance, Z_{BB}, thus changing the input matching.

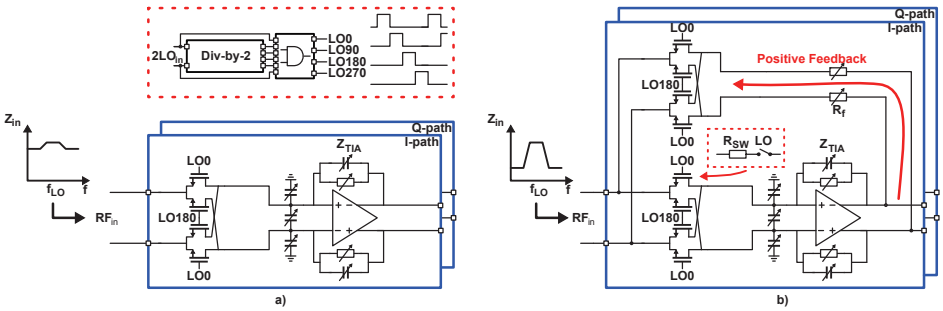


Fig. 1: Schematic of the passive mixer-first receiver front-end a) without positive feedback b) with positive feedback to increase input impedance near f_{LO}.

Similarly, decreasing the on-resistance of the mixer switches decreases the noise but also changes input matching. The input impedance of a passive mixer front-end with quadrature LO signals is given by (2) [3], and the gain is given by (3).

$$Z_{in} \approx R_{SW} + \alpha Z_{BB}(\Delta\omega), \quad \alpha = \frac{4}{\pi^2} \tag{2}$$

$$A_v \approx \frac{Z_{TIA}(\Delta\omega)}{Z_{in}} \frac{\sqrt{2}}{\pi} \tag{3}$$

In order to provide a 50Ω input match the noise figure can not reach less than about 4dB, assuming low noise and low input impedance of the baseband amplifier. Even if an unlimited number of phases are used in a harmonic rejection mixer ($\gamma = 1$, $\alpha = 0$), and a noiseless baseband amplifier with zero input impedance, the noise figure cannot reach below 3dB due to the matching constraint.

III Passive mixer first receiver with positive feedback

Positive feedback can be used to increase input impedance as is demonstrated in [4], where a frequency translational loop was used to increase the input impedance of a common gate LNA in order to increase the transconductance of the amplifier with maintained input matching. When using positive feedback, the input impedance is given by equation (4), where Z_{ol} is the open-loop input impedance of the passive mixer-first front-end (2). This impedance can now be designed to be lower than 50Ω by the use of large mixer switches and thus yielding lower noise.

$$Z_{in} = \frac{Z_{ol}}{1 - A_{loop}}, \quad A_{loop} \approx \frac{Z_{TIA}}{R_f} \tag{4}$$

By applying positive feedback, the input impedance can be increased to 50Ω. For instance if the input impedance of the front-end is 10Ω without any positive feedback, a feedback with $A_{loop} = 0.8$ provides $Z_{in} = 50\Omega$. If the loop gain is too large, the input impedance will become negative and the system will be unstable.

Frequency translational negative [5], [6] or positive [4], [7] feedback can be applied from the baseband output to the RF input if receiver front-ends. The signal will be filtered by the shunt cap at the mixer output and the TIA poles, and the feedback will thus only have a significant loop gain at frequencies in the baseband corresponding to the channel bandwidth. The baseband signal is up-converted by the feedback mixer, resulting in a decrease or increase of the input impedance around f_{LO}. With positive feedback the impedance is increased, and thus the mixer-first receiver front-end can be matched around f_{LO} and the input impedance is low far from the LO frequency where linearity is important. The feedback loop gain will be determined by the gain of the forward path (the gain of the passive mixer-first receiver front-end) and of the feedback path. It is thus of key importance to re-tune the global feedback resistance, R_f, if the front-end gain is changed. The noise of the positive feedback mixer-first receiver front-end is similar to (1), assuming R_f is large. It is also possible to tune the input impedance to better match different source impedances, by programming the feedback resistance.

IV Circuit implementation

The implemented circuit, see figure 1b, consists of a main path with double balanced passive mixers with switch sizes of 96/0.06μm. The mixer output feed OPAMP based TIAs with long and large input devices to achieve low thermal noise figure and flicker noise. The OPAMPs use large shunt capacitors at the TIA input to attenuate out-of-band blockers. The large input devices also contribute to the shunt capacitance at the TIA input. By using a combination of MIM, MOM and MOS capacitance, the density of the shunt capacitors can be increased and their area minimized. The gain and cut-off frequency of the TIAs are digitally controllable by a serial-to-parallel interface. This interface is also used to control the global positive feedback resistance, R_f. The outputs of the TIAs are converted into currents by the global feedback resistors and further up-converted by a second set of double balanced passive mixers of size 10/0.06μm.

The passive mixers are clocked by quadrature signals generated from a divide-by-2 circuit and implemented in Current Mode Logic (CML). The outputs from the divider are delayed and re-timed in AND gates with the original $2f_{LO}$ signal, to produce 25% duty cycle LO signals that are fed to both the feedforward and feedback mixers.

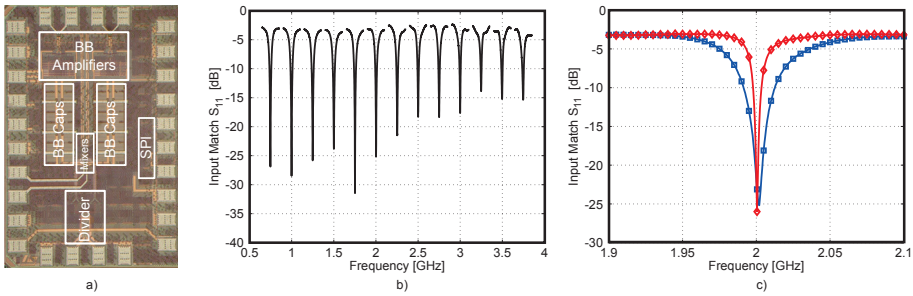


Fig. 2: a) Chip photo. The circuit measures 1x0.6mm^2 including pads. b) Input match S_{11} from $f_{LO} \pm 100$MHz where f_{LO} is increased in 250MHz steps. c) Input match around 2GHz for two different baseband bandwidths.

V Measurement Results

The circuit was manufactured in a 65nm CMOS process, see chip photo in figure 2a. The total size is 1x0.6mm^2 including pads, and the active area is 0.23mm^2. The silicon dies were wire-bonded to FR-4 substrates for measurement purposes.

For all measurements, the receiver front-end was programmed to a conversion gain of about 40dB. The operation frequency of the receiver front-end is 750 MHz to 3750MHz, limited by the LO frequency divider at low frequencies and by the noise figure at higher frequencies. The current consumption from the analog power supply, powering the baseband OPAMPs, is 6.8mA, while to LO generation consumes 16 to 56mA, depending on the frequency of operation. All circuitry is powered from a 1.2V supply. The losses of the measurement setup including balun, combiners, PCB, cables and the off-chip measurement buffer (AD830) are de-embedded from the presented data.

The input match, measured with an R&S ZVC and differential signals generated by a Krytar 4005040, is presented in figure 2b where the LO frequency, generated by an Agilent E8257D and Krytar 4020180, has been increased in 250MHz steps and the input match ±100MHz around the LO frequency is measured. As can be seen, the receiver front-end is well matched to the 50Ω impedance at f_{LO}. The input match for two different baseband bandwidths is presented in figure 2c, where the larger RF bandwidth corresponds to 20MHz and the lower corresponds to 6MHz. For some frequencies, the minimum S_{11} is slightly off-center, compared to the LO frequency due to reactive components at the chip input such as bond wires and PCB traces. This could be countered by the use of complex feedback where the effective phase of the feedback signal is tuned to compensate for the reactive components. As can be seen in figure 2b, the out-of-band S_{11} is about -3 dB thanks to the large switches with low on-resistance.

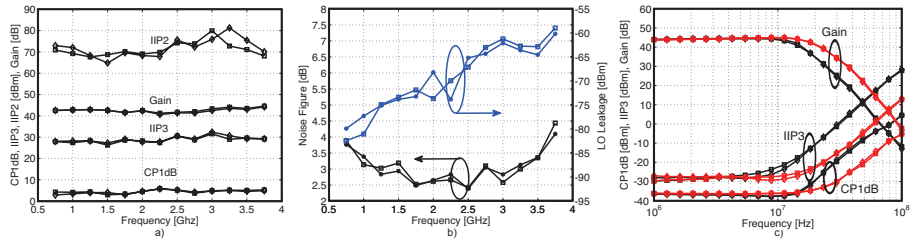


Fig. 3: a) Gain, out-of-band 1dB compression point, IIP3 and IIP2 vs. LO frequency for two samples. b) Noise Figure and LO leakage versus LO frequency. c) Gain, 1dB compression point and IIP3 vs. baseband frequency at f_{LO}=2GHz.

Again increasing the LO frequency in 250 MHz steps, the gain, generated by an R&S SMIQ, was measured by an R&S FSEB spectrum analyser at 1MHz baseband frequency for two samples and is slightly above 40dB over the frequency range, see figure 3a. Out-of-band third order linearity, figure 3a, was measured with two tones placed at $f_{LO} + 100$MHz and $f_{LO} + 199$MHz, generated by two R&S SMIQ signal generators and combined by a Krytar 4005040 and differential signals generated by a Marki BAL-0006. The IIP3 is above +26dBm over the frequency range, while IIP2 measured with two tones placed at $f_{LO} + 99$ MHz and $f_{LO} + 100$ MHz was measured to above +65dBm. The compression point at 100MHz offset from the LO was measured to be above +3dBm for all frequencies, and for many frequencies it was close to +5dBm.

The noise figure, measured for two samples, is presented in figure 3b and shows a minimum of 2.5dB. At the maximum frequency, the noise figure is slightly above 4dB. The LO leakage was measured and is presented in the same figure. It is below -60dBm for all frequencies.

The gain, compression and linearity versus baseband frequency, measured at an LO frequency of 2GHz for two different baseband bandwidths, are presented in figure 3c. In this measurement, the IIP3 is presented with respect to the lower baseband fundamental tone. As expected, the filtering provided by the baseband shunt capacitors and the pole of the TIA increase the out-of-band linearity. The 1dB compression point was measured to -40dBm in-band and +4dBm at 100MHz offset. Similarly, third order linearity IIP3 was measured to -30dBm in-band and +28dBm out-of-band.

The performance of the receiver front-end is presented with other recently published passive mixer-first receiver front-ends in table I. The noise figure is lower than for the other circuits, except for [8], which uses a noise cancellation path to break the 3dB limit. The linearity of our circuit, however, is higher, and in fact it shows the highest IIP2 and IIP3 if all the works. Despite a lower supply voltage the compression point is close to that of [1].

Table I: Comparison with previously published mixer-first receiver front-ends.

	This Work	**JSSC'10 [1]**	**RFIC'14 [9]**	**ISSCC'14 [8]**
Freq. [GHz]	**0.7–3.8**	0.1–2.4	0.1–0.8	0.1–3.3
NF [dB]	**2.5–4.5**	3–10*	3.6	1.6-2.1*
Gain [dB]	**40**	40–70	20–36	N/A
CP1dB [dBm]	**+3**	+4*	N/A	-2.5
Power [mW]	**27.5–75.4**	37–70	23	36.8–62.4
Supply [V]	**1.2**	1.2/2.5	1.2/1.6	1
OOB IIP3 [dBm]	**+26**	+25	+7	+11.5
OOB IIP2 [dBm]	**+65**	+56	+36	+55
Area [mm^2]	**0.23**	0.75	0.33	5.2
Process [nm]	**65**	65	65	28

*Estimated from figure.

VI Conclusions

We have presented a passive mixer-first receiver front-end where the input impedance is increased by means of frequency translational positive feedback. The receiver input is thereby well matched close to f_{LO}, whereas far from the LO frequency its impedance is low due to mixers with large switches. By employing positive feedback, the on-resistance of the passive mixers can be reduced and thus a noise figure below 3dB is achieved. The inductor-less prototype shows high out-of-band linearity and compression point.

Ackowledgement

This work was funded by the Swedish Foundation for Strategic Research (SSF) under the Digitally Assisted Radio Evolution (DARE) project. The authors would like to thank STMicroelectronics for supporting chip fabrication.

References

[1] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 2696–2708, Dec 2010.

[2] M. Soer, E. Klumperink, Z. Ru, F. van Vliet, and B. Nauta, "A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving >11dbm IIP3 and <6.5 db NF," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2009, pp. 222–223.

[3] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec 2012.

[4] C. Izquierdo, A. Kaiser, F. Montaudon, and P. Cathelin, "Reconfigurable wide-band receiver with positive feed-back translational loop," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2011, pp. 1–4.

[5] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2011, pp. 372–374.

[6] A. Nejdel, M. Törmänen, and H. Sjöland, "A noise cancelling 0.7-3.8 GHz resistive feedback receiver front-end in 65 nm CMOS," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 35–38.

[7] F. Lin, P.-I. Mak, and R. Martins, "An RF-to-BB current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 74–75.

[8] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver with enhanced resilience to harmonic blockers," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 68–69.

[9] I. Choi and B. Kim, "A passive mixer-first receiver front-end without external components for mobile TV applications," in *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, 2013, pp. 145–148.

Paper V

A 0.6—3.0 GHz 65 nm CMOS Radio Receiver with $\Delta\Sigma$-based A/D-Converting Channel-Select Filters

Abstract

We present a wideband quadrature radio receiver employing $\Delta\Sigma$-based A/D-converting channel-select filters (ADCSFs). The output of the quadrature passive mixer is directly connected to the input of the ADCSFs, which incorporate the functionalities of both channel selection and data conversion in a single power-optimized block. The 65 nm CMOS receiver has a frequency range of 0.6–3.0 GHz and can be programmed to support the 2xLTE20, LTE20, and LTE10 bandwidths. The receiver noise figure varies from 2.4 to 3.5 dB. In 2xLTE20 mode, the current consumption is between 33 mA at 0.6 GHz and 44 mA at 3.0 GHz, including 10–21 mA for LO generation and distribution, supplied from 1.2 V. The SNDR is 47–51 dB at an LO frequency of 1.8 GHz.

Anders Nejdel, Xiaodong Liu, Mattias Palm, Lars Sundström, Markus Törmänen, Henrik Sjöland and Pietro Andreani, "A 0.6—3.0 GHz 65 nm CMOS Radio Receiver with $\Delta\Sigma$-based A/D-Converting Channel-Select Filters," © 2015 IEEE, reprinted from *Proceedings of IEEE European Solid-State Circuits Conference*, Graz, Austria, Sep. 14–18 2015, pp. 229–302.

I Introduction

Recently, several works exploiting the idea of co-designing the channel-select filter (CSF) and the ΔΣ-based A/D converter in a radio receiver have been presented for the receiver baseband [1–3] and for complete receivers [4, 5], obtaining significant dynamic range or power-efficiency improvements while decreasing the total receiver area. By placing the ΔΣ modulator (ΔΣM) inside the global feedback loop of the CSF, additional noise shaping of the ΔΣM noise can be obtained, relaxing the noise requirements on the ΔΣM itself [1, 2, 6].

In this paper we present a single-ended receiver, where a wideband low-noise transconductance amplifier (LNTA) is followed by current-mode passive mixers directly connected to the current-to-digital ADCSFs, see Fig. 1. With respect to the ADCSF presented in [2], the ΔΣM section of the new ADCSF is reduced to a simple 1st-order design; nevertheless, the new ADCSF has a higher SNR/SNDR. Compared to the receiver in [5], we achieve a lower noise figure (NF), lower power consumption, and more aggressive filtering to attenuate adjacent channels.

II RF front end

To provide a wide frequency range of operation, a wideband noise-cancelling LNTA based on shunt-shunt feedback has been used, see Fig. 2. The first stage of the LNTA is a voltage-mode amplifier (A_m) providing a good impedance match over a wide frequency range, obtained by optimizing its gain together with the feedback resistor R_f. The output voltage of this stage is fed to a bank of transconductances, g_{mp}, which perform voltage-to-current conversion and deliver an output current in-phase with the input signal. The RF input also drives a second set of transconductances, g_{mn}, producing a current in phase opposition to the input signal; thereby, single-ended to differential signal conversion is achieved.

The LNTA also cancels the noise produced by the transistors of the A_m stage. A noise source in A_m is amplified by g_{mp} before reaching the output

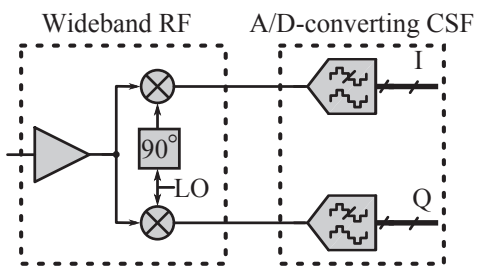


Figure 1: High-level view of the wideband receiver with ADCSFs.

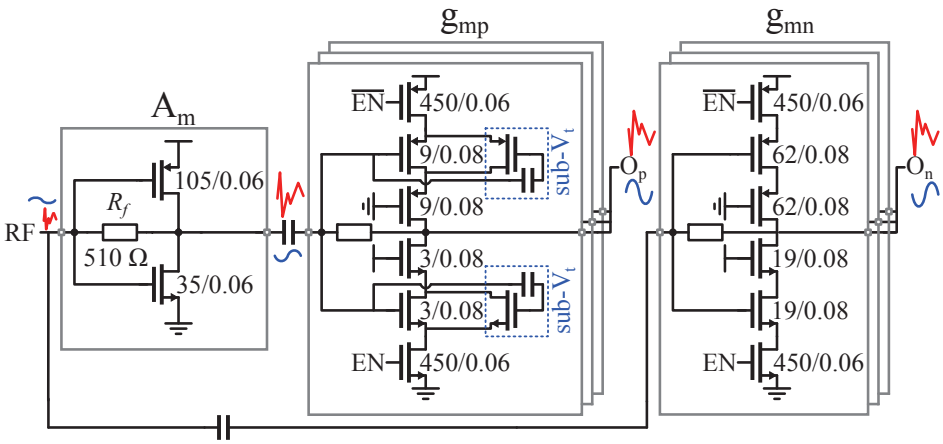


Figure 2: Wideband, shunt-feedback, noise-cancelling, single-ended-to-differential LNTA.

O_p; the same A_m noise source is also found at the RF input, attenuated by the factor $1 + R_f/R_s$, and is subsequently amplified by g_{mn} before reaching O_n [7,8]. The source impedance, R_s, is assumed to be 50 Ω. Since the resulting noise at O_p has the same polarity as the correlated noise at O_n, their overall impact is greatly attenuated by the common-mode rejection of the mixers and ADCSFs.

Optimal noise cancellation occurs when the condition $g_{mn}/g_{mp} = R_f/R_s+1$ is fulfilled, while perfectly balanced signals at O_p and O_n require $|A_v|g_{mp} = g_{mn}$, where $|A_v|$ is the voltage gain of A_m (set to 5 in this work). A third relation, demanded by optimal input matching, is $|A_v| = R_f/R_s - 1$.

As these three equations cannot be satisfied at the same time, a trade-off must be made between noise cancellation, input matching, and balanced outputs. Accordingly, we chose to optimize the LNTA for balanced outputs, to maintain a high 2nd-order linearity in presence of unavoidable mismatches in the double-balanced passive mixer. Furthermore, in order to reduce the noise contribution from R_f, to obtain additional gain in the matching stage, and to achieve a good compromise between input matching and noise, R_f has been increased beyond its value for optimal input matching. The simulated schematic level noise figure is below 1.6 dB.

In order to increase the 3rd-order linearity of the LNTA, limited by g_{mp} due to the relatively large voltage swing at the g_{mp} input, MOS transistors working in sub-threshold were placed in parallel to the gain transistors of g_{mp} [9], as shown in Fig. 2. By disabling some of the g_{mn} and g_{mp} cells, the gain of the LNTA can be decreased by 3, 6 or 12 dB. This provides part of variable gain control at RF.

To support quadrature LO signals to the passive mixer, a current mode logic frequency divide-by-2 circuit was used together with AND-gates to generate four 25% LO phases.

III ADCSF Implementation

The ADCSF, shown in Fig. 3, consists of a 5^{th}-order continuous-time loop filter, a 3-bit flash quantizer, and 5 non-return-to-zero feedback DACs. The first 4 integrators of the ADCSF implement a 4^{th}-order Butterworth CSF, while a 1^{st}-order $\Delta\Sigma$M is implemented with the last integrator. The overall cascade-of-integrators-in-feedback (CIFB) topology has been adopted in order to minimize peaking in the signal transfer function (STF) [10]. Resistive DACs have been preferred to current-steering DACs because of their lower thermal noise. The ADCSF bandwidth is tunable to 4.5 MHz (LTE10 mode), 9.0 MHz (LTE20 mode) and 18.5 MHz (2xLTE20 mode) by programming the integration capacitors while scaling the sampling frequency. The total gain of the receiver, set by the product of the LNTA and mixer transconductance and DAC_1 resistance, is 50 dB in nominal conditions.

To enable a high out-of-band linearity, 10 pF shunt capacitors have been added after the mixers (Fig. 3), together with 25 Ω series resistors to enhance the stability of the first integrator. Loop delay in the $\Delta\Sigma$M is compensated by DAC_5 and R_{pi}, while C_{ph} creates a phantom zero for phase margin enhancement of the last integrator.

The ADCSF synthesis starts with the choice of the CSF, which should attenuate both far out-of-band interferers, such as the leakage of the own strong TX signal, and adjacent RX channels. Since the primary task of the CSF is filtering, the high-frequency quantization-noise shaping afforded by the CSF is modest, compared to what would be achievable with an optimized 4^{th}-order $\Delta\Sigma$M. In fact, for a given CSF order, there is a trade-off between CSF filtering and CSF noise shaping, dependent on the ratio r of the −3 dB CSF cutoff

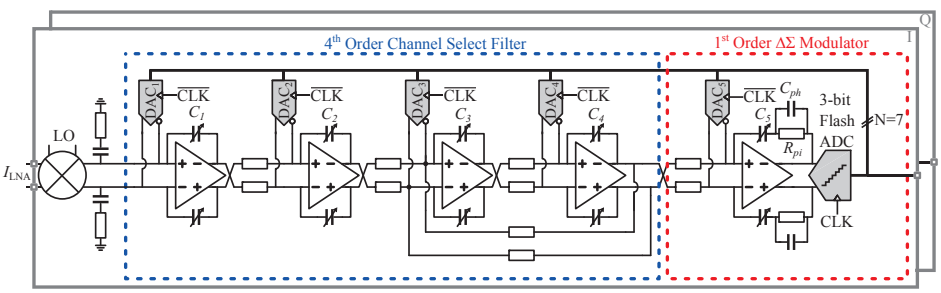


Figure 3: ADCSF with 4^{th}-order Butterworth CSF and 1^{st}-order $\Delta\Sigma$M.

frequency f_0 to the baseband signal bandwidth f_{sig} (i.e., $r = f_0/f_{sig}$) [6]. If the overall in-band noise of the ADCSF is too high, it is possible to increase r to obtain an improved noise shaping by the CSF. If further noise reduction is required and r cannot be increased without deteriorating the close-in filtering, a higher-order $\Delta\Sigma$M can be used.

In this design, the noise suppression afforded by the CSF is 23 dB for $r = 1.36$, which results in SNR/SNDR of 62/60 dB for the 2xLTE20 mode, measured on a stand-alone prototype of the ADCSF. Thus, the additional noise shaping by the CSF is a key feature to achieve such high SNR/SNDR values for the ADCSF, while allowing the use of a simple 1st-order $\Delta\Sigma$M. Crucially, the use of $r = 1.36$ is low enough to provide a strong filtering already at the first adjacent channel. It should be mentioned that a correct ADCSF design entails the recalculation of the CSF coefficients to account for the quantizer/DAC delays in the feedback loop [2].

IV Experimental Results

Manufactured in STMicroelectronics 65 nm CMOS process, the pad-limited die of the receiver measures 2x1 mm^2, with an active area of 0.7 mm^2, see Fig. 4. Dies have been wire-bonded to FR-4 PCBs and measured. Thanks to the single-ended LNTA, no external balun was needed at the RF input. All results are based on one circuit sample, and data for both I and Q outputs are presented when relevant. The PCB/cable/combiner losses have been de-embedded in all measurements to follow, and all results are presented at maximum receiver gain.

The receiver is powered by 6 different 1.2 V supply domains. The current consumed by the LNTA is 10.0 mA, while the LO input buffer, divider and distribution consume between 9.6 mA and 20.6 mA depending on the LO frequency. The ADCSFs, I and Q together, consume 10.0/11.1/13.6 mA for

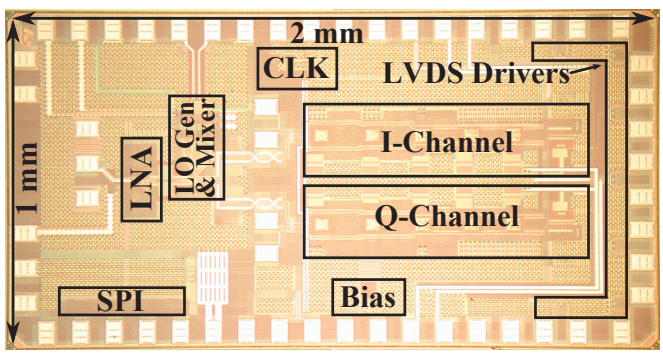


Figure 4: Die photograph of the receiver (core area is 0.7 mm^2).

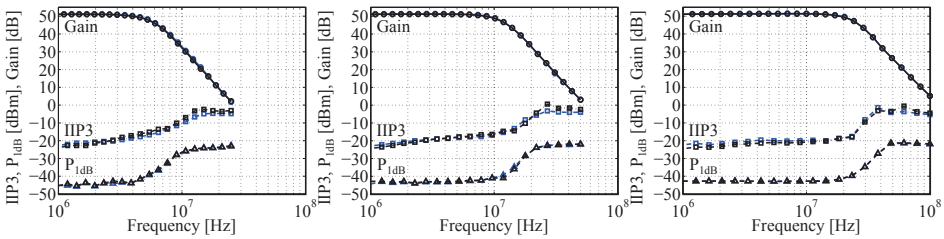


Figure 5: Signal transfer function, P_{1dB}, and IIP3 of the receiver for LTE10 (left), LTE20 (middle) and 2xLTE20 (right), with an LO frequency of 1.778 GHz.

LTE10/LTE20/2xLTE20, including clock buffering and distribution. The ADCSF outputs, buffered by differential LVDS drivers, were sampled by an Agilent 16902B logic analyzer and post-processed in MATLAB.

A sinusoid at two times the LO frequency was provided by an Agilent E8257D, from which differential signals were generated by a Marki BAL-0006.

The performance of the receiver versus baseband frequency is shown in Fig. 5 for the three different bandwidth settings at an LO frequency of 1.776 GHz. In order to set the different bandwidths, the value of the integration capacitors is changed via a serial-to-parallel digital interface. For a constant oversampling ratio of 16, the sampling frequency, f_s, was set to 148, 296 and 592 MHz for LTE10, LTE20 and 2xLTE20, respectively. The receiver gain is presented up to a frequency of 5 times the channel bandwidth. The STF follows the nominal 4^{th}-order Butterworth roll-off very closely.

For desensitization measurements, P_{1dB} is defined as the power of the interfering signal ("blocker") for which the in-band noise increases by 1 dB. Desensitization in the ADCSF occurs mostly via an increase of the noise floor, rather than a compression of the desired signal, particularly for in-band and close-in blockers; this makes P_{1dB} a more accurate metric than the more traditional cross compression.

The in-band and out-of-band P_{1dB} are approximately -45 dBm and -20 dBm, respectively, for all bandwidth settings (Fig. 5). The strong blocker was generated by a low phase noise generator (R&S SMHU) to ensure that desensitization is not set by the wideband noise floor of the blocker.

The input-referred 3^{rd}-order intercept point, IIP3, was measured versus frequency f_{off} with two tones placed at $f_{\text{LO}} + f_{\text{off}}/2 + 100$ kHz and $f_{\text{LO}} + f_{\text{off}}$, with results shown in Fig. 5. In-band, P_{1dB} and IIP3 are set by the ADCSF, while out-of-band they are dominated by the LNTA, where the mentioned linearization technique [9] increases out-of-band IIP3.

The receiver performance versus LO frequency, with the baseband in LTE10 mode, is presented in Fig. 6. The LO frequency is increased in steps of f_s

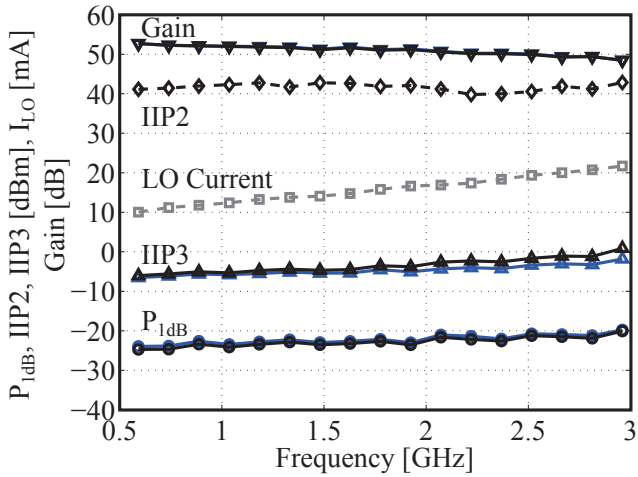


Figure 6: Receiver gain, LO current consumption, IIP3 and P_{1dB} versus LO frequency.

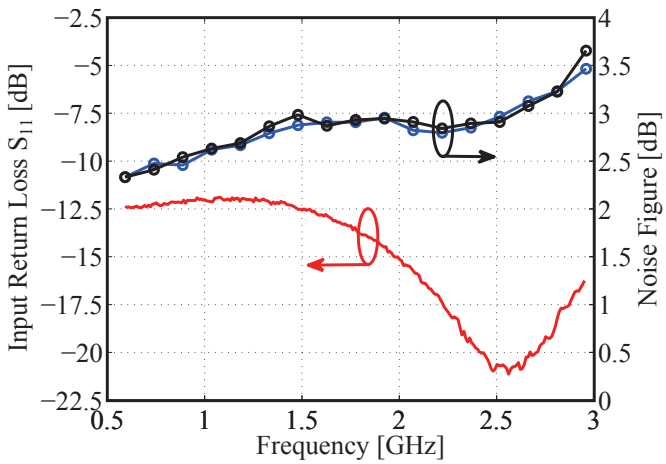


Figure 7: Input matching and noise figure versus LO frequency.

(148 MHz for LTE10), from $4f_s$ (592 MHz) to $12f_s$ (2.960 MHz). The RF-to-digital gain, measured at a baseband frequency of 1 MHz, is approximately 50 dB, as expected. P_{1dB}, measured with a blocker at 25 MHz, is between -24 and -20 dBm, and IIP3, measured with an f_{off} of 25 MHz, is between -6 and 0 dBm. The input-referred 2nd-order intercept point (IIP2) was measured to above +40 dBm for one output channel with two tones placed at f_{LO} + 24.9 MHz and f_{LO} + 25 MHz. For the other channel, IIP2 varies between +47 and +60 dBm. Similar values were observed for two samples.

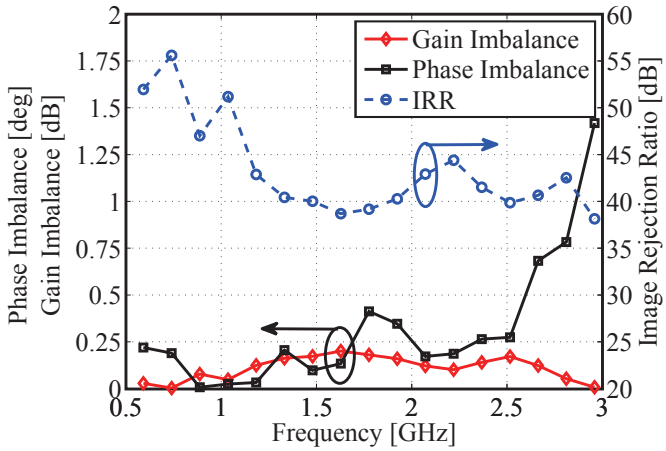


Figure 8: I/Q gain and phase imbalance versus LO frequency.

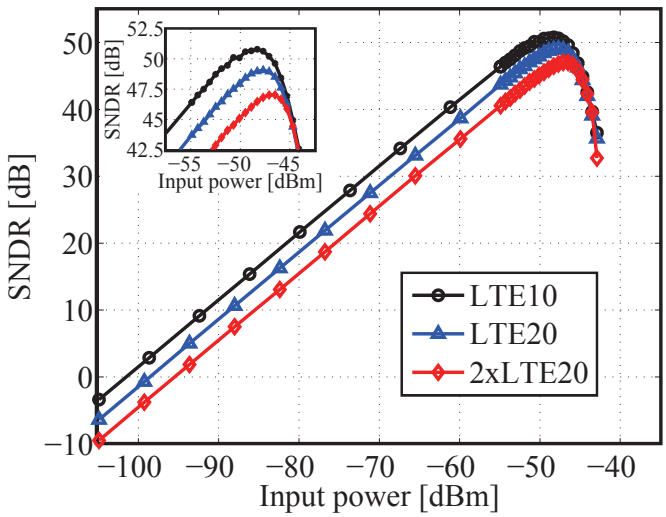


Figure 9: SNDR of the receiver for LTE10, LTE20 and 2xLTE20 at $f_{\mathrm{LO}} = 1.776\,\mathrm{GHz}$.

As shown in Fig. 7, the wideband shunt-feedback LNTA achieves a good input impedance match, with an S_{11} below $-12\,\mathrm{dB}$ over the entire 0.6–3.0 GHz range. The receiver NF is below 3 dB up to 2.5 GHz, increasing to 3.5 dB at 3 GHz for both I and Q outputs (Fig. 7), measured using the Y-factor method together with an HP 346A 5 dB ENR noise source.

Gain and phase imbalance between I and Q are displayed in Fig. 8. Measured at a baseband frequency of 1 MHz, the phase imbalance is below 0.5° up

to 2.5 GHz, while the gain imbalance is below 0.25 dB. The phase imbalance increases to 1.5° at 3 GHz. The corresponding image rejection ratio (IRR) calculated from these data exceeds 40 dB over almost the complete frequency range.

Finally, the complete receiver displays an SNDR of 47–51 dB for the three bandwidths, measured at a mid-band frequency of $f_{LO} = 1.776$ GHz and with an input tone placed at $f_{LO} + 1$ kHz. SNDR for all bandwidth setting versus f_{LO} varies between 45 and 52 dB.

The receiver is compared to other ΔΣM-based receivers in Table I. With respect to [5], we achieve a lower NF at a lower power consumption. Furthermore, [5] uses a high $r = 2.1$ (compared to our $r = 1.36$), which means that the first adjacent channel is not filtered at all. To summarize, we achieve the widest carrier bandwidth with a good linearity and the lowest NF and power consumption, at a comparable frequency range of operation.

V Conclusions

We have presented a wideband radio receiver where the traditional baseband with cascaded CSF and A/D converter is replaced by an A/D-converting CSF, increasing the overall power efficiency. The circuit supports operation over a wide frequency range and achieves a low noise figure and good linearity at a competitive power consumption.

Table I: Comparison with other ΔΣM-based receivers.

	This work	**[5]**	**[11]**	**[4]**
Type	**RX with ΔΣ-CSF**	Direct ΔΣ RX	Direct ΔΣ RX	RX with filtering A/D
RF Freq. [GHz]	**0.6–3**	0.7–2.7	0.4–4	0.04–1
NF [dB]	**2.4–3.5**	5.9–8.8	16	2.7–3.5*
Power [mW]	**35.5–53.0**	90	17-70.5	221.4
Supply [V]	**1.2**	1.1	1.5/1.2	1.8/1
IIP3 [dBm]	**-6–0**	-2	+13.5	-13
SNDR [dB]	**45–52**	40–43	52–68	–
RF Carrier BW [MHz]	**10,20,40**	1.4,15	4,10	5,6,7,8
Area [mm^2]	**0.7**	1	0.56	5.6**
Process [nm]	**65**	40	65	80

* Estimated, ** Incl. PLL and DSP

Acknowledgements

The authors are very grateful to STMicroelectronics for the generous silicon donation. This work was supported by the Swedish Strategic Research Foundation (SSF) under the Digitally-Assisted Radio Evolution (DARE) project.

References

[1] M. Sosio, A. Liscidini, R. Castello, and F. De Bernardinis, "A complete DVB-T/ATSC tuner analog base-band implemented with a single filtering ADC," in *Proceedings of IEEE European Solid-State Circuits Conference*, Sept 2011, pp. 391–394.

[2] M. Andersson, , M. Anderson, L. Sundström, S. Mattisson, and P. Andreani, "A filtering $\Delta\Sigma$ ADC for LTE and beyond," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1535–1547, July 2014.

[3] R. Rajan and S. Pavan, "Design techniques for continuous-time $\Delta\Sigma$ modulators with embedded active filtering," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 2187–2198, Oct 2014.

[4] J. Greenberg *et al.*, "A 40-MHz-to-1-GHz fully integrated multistandard silicon tuner in 80-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 2746–2761, Nov 2013.

[5] M. Englund *et al.*, "A programmable 0.7–2.7 GHz direct $\Delta\Sigma$ receiver in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 644–655, March 2015.

[6] M. Sosio, A. Liscidini, and R. Castello, "A 2G/3G cellular analog base-band based on a filtering ADC," *IEEE Transactions Circuits Systems II, Express Briefs*, vol. 59, pp. 214–218, April 2012.

[7] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 275–282, Feb 2004.

[8] M.-D. Tsai *et al.*, "A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2014, pp. 354–355.

[9] B. Kim, J.-S. Ko, and K. Lee, "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," *IEEE Microwave and Guided Wave Letters*, vol. 10, pp. 371–373, Sep 2000.

[10] K. Philips *et al.*, "A continuous-time $\Delta\Sigma$ ADC with increased immunity to interferers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2170–2178, Dec 2004.

[11] C. Wu, E. Alon, and B. Nikolic, "A wideband 400 MHz-to-4 GHz direct RF-to-digital multimode $\Delta\Sigma$ receiver," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1639–1652, July 2014.