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Published in:
Proc. IEEE NORCHIP

2009

A 65-nm CMOS Ultra-Low-Power LC Quadrature VCO

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***Abstract* — An ultra-low-power LC quadrature VCO (QVCO) is presented. It is designed in a single-poly seven-metal 65nm CMOS process. To minimize power dissipation an inductor with a high *LQ* product of 188nH at 2.4GHz, and a self-resonant frequency (f_o) of 3.8GHz, was designed. According to SpectreRF simulations the power dissipation is below 250µW at a 0.6V supply. At this supply the simulated tuning range and phase noise at 1MHz offset are 10.4% (2.34–2.59GHz) and -113.4dBc/Hz respectively. The phase noise figure of merit (FoM) is better than 187dB at all supply voltages of interest, which is competitive to other state-of-the-art QVCOs.**

I. INTRODUCTION

The ubiquity of wireless links in everyday life increases rapidly, medical implants and wireless sensor networks are two good examples. For such applications, not only production costs are important, but also maintenance costs and user satisfaction. Replacing the battery frequently is therefore unrealistic, so the power consumption of the whole system must be extremely small in order to maximize the battery life.

Zero-IF and low-IF receivers are widely used in modern radio systems because of their small size and low power dissipation compared to classical super-heterodyne receivers. In such receivers, quadrature down-conversion is required to reject the image signals. This requires quadrature local oscillator signals, which can be generated directly using ring oscillators. Unfortunately ring oscillators have poor phase noise performance compared to the LC oscillator counterparts.

To address these requirements, this paper presents the design of an ultra-low-power quadrature LC VCO in a 65nm CMOS process. To achieve low power consumption in an LC oscillator, the inductor *LQ* product should be maximized. An inductor with an *LQ* product of 188nH at 2.4GHz was

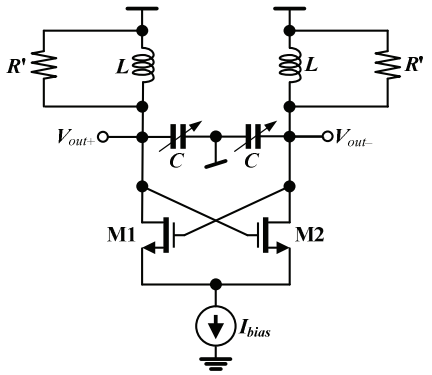

Fig. 1. Negative-resistance VCO

therefore designed. According to Spectre RF simulations this leads to a very low power consumption of the complete QVCO of less than 250µW at 0.6V supply. At such low supply voltages, the large-signal capacitance range of varactors usually becomes reduced and, thus, also the frequency tuning range. In this paper, the use of nMOS inversion-mode varactors, however, provide more than 10% tuning range in all cases of interest. Meanwhile, the FoMs are above 187dB, which is competitive to other state-of-the-art QVCOs.

II. LOW-POWER LC VCO DESIGN

A typical negative-resistance LC VCO is depicted in *Fig. 1*, with a cross-coupled pair connected in parallel to the LC tank to compensate the loss. *R*' is the equivalent resistance contributed by the inductor.

In order to start oscillation, the start-up gain of the oscillator must be larger than unity, which gives:

$$A_{start-up} = g_m \cdot R' = \frac{I_{bias}}{V_{OV}} \cdot R' \geq 1 \qquad (1)$$

Usually, $A_{start-up}$ is set to at least 2-3 to have some margin.

In order to drive connected circuits, there are always some requirements of the output voltage swing of the oscillator. Assume M1 and M2 are ideal switches, the differential output current can be regarded as the result of multiplying the drain current of M1 by a unit-amplitude square wave.

Since the amplitude of the fundamental component of a square wave is 4/π times the amplitude of the square wave:

$$I_O = \frac{4}{\pi} \cdot I_{bias} \qquad (2)$$

Hence the differential peak output voltage is:

$$V_{O-diff,peak} = I_O \cdot R' = \frac{4}{\pi} \cdot I_{bias} \cdot R' \qquad (3)$$

Eq. (1) and (3) are very important to power consumption of oscillators, and they show that the bias current is inversely proportional to *R*', where:

$$R' = \omega_o \cdot LQ \qquad (4)$$

The result is that in order to minimize the power consumption the *LQ* product of the inductor must be maximized.

III. INTEGRATED INDUCTOR

The single-π lumped model was adopted in this paper because of its simplicity. Refer to *Fig. 1*, instead of using two separate spiral inductors, the use of a single center-tapped inductor gives the benefit of higher inductance at a given area. A center-tapped octagonal inductor and its single-π model are shown in *Fig. 2*. Its parameters are discussed in this section.

The expression for spiral inductance calculation in [1] is adopted in this thesis:

$$L_s = \frac{\mu_o n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho_{fill}}\right) + c_3\rho_{fill} + c_4\rho_{fill}^2\right] \qquad (5)$$

where μ_o is the permeability of free space, *n* is the number of turns, c_i are layout dependent coefficients, ρ_{fill} and d_{avg} are the fill ratio and average diameter, respectively, given by:

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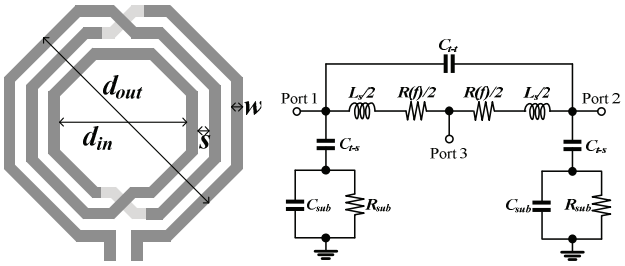


(a) (b)

Fig. 2. (a) Center-tapped octagonal inductor and (b) its single-π lumped model.

Inputs	Values
# of turns	9
w	4.5μm
s	3μm
d_{out}	200μm
d_{in}	71μm

(a)

Parameters	Values
C_{t-t}	120.4fF
C_{t-s}	64.6fF
R(f)	11Ω
L_s	11.7nH
Q	16.1
f_{SR}	3.8GHz
LQ Product	188nH

(b)

Table 1. (a) Input parameters and (b) simulation results at 2.4GHz.

$$\rho_{fill} = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \qquad (6) \qquad\qquad d_{avg} = \frac{d_{out} - d_{in}}{2} \qquad (7)$$

The capacitance expressions in [2] were adopted but not mentioned explicitly here.

Skin Effect

For a single metal line, at high frequency the skin depth can be comparable to or even smaller than the cross-sectional dimensions of the line and the AC current is pushed towards the surface of the conductor. This is described as skin effect and the skin depth is given by:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad (8)$$

where μ and σ are the permeability and conductivity of the conductor respectively.

When w or the thickness t of the conductor is larger than δ, AC resistance including skin effect equals [3]:

$$R_{skin}(f) = R_{DC}\left[1 + \left(\frac{f}{f_1}\right)^2 + \left(\frac{f}{f_u}\right)^5\right]^{\frac{1}{10}} \qquad (9)$$

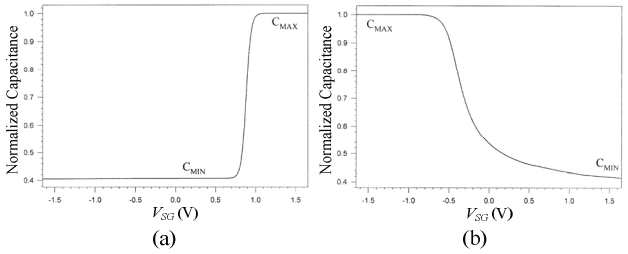
where f_l and f_u indicate at what frequency the skin effect starts to be significant and are given by:

$$f_l = \frac{\pi}{2\mu w t \sigma} \qquad (10) \qquad\qquad f_u = \frac{\pi^2}{2\mu t^2 \sigma}\left[\mathrm{K}\left(\sqrt{1-\left(\frac{t}{w}\right)^2}\right)\right] \qquad (11)$$

and K(m) is the elliptic function of the first kind.

Proximity Effect

For multi-turn inductors, the magnetic field generated by neighboring lines affects the current distribution and causes a higher current density at the edges of metal lines. This is the so-called proximity effect.



(a) (b)

Fig. 3. C-V characteristics of (a) inversion-mode and (b) accumulation-mode varactor.

The proximity effect can have a higher impact than the skin effect in increasing the wire resistance. In integrated circuits the proximity effect can be significant also at frequency below 500MHz. Meanwhile, the skin depth of copper is 2.1μm at 1GHz, and its influence is therefore limited for typical integrated inductors.

According to [4], the proximity effect begins to become significant at ω_{crit}:

$$\omega_{crit} = \frac{3.1}{\mu}\left(\frac{w+s}{w^2}\right)R_{\square} \qquad (12)$$

where $R_{\square}$ is the sheet resistance of the wire. And the AC resistance including proximity effect is:

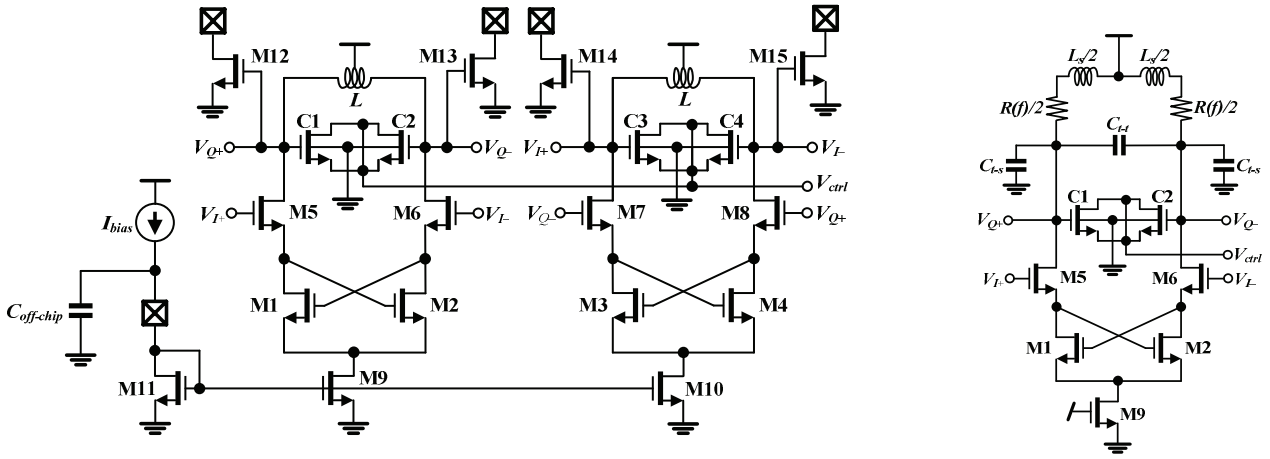
$$R_{prox}(f) = R_{DC}\left[1 + \frac{1}{m}\cdot\left(\frac{2\pi}{\omega_{crit}}\right)^2 \cdot f^2\right] \qquad (13)$$

where m is a layout-dependent parameter. Simulations show m is approximately equal to ten.

There is a misunderstanding that w should be as large as possible to improve the inductor quality by minimizing the winding resistance. The proximity effect is considered first, from (12) and (13) we see ω_{crit} is inversely proportional to w and $R(f)$ increases nonlinearly after ω_{crit}. The situation is similar for the skin effect, when w is larger than the skin depth.

Clearly, w should be set with careful attention to make a good balance between the DC and AC resistance. If there is not much freedom to increase w, how can we then improve the quality of the inductor? The answer, instead, is to decrease w. From (5)–(7), for a given area and filling ratio, more turns can be implemented with a smaller w. Hence more inductance and higher Q can be obtained. Moreover, a higher ω_{crit} can also be obtained, which is very important for high frequency performance. The major drawback is a reduced self-resonance frequency due to larger total turn-to-turn capacitance, C_{t-t}.

Considering all the points mentioned above, a nine-turn center-tapped symmetrical octagonal inductor was designed. The turns of the inductor were implemented in the combination of M7, CB and AP layers ($R_{\square}$=12mΩ/□). A patterned-ground shield was utilized in M1 layer to minimize substrate loss. The inductor performance was simulated using FastHenry. *Table 1* summarizes the input parameters and simulation results.



(a) (b)

Fig. 4. (a) Overall schematic and (b) simulation schematic for the QVCO

IV. VARACTOR

Fig. 3 shows example C-V curves of accumulation-mode and inversion-mode varactors. Clearly, the inversion-mode varactor is more favorable for low-power applications because of its sharper transition, which results in a larger achievable large-signal average capacitance range with limited output swing compared to its accumulation-mode counterpart. However, the sharper transition also means they are more sensitive to substrate noise [5], thus it may be necessary to put the varactor inside a deep n-well to avoid the noise coupling. nMOS is used because electrons have higher mobility than holes, hence a lower series resistance is obtained.

V. QUADRATURE VCO

Compared to other QVCO topologies [6][7][8], the series QVCO [9] (S-QVCO) shows a good compromise between power consumption, area and complexity [10]. The major drawback is that the parasitic capacitance of coupling transistors degrades the tuning range. However, in sub-100nm CMOS processes, this capacitance is not significant anymore.

The overall schematic is shown in *Fig. 4a*. The reference current source is implemented off-chip to provide more freedom to control the measurement. M5–M8 are the coupling transistors. $C_{off\text{-}chip}$ is added to filter out the noise contributed by the reference current source and the transistor M11. Open-drain buffers M12–M15 are added to output the quadrature signals off-chip. C1–C4 are nMOS inversion-mode varactors. Cross coupled nMOS negative-resistance pairs are used as they have better driving ability at a given area than their pMOS counterparts.

V. SIMULATION RESULTS

Because the parasitic extraction tools for the 65-nm process were not available up to the moment this paper is written, only pre-layout simulations were performed.

The single-π lumped inductor model was adopted for the circuit simulation because it gives more insight to the system and shorter simulation time compared to its S-parameter counterpart [11]. The drawback is that it is only accurate for a limited frequency range because of the rapid change of *R(f)* at radio frequencies. The simulation schematic, only one VCO is shown for readability, appears in *Fig. 4b*.

Fig. 5 shows $V_{O\text{-}diff}$ and power dissipation at different V_{dd} when f_o is 2.4GHz. When V_{dd} is between 0.7V and 1.2V, $V_{O\text{-}diff}$

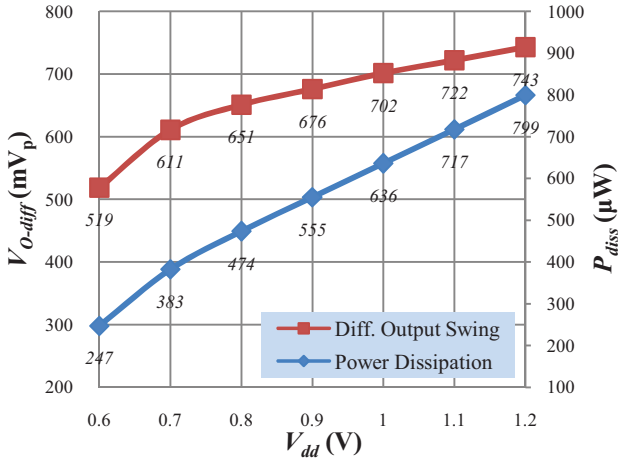


Fig. 5. Power dissipation and output swing vs. V_{dd}.

increases constantly with V_{dd} because short-channel effects change the output current of the current mirrors (M9 and M10). When V_{dd} is smaller than 0.7V, the transistors enter the weak-inversion region, and $V_{O\text{-}diff}$ and the power dissipation drop rapidly.

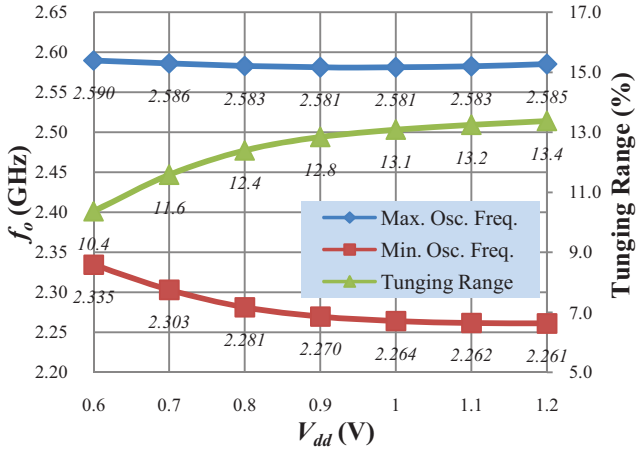


Fig. 6. Tuning range vs. supply voltage.

Despite *R(f)* changing rapidly, the oscillating frequency of the QVCO is not affected if Q is high enough. This allows the single-π model to be used when simulating the frequency tuning range. The result is depicted in *Fig. 6*. When V_{dd} is below 0.8V, $V_{O\text{-}diff}$ is not large enough to exercise the entire

Design	Technology	f_o(GHz)	V_{dd} (V)	P_{diss} (mW)	Tuning Range (%)	$\mathcal{L}$(1MHz) (dBc/Hz)	FoM (dB)
This Work	65nm CMOS	2.4	0.6	0.247	10.4	-113.4	187
			0.8	0.474	12.4	-116.6	187.4
			1.0	0.636	13.1	-118	187.5
			1.2	0.799	13.4	-119.3	187.9
[6]	0.25µm CMOS	1.8	2.5	20	17	-143 @3MHz Δf	185.5
[9]	0.35µm CMOS	1.8	2	50	18	-140 @3MHz Δf	182
[7]	0.18µm CMOS	17	1	5	16.5	-110	187.6
[8]	0.25µm CMOS	4.88	1.8	22	13	-125	185
[12]	0.18µm CMOS	5.1	1.8	27.7	17	-132.6	192

Table 2. Summary of simulation results, and comparisons to other published QVCOs

capacitance transition of the varactors. This confines the tuning range to 10.4% at 0.6V supply, and 11.6% at 0.7V. Otherwise, the tuning range is about 13%.

To fairly compare different VCOs, FoM is usually adopted and defined as:

$$\mathrm{FoM} = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \cdot \frac{1}{\mathcal{L}(\Delta f)\cdot P_{diss}\,|_{\mathrm{mW}}}\right] \qquad (14)$$

Fig. 7 depicts the phase noise at 1MHz offset and the corresponding FoM of the QVCO. Note that the FoM is better than 187dB at all interesting supply voltages.

A summary of the simulation results and comparisons to other recently published QVCOs are shown in *Table 2*. The pre-layout simulations show that the designed QVCO performs very well, especially in terms of power dissipation, and is competitive to the state-of-the-art QVCOs.

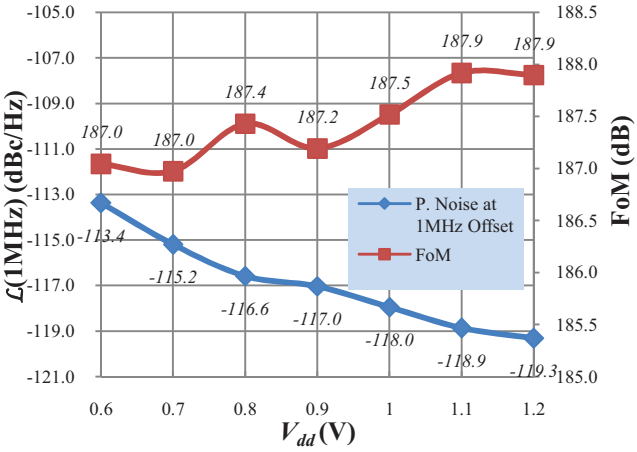


Fig. 7. Phase noise and FoM vs. supply voltage.

VI. CONCLUSION

The design of an ultra-low-power QVCO in a 65nm CMOS process has been presented. A high performance center-tapped octagonal inductor with a *LQ* product of 188nH at 2.4GHz and an f_{SR} of 3.8GHz was designed. This results in a very low power dissipation of 247µW at 0.6V supply according to pre-layout simulations. At this supply voltage, the tuning range and the phase noise at 1MHz offset are 10.4% and -113.4dBc/Hz, respectively. The FoM is better than 187dB at all interesting supply voltages, which is competitive to the state-of-the-art QVCOs.

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