Power Constrained Test Scheduling for 3D Stacked Chips: poster

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Power Constrained Test Scheduling for 3D Stacked Chips
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Purpose:
- Schedule core tests for stacked 3D chips
- Minimize the Test Application Time (TAT)
- A maximum power limitation
- The cost of control lines is considered

Non Stacked Chip Testing
- Two stages
- Wafer sort
- Final test
- Single schedule

3D Stacked Chip Testing
- Two stages
- Pre-bond (individual chips)
- Post-bond (all chips combined)
- Multiple schedules

Experimental Results:

<table>
<thead>
<tr>
<th>Chip</th>
<th>Pre-bond Test</th>
<th>Chip2</th>
<th>Chip1 &amp; Chip2</th>
<th>TAT</th>
<th>Increment in control lines</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>T0</td>
<td>T1</td>
<td>T2</td>
<td>T3</td>
<td>R (%)</td>
</tr>
<tr>
<td>Z</td>
<td>300 300 300 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0%</td>
</tr>
<tr>
<td>L</td>
<td>1234 1234 1234 0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>10%</td>
</tr>
<tr>
<td>M</td>
<td>26 26 27 38</td>
<td>M</td>
<td>M</td>
<td>M</td>
<td>20%</td>
</tr>
<tr>
<td>Z</td>
<td>300 300 300 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0%</td>
</tr>
<tr>
<td>Z</td>
<td>1234 1234 1234 0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>10%</td>
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<tr>
<td>Z</td>
<td>1234 1234 1234 0</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>10%</td>
</tr>
</tbody>
</table>

Conclusions:
- Testing of stacked 3D chips is different from non-stacked chip testing, as the same test schedule does not hold good in pre-bond and post-bond stages
- Splitting of sessions ⇒ Increase in Number of Control Lines ⇒ Increased Cost
- ReScheduling focuses on minimal splitting of pre-bond sessions
- Experimental results depict up to 42% reduction in post-bond test time and 17% in overall test time