Test Scheduling and Test Access Optimization for Core-Based 3D Stacked ICs with Through-Silicon Vias: poster

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Purpose

- Schedule core tests for 3D stacked ICs (SICs) with Through-Silicon Vias (TSVs)
- Reduction of overall test time (wafer sort + package test)
- Consider hardware cost of test data registers (TDRs)

1 Manufacturing Test

**Testing of non stacked chips**
- Two stages
  - Wafer sort
  - Package test
- Same schedule in both stages

**Testing of 3D Stacked chips**
- Two stages
  - Wafer sort (individual chips)
  - Package test (all chips combined)
- Creating the schedule for package test by applying wafer sort test schedules serially may lead to sub optimal test time
- Test scheduling is therefore different from non stacked chip testing

2 Wafer Sort

Above: Test access mechanism for a single chip during wafer sort
- Cores in the chips are accessed by JTAG
- On each chip, only one TDR can be accessed at a time
- Cores on the same TDR are in the same session
- Core1 and Core2 share the same TDR, therefore must be tested in the same session (Session1)
- Core3 has an independent TDR, therefore Core3 must have a separate session (Session2)
- Therefore, additional sessions ⇒ Additional TDR hardware cost

3 Package Test

Above: Test access mechanism for a stack during package test

When Core3, Core4 and Core5 are in the same session
- TDRs required: 2
- Test time required: \( T_{(3,4,5)} = 340 + 3600 = 3940 \)

When Core3 is in a different session with Core4 and Core5
- TDRs required: 2
- Test time required: \( T_{(3,4,5)} = \max(340,3600) = 3600 \)
- Number of TDRs required remains same
- Required test time decreases
- To obtain the lowest overall cost (test time and hardware), cores of different chips should be tested concurrently

4 Objective

Co-optimization of overall test time (wafer sort + package test) along with the TDR (hardware) cost

5 Experimental Results

The \( L \) and \( P \) values for each core is provided in the table below, for the 3D TSV-SIC design considered

<table>
<thead>
<tr>
<th>Cases</th>
<th>Chip1 Core1</th>
<th>Chip1 Core2</th>
<th>Chip1 Core3</th>
<th>Chip1 Core4</th>
<th>Chip2 Core1</th>
<th>Chip2 Core2</th>
<th>Chip2 Core3</th>
<th>Chip2 Core4</th>
<th>Chip2 Core5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
<td>Core Test in Session</td>
</tr>
<tr>
<td></td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
<td>Time</td>
</tr>
<tr>
<td>1</td>
<td>1 + (2) + (3)</td>
<td>1400</td>
<td>4 + (5)</td>
<td>500</td>
<td>(1) + (2) + (3) + (4) + (5)</td>
<td>4000</td>
<td>10000</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>(1, 2) + (3)</td>
<td>2000</td>
<td>4 + (5)</td>
<td>3600</td>
<td>(1, 2) + (3) + (4, 5)</td>
<td>5600</td>
<td>11200</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>(1, 2) + (3)</td>
<td>2000</td>
<td>4 + (5)</td>
<td>3600</td>
<td>(1, 2) + (3, 4, 5)</td>
<td>4700</td>
<td>10300</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>(1, 2, 3)</td>
<td>3000</td>
<td>4 + (5)</td>
<td>3600</td>
<td>(1, 2, 3) + (4, 5)</td>
<td>6600</td>
<td>13200</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>(1, 2, 3)</td>
<td>3000</td>
<td>4 + (5)</td>
<td>3600</td>
<td>(1, 2, 3, 4, 5)</td>
<td>7500</td>
<td>14100</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

- It is seen that Case 3 has lower test time as well as number of sessions when compared to Case 6
- Compared to Case 4, Case 3 has lower test time but more TDRs
- The lowest total time is achieved at the highest TDR cost
- The lowest number of TDRs is achieved at a high cost in terms of test time

Conclusions

- Testing of stacked 3D chips is different from non-stacked chip testing, since, in the case of 3D TSV-SICs, the package test requires all chips in the stack to be tested together
- Increase in number of sessions ⇒ Increase in number of TDRs ⇒ Increased Cost
- Core tests of different chips performed simultaneously during package test may lead to reduction in the total test time
- This also leads to lower TDR cost