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A 24-GHz Quadrature Receiver Front-end in 90-nm CMOS

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Abstract — A 24 GHz quadrature receiver front-end in 90-nm CMOS is presented. It consists of a two-stage LNA, passive mixers, and a QVCO. The RF input is single-ended and is converted to differential form in the first LNA stage. The LNA has two bands of operation within the frequency range of the QVCO. The oscillator measures a centre frequency of 23.7GHz with a 7.2% tuning range, a worst case phase noise over the tuning range of -102 dBc/Hz at 1MHz offset, and a power consumption of 22mW. The front-end achieves; 18dB conversion gain, 8.9dB NF, -23dBm ICP1dB, -11dBm IIP3, 12dBm IIP2, and a power consumption of 42mW (excluding QVCO).

Index Terms — CMOS integrated circuits, Frequency conversion, Microwave mixers, Microwave oscillators, Microwave receivers, Phase noise, Voltage controlled oscillators.

I. INTRODUCTION

With an increasing demand for high data rates, wireless communication systems utilize more and wider bands at higher frequencies. The evolution of Si CMOS has made it a viable technology for cost sensitive radio transceivers operating at micro-wave and millimeter-wave frequencies. Publications have demonstrated high performance for silicon receivers in the Industrial, Scientific, and Medical (ISM) bands at 60 GHz [1]-[2], and 24 GHz [3]-[4].

In this paper we present measurement results of a quadrature receiver front-end consisting of a two-stage LNA, passive mixers, and a quadrature voltage controlled oscillator (QVCO). The performance of the QVCO has been measured separately. Differential topologies are known to have a higher linearity and better stability compared to single-ended topologies, at the cost of higher power consumption. The larger part of the front-end is therefore designed using differential topologies. However, the RF input signal to the chip is single-ended and is converted to differential form in a merged LNA and balun implemented in the first stage of the LNA [4]-[5]. This eliminates the need for an external RF input balun.

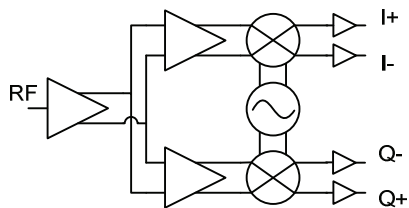


Fig. 1. Front-end block schematic.

II. CIRCUIT DESIGN

The block schematic of the front-end is shown in Fig. 1. The implementation consists of a two-stage LNA with separated second stages for the I and Q branches, passive double balanced mixers, a QVCO, and open-drain IF output buffers. The separated second LNA stages isolate the two passive mixers from each other, minimizing performance degradation due to mixer interaction.

A. LNA and Mixer

The first and second stages of the LNA are shown in Fig. 2(a), and Fig. 2(b), respectively. The first stage consists of a differential common gate (CG) stage with cascode devices for increased isolation. CG stages are known to provide wide band input match. Although the stage is differential, a single ended input is used, connected to one of the differential input terminals. Capacitive cross-coupling with capacitors C1 is used to increase the noise performance, and also to make the stage perform as a balun. The differential output signal is achieved through the capacitive cross-coupling and the coupling of the differential source inductor, L_a , [4]-[5]. A capacitive cross-coupling technique, with capacitors C2 and C3, is used also at the output. The purpose is to further increase the differential isolation by cancelling the currents due to the drain-source conductance for differential signals [4]. The output of the first stage is loaded by the inputs of the two second stages, one for I branch and one for Q, and is tuned to the operating frequency by the differential inductor L_b . The second stage consists of a differential common source (CS) stage with cascode devices and capacitive cross-coupling.

Both LNA stages have a small varactor in the resonator enabling two frequency bands of operation, denoted hereon after as (00) and (11). The varactors were sized for a 4% frequency difference between the two bands. The lower band, (00), is enabled when the varactor control voltages are at ground potential, whereas the upper band, (11), is enabled when the control voltages are at the same potential as the supply.

The two LNA stages provide sufficient gain for passive mixers to be used. In each branch, the output of the second LNA stage is loaded by the input impedance of a mixer and is tuned to the operating frequency by the differential inductor L_c . Inductor data for the LNA is shown in Table I. The passive double-balanced mixer is shown in Fig. 3(a). To facilitate measurements, the mixer outputs are connected to

open-drain output buffers designed to drive 50 Ohms. The buffer schematic is shown in Fig. 3(b).

B. QVCO

The oscillator schematic is shown in Fig. 4. The QVCO consists of two differential LC oscillators coupled through capacitor C_c to oscillate in quadrature. The source node inductor, L_d , and the capacitor in parallel with the FET current source form a source node filter [6]. The filter is designed to not dominate over the capacitive coupling of the source nodes. As long as the oscillator works in the current limited region the second-order harmonics of the source nodes will be in anti-phase, and the two VCO outputs will have a quadrature phase relation to each other [7]-[9]. Inductor data for the QVCO is also shown in Table I.

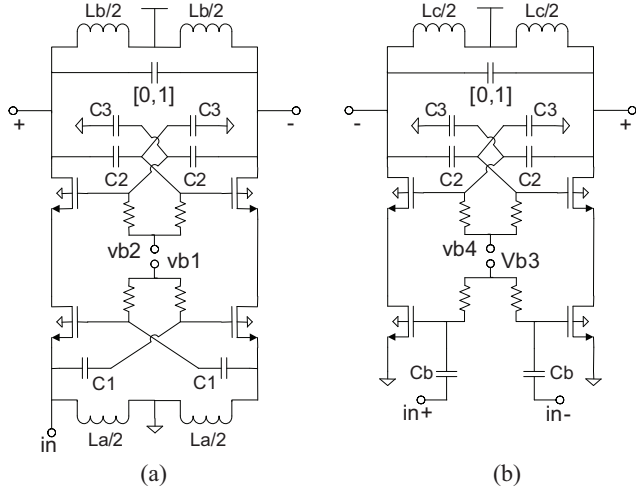


Fig. 2. LNA. (a) The input stage. (b) The second stage.

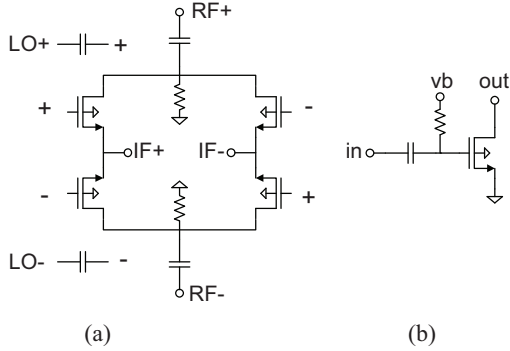


Fig. 3. (a) Passive mixer. (b) Open-drain output buffer.

III. MEASUREMENTS

The circuits were implemented in a 90nm RF CMOS process. The layouts were designed as symmetrical as possible to minimize amplitude and phase errors. Die microphotographs of the complete front-end and a separate QVCO are shown in Fig. 5(a), and Fig. 5(b), respectively. The RF input can be seen on the left side of the front-end die. The supply, bias and IF output signals were wire bonded

from the chip to a PCB. Decoupling capacitors were used both on chip and PCB for the supply and bias lines. The oscillator output signal pads are on the top side of the QVCO die, and the supply and bias pads on the bottom side.

TABLE I
INDUCTOR DATA

| Inductor | Turns | Inductance (pH) | Q | fs (GHz) |
|----------|-------|-----------------|------|----------|
| La | 3 | 554 | 18.4 | 74.1 |
| Lb | 2 | 300 | 20.8 | 95.6 |
| Lc | 2 | 476 | 22.2 | 75.3 |
| Ld | 2 | 245 | 14.5 | 111.8 |
| Le | 2 | 290 | 20.6 | 100.2 |

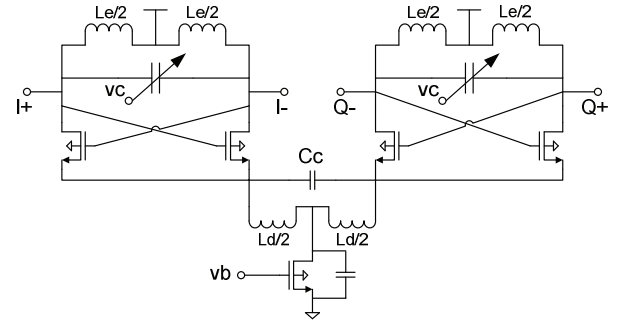


Fig. 4. QVCO schematic.

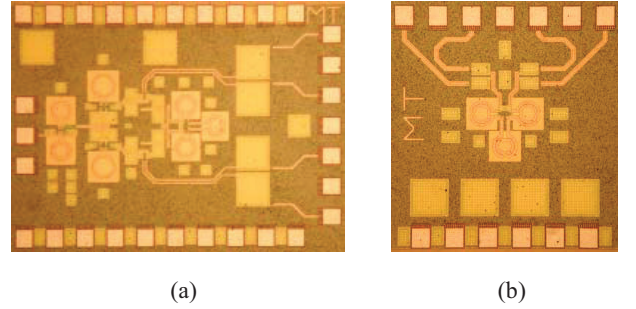


Fig. 5. Die microphotographs. (a) Complete front-end including QVCO (1075μm x 800μm). (b) Separate QVCO (650μm x 720μm).

Two different samples of each front-end and QVCO have been measured. The measurements were performed using on-chip probes from Cascade Microtech. Infinity RF probes were used for the front-end RF input and the QVCO output signals, and a 6 needle DC Quadrant probe was used for the QVCO biasing.

The performance of the oscillator was measured at a power consumption of 21.6mW from a 1.2V supply for the QVCO core, and the open-drain buffers were biased to a drain voltage of 1 V and a current of 6.5mA per buffer. The tuning characteristic of oscillator can be seen in Fig. 6. As can be seen in the figure the tuning range is 7.2%. The output power from the buffers is between -1.8dBm and -0.6dBm over the tuning range. The phase noise was measured with a Europtest PN9000 phase noise measurement system together with an

external down conversion mixer. The phase noise versus varactor control voltage is shown in Fig. 7. The legend of the figure includes the phase noise figure of merit (FOM), calculated at 1 MHz offset frequency using (1), where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L(\Delta f)$ the phase noise at Δf .

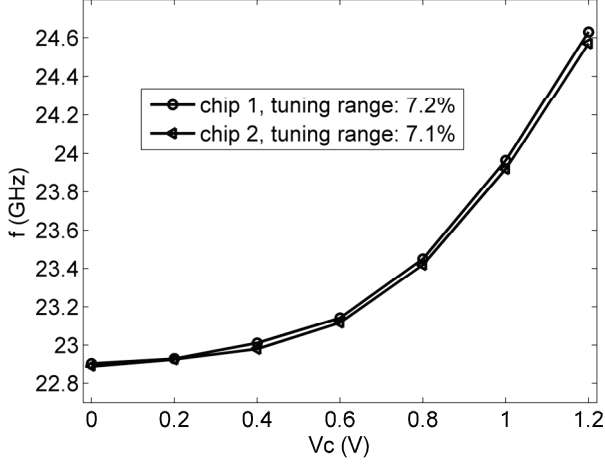


Fig. 6. QVCO frequency tuning characteristic.

$$FOM = 10 \log_{10} \left(\left(\frac{f_0}{\Delta f} \right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P} \right) \quad (1)$$

A performance comparison with some previously reported QVCOs and this work is shown in Table II. The table also includes the figure of merit taking the tuning range into account, FOM_T (2).

$$FOM_T = 10 \log_{10} \left(\left(\frac{f_0 \cdot \text{tuning}(\%)}{10 \cdot \Delta f} \right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P} \right) \quad (2)$$

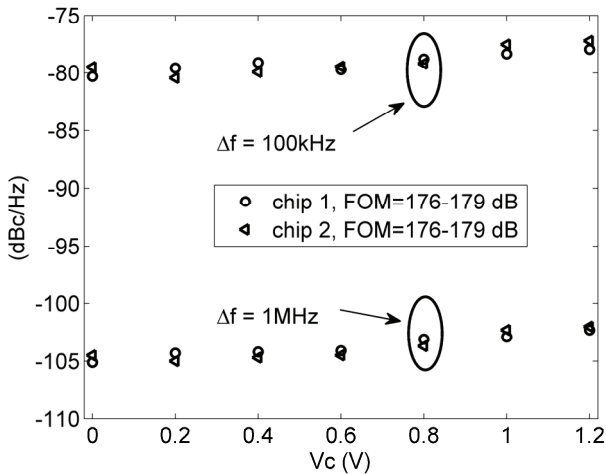


Fig. 7. Phase noise versus varactor control voltage.

The performance of the front-end was measured at a power consumption of 41.8mW from a 1.1V supply, excluding the power consumption of the QVCO. The open-drain buffers were biased to a drain voltage of 1 V and a current of 6mA per buffer. The measured input match, for both LNA bands, is shown in Fig. 8.

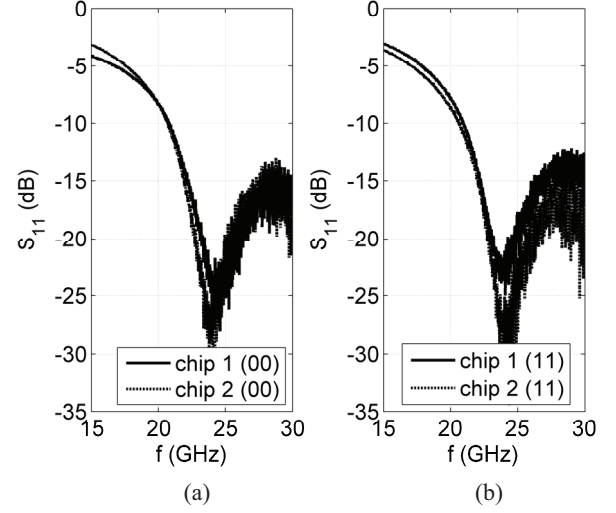


Fig. 8. Front-end input match. (a) The (00) band. (b) (11) band.

The measured and de-embedded conversion gain and noise figure for an IF of 10MHz is shown in Fig. 9. In the (11) band the conversion gain and NF measures 18.1 dB and 8.9 dB, respectively, and in the (00) band the conversion gain and NF measures 15.7 dB and 9.5 dB.

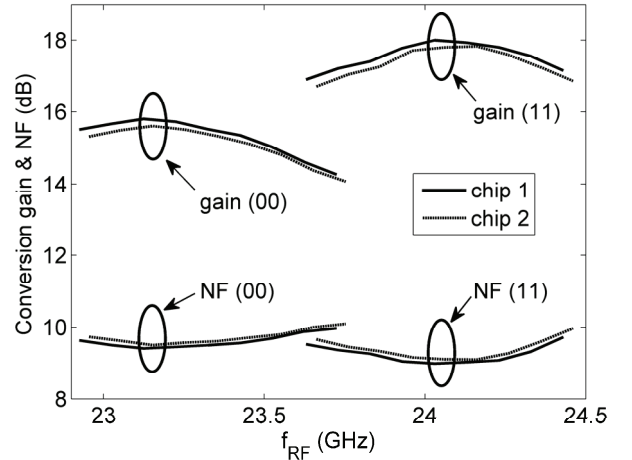


Fig. 9. Front-end conversion gain and NF.

The front-end linearity was measured and summarized in Table III, where the result is an average of the two measured samples. The linearity was measured using two-tone tests, one for third order and one for second order intermodulation. The tones were chosen such that the intermodulation product of interest occurred at an IF of 3MHz. A fifth order passive low-pass filter with a cut off frequency of 5 MHz was used when measuring the second order nonlinearity. This

TABLE II
SUMMARY OF SOME PREVIOUSLY REPORTED QVCOs AND THIS WORK

| Ref. | Technology (μm) | Frequency (GHz) | P_{DC} (mW) | PN@1MHz* (dBc/Hz) | FOM (dB) | FOM _T (dB) |
|-----------|---------------------------------|--------------------|-------------------------|----------------------|-------------|--------------------------|
| This work | CMOS 0.09 | 22.9-24.6 | 21.6 | -102* | 176 | 174 |
| [10] | CMOS 0.13 | 24.19-25.25 | 24 | -111.6* | 186 | 178 |
| [11] | CMOS 0.18 | 10.18-11.37 | 11.8 | -118.7 | 188 | 189 |
| [12] | CMOS 0.13 | 44.8-45.8 | 40 | -98.9 | 176 | 163 |
| [13] | SiGe 0.40 | 24.8-28.9 | 129 | -84.2 | 152 | 156 |
| [14] | SiGe 0.25 | 30.6-32.6 | 140 | -97 | 166 | 162 |

* worst case phase noise over the tuning range

prevented the intermodulation of the first order IF output tones in the spectrum analyzer from affecting the measurement result.

TABLE III
FRONT-END LINEARITY

| Band | CP _{1dB} (dBm) | IIP3 (dBm) | IIP2 (dBm) |
|------|----------------------------|---------------|---------------|
| (00) | -21.4 | -10.3 | 13.7 |
| (11) | -22.8 | -11.2 | 12.1 |

The quadrature phase error of the complete front-end including QVCO was measured with a digital oscilloscope at an IF of 10MHz, Fig. 10. The quadrature error is below 6 and 8.5 degrees in the (00) and (11) band, respectively.

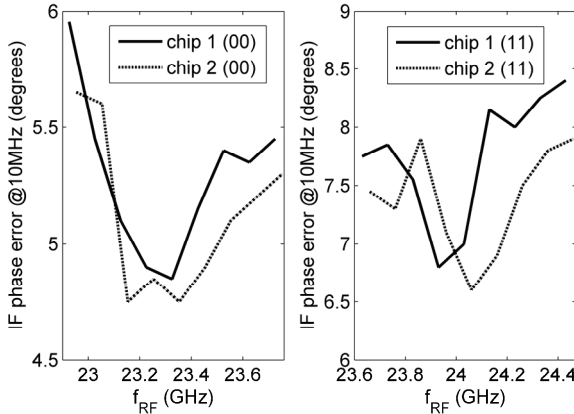


Fig. 10. Front-end IF quadrature phase error.

The oscillator leakage to the front-end RF input was also measured. The measured LO power at the RF port was below -84dBm over the VCO tuning range for both LNA frequency bands. This low value was achieved by using an on-chip oscillator, a symmetric layout, and cross-coupled cascodes in the LNA.

IV. CONCLUSION

A complete 24 GHz RF front-end featuring LNA, passive mixers, and QVCO, has been implemented in a 90-nm RF CMOS process. The LNA has two bands of operation within the tuning range of the QVCO. Measurement results for the complete front-end have been presented and the oscillator performance was also measured separately.

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