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Vertical Heterojunction InAs/InGaAs Nanowire MOSFETs on Si with I_{on} = 330 μA/μm at I_{off} = 100 nA/μm and V_D = 0.5 V

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Abstract

We present vertical InAs nanowire MOSFETs on Si with an $In_{0.7}Ga_{0.3}As$ drain. The devices show I_{on} and g_m/SS record performance for vertical MOSFETs and I_{off} below 1 nA/μm at V_D 0.5 V. We show a device with g_m=1.4 mS/μm and SS=85 mV/dec, therefore having Q-value (g_m/SS) of 16. The device has I_{on}=330 μA/μm and 46 μA/μm at I_{off} 100 nA/μm and 1 nA/μm, respectively. Furthermore, we show a device with SS=68 mV/dec and I_{on}=88 μA/μm at I_{off} 1 nA/μm and V_D 0.5 V.

Introduction

Performance evaluations have shown performance advantages for vertical MOSFETs at the 5 nm node, which makes them a viable option for extending the CMOS roadmap [1]. The vertical structure allows decoupling of the footprint from the gate-length and simultaneously reduced I_{off} due to the lack of substrate leakage. The III-V compound semiconductors, InAs and InGaAs, have shown improved performance compared to Si [2, 3]. However, III-V MOSFETs are typically not integrated on Si and suffer from comparably high I_{off} due to the narrow band gap and parasitic substrate leakage. Previously planar InGaAs MOSFETs on III-V substrates have achieved I_{off} 1 nA/μm by introducing wider band gap on drain side [4, 5]. In this work, we demonstrate vertical III-V nanowire MOSFETs on Si having I_{off} below 1 nA/μm by introducing a gate-all-around structure and an InGaAs drain. We further demonstrate a device with g_m=1.4 mS/μm, SS=85 mV/dec and I_{on}=330 μA/μm at I_{off} 100 nA/μm and V_D 0.5 V.

Fabrication

Process flow and schematics of the MOSFETs are shown in fig.1. The fabrication is started by growing a 300-nm-thick InAs n^+ source contact on the Si substrate by Metal Organic Vapor Phase Epitaxy and is followed by fabrication of three differently sized electron beam lithography defined gold particles (diameters 32, 36, and 40 nm). The nanowires are grown by the VLS method and includes 100 nm undoped InAs and a transition to highly doped $In_{0.7}Ga_{0.3}As$, which also overgrows the entire nanowire. The core diameter corresponds to the gold particle diameter, while the shell thickness is approximately 5 nm.

The MOSFET processing utilizes a self-aligned gate-last process in order to reduce the access resistance [6]. The process starts by forming a 10-nm-thick W/TiN top-metal contact with a contact length L_c= 200 - 300 nm. A 50-nm-thick SiO_2 bottom spacer is then formed. Using the top metal and the bottom spacer as masks, the channel region is digitally etched by ozone oxidation and HCl wet etching until the highly doped shell is removed. An atomic layer deposited 1 nm / 4 nm Al_2O_3/HfO_2 bilayer (EOT ~ 1.5 nm) is deposited before applying 60-nm-thick W gate-metal. The device is finalized by depositing a S1813 resist spacer, formation of via holes and metal contacts.

Results

Transfer characteristics of a device with a total gate length (L_g) of 260 nm (the gate length without contact overlap, $L_{g,eff}$, 160 nm) and channel diameter of 28 nm is shown in fig. 2. The device has a g_m = 1.4 mS/μm and SS = 85 mV/dec, corresponding to the highest Q-value (g_m/SS = 16) and I_{on} (330 μA/μm) at I_{off} 100 nA/μm (V_D = 0.5 V), reported for vertical MOSFETs. Furthermore, this is the first demonstration of a non-planar, III-V MOSFET on Si achieving I_{off} = 1 nA/μm. The output characteristics of the same device, fig. 3, shows good saturation and on-resistance (R_{on}) of 690 Ωμm. The device has the same SS at V_D = 50 mV and V_D = 500 mV, as shown in fig. 4. The device also shows good electrostatics by having DIBL = 88 mV/V at 1 μA/μm.

Fig. 5 shows transfer characteristics of a device with a diameter of 35 nm and effective L_g = 145 nm. The device has SS = 68 mV/dec and g_m = 0.58 mS/μm. The MOSFET in fig. 5 has good I_{on} at I_{off} 1 nA/μm due to the low SS, showing I_{on} 170 μA/μm and 88 μA/μm at I_{off} 100 nA/μm and 1 nA/μm, respectively. Fig. 6 shows the transfer characteristics of a device with diameter 24 nm and $L_{g,eff}$ = 130 nm at V_D between 0.3 V and 0.8 V. The device has I_{off} below 100 nA/μm at all measured V_D while I_{on} increases as a function of V_D.

Fig. 7 (a)-(d) show I_{on} at different I_{offs} (1, 10, and 100 nA/μm, respectively) for 18 devices fabricated on the same sample plotted versus R_{on} (a), SS (b), diameter (c), and g_m (d). The statistics demonstrate that I_{on} at I_{off} 1 nA/μm is limited by SS, hence limited improvements are seen with improved on-state metrics. In contrast, I_{on} at I_{off} 100 nA/μm is limited by on-state metrics, hence clear improvements are observed with improved R_{on} and g_m.

Table 1 summarizes the two most significant devices in the data set, one with the highest I_{on} and Q-value and one with the lowest SS. Fig. 8 benchmarks the devices versus state-of-the-art vertical MOSFETs. A clear improvement in g_m/SS is demonstrated. Fig. 9 benchmarks I_{on} of the best devices versus the best III-V MOSFETs demonstrated. Our devices show clear improvement compared to vertical MOSFETs, although state-of-the-art planar/lateral MOSFETs still have higher I_{on}. This is mainly due to the high contact resistance of the vertical devices.

Conclusions

We have fabricated vertical heterojunction InAs/InGaAs MOSFETs. We have shown a device with g_m = 1.4 mS/μm and SS = 85 mV/dec. The device has I_{on} 330 μA/μm and 46 μA/μm at I_{off} 100 nA/μm and 1 nA/μm (V_D=0.5), respectively. Furthermore, we have shown a device with g_m = 0.58 mS/μm, SS = 68 mV/dec and I_{on} = 88 μA/μm at I_{off} = 1 nA/μm.

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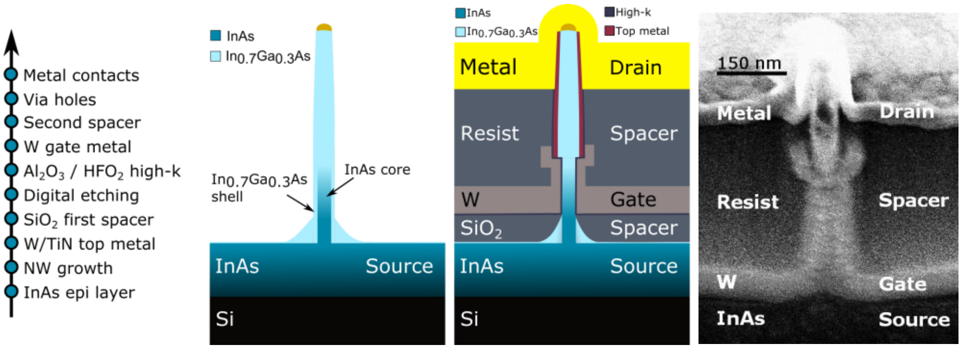

Fig. 1 Illustrations of the process flow (a), cross-section schematic of the device after growth (b), cross-sectional schematic of the finalized device (c) and scanning electron micrograph of the finalized device.

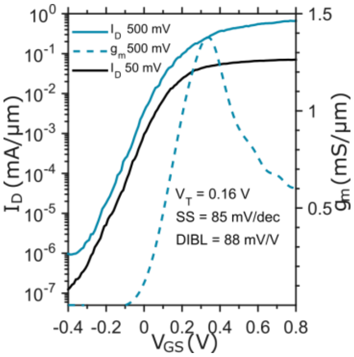

Fig. 2 Transfer characteristics of the device with $L_{g,eff}$ 160 nm and diameter 28 nm.

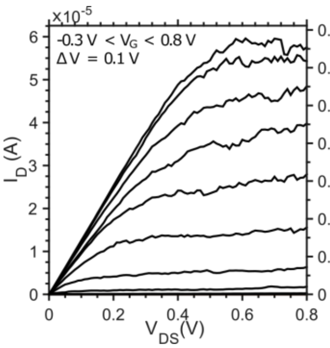

Fig. 3 Output characteristics of the device with $L_{g,eff}$ 160 nm and diameter 28 nm.

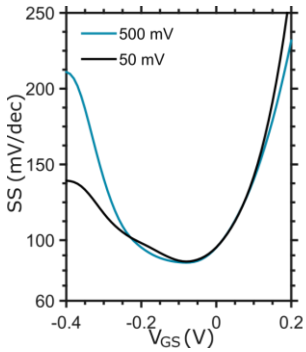

Fig. 4 Subthreshold swing of the device with $L_{g,eff}$ 160 nm and diameter 28 nm.

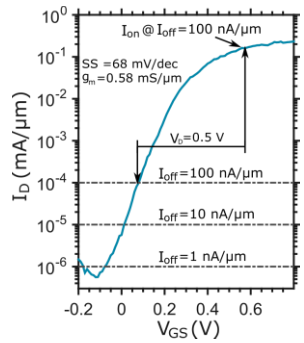

Fig. 5 Transfer characteristics of the device with $L_{g,eff}$ 145 nm and diameter 35 nm. The figure shows also I_{on} defined by V_D and I_{off}.

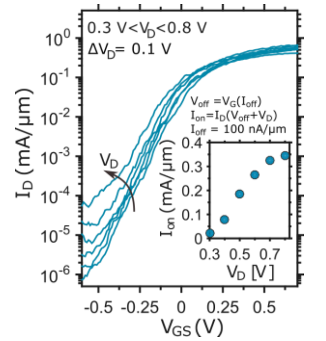

Fig. 6 Transfer characteristics of the device with diameter 24 nm and $L_{g,eff}$ 120 nm. Inset shows I_{on} (defined as in fig. 5) at I_{off} 100 nA/μm.

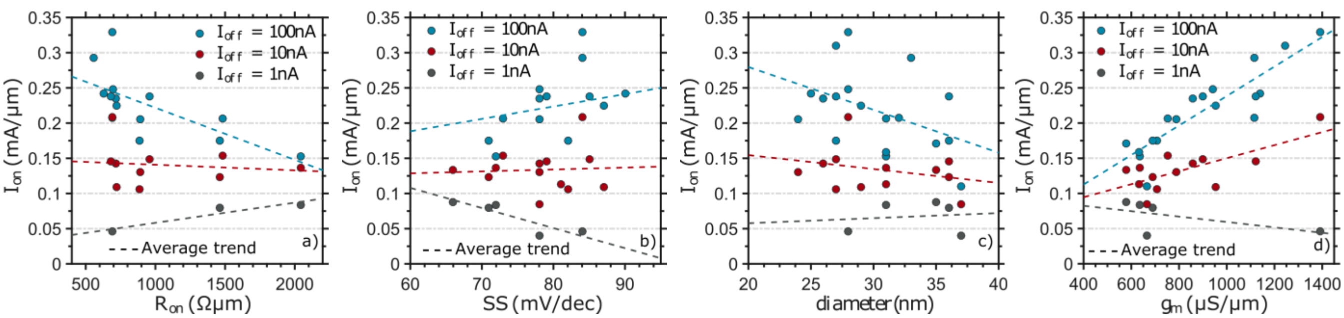

Fig. 7 I_{on} of 18 devices at different I_{offs} (1, 10 and 100 nA/μm) and V_D=0.5 V plotted versus R_{on} (a), *SS* (b), diameter (c) and g_m (d). The statistics shows that I_{on} at I_{off} 100 nA/μm is mostly dependent on R_{on} and diameter, while I_{on} at I_{off} 1 nA/μm is mostly dependent on *SS*. The dashed lines describe the average trend to guide the eye.

Table 1 Metrics of two devices, one with the best Q-value and one with the best SS.

Metric (V_d=0.5V)	**High I_{on} device**	**Low SS device**
SS	85 mV/dec	68 mV/dec
g_m	1.40 mS/μm	0.58 mS/μm
I_{on} at I_{off} =100 nA/μm	330 μA/μm	170 μA/μm
I_{on} at I_{off} =1 nA/μm	46 μA/μm	88 μA/μm
diameter	28 nm	35 nm
$L_{g,eff}$	160 nm	145 nm

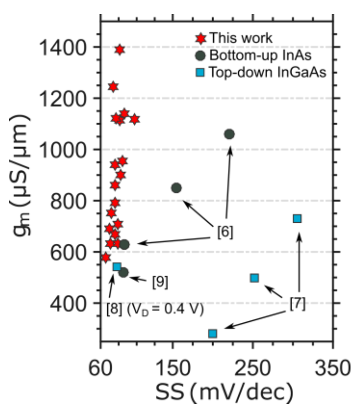

Fig. 8 The devices benchmarked versus the state-of-the-art vertical III-V MOSFETs.

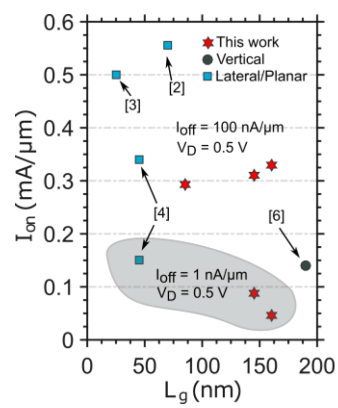

Fig. 9 The best devices benchmarked against state-of-the-art planar, lateral and vertical III-V MOSFETs.