A fully integrated 2.45 GHz 0.25 mu m CMOS power amplifier

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A FULLY INTEGRATED 2.45 GHz 0.25μM CMOS POWER AMPLIFIER

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ABSTRACT

A fully integrated differential class-AB power amplifier has been designed in a 0.25um CMOS technology. It is intended for medium output power ranges such as Bluetooth class I, and has an operating frequency of 2.45GHz. By using two parallel output stages that can be switched on or off, a high efficiency can be achieved for both high and low output power levels. The simulated maximum output power is 22.7 dBm, while the maximum power-added efficiency is 22%.

I. INTRODUCTION

With the recent emergence of short-range communication standards such as Bluetooth, the research interest for highly integrated power amplifiers (PAs) has increased [1-13]. For frequencies up to several GHz and low to medium output power, CMOS may be an alternative to stand-alone power amplifiers, offering a higher level of integration in a relatively cheap technology, in exchange for less efficiency and a lower maximum output power.

In most communication systems transmitter output power control is required. In order to increase the battery lifetime, it is important to have a relatively high efficiency over the whole PA output power range, i.e. for both lower and higher output power, since the PA is more likely to operate at lower than higher output power.

For the Bluetooth standard the highest output power is 20 dBm (class I, [14]) which is feasible for CMOS implementation (see [1-13]). Moreover, a constant envelope modulation scheme is used, implying that linearity of the PA is not a critical issue for this standard.

In this work a class-AB power amplifier is described that consists of two stages, with the output stage comprising two parallel blocks that may be switched *on* or *off* (see fig. 2). In this way the efficiency may be optimized for different output power settings. The output impedance transformation network is fully integrated.

The paper is structured as follows: First some PA theory is described, then the design itself is presented. Simulation results are shown in Section 4, and finally conclusions are presented.

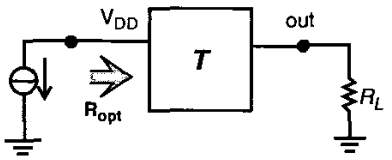

Figure 1. Principle of impedance transformation.

II. ANALYSIS

In fig. 1 a current source with impedance transformation network *T* is shown. This serves as a model for an ideal output stage, where the transistor operates as a controlled current source driving R_{opt}, the transformed load impedance R_L. The maximum signal amplitude is V_{DD}, and the ideal maximum output power is given by

$$P_{out,max,ideal} = \frac{V_{DD}^2}{2R_{opt}} \qquad (1)$$

Thus, for a given V_{DD}, R_{opt} determines $P_{out,max}$ assuming a maximum voltage swing. For $P_{out,max}$ = 22 dBm and V_{DD} = 3.3 V, the optimum load resistance R_{opt} is equal to 34 Ω.

The power added efficiency (PAE) is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \qquad (2)$$

where P_{DC} is the power supplied by the battery, which is signal-dependent for most types of PAs. The PAE typically is maximum for an output power close to $P_{out,max}$ and decreasing fast for lower output powers [5]. Therefore, for a high average efficiency, the PA may be designed to have different $P_{out,max}$ by changing R_{opt} or V_{DD}. In this work the former strategy is used.

Non-idealities

For high voltage swings the transistor will enter the linear region, and no longer behave as an ideal current source. This is commonly modeled with the knee voltage V_{knee} [15]. The output voltage swing is reduced to V_{DD} - V_{knee}, and the maximum output power may be written as

$$P_{out,max} = \frac{(V_{DD} - V_{knee})^2}{2R_{opt}} \qquad (3)$$

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Assuming an output stage with an integrated current-supplying inductor and a switch at V_{DD}, allowing the whole stage to be turned *on* or *off*, other non-idealities may be identified such as the series resistance of the inductor and the on-resistance of the supply switch, both reducing the bias voltage at the drain. Moreover, the finite output impedance of the transistor and the finite quality factor Q of the passives in the matching network will cause power loss. To compensate for these losses, a PA is generally designed for a higher $P_{out,max}$ by reducing R_{opt} in Eq. 3.

III. DESIGN

A fully integrated 2.45 GHz PA was implemented in a 0.25um CMOS technology. In order to implement different output power settings and increase the average efficiency, two parallel output blocks were used (see fig. 2). Due to die size considerations the number of parallel blocks was limited to two.

The matching network was chosen so that a maximum output power of 22 dBm was achieved with both blocks *on*. When one stage is *off*, the matching network provides a higher R_{opt} and thus a lower $P_{out,max}$. In this way a relatively high average efficiency over the total PA output power range can be achieved.

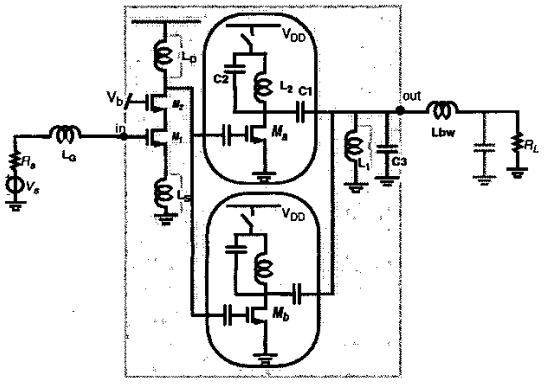


Figure 2. Simplified single-ended schematic of the PA with two parallel output stages.

For the output stage no cascode transistors are used, since this would increase the knee voltage and thus decrease $P_{out,max}$. A switch in the signal path at the output would also have a negative impact on the output power and thus on the efficiency, and was therefore avoided as well.

The input capacitance of the output stage forms a large part of the total capacitance at the drain of M_2 which is parallel to L_D, see fig. 2. When switching *off* one stage (by changing the gate bias to V_{DD} and opening the V_{DD} switch), the input capacitance will change significantly. In order to decrease the impact on input stage tuning, a rather small AC coupling capacitance is used between the input- and output stage.

By connecting the two output nodes as shown in fig. 2, the two parallel stages share L_1, C_3 and L_{bw}. Only C_1, L_2 and C_2 are available to separately design R_{opt} for each stage. Moreover, due to numerous parasitic capacitances and size restrictions of integrated passives, the impedance transformation ratio cannot be varied over a wide range.

Generally when parallel output stages are used, power combining is implemented either through a transformer [3] or transmission lines [5]. In this design, however, the two stages are not isolated, meaning that the network of one stage has an impact on the impedance transformation of the other.

The matching network for one output stage may be drawn as shown in fig. 3. The two output stages are connected at point *P*.

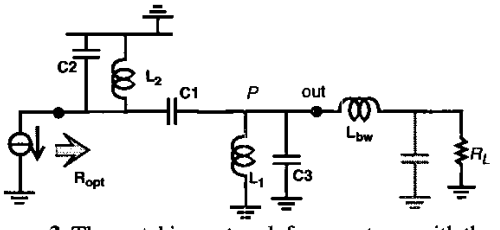


Figure 3. The matching network for one stage, with the FET represented as an ideal current source.

When for example the lower stage in fig. 2 is switched *off*, FET M_b is brought into the linear region, thus providing a low impedance. Assuming this to be a short, one can see from fig. 2 that the equivalent capacitance parallel to C_3 will be larger. This decreases the transformation ratio for the upper stage, thus increasing R_{opt}, which is desirable when only one stage is *on*.

The two stages are unequal, having different FET widths and different capacitance and inductance values, and thus different transformation ratios and gains.

Comparing fig. 2 with fig. 3 one can see that the matching network includes parasitic capacitance at the drain of the FET (incorporated in C_2), as well as the on-chip output node (in C_3).

The 5M1P 0.25um CMOS technology offers thick-metal inductors with quality factors ranging from approximately 5 to 15. For L_2 and L_S inductors provided by the manufacturer were used. L_D and L_1 were designed using Fast Henry [16] and ASITIC [17]. For the integrated matching network, MOM (metal-oxide-metal) capacitors with highest quality (Q) factor available in this technology were used. The FETs M_a and M_b in fig. 2 do not have minimum gate length, but 0.32µm, and have a higher breakdown voltage.

IV. SIMULATION RESULTS

The above described design was simulated using SpectreRF, with BSIM3v3 models. Post-layout parasitics were taken into account. The layout is shown in fig. 4.

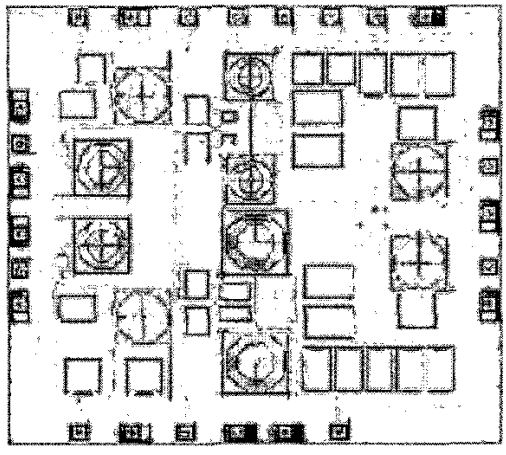
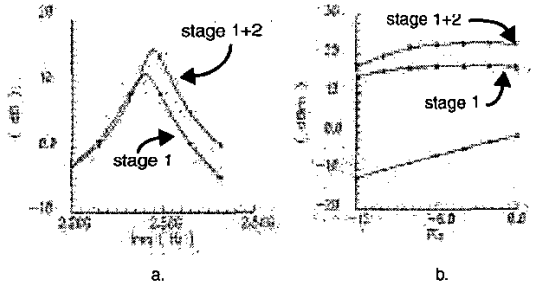


Figure 4. Plot of the PA layout.

A large area is occupied by the integrated passives, and a substantial area saving may be achieved by using differential inductors [18].

In fig. 5 some simulation results are shown.



a. b.

Figure 5. Simulation results, a). Frequency response, b). P_{out} as a function of P_{in}.

The maximum PAE (22 %) is achieved for P_{out} slightly below $P_{out,max}$ (which is about 23 dBm, see fig. 5.b). The center frequency for both cases (stage 1+2 and stage 1 only) is approximately 2.45GHz. The simulation results are summarized in table 1.

From table 2 a comparison can be made between this PA and previously published work. It can be seen that the PA presented in this work performs quite well, given the limitations of an on-chip matching network and class-AB. Moreover, the PA includes measures to improve the average efficiency.

V. CONCLUSIONS

A 2.45 GHz power amplifier has been designed in a 0.25um CMOS technology. The PA is fully integrated, including output matching network. Simulations show that an output power of 22.7 dBm may be achieved with a maximum PAE of 22%. The average efficiency has been improved by using two parallel output stages.

Table 1. Simulation results, summary

PAE_{max}	22%	
P_{out} (differential)	22.7 dBm	@2.45GHz @PAE_{max}
power gain	28 dB	@PAE_{max}
total die area	6.25 mm^2	including pads
P_{out} (stage1 only)	17.2 dBm	PAE=15.8%
P_{out} (stage 2 only)	12.4 dBm	PAE=6.1%

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Table 2. Comparison of medium power PAs

	Pout (dBm)	frequency (GHz)	efficiency (max)	technology	output matching	power control	class
[1]	15 (@P_{-1dB})	0.9	<30% (η)	1um CMOS	off-chip	steps, 5dB	C
[2]	23.5 (max)	1.9	35% (PAE)	0.35 um (Bi)CMOS	off-chip	-	AB
[3]	33.4 (@max PAE)	2.4	31% (PAE)	0.35um (Bi)CMOS	on-chip	-	E/F3
[4]	28.2	1.9	30% (PAE)	30GHz BiCMOS	off-chip	-	AB
[5]	24.8 (max)	1.4	49% (PAE)	0.25um CMOS	off-chip (transm. lines)	3 parallel stages	F
[6]	31.8 (max)	0.9	43% (PAE)	0.2um CMOS	off-chip	-	F
[7]	30 (@max. PAE)	1.8	45% (PAE)	0.35um CMOS	off-chip	-	AB
[8]	20 (max)	1.9	16% (η)	0.8um CMOS	on-chip	-	F?
[8]	22 (max)	2.4	44% (η)	0.25um CMOS	off-chip	-	F?
[9]	17.5 (max)	2.4	16.4% (PAE)	0.35um CMOS	partly on-chip	-	A
[10]	23 (max)	2.4	42% (PAE)	0.18um CMOS	off-chip	-	AB
[11]	30 (max)	0.7	62% (PAE max)	0.35um CMOS	partly on-chip	-	E
[12]	9 (@P_{-5dB})	2.4	16% (P_{-5dB})	0.18um CMOS	partly on-chip	-	AB?
[13]	18.6 (@max PAE)	0.9	30% (PAE max)	0.6um CMOS	on-chip	-	C
this work	22.7 (@max PAE)	2.45	22% (PAE max)	0.25um CMOS	on-chip	2 settings	AB