LUND UNIVERSITY

Optimization of High-κ films on Si Substrate

Fabrication and characterization

A Master of Science Thesis

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Abstract

In the present diploma project work, metal oxide semiconductor capacitors were fabricated on Silicon substrate. The oxide layer was formed by atomic layer deposition of high permittivity materials, HfO_2 and Al_2O_3. The high-κ films were grown using 65 ALD cycles at various deposition temperatures. For each deposition temperature, a series of samples were prepared using different precursor pulse lengths. The effect of growth conditions were investigated by current-voltage and capacitance-voltage characterization on 42 samples. *C-V* and *I-V* curves of different devices were found to be highly influenced by traps at high-κ/Si interface and border traps within the oxide layer.

HfO_2 film deposited at 250 °C substrate temperature, using 450 ms Hf-precursor pulse length and Al_2O_3 film deposited at 350 °C were shown to have the low density of interface traps and *CV* hysteresis.

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References

1. Introduction

Oxides with high permittivity have been introduced to metal oxide semiconductor (MOS) technology as an alternative to the conventional gate dielectric, silicon dioxide.

The down scaling trend in transistor structures caused SiO_2 gate dielectrics reaching their limit associated with high leakage current at the thickness below 15Å. Using high-κ dielectrics allow having the same capacitance for a thicker oxide layer and lower leakage current. It has been reported that leakage current through HfO_2 dielectric films are several orders of magnitude lower than that of SiO_2 with the same equivalent oxide thickness, 0.9–2 nm [1].

$$\varepsilon_0 \varepsilon_{SiO_2} \frac{A}{EOT} = \varepsilon_0 \varepsilon_{high-\kappa} \frac{A}{t_{ox}} = C \qquad (1.1)$$

Using high-κ materials such as hafnium oxide and Aluminum oxide enables fabrication of field effect transistors with promising device performances, but there are still shortcomings that need to be improved. One of the challenges to fabricate high quality devices is to improve the interfacial layer of the gate oxides with the semiconductor substrate. Defects and imperfections at the interface of high-κ films on silicon and III-V semiconductors as well as charge trapping within the oxide layer affect capacitance-voltage characteristics of devices. One approach to optimize the device performance is to improve the oxide-semiconductor interface.

This work focuses on fabrication and characterization of metal oxide semiconductor capacitors with atomic-layer-deposited HfO_2 and Al_2O_3. The oxides were grown with different ALD conditions, like different precursor pulse lengths and deposition temperatures. The effect of growth conditions on current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) characteristics of the MOS structures was investigated in order to find an optimized condition with reduced frequency dispersion and hysteresis.

2. Background

2.1 Ideal MOS Structure

The MOS structure is a parallel plate capacitor consisting of two electrodes, which are separated by a thin layer of oxide. The first electrode is a metal contact called the gate and the other electrode is a semiconductor material.

In the MOS capacitor of Figure 2-1, the large energy barrier between the metal and the oxide is defined as the work function $q\varphi_m$ for the metal-oxide interface, which is the energy required for an electron to move from the metal Fermi level to the conduction band of the oxide layer. In equilibrium, $q\Phi_m$ is equal to the work function at the semiconductor-oxide interface $q\Phi_s$. This is called flat band condition. There is normally very low current flow from the metal to the semiconductor and vice versa. Thus applying a voltage between the metal and the semiconductor, merely changes surface charge layers in the metal and the semiconductor. There are different charge distributions depending on the applied bias [2], [3]. Figure 2-1 shows the band diagram for an ideal MOS structure with n-type substrate at different bias regimes.

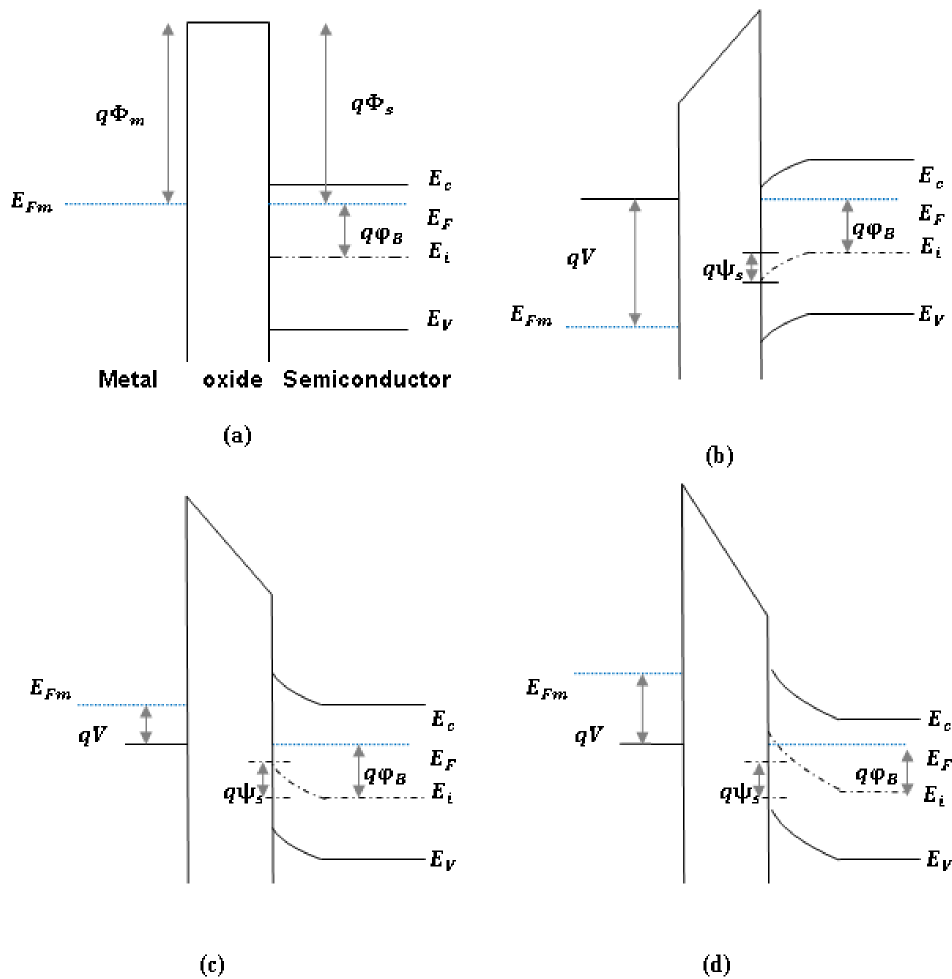


Figure 2-1. Band diagram of an ideal MOS diode in; (a) equilibrium (flat band condition); (b) accumulation; (c) depletion and (d) inversion cases.

When a positive voltage is applied to the gate with reference to the semiconductor, a positive charge density builds at the metal surface. Subsequently, an equal amount of negative charges would be attracted to the surface of the semiconductor in order to preserve charge neutrality

condition (Figure 2-1b). This occurs by accumulation of majority carriers (electrons in an n-type substrate) at the semiconductor-oxide interface. Electrons and holes densities in the semiconductor are given by,

$$n = n_i \exp{(E_F - E_i)/kT}\ ,\ p = n_i \exp{(E_i - E_F)/kT}. \qquad (2.1)$$

Thus, accumulation of electrons at the semiconductor-oxide interface implies an increase in $E_F - E_i$, which causes the energy bands of the semiconductor bending downward near the interface. The applied positive bias raises the electrostatic potential of the metal. As a result, the electron energies decrease in the metal and the metal Fermi level is lowered by qV relative to its equilibrium position. Since Φ_m and Φ_s are not changed with the applied bias, lowering the metal Fermi level causes a tilt in the oxide conduction band to maintain $\Phi_m - \Phi_s = 0$. This tilt is expected because the surface charge layers in the metal and semiconductor establish an electric field across the oxide and the electric field causes a gradient in the energy band.

If we apply a small negative voltage, the electrostatic potential of the metal decreases relative to the semiconductor. The electron energies are raised and the Fermi level of the metal lies above its equilibrium position by $qV.$ The conduction band of the oxide is tilted with respect to the applied field. The negative voltage results in negative charges on the gate surface, repelling the electrons from the semiconductor surface and leaving behind uncompensated positive donor ions. Depletion of electrons from a region near the surface causes $E_F - E_i$ to decrease and the bands bend upward near the semiconductor interface. Figure 2-1c shows the depletion regime.

As the negative bias increases, the bands bend even more and the hole density builds up at the semiconductor surface. At a sufficiently large negative bias, $E_i - E_F > 0$ the density of holes (minority carries) at the surface is much larger than the density of electrons. This condition, which is shown in Figure 2-1d, is called inversion.

As it is explained, for an n-type semiconductor, charge distribution at different bias regimes consists of electrons in the accumulation, ionized donors in depletion and minority carriers (holes) in the inversion layer. In the Figure 2-1, $q\psi_s$ shows the extent of band bending at the semiconductor surface, which varies with respect to the charge distribution in the semiconductor. Thus the semiconductor capacitance C_s varies with the bandbending potential ψ_s. The bandbending ψ_s is the total potential difference between the silicon surface and the bulk [2] and it is defined as

$$\psi_s = \varphi_s - \varphi_B, \qquad (2.2)$$

where φ_s is the surface potential and defined by $E_F - E_i$ at the silicon surface.

2.2 MOS Capacitance-Voltage characteristics

The equivalent circuit of an ideal MOS structure can be simply modeled as a series combination of the semiconductor capacitance, C_s, and the oxide capacitance, C_{ox}. Different charge distributions in accumulation, depletion and inversion make up the semiconductor capacitance at different bias regimes. Therefore, the total capacitance strongly depends on whether the device works in accumulation, depletion or inversion mode.

$$^1/_{C_{tot}} = {}^1/_{C_s} + {}^1/_{C_{ox}} \tag{2.3}$$

A strong positive DC bias raises the density of majority carries on the semiconductor surface. In the case of n-type semiconductor, high density of electrons will result in a large C_s. Hence, in accumulation the total capacitance equals to C_{ox} according to equation (2.3).

If we sweep the voltage toward negative values, C_s decreases. As the bias becomes negative, the semiconductor becomes depleted, so the depletion layer capacitance is in series with C_{ox}. The capacitance decreases as the width of the depletion layer increases. When the inversion is reached, both depletion layer fixed charges and minority carriers (holes) contribute to the semiconductor capacitance and $C_s = C_D + C_I$. At strong inversion, the minority carriers become dominant and inversion layer capacitance C_I is large. Therefore, the total capacitance equals the oxide capacitance. If a small AC signal is superimposed on the gate bias, the small signal capacitance depends on the frequency at which the measurement is done. The capacitance follows different trends at high frequency (typically ~ 1MHz) and low frequency (typically below 100kH) C-V curves.

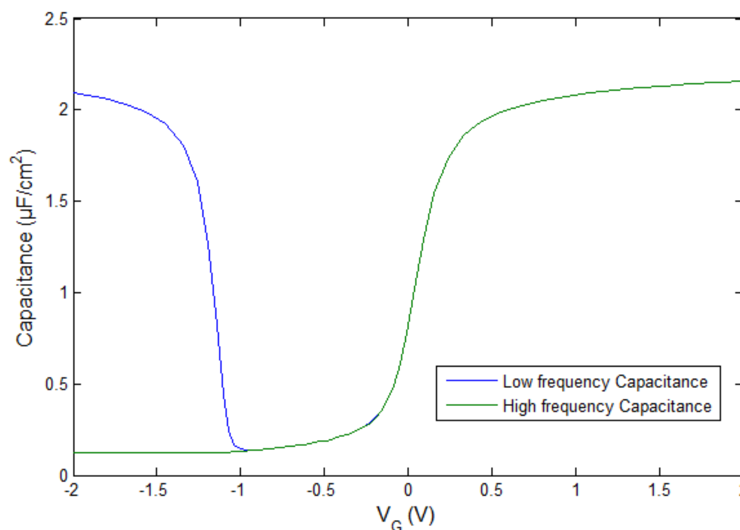


Figure 2-2. High frequency and low frequency C-V curves of an ideal capacitor with EOT of 7.6 nm and dielectric constant of 15 [4].

The difference, which is shown in Figure 2-2, is related to how the minority carriers in the semiconductor respond to the AC voltage. The carriers can follow the AC signal if their time constant $\tau \ll 1/\omega$, where ω is angular frequency of the AC voltage. If the voltage is rapidly varied (high frequency) in inversion region, the minority carriers cannot respond to the AC signal and do not contribute to the small signal capacitance. Therefore the semiconductor capacitance is only formed by the maximum depletion capacitance and is at its minimum (green curve). In contrast if the voltage changes slowly, the minority carriers follow the AC signal and the capacitance in the inversion layer increases to C_{ox}.

2.3 Effect of Interface charges

One of the factors that make real devices deviate from the ideal C-V behavior (Figure 2-2) is defects at the oxide-semiconductor interface and defects within the oxide layer. There are different classifications of them presented in literature based on the location, electrical response, and structure of the defects. Emphasis of this study is more on interface traps and the near interfacial traps in the oxide called border traps.

Interface trap states are defects at the oxide-semiconductor interface, which change occupancy in interaction with majority carriers. Interface trap capacitance is added in parallel to the semiconductor capacitance. Trapped charges make the capacitance stretched-out along the voltage axis. Moreover, at lower frequencies, the interface traps follow the AC signal and results in an increase in the capacitance.

3. Atomic Layer Deposition

Atomic layer deposition (ALD) is proven to be a suitable technique for growing thin dielectric films. This technique provides a good control on thickness, uniformity, quality, and material properties of the grown films.

In this technique, the substrate is alternatively exposed to gas reactants in a vacuum chamber. There are usually two molecular precursors. The deposition process consists of four steps; exposure of the substrate by a pulse of the first precursor, purging the reaction chamber usually by N_2 to remove the by-products and non-reactant gas molecules, exposure of the second precursor, which is followed by an evacuation of the reaction chamber. Figure 2-3 illustrates the sequence of reactions in one cycle of ALD. The film is grown layer by layer as the process is repeated for more cycles. The amount of material, which is deposited in one cycle, is around 1 Å per cycle for HfO_2 and Al_2O_3 [5].

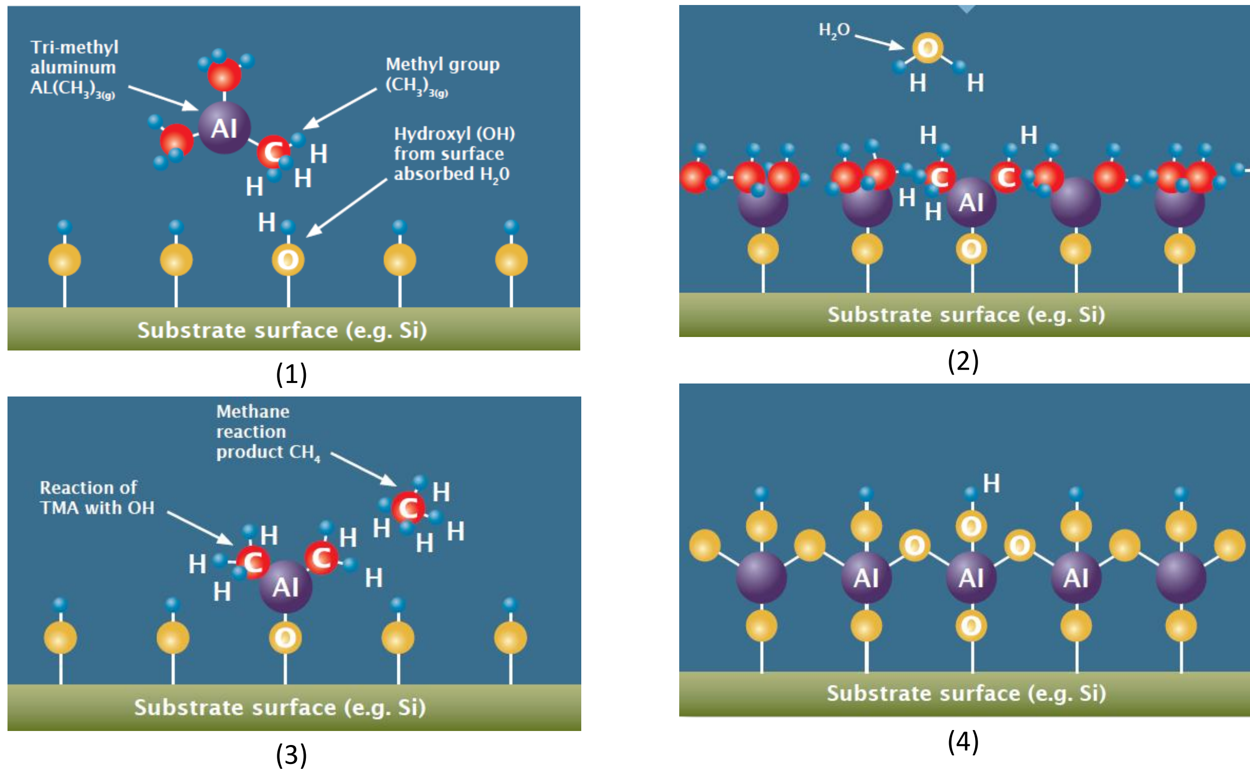


Figure 2-3. An ALD cycle with Trimethylaluminum (TMAl) and H2O precursors to deposit Al_2O_3 [5]

Atomic layer deposition is a self-limiting surface process. As the substrate is exposed to the reactant gas, precursor molecules are adsorbed on the substrate surface making weak bonds on the surface. These weakly adsorbed molecules can be desorbed from the surface or can make strong bonds with the surface reaction sites and be deposited on the surface. In each cycles deposition continues to the point when surface saturation is reached. Therefore, the precursor pulse length should be set above the saturation limit with respect to the duration and the amount. The film thickness grown per cycle is independent of the evacuation time. However, purge time should be long enough to purge all the by-products and excess gas molecules from the chamber. Moreover, ALD process is sensitive to the deposition temperature. Decomposition of the precursors and deposited films at high temperatures increases the contamination content and defects during growth [6]. The self- limiting reaction enables us to control the growth mechanism by changing deposition parameters like exposure time of the precursors and deposition temperature.

4. Experimental

4.1 Fabrication

In the current study, MOS capacitors were fabricated on n-type Si substrates with a (100) crystallographic orientation and thickness of 250-300 μm. Silicon wafers were phosphorus doped with $\mathbf{2 \times 10^{17} cm^{-3}}$ doping concentration. The processing work done, could be divided into two major steps.

1- Deposition of dielectric film by atomic layer deposition.

2- Metallization: Forming top contact (the gate) and ohmic contact to the Si substrate.

A thin layer of native SiO_2 existed on the surface of Si wafers. The thickness of SiO_2 was measured to be around 1.8 nm by using Ellipsometery technique. No chemical surface treatment was done on the substrate prior to film deposition. It is hence expected that films to be a bi-layer combination of SiO_2 and high-κ material.

4.1.1 Deposition of high-κ films with atomic layer deposition

To fabricate a MOS capacitor, the first step is the deposition of the oxide films on the semiconductor surface. Hafnium oxide and Aluminum oxide were deposited using the Cambridge Nano-Tech Savannah 100 (ALD) system.

HfO_2 Deposition:

Tetrakis [dimethylamido] Hafnium (TEMAHf) was used as Hf precursor and H_2O was used as oxidizer. N_2 was used as carrier and purge gas. One cycle of ALD included a pulse of H_2O, 10 s of N_2 purge, a pulse of Hf-precursor and 10 s of N_2 purge. The duration of H_2O pulse was 60 s for all samples. In total 9 samples were prepared. Films were grown at three different deposition temperatures, 100, 250, and 350 °C. For each deposition temperature, growth was done with different Hf-precursor pulse lengths 100 ms, 450 ms, and 1500 ms. Films were deposited using 65 cycles of ALD. The thickness of deposited films were measured by Ellipsometer and presented in Table (1).

Table 1. Thickness (Å) of HfO_2 films grown on Si substrate for 65 cycles of ALD.

T(°C) / Pulse time (ms)	**100**	**250**	**350**
100	80.21	55.30	42.47
450	89.59	56.80	61.24
1500	93.79	50.08	54.32

Al_2O_3 Deposition:

Al_2O_3 films were deposited by subsequent pulses of Trimethylaluminum (TMAl) and H_2O. Similarly, in total 9 samples were prepared with different precursor pulse length and at different temperatures. Films were grown at 100, 250, and 350 °C temperatures using 10, 25, and 100 ms pulses of Aluminum precursor. Other parameters like purge time, oxidizer pulse length and number of ALD cycles were kept the same as the HfO_2 films. The thicknesses of deposited films are indicated in Table (2).

Table 2. Thickness (Å) of deposited Al_2O_3 films on Si substrate with 65 cycle of ALD.

T(°C) / Pulse time (ms)	**100**	**250**	**350**
10	46.60	55.26	49.16
25	47.76	59.76	54.18
100	48.10	60.16	51.43

4.1.2 Metallization

The next step was to deposit a metal contact on the oxide layer. Top contact (the gate) consisted of a layer of Titanium followed by a layer of Gold. 5 nm Ti and 100 nm gold were deposited using evaporation technique. The contacts were patterned by stencil masks during the evaporation. As shown in Figure 4-1, Ti/Au contacts with diameter of 50-200 µm were obtained.

In this part of the processing work, a metal layer should be deposited on the back side of the Si substrate in order to form an ohmic contact to the semiconductor. The back contact was formed by deposition of 50 nm Aluminum using evaporation technique.

Prior to making the back contacts, the back sides of samples need to be cleaned. During the deposition of oxide in the ALD chamber, it is likely that the oxide film is deposited on the back side of the Si wafers. In order to have a good contact, this unwanted oxide layer should be etched before depositing the Aluminum back contact.

The approach was to etch the oxide using a solution of buffered HF. To protect the top oxide layer and the contacts during the chemical etching, the top sides of the samples were coated by a layer of polymer. A layer of resist (S1813) was spun on the sample at 3600 rpm. Then it was baked at 115 °C on the hotplate for 1 minute. After that the sample were immersed in buffered HF solution (1:10). The HfO_2 samples were etched about 5 minutes with an etch rate of 1nm per minute and the Al_2O_3 samples were etched for 5 seconds with the etch rate of 1 nm per second.

After oxide etching, aluminum back contacts were evaporated. Finally, the resist layer was removed by cleaning the sample with Acetone and Isopropanol. The same metallization scheme

followed for all the samples with HfO_2 and Al_2O_3 dielectrics. Figure 4-1 shows a schematic of the samples together with a top view image of a sample taken by an optical microscope.

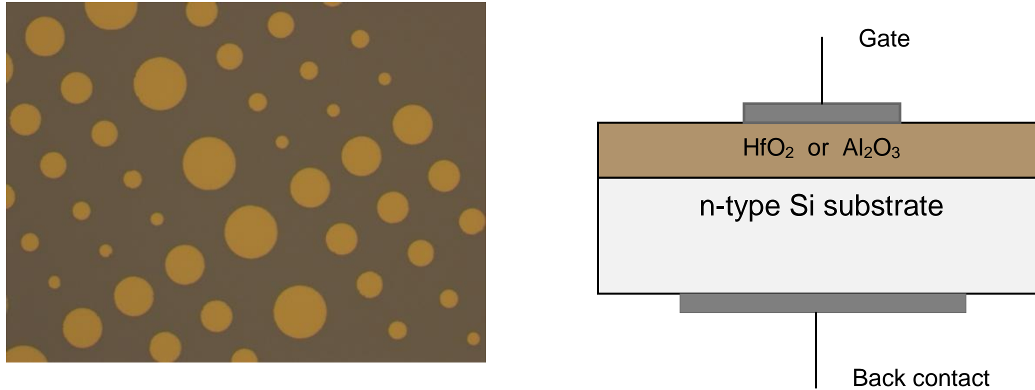


Figure 4-1. Schematic of the prepared MOS structure

4.2 Characterization

The fabricated Ti/HfO_2/Si/Al and Ti/Al_2O_3/Si/Al capacitors were characterized with current-voltage (*I-V*) and frequency dependent capacitance-voltage (*C-V*) measurements.

I-V curves were measured by Keithley 4200 Semiconductor Characterization system. Current was measured as the voltage swept from -2 to 2V. Impedance measurements were done at the same bias range using an Agilent 4294A impedance analyzer at room temperature 300 K. Measurements were done at frequencies of 1 MHz, 100 kHz, 10 kHz and 1 kHz for different samples.

C-V measurements

It is important to determine the actual capacitance of the devices from impedance measurements. Small signal equivalent circuit model of a MOS capacitor consists of three elements as shown in the Figure 4-2a. C is the capacitance of the device, R_p is the parallel resistance due to leakage current through the oxide and R_s is the series resistance of the semiconductor and the contacts. For devices with large leakage current, in which R_p is large or devices with low series resistance, a parallel circuit model in the Figure 4-2b is used that neglects R_s [7].

Doping concentration in the substrates of the fabricated samples and ohmic contact of Al on Si provide a low series resistance, initial characterization of the samples using two-element model showed distortion in the obtained capacitance. Chen et al [8] suggested that in capacitors with high leakage, interface traps recombination contributes to the series resistance. Therefore, R_s contains a frequency dependant term that should be taken into account.

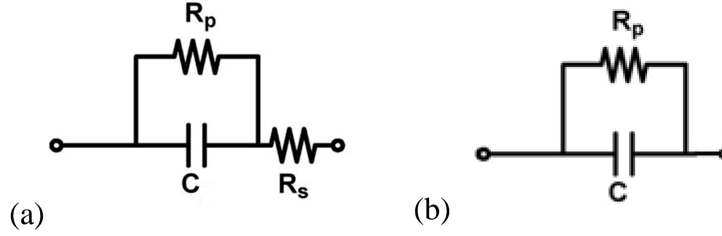


Figure 4-2. Small-signal equivalent circuit model of a MOS capacitor (a) accurate model, (b) parallel circuit model for low series resistance devices.

In this study, high leakage current was measured for the samples and capacitance is extracted from impedance measurements using a three element method developed by Chen. Considering $Re(Z)$ and $Im(Z)$ as real and imaginary parts of the impedance, the measured impedance of the samples is expressed as

$$Z = Re(Z) + jIm(Z) = \frac{R_p + R_s + (\omega C R_p)^2 R_s}{1 - (\omega C R_p)^2} - j\frac{\omega C R_p^2}{1 - (\omega C R_p)^2}, \tag{4.1}$$

where ω is the frequency at which the measurements are done ($\omega = 2\pi f$). As mentioned, we have different DC and AC series resistances.

$$R_{dc} = R_s + R_p \text{ and } R_{ac} = R_s(\omega) + R_p . \tag{4.2}$$

If the difference between DC and AC resistance is defined with a frequency dependent term r(ω), solving equations (4.1) and (4.2) results in

$$R_p = \frac{1}{\omega C}\frac{Re(Z) - R_{dc} - r(\omega)}{Im(z)} \tag{4.3}$$

and

$$C = -\frac{1}{\omega Im(Z)[1 + \left(\frac{1}{\omega C R_p}\right)^2]} . \tag{4.4}$$

The DC resistance across the device is extracted from *I-V* measurements by $R_{dc} = \frac{\Delta V}{\Delta I}$. The obtained capacitance was plotted as a function of gate bias.

4.3 Extracting density of interface traps

There are different methods for determining the density of interface traps. In this part, a brief introduction to two methods that were used in this study is presented.

High frequency capacitance method (Terman method)

This method is based on comparison of a measured capacitance at a high frequency with an ideal capacitance without interface traps. The ideal capacitance is theoretically calculated for a MOS capacitor with the same doping concentration and oxide thickness. As briefly mentioned in Chapter 2, the interface traps capacitance is negligible at high frequencies, thus the high frequency capacitance is determined by

$$C_{HF} = \frac{C_s C_{ox}}{C_s + C_{ox}} \ . \tag{4.5}$$

The semiconductor capacitance varies with the bandbending potential ψ_s. Therefore, at the same bandbending potential, the experimental C_{HF} would be equal to the ideal C_{HF}. It means any C_{HF} at a certain voltage on the experimental curve, corresponds to a bandbending potential with the same capacitor on ideal curve. In order to determine the density of interface traps, D_{it}, we should find how band bending ψ_s changes with voltage.

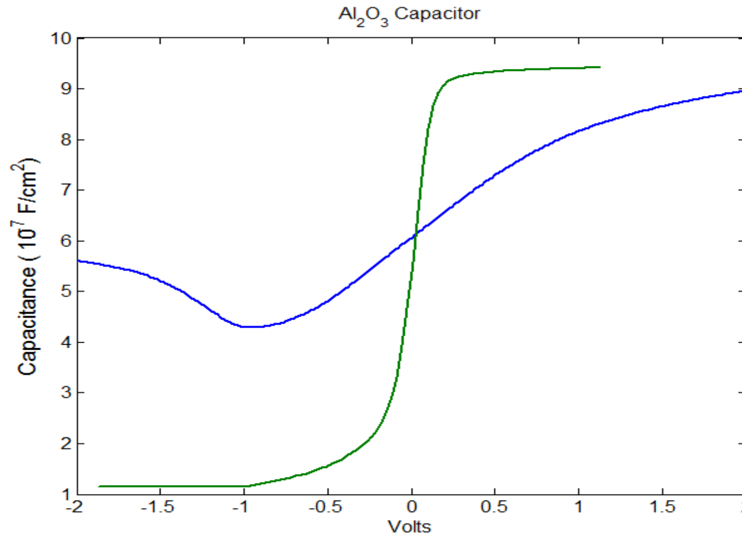


Figure 4-3. A theoretical high frequency capacitance vs ψ_s (V) (green curve) and high frequency measured C-V of an Al_2O_3 capacitor fabricated at deposition temperature of 350 °C and 25 ms Al-precursor.

First step is to plot the ideal high frequency capacitance as a function of the band bending potential ψ_s. Figure 4-3 shows the comparison of an experimental C_{HF} versus $V_G(V)$, with the

ideal $C_{HF}(\psi_s)$ versus $\psi_s(V)$. Then, for each value of the C_{HF}, we extract the corresponding $V_G(V)$ from C-V_G and corresponding $\psi_s(V)$ from C- ψ_s. Repeating this step gives ψ_s as a function of V_G for all of the capacitance range. Differentiation of $\psi_s$versus V_G is used to calculate the capacitance of the interface traps by

$$C_{it}(\psi_s) = C_{ox}\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\psi_s) \quad (4.6)$$

Finally, D_{it} is obtained from$C_{it} = qD_{it}$.

Conductance method

Another method for extracting the density of interface traps is to measure the conductance related to D_{it}as a function of gate bias. The measured admittance is

$$Y = \frac{1}{Z} = G_m + j\omega C_m \ . \quad (4.7)$$

C_m is the equivalent capacitance and G_m is the equivalent parallel conductance. The part of the admittance that is related to the interface trap is obtained by subtracting the oxide capacitance. Finally, the real part is obtained as

$$\frac{< G_p >}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \ . \quad (4.8)$$

The density of interface traps is obtained from the conductance peak by

$$D_{it} \approx \frac{G_{peak}}{0.4\omega q} . \quad (4.9)$$

The methods above give us the density of interface traps as a function of gate bias, since for each V_g, we have the corresponding band bending at the semiconductor surface. We can have D_{it} versus ψ_s. Each value of ψ_s is related to a position in the semiconductor band gap (Figure 2-1). At the interface [2], energy position with respect to the Fermi level is given by

$$\frac{E_c - E_T}{q} = \frac{E_{gSi}}{2q} + \psi_s - \varphi_B . \quad (4.10)$$

Consequently, the energy distribution of interface traps within the band gap is determined.

5. Experimental results

5.1 Current-Voltage Measurements

5.1.1 HfO_2/Si structures

Figure 5-1 shows the current density as a function of voltage. The *I-V* curves were measured for different HfO_2/Si structures in which oxide layers were deposited at temperature of 100, 250 and 350 °C using the Hf- precursor pulse length of 100, 450, and 1500 ms. Five different devices on each structure were measured.

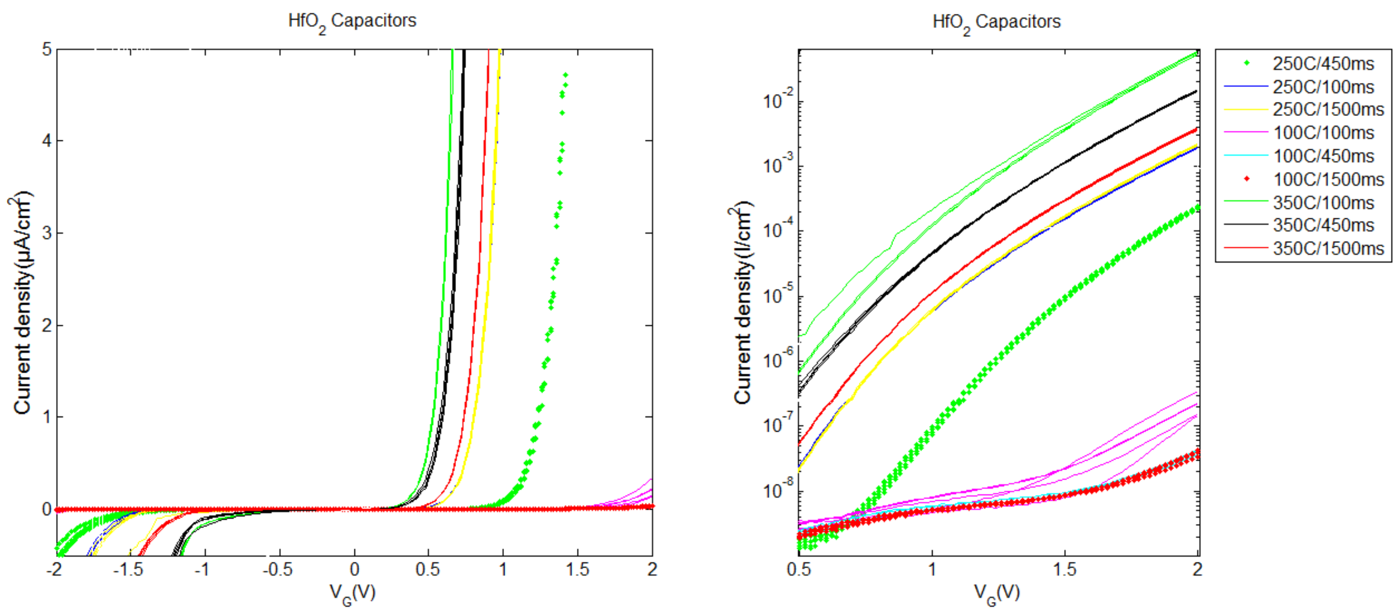


Figure 5-1. Current density measured for different HfO_2 samples.

Current magnitude is in the order of micro ampere that shows a large leakage current through the oxide. According to the measured *I-V*s, for a given pulse duration, there is an increase in the current with increasing the deposition temperature. The current also decreases with increase in the precursor pulse length at a specific temperature. This trend is clearly seen for devices with deposition temperature of 100 °C and 300 °C. However at 250 °C, oxides that are deposited with 450 ms pulse duration have the lowest leakage current.

5.1.2 Al_2O_3/Si structures

I-V measurements of Al_2O_3/Si structures are shown in Figure 5-2. The measured currents were not significantly different for different Al_2O_3 capacitors. However, the current levels was much

higher that HfO_2 samples. As seen, in oxides deposited by precursor pulses of 10 ms and 25 ms, current density increases with increasing the temperature. Whereas, the currents in the samples with longer pulse length 100 ms, do not increase by increasing the temperature. Moreover, for a given temperature, there is no specific trend as the precursor pulse length changes.

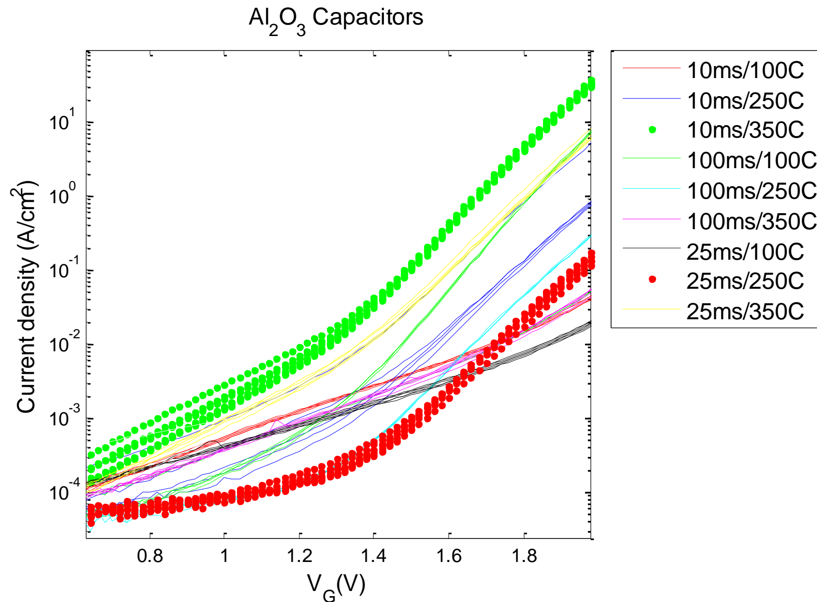


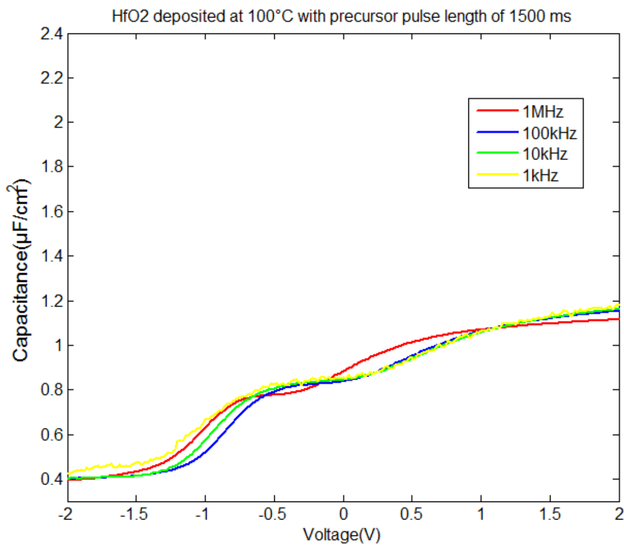
Figure 5-2. Current density measured for different Al_2O_3 Oxide samples

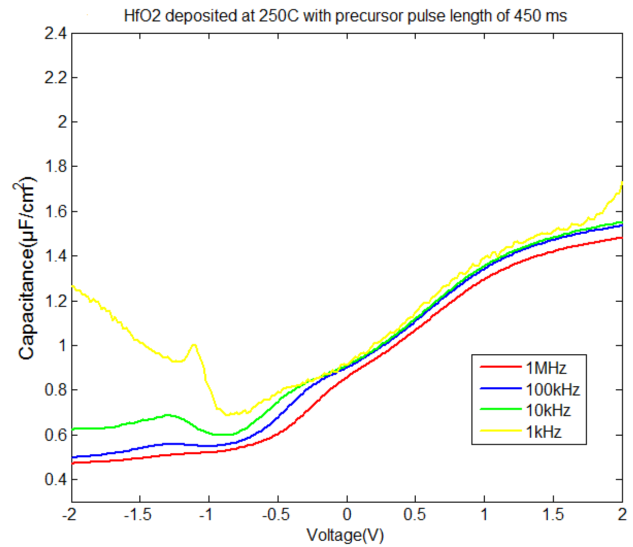
The current densities seen are in agreement with the oxide thickness in Tables (1) and (2). The current density that is caused by direct tunneling through the oxide is related to the equivalent oxide thickness. Then, a lower leakage current is potentially expected for thicker oxides. This is clearly observable for HfO_2 capacitor. But it should be noticed that in addition to direct tunneling, because of traps in the oxide layer and small band gap of high-κ oxides, other conduction mechanism might affect the current.

5.2 Capacitance-Voltage Measurements

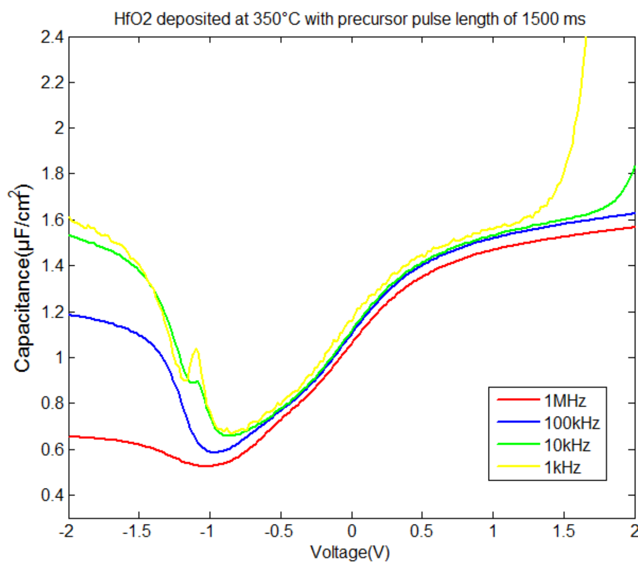
5.2.1 HfO_2 /Si structures

The *C*-*V* curves of the HfO_2 samples are shown in Figure 5-3. Measurements on the samples revealed that capacitance-voltage behavior for any given deposition temperature has a typical shape. Here just a few of the obtained results with typical *C*-*V* behavior are presented. Measurements were done at different frequencies for each device. Frequency dispersion is due to the existence of interface traps. As the frequency decrease from 1MHz to1kHz, more traps can follow the AC signal and contribute to the capacitance. That's why the measured capacitance is larger at lower frequencies for the same device.





(a) (b)



(c)

Figure 5-3. C-V characteristics of HfO_2 Samples

Smaller capacitance was measured at lower deposition temperature, which could be due to thicker oxide layer according to Table (1). Increase in the thickness at 100 °C temperature could be the result of insufficient purge time. Short purge time may result in growth of more than one monolayer per cycle and incorporation of more impurity in the oxide layer. The *C-V* curve of the structure at 100 °C shows a small peak in depletion region. This peak is reduced as deposition temperature is raised from 100 °C and almost vanishes at 350 °C. This might de due to the presence of a large amount of traps located near the interface, caused by the poor quality SiO_2 in the interfacial layer or insufficient purge time. Longer purge time is usually chosen for the growth at 100 °C. The purge duration should be typically 3 times of precursor pulse length [9].

Thermal annealing on the sample of Figure 5-3b diminished the peak in the depletion region. Annealing was done at 400 °C for 2 min and may suggest that the peak is due to the presence of hafnium oxide traps near the HfO_2/SiO_2 interface. This peak is also reported in previous studies [10], [11].

As illustrated in the Figure 5-3, the *C-V* did not saturate in the accumulation region. The measured capacitance was more than the capacitance that was expected from theory for the equivalent oxide thickness. This upturn in capacitance depends on frequency and is stronger at lower frequencies. This effect could be due to trapping of electrons in the near interfacial traps within the oxide (border traps). As the voltage increases in accumulation, more oxide traps interact with the majority carriers of the substrate. The contribution of the oxide traps makes the capacitance larger than the actual oxide capacitance. This capacitance upturn has been explained for thin oxide in the literature [8], [12-14].

The *C-V* curve of devices with high deposition temperature and pulse length (350 °C - 450 ms and 1500 ms) were highly distorted at low frequencies. Since the Hf-precursor starts to decompose at temperatures about 200 °C to 250 °C, more impurities and defects are incorporated in the oxide layer during the growth. The combination of Hf-precursor decomposition and an increase in pulse length may raise the growth per cycle but a high value of carbon content would be incorporated [9]. The thickness of deposited HfO_2 at 350 °C slightly increases as the pulse length changes from 450 ms to 1500 ms.

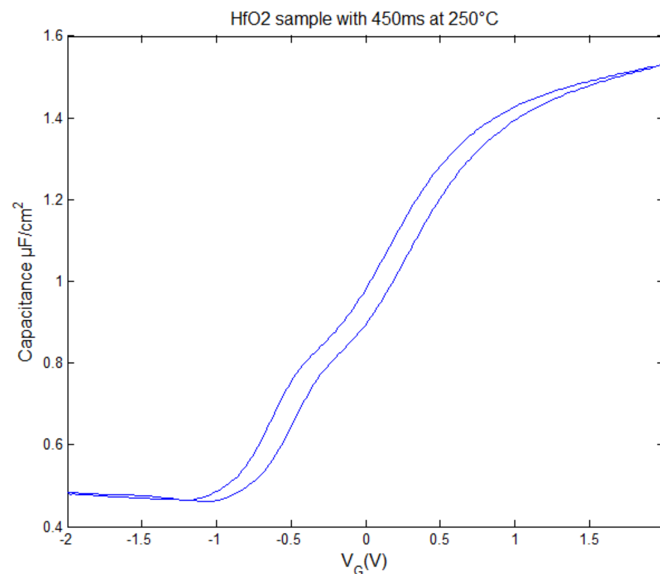


Figure 5-4. C-V hysteresis characteristics for the HfO_2 capacitors measured at the frequency of 1MHz

One of the methods used to evaluate charge trapping in the oxide layers is the measurements of capacitance-voltage hysteresis. The *C-V* hysteresis was measured by sweeping the gate voltage in two directions and can be presented as a shift in flat-band voltage. Figure 5-4 shows a typical

C-V hysteresis characteristics measured at the frequency of 1 MHz while the voltage swept up and down between -2 and 2 volts. The lowest hysteresis, 120 mV, is measured for the film deposited at 250 °C and 450 ms as depicted in Figure 5.5.

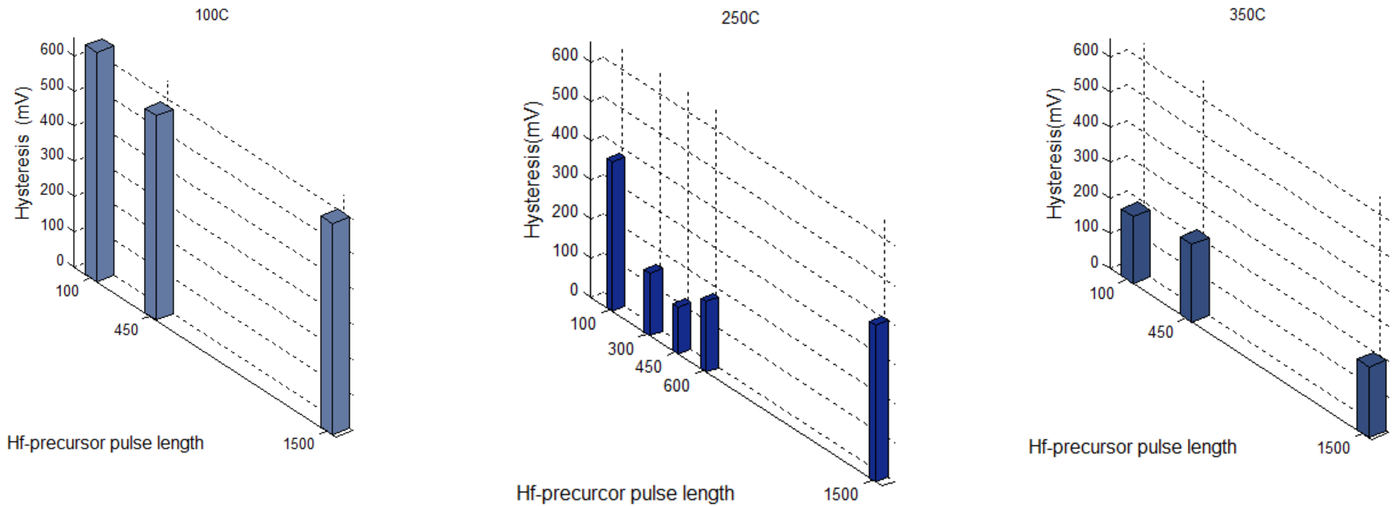


Figure 5-5. C-V hysteresis measured for HfO_2 capacitors

The presented results for HfO_2 samples were further investigated by measurements on nine HfO_2 capacitors fabricated at different deposition temperature and pulse lengths. In general, the same trends was observed in *C-V* characteristics of the HfO_2 films deposited at 225, 250, and 275 °C with the precursor length of 300, 450, and 600 ms. Table (3) is presented the hysteresis that measured for all of the samples.

Table 3: CV hysteresis for HfO_2 samples in mV

T(°C) / Pulse time (ms)	**100**	**225**	**250**	**275**	**350**
100	580		380		220
300		320	160	360	
450	650	220	**120**	220	190
600		240	180	260	
1500	600		400		200

5.2.2 Al_2O_3 /Si structures

Measurements were done on different Al_2O_3 /Si structures prepared at deposition temperature in the range of 100-375 °C and pulses of 10 to 100 ms. In total, 24 capacitors were fabricated. Figure 5-6 shows two *C-V* curves, which were measured on Al_2O_3 samples with 25 ms Al-precursor at 100 and 350 °C. Similar to HfO_2 samples, there is a peak at the depletion region of

the device with low deposition temperature of 100 °C. This hump seems to be larger at longer Al-pulses whereas it diminishes as the deposition temperature increases.

The *C-V* curves were compared with the ideal simulated capacitance with the same thickness and dielectric constant of 8.1. The effect of border traps was found stronger in the samples deposited at lower temperatures. The capacitance upturn is weaker compared to HfO_2, which may show the lower density of border traps in the Al_2O_3 layer.

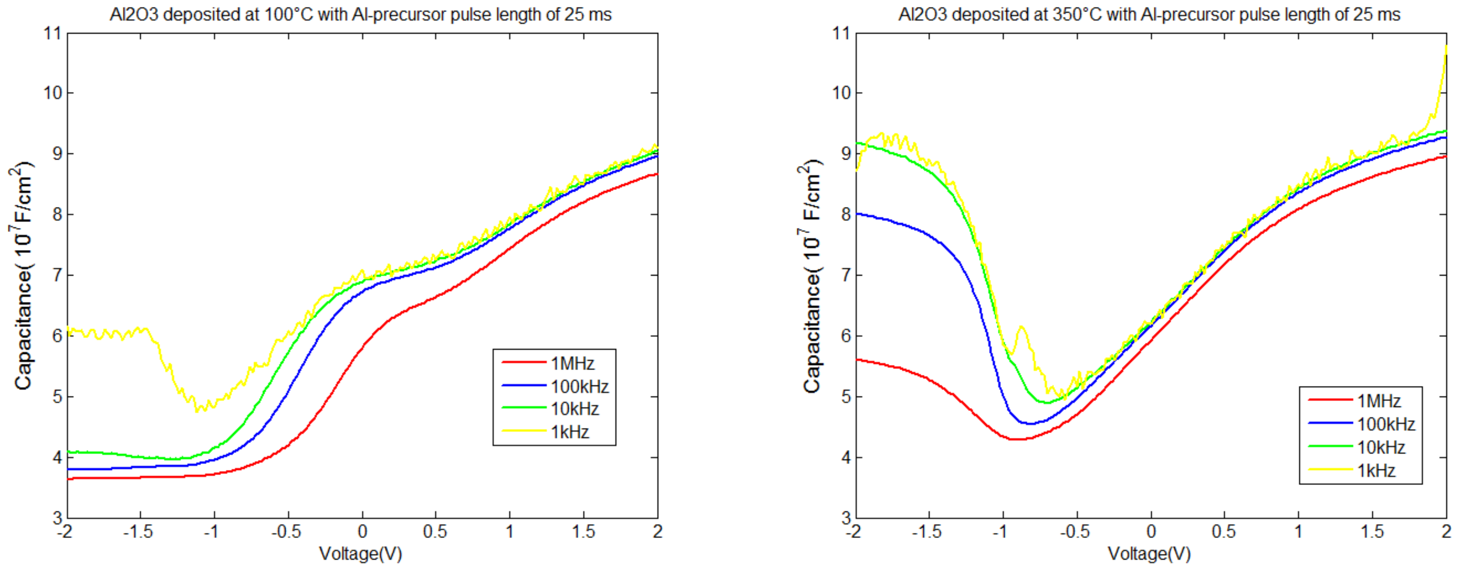


Figure 5-6. C-V characteristics of Al_2O_3 Samples

C-V hysteresis was measured using a back and forth voltage sweep. The *C-V* characteristics of the samples with deposition temperatures between 300 °C to 375 °C exhibited very low hysteresis. The lowest hysteresis was measured to be about 20mV for Aluminum oxides deposited at 350 °C. This result was approximately the same for different pulse lengths. Table (4) listed the hysteresis measured for different Al_2O_3 /Si structures. A good comparison between the results that obtained for some of the samples is depicted in Figure 5-7.

Table 4: CV hysteresis for Al_2O_3 samples in mV

Pulse time (ms) \ T(°C)	**100**	**250**	**300**	**325**	**350**	**375**
10	220	120	60	20	40	20
15				20	40	40
25	320	120	40	40	20	20
40				60		20
100	280	140	40	40	60	40

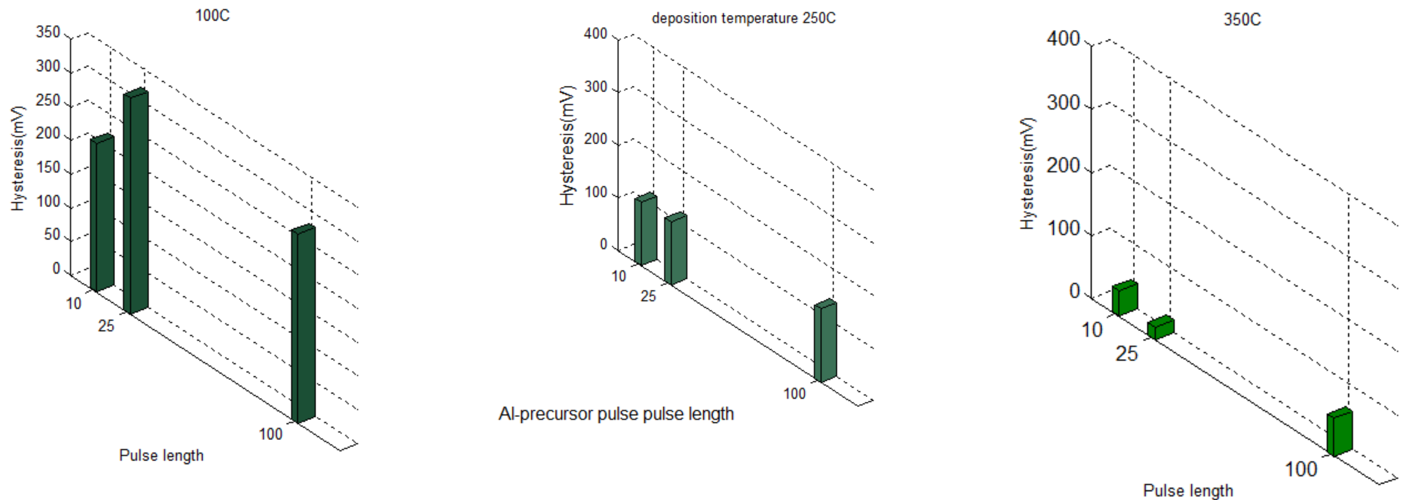


Figure 5-7. C-V hysteresis measured for Al_2O_3 capacitors

5.3 Density of Interface Traps

The density of interface traps was extracted for different samples using the methods explained in Section 4.3. The D_{it} values were extracted for capacitors with different deposition temperatures and precursor pulse durations by conductance-voltage characteristics at the frequency of 10 kHz and were presented in Tables (5) and (6). Comparison of the D_{it} for HfO_2 capacitors reveals that the density of interface traps is minimum for the deposition temperature of 250 °C and the middle pulse length of 450 ms. In case of Al_2O_3, minimum D_{it} occurs at a higher deposition temperature of 350 °C.

The energy distribution of traps in Figure 5-8 depicts location of interface traps with respect to the conduction band for an HfO_2 Sample. This was observed for all different HfO_2 samples with no significant changes. The measured density of interface traps was in the order of $10^{12}\ eV^{-1}cm^{-2}$ and in agreement with the conductance method results.

HfO_2 capacitors

Table 5: Extracted density of interface traps using conductance method for HfO_2 samples, in units of ($\times\ 10^{12}eV^{-1}cm^{-2}$)

T(°C) / Pulse time (ms)	**100**	**225**	**250**	**275**	**350**
100	0.91		3.82		3.33
300		8.97	1.11	3.65	
450	0.84	1.02	0.66	4.67	2.52
600		1.05	3.91	3.69	
1500	0.94		1.27		3.21

Al_2O_3 capacitors

Table 6: Extracted density of interface traps using conductance method for Al_2O_3 samples, in units of ($\times$ $10^{12} eV^{-1} cm^{-2}$)

T(°C) / Pulse time (ms)	**100**	**250**	**300**	**325**	**350**	**375**
10	6.11	1.79	1.89	0.88	0.55	0.67
15				2.39	0.66	0.69
25	0.59	1.84	1.13	0.99	0.89	0.75
40				1.32	0.93	0.86
100	1.75	1.79	1.29	0.79	0.46	0.0002

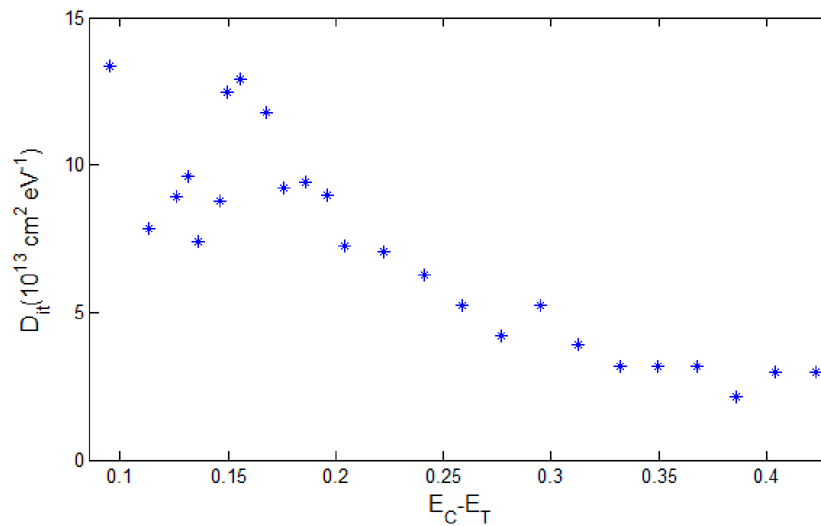


Figure 5-8. Distribution of interface traps for HfO2 deposited at 250 °C and 450 ms of Hf-precursor pulse length)

Assuming that the SiO_2 layer is thin enough that electron can tunnel through the SiO_2 layer, the measured D_{it} values might represent the density of states at the High-κ/SiO_2 interface rather than Si/SiO_2. The experimental C-V curves were also found to be influenced by trapping of the majority carriers (electrons) in the border trap levels within the oxide layer. It has been reported that a trap density of $10^{18}\ cm^{-3}$ in the oxide results in a typical surface state density of $10^{12}\ cm^{-3} eV^{-1}$[15]. Therefore, the energy band diagram of the MOS structures can be expected to be as shown in Figure 5-9, with a volume density of the traps, N_{bt} reside within the oxide layer and a density of interface traps in the order of $10^{12}\ eV^{-1} cm^{-2}$ at High-κ/SiO_2 interface.

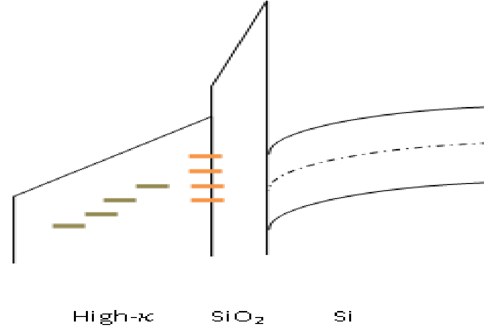


Figure 5-9. Energy band diagram of the samples

6. Discussion

The experimental results showed that trapping and de-trapping of electrons in the border traps depends on the bias condition and the frequency of the measurements. It means that fewer border traps follow the AC signal at high frequency rather than low frequency. It is also expected that the effect of border traps reduces as we approach the depletion region. Because in accumulation the surface potential is positive for an n-type substrate, therefore it is easier for negative electrons to occupy border traps. Sweeping the voltage toward negative values, band bending gradually becomes negative and fewer oxide traps interact with the electrons at the substrate surface. Furthermore, studies show that the number of border traps filled by electrons decreases by increasing the distance from oxide-semiconductor interface [16].

In order to understand the effect of border traps on the capacitance measurements, we should find a model that interprets the contribution of these traps to the equivalent circuit of the device. First, quantum mechanical tunneling can help to account for the electron exchange between the semiconductor and the border traps. The problem can be considered as an electron impinging a barrier with a specific height. In the case of the MOS structure, the tunneling barrier is defined from the oxide conduction band to the bottom of the semiconductor conduction band at the interface [16-18].

With this approach, Heiman et al. [15] has shown that the capture cross section of a trap is reduced by a factor of e^{-2kx} at a distance x from the interface into the oxide layer.

$$\sigma_{nx} = \sigma_n e^{-2kx} \tag{6.1}$$

The factor k is the decay constant associated with the tunneling of the electron in x direction into the oxide, and as shown in equation (6.2) depends on the tunneling barrier.

$$k(\varphi_s) = \frac{\sqrt{2m_e(E_C^{0x} - \varphi_s)}}{\hbar} \tag{6.2}$$

The time constant of the traps, which is the mean time before a trap captures an electron is also defined by

$$\tau_t = (n_s v_t \sigma_{nx})^{-1}, \tag{6.3}$$

where $v_t$is the thermal velocity of electrons. Since the trap time constant become longer as the distance increases from the interface, it suggests that the number of filled border traps decreases from the interface with an exponential function. The exponential change in the filled border traps as a function of distance from the interface is also studied elsewhere [19], [20].

Each trap level in different depth of the oxide, with the specific time constant, can be modeled by a series R-C circuit, which expresses the capacitance of the trap and the corresponding electron capture resistance. For a distribution of traps a parallel combination of R-C branches is added to the equivalent circuit model of an ideal MOS capacitor. If the circuit is simplified to a lumped model by adding all the equivalent parallel branches with the same as interface traps capacitance, it could be shown as in Figure 6-1. But in order to consider the capacitance of the all border traps distributed over the depth of the oxide, the border traps capacitance was calculated by using an exponential spatial distribution of traps by (6.4).

$$N_{bt}(x) = N_0 \exp(-k\Delta x) \tag{6.4}$$

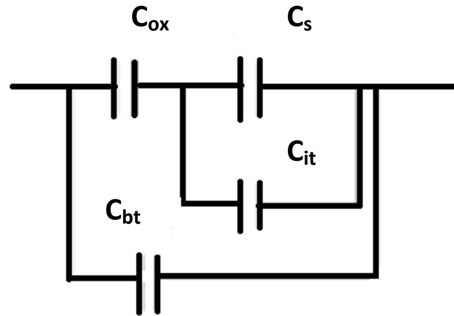


Figure 6-1. Circuit model including border trap capacitance and interface traps

To obtain the equivalent capacitance of this model, the interface capacitance was calculated using D_{it} values obtained in Section (5.3). The border traps distribution was calculated by equation (6.4) using N_0 equals to $1.85 \times 10^{19}\ eV^{-1}cm^{-3}$ for the HfO_2 capacitors. The factor k was obtained by equation (6.2) considering E_C^{0x} equals to 1 eV. Then the total capacitance was calculated and plotted against the voltage for a capacitor with the HfO_2 film deposited at 250 °C and 450 ms of Hf-precursor. Figure 6-2 compares the *C-V* curve that is measured for this HfO_2 capacitor with two simulated *C-V*s. The red curve is simulated for the ideal case without any

interface and oxide traps [4]. As illustrated, the transition from accumulation to inversion region is less abrupt in the measured *C-V* curve because of interface and border trap capacitances. The green curve was simulated using the model that is explained above and showed a better fit to the measured capacitance.

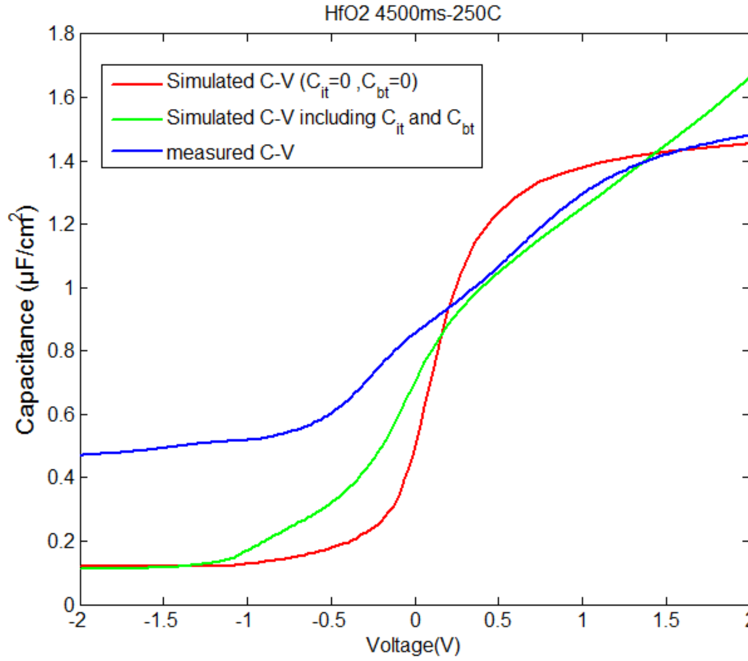


Figure 6-2. Comparison of the experimental C-V with the simulated C-V curves

The presented model indicates that the capacitance is influenced by the effect of the border traps in accumulation region and as we approach the depletion region interface trap effect dominates. But a more precise model is needed to account for the spatial distribution of the border traps and explain the frequency dispersion. A detailed RC equivalent circuit for a distribution of oxide traps over the thickness of the oxide layer has been developed by Yuan et al. [17]. In this model, the oxide with the thickness of x is divided to small fractions as illustrated in Figure 6-3[17]. Each incremental depth of Δx has an incremental capacitance that is given by

$$\Delta C_{bt} = q^2 N_{bt} \Delta x \,, \tag{6.4}$$

where the volume density of border traps N_{bt} is a constant in the unit of $cm^{-3}J^{-1}$. This distributed model has been currently used in the studies to analyze the effect of border traps.

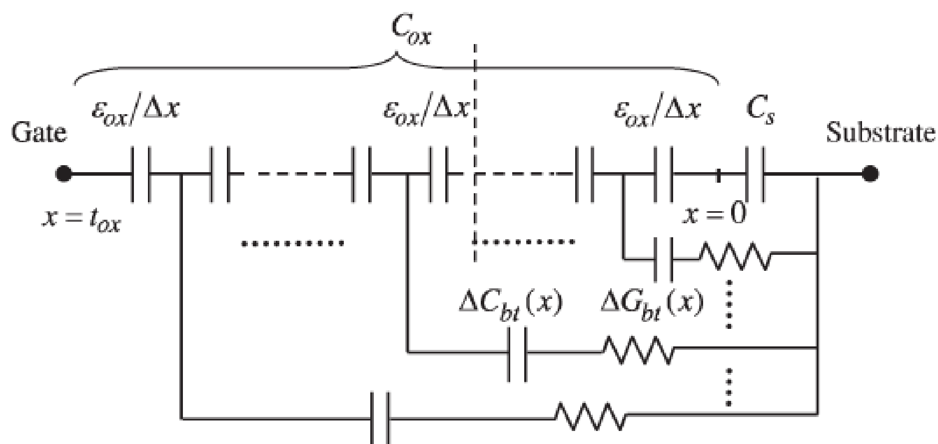


Figure 6-3. [17] RC equivalent circuit for border traps distributed over the depth of the oxide.C_s shows the semiconductor capacitance.

7. Conclusion and outlook

The effect of ALD growth of the HfO_2 and Al_2O_3 on Si substrate was investigated. The HfO_2 deposited at 250 °C with 450 ms Hf-precursor pulse length had the lowest density of interface traps and *C-V* hysteresis. The *C-V* measured for this sample also showed a better fit with the simulated ideal capacitor with the same oxide thickness and with dielectric constant of 15.
For Al_2O_3 capacitors, low density of interface and hysteresis were measured at high deposited temperatures of 350 °C and 375 °C.

There was a good agreement between some of the experimental observations in this work and the results of previous studies on Si and III-V substrates. Thus, it is interesting to understand and quantify the effect of interface and border traps on the MOS structures in order to interpret the *C-V* behavior of the devices. Finding a good model needs a more comprehensive theoretical and experimental study. For example, investigating the effect of annealing on the *C-V* characteristics of the fabricated samples could reveal more information on the defects and trap levels at the interface and within the oxide layer. In addition, with the same approach, finding an optimized condition for depositing the high-κ films on III-V substrates could help to improve III-V MOS devices.

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