ADVANCED PROCESSING OF VERTICALLY ALIGNED NANODEVICES

FYSB06

May 9, 2013

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A report submitted to the Department of Physics in Lund University.

Abstract: Lithography technique is highly dependent on the photoresist that is used for the processing of the nanodevices. S1800 series photoresist is probably the most used positive photoresist for UV-lithography process. In this project the electrical and optical properties of the photoresist S1800 are studied in order to find if photoresist could be used as a transparent insulator for photo detectors/solar cells/LEDs. Spinning speed dependent thickness and breakdown voltage of the resist is studied, as well as its photoabsorption. It was observed that S1800 photoresist possess high resistivity and remains a strong insulator upto 400 nm thickness even with an applied bias of 100 V. It was also observed that S1800 photoresist shows higher transmission intensity comparing with ITO (Indium-Tin-Oxide) layer.
Key words: photoresist, S1800, photodetector, nanowire, metal contact.

1. Introduction

Lithography technique plays a very important role in microfabrication and photolithography is one of the most popularly used lithography techniques because of its high throughput. Different photoresists have been developed depending on the requirements and their properties have been well studied [**?**]. S1800 photoresist series is one of the most used resists all over the world that is used in nanofabrication. However, no specific study on the electrical properties of the photoresist S1800 series has been reported so far. In this project we studied the electrical and optical properties of the photoresist S1800 and the breakdown voltage corresponding to different thickness is reported.

2. Background

It is always a challenge to make contacts to vertically aligned nanodevices e.g. nanowires (NW). An insulating layer is necessary between the two device terminals. An oxide layer is usually used as an insulator (figure-**??**) due to its high dielectric constant. The essential requirements for a good insulating layer for the photodiodes are: high resistivity and transparency to the desired wavelengths. This project is motivated towards fabrication of photodetectors using vertically aligned NWs in which junction is defined axially. NW positions are patterned using Nanoimprint Lithography (NIL) with a pitch of 500 nm and the diameter of the wires is 180 nm. NWs are covered with a 50 nm thick silicon oxide layer and then Indium Tin Oxide (ITO) is used as a top contact. The schematic processing steps are illustrated in figure-**??**. In figure-**??** scanning electron micrograph (SEM) of InP nanowires is shown and in figure-**??** SEM image of InP NW-photodiodes with SiO_2 is presented.

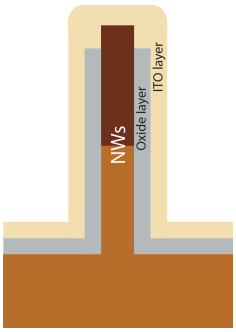


Figure 1: Schematic illustration of the different layers on nanowires to make a top contact with the nanowires. The oxide layer acts as an insulator which is buried beneath the ITO layer.

In this processing scheme the problem arises for core-shell nanowires where junction is defined radially. These nanowires have a diameter of 350 nm and another 50 nm of oxide layer is needed which leaves a distance of 50 nm between wires. When NWs are coated with SiO_2 using atomic layer deposition (ALD) a planar SiO_2 layer is deposited which cannot be further etched from the tip of the NWs using a resist layer. This problem could be solved if the resist layer itself could be used as an insulator layer instead of any oxide layer. Here we tested the electrical and optical properties of the photoresist S1800 series to check whether it is suitable for such a layer.

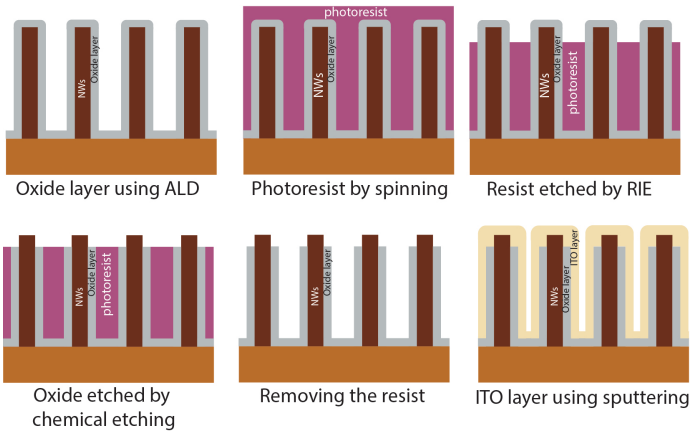


Figure 2: Schematic processing steps of forming top contact on nanowires. First, an oxide layer is deposited uniformly on top of the NWs and then photoresist is spun. Next, resist layer is removed partly on the top of the NWs using RIE to open the oxide layer which is removed in the next step by chemical etching. Then resist is removed completely and uniform ITO layer is sputtered.

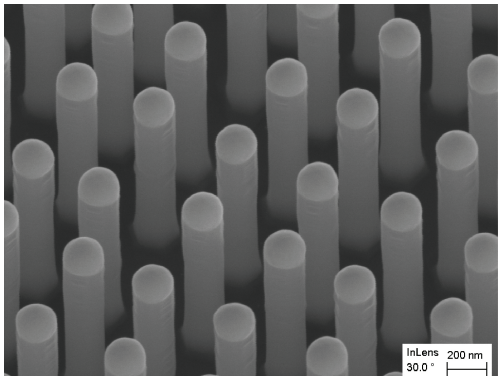


Figure 3: SEM image of InP photodetectors with Au-nanoparticles on top of the nanowires. The junction is defined axially. The diameter of the wires are 180 nm with a pitch of 500 nm.

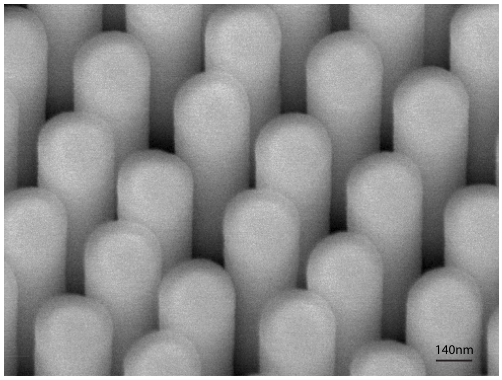


Figure 4: InP NW-photodiodes with SiO_2 layers surrounding the nanowires. The thickness of the oxide layer is approximately 50 nm. Atomic layer deposition (ALD) was used to form the oxide layer.

Polymer S1800 is a positive photoresist in which the bonds are broken upon UV exposure and MF319 developer is used to remove the soluble resist whereas the unexposed resist remains intact [**?**]. The solvent used for S1800 series photoresist is Propylene Glycol Monomethyl Ether Acetate ($C_6H_{12}O_3$) [**?**]. The chemical formula is presented in figure-**??**.

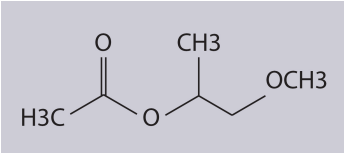


Figure 5: Chemical formula of the Propylene Glycol Monomethyl Ether Acetate ($C_6H_{12}O_3$).

3. Fabrication

In brief fabrication steps that were followed in this project are:

1. cleaning the samples,
2. first lithography (UV-lithography),
3. hard baking,
4. metal deposition (AVAC),
5. second lithography, and
6. chemical etching

Before discussing the details about the fabrication steps, I will briefly discuss the basic principles of photolithography technique and the evaporation method of depositing thin film layer.

3.1. Photolithography

In photolithography resolution of the patterns is limited by the diffraction and wavelength of the light. The resolution can be simply calculated by:

$$\text{Resolution} = \sqrt{\lambda d}$$

where, λ is the wavelength of the light and d is the distance between mask and the sample including resist thickness. This limitation can be minimized to a certain value by reducing λ and d. The resolution is also limited by the efficiency of the photoresist.

Depending on the photoresist, photolithography can be of two kinds: positive and negative as shown in figure-**??**. In the first type the exposed resist is removed where in the negative process unexposed resist is removed. The basic lithography process for both positive and negative is the same, the main difference is the chemical properties of the photo-resist. For a positive resist the bonds are broken after exposure by UV-light which makes it soluble in the developer. In the case of negative resist cross-linking occurs after exposure by UV-light making ut insoluble in the developer, whereas the rest of the unexposed resist is soluble in the developer.

3.2. Evaporation

In this project Ti/Au metal was deposited on top of the resist as top contact. In order to do this we used thermal evaporation of Ti/Au using AVAC. The basic principle is that in high vacuum the mean free path of Au-particles increases to several meters, so they can travel straight without

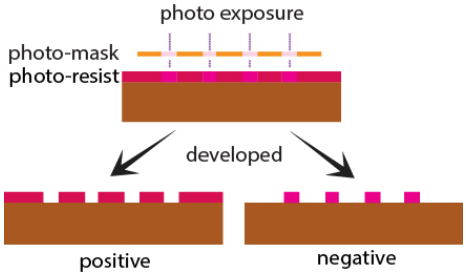


Figure 6: Schematic of positive and negative photolithography. Positive and/or negative photoresists are used to obtain opposite patterns from the same mask.

colliding any other particles or surrounding gas into cells and can be deposited to the substrate surface. This process is characterized by the dimensionless number known as *Knudsen Number*, $\mathrm{K_n}$:

$$\mathrm{K_n} = \frac{l}{L}$$

where *l* is the mean free path of the deposited particles and *L* is the physical distance between the source and the target. The value of *l* depends on the pressure in the chamber, thus by minimizing pressure it is possible to increase the physical size of the chamber.

3.3. Fabrication

In this project n-type silicon substrate was used to fabricate the devices after a rapid wash by HF to remove the thin $\mathrm{SiO_2}$ layer present on wafers and then the sample was cleaved. The Si pieces were rinsed on a spinner with acetone followed by IPA (figure-**??**). S1800 series photoresists were used on the spinner which can be rotated with different spinning speed. Few droplets of resist make a homogeneous layer on substrate with certain thickness on the spinner. To obtain different resist thickness, resists with different viscosity (S1805, S1813, S1818, S1828) and different spinning speeds were used. Then the samples were soft baked on a hot plate at $115^{\circ}\mathrm{C}$ for 90 seconds to solidify the resist layer and then exposed with soft-UV (360 W Hg lamp) with the mask aligner MJB4 using a predefined photomask. The exposure was set for different time parameters depending on the photoresist (table-**??**). Samples were then developed with MF319 developer for 90 seconds to remove the unexposed resist and cleaned in DI and gently dried under nitrogen flow. The patterns were then hard baked at $200^{\circ}\mathrm{C}$ for 30 minutes and then cooled down for another 10 minutes on the hotplate by turning the switch off in order to make the resist stable. The resist thickness was then measured using profiler (Dektak 6M).

The second step was to deposit metal contact on the resist and that was done by thermal evaporation using AVAC at high vacuum ($10^{-7}\mathrm{mbar}$). Initially, 10 nm of Ti was deposited to get good adhesion to the resist surface and then 200 nm of Au was deposited on top of Ti. After that samples were again spin coated with photoresist S1818 at 3000 rpm and soft baked at $115^{\circ}\mathrm{C}$ and exposed after mask alignment with soft-UV for 10 seconds and developed with MF319 for 90 seconds and dried under nitrogen flow.

The third fabrication step was to etch the unwanted metal that is exposed due to the second lithography. $\mathrm{KI-I_2-H_2O}$ and buffer HF (1:10) was repeatedly used to etch Au and Ti respectively and washed by DI water, and finally samples were rinsed with acetone to remove the remaining resist and dried under nitrogen flow.

Figure-**??** shows the optical microscope images of the final devices. In figure b an extended view of a single device is shown. The size of the base device is $150\mu\mathrm{m} \times 150\mu\mathrm{m}$ and the size of the top metal contact (Au) is $50\mu\mathrm{m} \times 50\mu\mathrm{m}$. The dark lines surrounding the devices are the undercut of the photoresist.

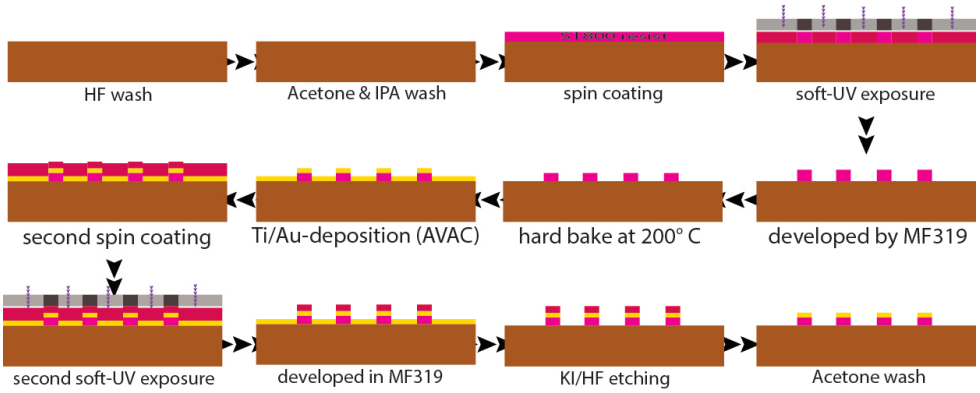
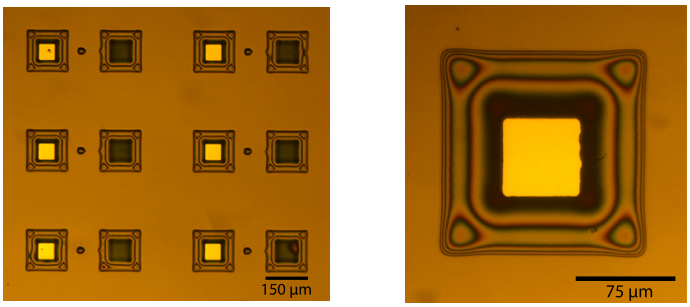


Figure 7: Schematic fabrication steps. First lithography was done with different recipe for each sample and metal (Ti/Au) was deposited with AVAC after hard baking of the photoresist. Second lithography was same for all samples and then unwanted metal was removed by KI/HF etching. Finally samples were rinsed with acetone to remove the remaining resist.



(a) (b)

Figure 8: Optical micrographs of one of the final samples. Figure **??**a is a wider view of the samples taken with 5X objective and figure **??**b is the image of a single device taken with 20X objective. The base size of the device is $150\mu\mathrm{m} \times 150\mu\mathrm{m}$ and the size of the top metal contact is $50\mu\mathrm{m} \times 50\mu\mathrm{m}$.

4. Experiments and Result

For the first lithography, different resists with different spinning speeds were used to obtain different thickness of the resist. Table-**??** represents the summary of the first lithography step. It is to be noted that the thickness presented here were obtained after the hard baking.

The electrical properties of the samples were studied using probe station (Cascade 11000B) based on the schematic shown in figure-**??**.

It was observed that photoresist S1800 series shows high resistivity and does not easily breakdown due to the applied bias voltage.

Bias was applied between the top metal contact of the devices and the substrate which are separated by photoresist layer in order to find the breakdown voltage of the photoresist. To find this we tested several devices with different thickness of the resist. Initially, we started from -5 V to +5 V and later it was increased to 50 V and even further to 100 V. None of the devices broke for the ap-

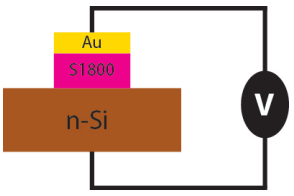


Figure 9: Schematic illustration of the electrical measurement setup using probe station for a single device.

Resist	Spinning speed (rpm)	Exposed time (s)	Developing time (s)	Thickness (μm)
S1805	4000	5	60	0.33
S1805	6000	5	60	0.275
S1805	9000	5	60	0.225
S1813	3000	7	90	1.3
S1813	6000	7	90	0.8
S1818	3000	10	90	1.5
S1818	6000	10	90	1.1
S1828	3000	15	90	2.9
S1828	6000	15	90	1.8

Table 1: Summary of the first lithography and obtained resist thickness after the hard baking at 200°C

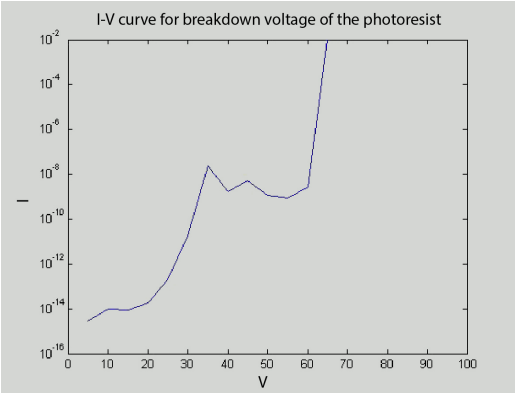


Figure 10: I-V curve for the applied bias on metal and n-Si with a photoresist layer in between. The thickness of the resist was 225 nm. Vertical axis represents the current in log scale whereas the horizontal axis presents the applied bias.

plied bias above the resist thickness of 250 nm. Most of
the devices with the thinnest resist thickness of 225 nm acted as a good insulator for an applied bias of 100 V. However, only few of the devices showed leakage at an applied bias of 30 V or higher. We tested a about 25 such devices and approximately 15% of them showed leakage current. As shown in figure-**??**, the photoresist layer started leaking at about 30 V.

In the next experiment we studied the effect of reactive ion etching (RIE) on the photoresist. In order to study this, we prepared several samples with a photoresist thickness of 1.5μm after hard baking following the previous recipe and then etched down the photoresist using RIE (Trion T2). Several samples were etched with different initial thickness to different final thickness with an approximate etching rate of 1 nm/s using O_2 plasma. Then the samples were processed following the same steps as before. Table-**??** represents the summary of the RIE experiments.

Next, samples were tested by the probe station to study the electrical properties. A bias was

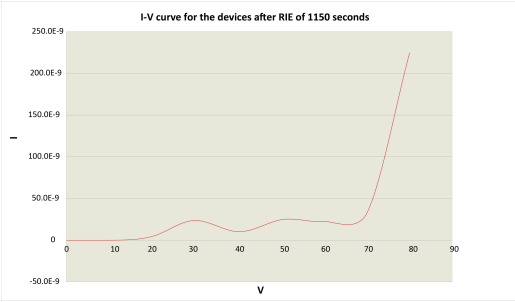


Figure 11: I-V curve for the applied bias on metal and n-Si with a photoresist layer in between. The resist was etched using RIE for 1150 seconds to obtain 400 nm thick resist layer. Initially the resist thickness was 1.5μm.

Photoresist	Spinning speed (rpm)	Initial thickness (nm)	RIE time (s)	Final thickness (nm)
S1818	3000	1500	500	1000
S1818	3000	1500	1150	400
S1813	4000	1000	595	400
S1813	5000	980	545	400
S1813	6000	835	430	330
S1813	7000	785	385	400

Table 2: Summary of the RIE etching. Initial resist thickness measured after 10 minutes of hard baking at 200°C and another 10 minutes of cooling on the switched off hot plate.

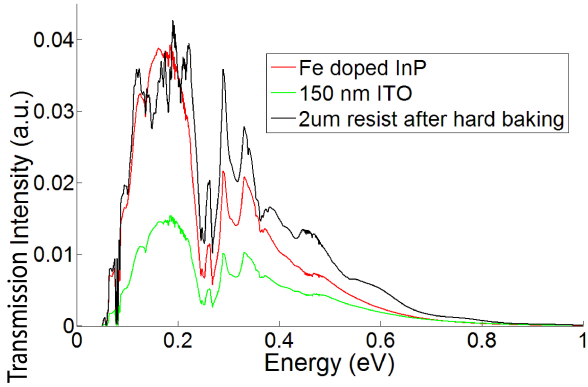


Figure 12: Energy dependent intensity curves for bare Fe-doped InP (red), 150 nm thick ITO layer with Fe-doped InP substrate (green) and 2μm of photoresist layer after hard baking with Fe-doped InP substrate (black).

applied between the device and the substrate as presented before. First, the sample with 1μm photoresist thickness was tested with up to a bias of 100 V and that showed no breakdown of the resist. Next, the samples with photoresist thickness of 400 nm after RIE of 1150 seconds was studied. In this case few devices showed leakage current after certain voltage as shown in figure-**??**, though we did not find any devices with a photoresist thickness of 400 nm without RIE that leak with an applied bias of 100V. In the statistical view 10% of about 20 tested devices showed leakage current.

These experiments implies that RIE has some effect on the resist that makes it breakdown easily. In order to study this result further we prepared several samples with different initial resist thickness and etched for different time duration to obtain same final resist thickness (400 nm). Table-**??** represents the summary of the experiments. Most of the devices acted positively with an applied bias of 100 V. Few of the devices those were etched for 595 seconds to obtain 400 nm final thickness showed leakage current in pico-amperes (approximately 30%). Next we tested the devices with final resist thickness of 330 nm after 430 seconds of RIE. This was the thinnest sample prepared by RIE. Studying these devices with an applied bias of 100 V we found a leakage current in pico-amperes after 40V. About 40% of the 10 measured devices showed leakage current. This result implies that different RIE time duration plays a major role in affecting the electrical properties of the resist.

In another experiment, we studied the optical properties of the photoresist S1800. In order to do that we spin coated the resist S1828 at 5000 rpm on p-InP plane substrate which gives 2μm thick resist layer. And then optical absorption and transmission in infrared wavelength region was studied.

Figure-**??** shows the energy dependent transmission intensity of the photoresist layer on Fe-doped InP substrate (black line), ITO layer on Fe-doped InP substrate (green line) and Fe-doped InP substrate (red line). As observed 150 nm thick ITO layer with substrate shows almost half

transmission intensity comparing with the bare substrate whereas $2\mu\mathrm{m}$ thick resist layer shows almost same transmission intensity as the bare substrate does. Which implies that S1800 photoresist has a higher transmission intensity than ITO.

5. Conclusion

In this project we studied the photoresist S1800 series in order to find the possibility of using the photoresist as an insulator layer instead of an oxide layer in between nanowires and ITO. In order to do that we tested electrical and optical properties of the photoresist.

It was observed that 225 nm thick photoresist layer shows strong insulator properties, which rarely breakdown with an applied bias of 100 V. It was also observed that a 275 nm thick or thicker resist layer results no leakage current due to an applied bias of 100 V. However, with the RIE process the resistivity of the photoresist decreases but works as good insulator until 400 nm of resist thickness.

The optical properties of the photoresist is very promising to be used as an transparent insulator layer. $2\mu\mathrm{m}$ thick S1800 series photoresist shows higher transmission intensity comparing with ITO layer.

In conclusion, we can say that the S1800 photoresist can be used as a proper insulator layer instead of the oxide layer which can solve several problems and would also make the fabrication steps easier.

Acknowledgment: I sincerely acknowledge *Ali Nowzari* for his help and discussion through this project.

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