# Surface Chemistry and Electrical Properties of Nanowire Devices

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A MASTER THESIS EQUIVALENT TO 60 CREDITS


DIVISION OF SYNCHROTRON RADIATION RESEARCH

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# Abstract

Surface chemistry and electrical properties of InAs and InP III-V semiconductor nanowires and nanowire based devices were studied using Scanning Tunneling Microscopy (STM) and Spectroscopic Emission and Low Energy Electron Microscopy (SPELEEM). Changes of the surface as well as electrical properties in these devices as a function of annealing temperature under atomic hydrogen background were studied and discussed. First, the cleaned surface of InAs (111)B substrate is analyzed and then the surface studies of InAs nanowires were done. SPELEEM technique with several mode of operations like XPEEM, LEEM and MEM, were done to find the temperature at which the InAs nanowire based device changes, not only the nanowire itself but also the over-all device surface features like contacts and the substrate. Finally, the $I$-$V$ measurements were performed for the n-doped InP nanowire based device and InAs nanowire based device for the electrical properties of the devices. SEM images were analyzed for the annealed devices for more information. The conclusion is that the surface oxides were successfully removed by H-cleaning while at moderate temperatures there is only a tiny effect on the conductance of the nanowire device. There is a strong change in metallic contacts at temperatures above than 500°C, which then strongly affects the device conductance.

# Acknowledgements

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# Popular Science Abstract

*Jalil Shah*

**Nanotechnology is generally considered as a key technology for the future of electronic and LEDs as well as from medical point of view. Different research fields of science are involved in nanotechnology, with semiconductor physics playing an important role. Using different fabrication techniques nanometer sized electronic and photonic devices can be made from different semiconductor materials.**

One dimensional rod-shaped nano-crystal structures, called nanowires, have tremendous applications. The growth and characterization of single crystalline semiconductor nanowires and nanowire based devices are major areas of research at Lund University. Nanowires have diameters in tens of nanometer (nm) range and lengths up to several micrometers (µm). III-V hetero-structure semiconductor nanowires consist of atoms from groups III and V in the periodic table. They have direct band gap and high electron mobility, so can be used both for high speed devices and photonics.

The surfaces of the III-V semiconductor nanowires are important because of their large surface-to-volume ratio, as surface atoms are more exposed to the environment compared to bulk atoms. Therefore the surfaces of these semiconductors are very sensitive to oxides. These native oxides create surface states which affect band bending, limiting the conductance of the nanowire devices. So these native oxides should be removed without changing the surface structure of the sample. In order to clean the surfaces of the III-V substrate and nanowires from the native oxides, the sample under study is exposed to atomic hydrogen during annealing. With this approach we can clean the surfaces of most III-V semiconductors at temperatures below thermal dissociation of the surface.

However, until now it has not been studied how such cleaning procedures will affect the performance of nanowire devices. Surface sensitive characterization techniques like Scanning Tunneling Microscopy (STM), Photo Emission Electron Microscopy (PEEM), Low Energy Electron Microscopy (LEEM) and Scanning Electron Microscopy (SEM) contribute a lot to the research by obtaining information not only about the surface but also about electrical properties for nanowires and nanowire based devices.

In this thesis, the changes of the surface structure and conductance of planar InAs, InAs nanowires and n-doped InP nanowires during cleaning have been studied with STM, PEEM, LEEM and SEM. The surface oxides of InAs(111)B substrate and InAs nanowires, are successfully removed by H-cleaning. At moderate temperatures there is only a tiny effect of the H-cleaning on the conductance of the nanowire device, but at temperatures above 500˚C the metallic contacts change strongly, which then considerably affects the device conductance. The most pronounced changes are because of chemical reactions of Aluminum wires which are used to connect the device externally with the metallic-(gold) contacts of the device, and because of some defects which have already been incorporated during the lithographic device processing.

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# Chapter 1: Introduction

Technological advancement in the field of nanotechnology has the potential to revolutionize the daily life of a human. Nanotechnology has many sub fields but one of the major is that of semiconducting nanowires and nanowire based devices. This is a main area of research at Lund University, Sweden. Nanowires are one dimensional rod shaped crystal structures having diameters in the range of tens of nanometer (nm) and lengths up to several micrometer (μm). Of special interest among these semiconductor nano-devices are III-V hetero-structure nanowires which consist of atoms from groups III and V in the periodic table. These nanowires have great potential for multipurpose use within the field of electronics and photonics [1-3]. Scanning Tunneling Microscopy (STM), Photo Emission Electron Microscopy (PEEM), Low Energy Electron Microscopy (LEEM) and Scanning Electron Microscopy (SEM) contribute a lot to the research by obtaining information about the surface and electrical properties [4].

The title of my thesis is '*Surface chemistry and electrical properties of nanowire devices*'. The surfaces of the III-V semiconductor nanowires are important because of their surface-to-volume ratio, but the surfaces of these semiconductors are very sensitive to oxides. These native oxides create surface states affect band bending, limiting the conductance of these nanowire devices. So these native oxides should be removed without changing the surface structure of the sample. In order to clean the surfaces of the III-V substrate and nanowires from the native oxides, the sample under study is exposed to atomic hydrogen during annealing. With this approach we can clean the surfaces of most III-V semiconductors at temperatures below thermal dissociation of the surface. In my thesis I have studied the changes of the surface structure and conductance of planar InAs and InAs nanowires during cleaning. The applied techniques are Scanning Tunneling Microscopy (*JEOL UHV STM*), Scanning Electron Microscopy (LEO SEM), Spectroscopic Photoemission and Low Energy Electron Microscopy (SPELEEM) at the MAX IV laboratory (MAX-lab) in Lund, and Optical Microscopy as well as conductance spectroscopy (*I-V* measurements).

The experiments and results of my thesis can be grouped in three parts:

1. The 1$^{st}$ part is to study the atomic-scale surfaces of InAs(111)B and of InAs nanowire surfaces using *JEOL STM*. For this purpose, the surfaces were exposed to atomic hydrogen while annealing to 450°C to remove native oxides (H-cleaning). I prepared the sample, performed the STM experiment, and analyzed the data.

2. In the 2$^{nd}$ part of my thesis, I used SPELEEM to image an individual nanowire device in-situ during H-cleaning and analyze with different contrast modes the effect of increasing temperature on the semiconductor nanowire and the integrity of the metal contacts. I prepared the sample, took part in the experiment, and analyzed the data.

3. The 3$^{rd}$ part of my thesis is to measure *I-V* curves of individual nanowire devices at different temperatures and to study the effect of the H-cleaning on the device performance. The *I-V* measurements were done in the UHV chamber of the *JEOL STM*. I prepared the sample, took the *I-V* data, and analyzed the data.

In conclusion I have successfully removed the surface oxides of InAs(111)B substrate and InAs nanowires by H-cleaning. At moderate temperatures there is only a tiny effect of the H-cleaning on the conductance of the nanowire device, but at temperatures above 500˚C the metallic contacts change strongly, which then strongly affects the device conductance. The most pronounced changes are because of chemical reactions of Aluminum wires which are used to connect the device externally with the metallic-(gold) contacts of the device, and because of some defects which have already been incorporated during the lithographic device processing.

# Chapter 2: Theory

## 2.1 Nanowires

Nanowires are 1D rod-shaped nanostructures with diameters within the nanometer ($1nm=10^{-9}m$) range. NWs can consist of metallic materials like Pt, Ni, Au etc, of insulating materials like $SiO_2$, $TiO_2$, etc., or can be made from semiconducting materials like Si, InAs, GaAs, etc. In this thesis we will discuss only III-V semiconductor NWs [5].

III-V semiconductors are made up of elements from the third and fifth groups of the periodic table. The elements which are most commonly used in III-V semiconductors are Gallium 'Ga' and Indium 'In' as group-III elements and nitrogen 'N', phosphorous 'P', arsenic 'As', and antimony 'Sb' as group-V elements. The elements from both III and V groups are arranged in crystal structures as binary compounds, ternary compounds, or quaternary compounds, or even more complex. Generally III-V semiconductor materials can be arranged in different shapes but in this thesis it is rod-shaped means wire shaped.

### 2.1.1 Properties and applications of III-V semiconductor NWs

The good points about all III-V semiconductors are that they have direct band gaps (except GaP) [5] and high electron or hole mobility compared to Si. The direct band gap means that electrons and holes can recombine directly with conserved momentum by emitting photons during the recombination process and so having advantages for optical application. Due to the high electron mobility, III-V semiconductors are useful for high-frequency electronic application. Because of these advantages, III-V semiconductors can be used in high speed devices, light emitting diodes (LEDs) as well as in solar cells. Although having these properties III-V semiconductors have only a small part of the semiconductor market nowadays and the basic reasons are those of higher production costs and problems when integrated with Si [5]. However these problems can be overcome when these materials are grown as nanowires. For the growth of III-V materials on Si wafers lattice mismatch is usually a large problem, but in the nanowire geometry this lattice mismatch gets easily compensated.

When the nanowire diameter is so small that the charge carriers are confined to 1D (typically for the diameter smaller than about 20nm), these nanowires are called quantum wires. For the NW to act as ID structure electrons should be quantum confined in the structure which is only possible when the diameter of the structure is less than the Fermi wavelength of an electron. Then this quantum confinement gives rise to novel photonic and electronic applications as well as fundamental studies of transport phenomena [5].

Besides the confinement, NWs also have two more interesting and unique properties related to surface and structure effects. The surface effect is the very large surface-to-volume ratio of NWs with surface atoms being more exposed to their environment than bulk atoms. Also NWs have more bulk than surface atoms, but the ratio is very different from thin films or large structures. This effect can be good in one application but can be bad in another. This surface related effect can be good for medical applications, since nanowires with their large surface can be used as biosensors, rectifiers and as guide for the nerve cells which opens new possibilities for neural network design [5]. The crystal structure is related to the production of the nanowires, meaning

that nanowires grow as crystals having either zincblende or wurtzite structure, resulting in different electronic properties. For example, GaP has an indirect band gap in zinc blende crystal structure which can't be used as LED but in some calculations it is shown that GaP grown in wurtzite crystal structure can have a direct band gap and thus could be used for LEDs, which is mainly depending on the quality of the production. The control of the crystal structure and the possibility of obtaining defect free hetero-structures make these nanowires applicable in industry [5].

### 2.1.2 Growth of III-V semiconductor NWs

For the growth of free standing NWs, two approaches are used: top-down or bottom-up. In top-down production of NWs, NWs are grown lithographically carving out the structures from the bulk materials, while in bottom-up production the NWs are grown by self-organized growth atom by atom in a highly controllable manner. For the growth of NWs mostly the bottom-up approach is a good option because in top-down approach the surface of the structures can be damaged having poor crystal quality because of the lithographic process. And second in the nanometer scaled semiconductor productions the top-down approach is not that much efficient because we can't get very small structures like nanowires [5].

Most widely, free standing nanowires are grown in a bottom up approach using a particle assisted growth method. In particle assisted growth, different materials are used as seed particles to grow NWs. The seeds are either metallic or organic in the form of particles. Upon metallic particles, gold is by far the mostly used seed materials probably because nanowire growth with gold particles was quite successful in the past, while it was difficult to achieve and control NW growth when using other materials [5]. But research is exploring other metallic materials as well, and there are free standing NWs grown using copper as a growth material, which is discussed in [6] and [8] and recommended for any interested reader but not covered in this thesis. For the growth of III-V semiconductor nanowires on Si substrate gold is often avoided, because gold makes deep levels (traps electrons and holes by deep-level recombination centers) in Si. In this case self-assembled organic films can be used for the growth of nanowires [7-8].

In order to obtain high crystalline quality of nanowires, epitaxial growth techniques are often used. Epitaxial nanowire means that a substrate of a specific crystal structure is used to orient the growth of the nanowire in an ordered manner so that the nanowire adopts the same crystalline structure as substrate [5]. Different epitaxial growth techniques are used for the growth of NWs where the word epitaxy means the single crystal growth on the surface of the crystalline substrate. The epitaxial growth techniques used for the growth of nanowires are Chemical Beam Epitaxy (CBE), Metal-Organic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE). The use of different types of precursors, growth performed under different pressures, and different ways of distributing the precursors can - among other things - differentiate these epitaxial growth techniques [5]. In this thesis, the NWs used in NW-based devices were grown by MOVPE technique, so only this technique will be described in detail.

### 2.1.3 Metal Organic Vapor Phase Epitaxy

In MOVPE for the growth of III-V semiconductor NWs, usually group III precursors are metal organic compounds like trimethylindium (TMI) and trimethlgallium (TMG) while group V

precursors are hydrides like Arsine ($AsH_3$) and Phosphine ($PH_3$). The crystal growth process starts because of the surface reactions of the decomposed of metal organic compounds and hydrides at the substrate. Carbon hydrogen compounds are as the rest products in such processes. Epitaxial layer growth for III-V occurs in a temperature range of 600˚C to 700˚C to ensure the decomposition of the precursors into individual elements. All methyl groups should be desorbed from the surfaces; otherwise the residual carbon levels will contaminate the III-V crystal [5].

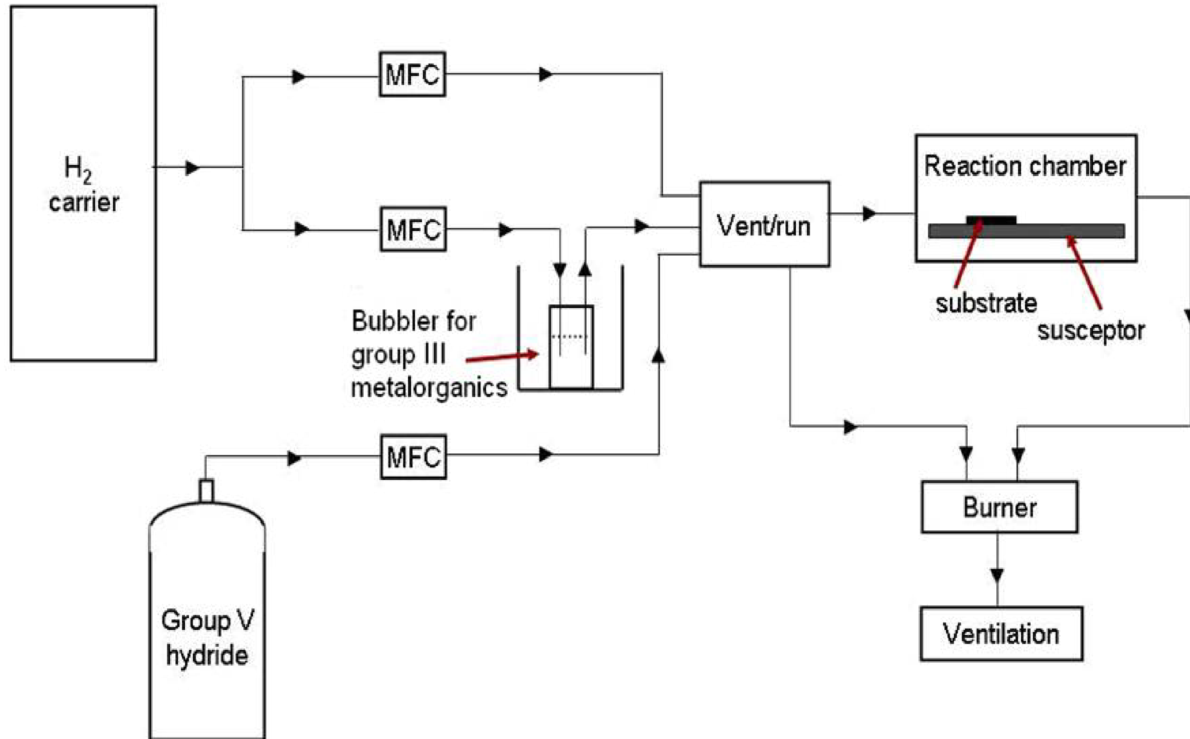



***Figure 2.1:*** *A schematic diagram of the MOVPE technique. Hydrogen is used as carrier gas for the precursors to the reaction chamber while the substrate is placed onto a susceptor and heat is applied. The excess gases as well as waste material are transported away [5].*

*Figure 2.1* shows the schematic diagram for a MOVPE system where the substrate is placed in the reaction chamber on a graphite susceptor which then is heated by radio frequency or by halogen lamps. In order to ensure that chemical reactions take place only on the substrate surface, the walls of the reactor chamber are kept cold [5]. The growth precursors are transported by the hydrogen gas through gas lines to the reaction chamber where the gas forms a laminar flow across the substrate surface [9]. The flow of the gases is regulated by mass flow controllers (MFCs) while the waste products like unreacted materials are transported away [5].

### 2.1.4 Gold particle assisted NWs Growth

The most common catalyst metallic material for bottom-up NW growth is gold. Gold particle assisted epitaxial growth of semiconductor nanowires usually starts with the deposition of gold nanoparticles on a clean semiconductor substrate. Gold particles with specific diameter and known surface density are desirable because the diameter and surface density of the nanowires depend on the diameter and surface density of gold particles [5]. The diameter of the nanowire is set by the

size of the gold particle while the length is set by the growth time [6]. The schematically view for the growth of nanowires is shown in the *figure 2.2*, below.

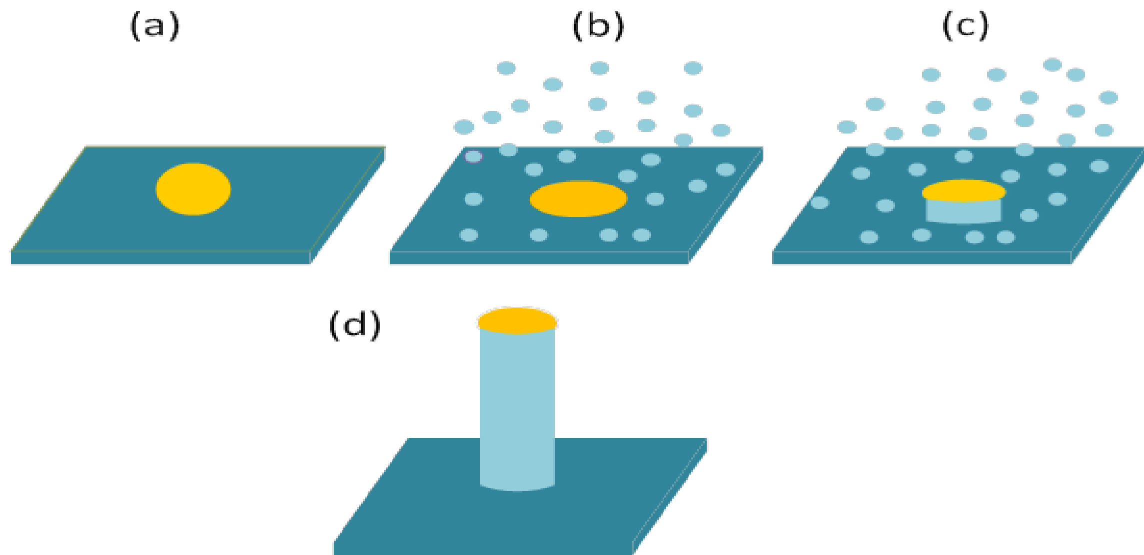



***Fig 2.2:*** *Schematic diagram for the growth of the NW.* ***(a)*** *The Au growth particles are deposited on the substrate.* ***(b)*** *The growth precursors are allowed to enter the growth chamber after temperature is increased for desorption of oxides residues.* ***(c)*** *The growth precursor atoms are combining under the Au particle.* ***(d)*** *The grown free-standing nanowire having Au particle on top.*

In the case of MOVPE, the substrate with deposited gold nanoparticles on the surface is placed in the reactor chamber as shown in *figure 2.2*. In the first step, the substrate is heated till desired growth temperature or to a temperature slightly above growth temperature for annealing. The purpose of this annealing step is to decompose the native surface oxides. During heating, constant partial pressure of group-V is maintained in order to prevent the decomposition of the substrate surface at elevated temperatures [5]. After this annealing step, the supply of the group III precursor is turned on because of which the actual growth is started (Figure 2.2 (b)). At elevated temperature and when the precursor materials come into contact with the gold particle an alloy is typically formed. Depending on the melting temperature of this particle compared to growth temperature it can be either liquid or solid [5]. When a certain amount of precursor material has been available for the particle then it will become supersaturated while the precipitation of the material will occur at the particle/substrate interface. This process is called nucleation shown in *figure 2.2 (c)*. As long as the continuous supply of the precursor is available nanowire growth takes place at the particle/nanowire interface (*figure 2.2 d*) and when the supply is not available upon turning off the group-III precursor then the growth process is terminated [5].

The gold particle assisted NW growth is most often described by the Vapor Liquid Solid (VLS) model, proposed by Wagner and Ellis in 1960 [10]. The different states of aggregation occurring in this model are vapor for the phase of precursor, liquid for the phase of particles and solid for the phase of nanowires. The phase of the particle can also be solid and here the model is called Vapor Solid Solid (VSS) [5] [10].

In some cases where we avoid gold as catalyst for the growth of NWs, the growth of the NWs can be done by self-assembled organic coatings which create an oxide template that guides the NW nucleation [8]. This technique is used for the processing of complementary metal oxide semiconductor (CMOS) NW devices where the oxide layer of $SiO_2$ is necessary. In this technique III-V NWs are grown on the substrate of Si, where gold particles would create deep levels in Si, see details in references given in section 2.1.2 [8].

## 2.2 Scanning Tunneling Microscopy (STM)

STM is working on the principle of the quantum tunneling effect in which electrons tunnel between a conducting tip and a conducting sample surface. STM was invented by Gerd Binning and Heinrich Rohrer in 1982 [11] for which they were awarded the Noble Prize in 1986 because with this invention the study of surface was revolutionized. This was also the birth of nano science because with the STM one can image surfaces down to the atomic level. Generally an STM has several components which are a scanning tip, a piezoelectric element which controls the height and the x-y scanning movement, a coarse movement for controlling the sample-to-tip approach, a vibration isolation system which protects the STM from vibration during scanning, an electronic feedback system and a computer as shown in the *figure 2.3 (a)* [12].

In STM, a very sharp metallic tip (having one atom at the apex for an ideal tip) is brought close to the conducting sample surface, having a gap of about 10Å. The gap between the tip and sample will act as a barrier for the electrons to tunnel. When a voltage is applied between the tip and sample, tunneling electrons produce a current in the range of pA-nA [6]. For imaging, the STM can be operated in two modes, the constant current mode and the constant height mode. In constant current mode a feedback mechanism is enabled which provides a constant current while a constant bias voltage is applied between the tip and sample. The tip is scanned over the sample surface by a piezoelectric element which realizes the $x$, $y$, and $z$ motions of the probe tip. The vertical/$z$ position is changed by the feedback electronics so that the current between the sample and probe tip is kept constant. The signal of the vertical tip position is transformed into the STM image contrast which represents the integrated local density of states. In constant height imaging mode, the tip is scanned at a constant height and a constant bias voltage is applied simultaneously. When the tip scans the surface including some topographic structures there is a variation in the tunneling current. This current forms the image and can be related to the integrated local density of states [12]. Both modes have advantages like in constant height mode one can image a flat surface with high speed while in constant current mode also samples with a larger corrugation can be studied where the tip height is adjusted and crashing into higher structures of the sample is avoided. Nanowires lying down on a surface can only be imaged in the constant current mode, since the tip has to move in $z$ direction in the 100 nm range while scanning across the surface.

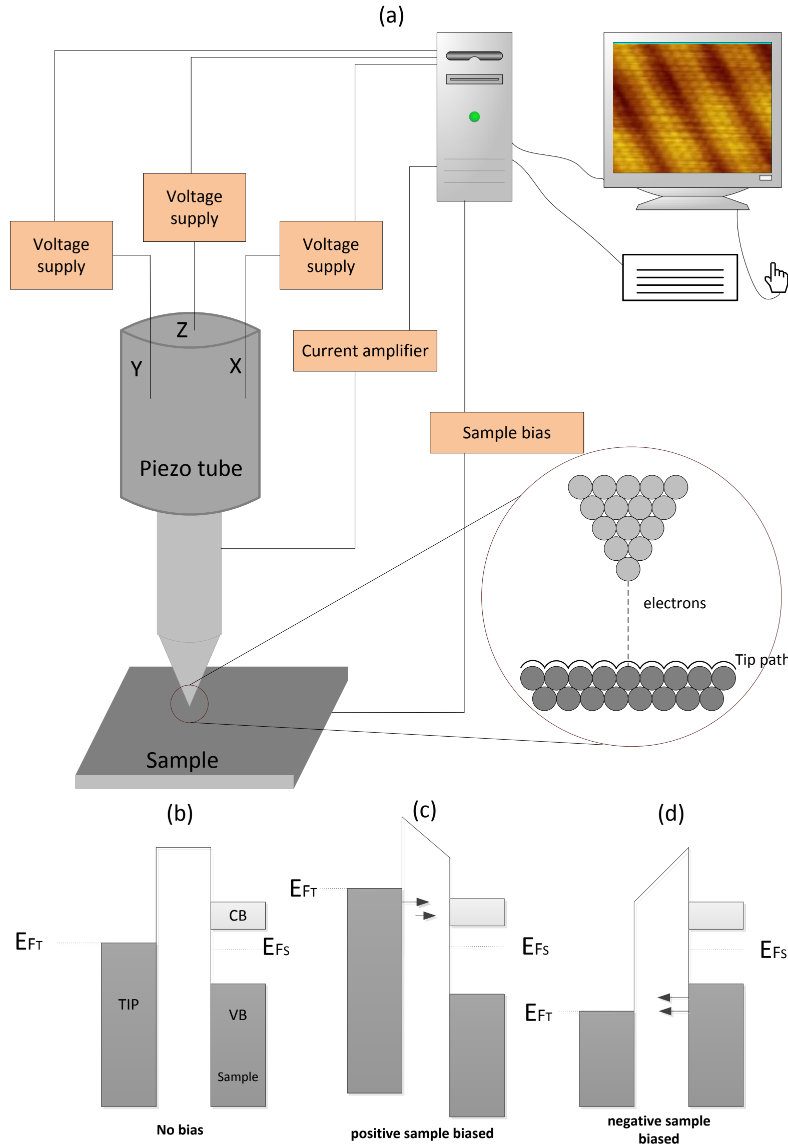



***Fig 2.3:*** *A typical STM diagram.* ***(a)*** *shows different parts of the STM and its principle.* ***(b)****,* ***(c)*** *and* ***(d)*** *show the energy diagram, when there is no sample bias, when the sample is positively biased and when the sample is negatively biased.*

In *figures 2 (b)* to *(d)* the tunneling of the electrons is shown schematically. In *figure 2(b)*, when there is no bias applied to the sample, there will be no flow of current in either direction. In *(c)* the tip is negatively biased, so the direction of flow of electrons is from the tip to the sample (the current is from the sample to the tip). While in *(d)* the flow of electrons is from sample towards the tip when there is negative bias on the sample.

In the simplest approximation of a one dimensional vacuum barrier, the tunneling current has exponential dependence on the separation between the tip and sample, *d* [6].

$$I \alpha \exp[-2\kappa d] \qquad (1)$$

Here $\kappa$ is the inverse electron decay rate which mainly depends on the sample bias [6] with

$$\kappa = \frac{\sqrt{2m(\phi - eV)}}{\hbar} \quad (2)$$

Here $\phi$ is the potential of the barrier, $eV$ is the energy of the electron given by the sample bias, $m$ is the mass of the electron and $\hbar$ is the Planck constant [12].

### 2.2.1 Theoretical description

In order to theoretically describe an STM image of surfaces at the atomic level, Tersoff and Hamann were using the Bardeen formulism and described the tunneling current by using perturbation theory. They took the tip and sample as independent systems, and the tunneling is the transition of the charge carrier from a certain state of one system to the certain state of another system [6]. The tunneling current, I, is then expressed as

$$I = \left[\frac{2\pi e}{\hbar}\right] \sum_{\mu,\nu} f(E_\mu^t)\left[1 - f\left(E_\nu^s + eV_T\right)\right] \left|M_{\mu\nu}\right|^2 \delta\left(E_\mu^t - E_\nu^s\right) \quad (3)$$

where $e$ is the electronic charge, $V_T$ is the tunneling voltage, $\hbar$ is the Planck constant, $f(E)$ is the Fermi distribution function, $E_\mu$ and $E_\nu$ are the energies of the states $\psi_\mu$ and $\psi_\nu$ of the sample and tip, respectively, and $M_{\mu\nu}$ is the transition matrix element between the states of the tip and the sample with

$$M_{\mu\nu} = -\frac{\hbar^2}{2m} \int \left(\psi_\mu^{t*} \nabla \psi_\nu^s - \psi_\nu^s \nabla \psi_\mu^{t*}\right) d\vec{S} \quad (4)$$

The transition matrix element is parameterized as an integral over an arbitrary plane, $S$, between the two subsystems [6]. In order to know the current one needs to know the wave functions of the tip and sample i.e. to calculate the matrix element. But most often these parameters are not exactly known, so some assumptions have to be made. Tersoff and Hamann assumed an ideal tip having spherical shape, electrically and geometrically isotropic, having s-like wave functions dominating the tunneling current. By using this model the tunneling current is proportional to the integrated local density of states (LDOS) integrated from the Fermi level up to $(E_F+eV)$ at the position $r_0$ of the tip

$$I \alpha \rho_t \int_0^{eV} \rho_{s.loc}\left(\vec{r}_0, E_F + \varepsilon\right) d\varepsilon \quad (5)$$

where $\rho_t$ is the LDOS for the outermost tip atom which is approximated as constant, and $\rho_{s,loc}(r,E)$ is the sample surface LDOS at the position $r_0$ and energy $E$ [6].

The electronic effects play a major role in the correct interpretation of the STM images correctly. Metals often have no strong variation in the LDOS near the Fermi level and the STM images are constant with $V_T$, typically showing positions of the atoms. On the other hand for semiconductors $V_T$ does not necessarily correspond to the surface topography. So to obtain images

of the same area, one uses different sample voltages to deduce the role of the electronic structure which is called voltage dependent imaging [6].

## 2.3 Spectroscopic Emission and Low Energy Electron Microscopy (SPELEEM)

A microscope is to study the surfaces of the samples, having several modes of operation i.e. chemical as well as structural contrast [8]. In this instrument, the sample is exposed to either low energy electrons or to photons. When reflected electrons are used for microscopy then this type of microscopy is called Low Energy Electron Microscopy (LEEM) and when the photoelectrons ejected from the sample exposed to high energetic photons are used for the microscopy then this type of microscopy is called Photo Emission Electron Microscopy (PEEM). *Figure 2.4*, shows the schematic diagram for SPELEEM in which the sample is shown exposed to electrons, synchrotron light, or ultraviolet/UV light [8].

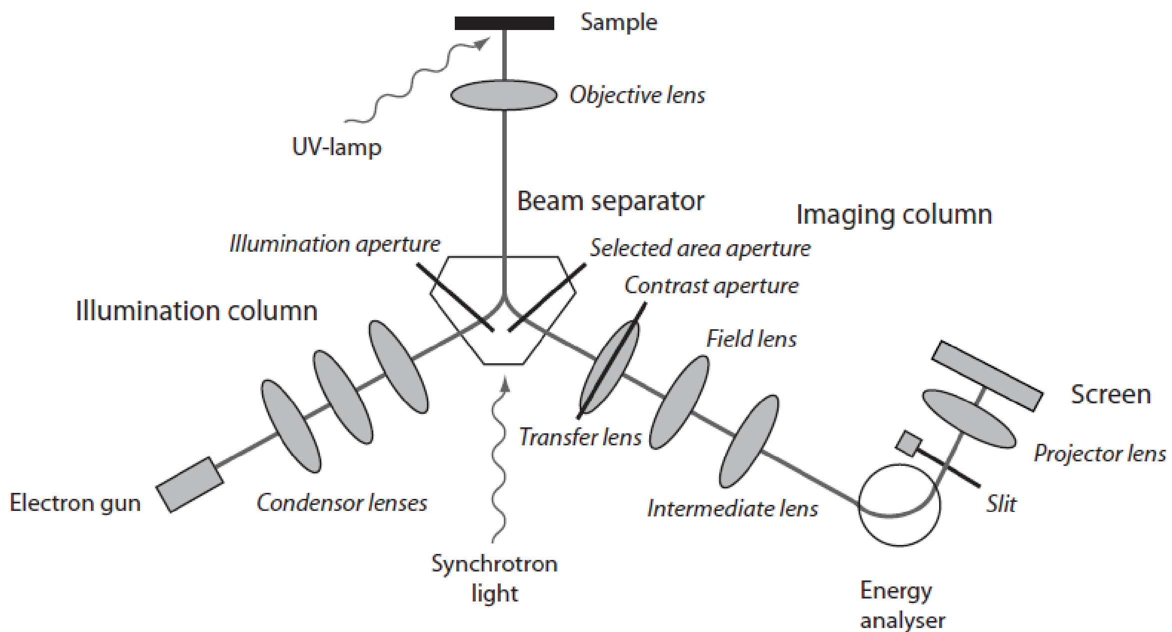



***Figure 2.4:*** *Schematic diagram for SPELEEM. The sample can be illuminated with low energy electrons or photons [9].*

### 2.3.1 Low Energy Electron Microscopy (LEEM) and Mirror Electron Microscopy (MEM)

In LEEM and MEM, the sample can be exposed to a parallel beam of low energy electrons which then are reflected from the surface of the sample, refocused for the image on a phosphorous screen. The electron source is an electron gun (Lanthanum hexaboride/$LaB_6$ cathode) which is kept at -20keV [6]. The electrons then enter into an illumination column having three condenser lenses, in which the electrons are brought into beam and focused at the sample. Then the electron beam passes through the magnetic beam separator where it is deflected at 60˚ [6] and through an objective lens, before it hits the sample. The sample is kept at the same high voltage as the electron gun plus an additional small starting voltage (*SV*) therefore the sample acts as a cathode lens [8]. The starting voltage is typically a few volts; therefore the method is called low energy electron

microscopy. Because of the *SV* the electrons which are supplied by the electron gun and come close to the sample are slightly decelerated by the electric field on the sample. So the energy of the electrons after interacting with the sample surface is still to 20keV-eSV, when they again in the same path then enter once more the magnetic beam separator. After being deflected in the magnetic beam separator the reflected/interacted electrons enter the image column where they are focused by a couple of lenses. Then these electrons enter into the hemispherical electron energy analyzer and are sorted out according to their energies. Finally the electron signal is projected onto a micro channel plate (MCP) and detected on the phosphorous screen by the CCD camera [8].

By changing the strength of the lenses in the imaging column one can project either the image plane (IP) or the back focal plane (BFP) onto the MCP, obtaining either the LEEM images or a Low Energy Electron Diffraction (LEED) pattern on the screen, as sketched in *figure 2.5* [8]. Crystallographic ordered samples are needed for diffraction-based LEED patterns

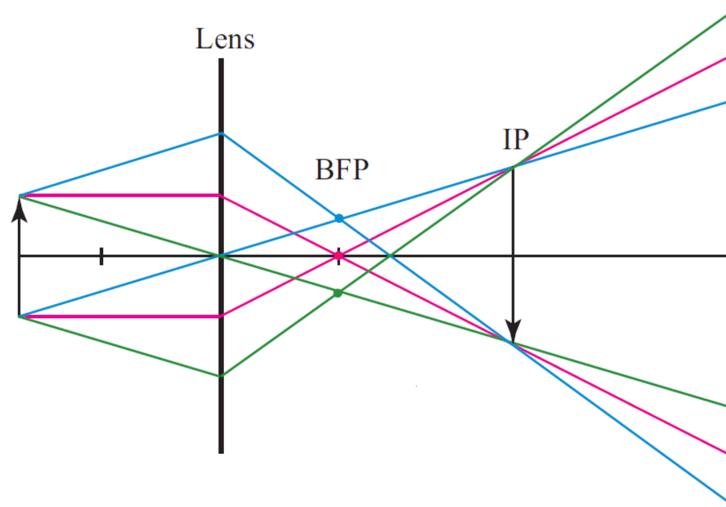



***Figure 2.5:*** *Schematic ray diagram for the LEEM image formation. Parallel rays are united at the back focal plane, BFP, which can be used for obtaining a LEED pattern. Rays from the same object unite at the Gaussian image plane, IP, where the LEEM image is formed [8].*

LEEM images can be either Bright Field (BF) or Dark Field (DF) images depending on the position of the contrast aperture (CA) in the image column, as shown in *figure 2.6*. In bright field LEEM the diffraction spot is centered around the axis while in dark field LEEM it is centered on another reflection spot as shown in *figure 2.6*.

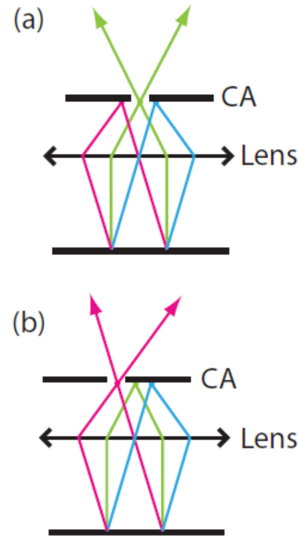



***Figure 2.6:*** *Principles of bright field (BF) and dark field (DF) LEEM imaging.* ***(a)*** *BF LEEM image was done when the on-axis spot of the diffraction pattern is chosen by the contrast aperture, CA.* ***(b)*** *DF LEEM image is formed when off-axis spots are chosen by CA [8].*

If the *SV* is approximately in the range of *1V* then the electrons will only interact with the electric field of the samples which means that electrons will not interact with the sample surface but will be reflected back a few nanometers away from the surface. This imaging mode is called Mirror Electron Microscopy (MEM). The contrast in MEM is because of the work function differences and topography variations [6]. MEM imaging is considered as non-destructive and is a very useful technique because it does not require a crystallographic surface [8].

### 2.3.2 Photo Emission Electron Microscopy (PEEM)

The PEEM works on the principle of the photoelectric effect in which photons are absorbed by the sample and photoelectrons are emitted. Therefore in PEEM the sample is exposed to photons and photoelectrons are emitted. These photoelectrons are then used for making the image of the sample surface. These photoelectrons can be secondary electrons resulting from multiple scattering within the sample, resulting in an image contrast which depends on work function differences, or can be valence band core level electrons which give chemical contrast. The energy of the excited photons must be larger than energy of the emitted electrons; therefore UV photons can only excite secondary electrons or valence band electrons, while photons from synchrotron radiation can excite secondary electrons, valence band electrons, and core level electrons. In SPELEEM shown in *figure 2.4*, the electron gun is turned off and instead the sample is exposed to photons. The photoelectrons from the sample are refocused, energy filtered in the energy analyzer and projected onto the screen as was also done for the reflected electrons of LEEM imaging [6]. The energy analyzer sorts the photoelectrons according to their energies, and by inserting a slit in the dispersive plane only electrons of certain energies are used for imaging [8]. So one can get either secondary electron (SE) XPEEM images or can get core level electron XPEEM images.

## 2.4 Studying surfaces of III-V Semiconductors

For the technological as well as academic point of view the studies of both surfaces and interfaces of III-V semiconductor materials are very important [13]. The microscopic study of clean

and ordered surfaces and interfaces of III-V semiconductor is now possible due to the advancement in the Ultra High Vacuum technology. The movement of the atoms during reconstruction (to reduce the energy of their surfaces), the layer of atoms involved in this reconstruction, the electronic and vibrational states for this movement, and the final symmetry of the surfaces or interface are all important for the fundamental and microscopic understanding of the nature of III-V semiconductor surfaces [13].

As we come down from large structures to the nanostructures like nanowires, the surface-to-bulk ratio increases. Surface atoms are very important for the electrical and optical properties of a nanowire [8].

## 2.5 Surface of III-V substrates and NWs

The atomic scale surface structure and morphology of the freestanding semiconductor nanowires is important for their electrical, chemical and optical properties. Also important for the growth. Therefore the detailed information of the nanowire surface is important for electronics, photonics and biology.

If a III-V zincblende crystal is cleaved along its (111) plane, then the resulting surfaces will be polar and terminated by one atomic species. Generally the group V terminated surface is called (111)B, while the group III terminated one is called (111)A surface. The (111)B surfaces of III-V semiconductors like GaAs(111)B, InAs(111)B, etc are very important for the growth of nanowires because III-V semiconductor nanowires prefer to grow perpendicular to these (111)B surfaces. The (111)B surfaces are quite difficult to prepare for atomic scale studies because the surface decomposes at a temperature below the temperature at which the oxides desorbs [8].

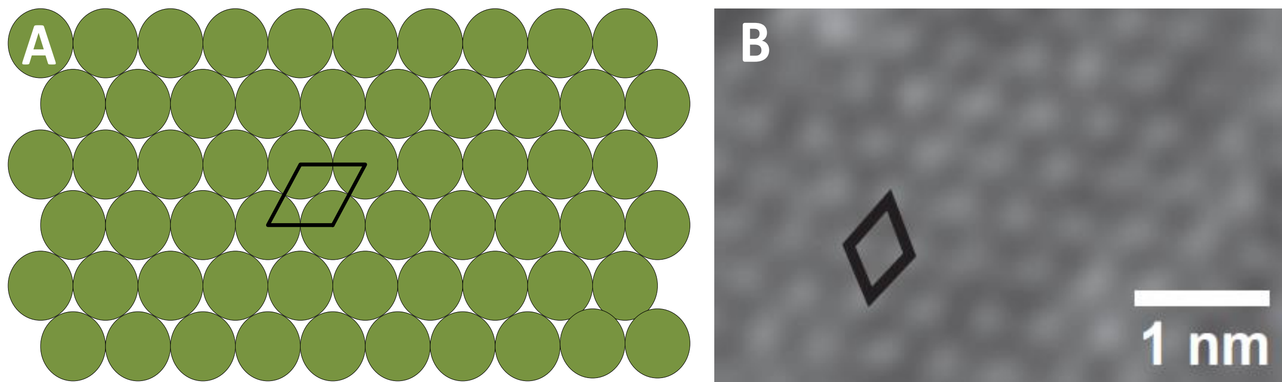



***Figure 2.7:*** *Arrangement of the atoms in (111) surfaces of III-V semiconductors. (A) Sketch of the arrangement of atoms. (B) STM image for (1×1) structure of InAs(111) surface with bias voltage of -2V [8].*

*Figure 2.4 (A),* shows the sketch for the arrangement of the atoms in zincblende (111) structure for III-V semiconductors which is a theoretical sketch. While *figure 2.4 (B)*, shows the STM image of a cleaned InAs (111)B surface, where the arrangement of the atoms is the same as in the theoretical arrangement of the atoms in *figure 2.4 (B)*.

# Chapter 3: Experimental setup

In this thesis three experiments were done to investigate the surface chemistry and electrical properties of the NW based devices. In the 1st experiment, a *JEOL Scanning Tunneling Microscope (JEOL STM)* was used for surface investigation of InAs(111)B substrates and InAs nanowires. The *JEOL STM* setup is present in the Department of Physics, Lund University, Lund, Sweden. In the 2nd experiment, *Spectroscopic Emission and Low Energy Electron Microscopy (SPELEEM)* present at beamline I311 of the *MAX IV Laboratory (Max-lab) Lund, Sweden*, was used to investigate structural and chemical changes of the nanowire and metallic contacts of a NW based device as a function of temperature. *SPELEEM* has several modes of operation like *Low Energy Electron Microscopy (LEEM)*, *Mirror Electron Microscopy (MEM)*, and *PhotoElectron Emission Microscopy (PEEM)/PhotoElectron Spectroscopy (PES).* The Max-lab *SPELEEM* has been described in section 2.3 of chapter 2, for further details refer to ref. [8]. Also in the second experiment Scanning Electron Microscopy (*SEM,* present in the *Nanometer Consortium* at *Lund University, Sweden*) images were obtained for the NW device heated to 700˚C in the *SPELEEM*. In the 3rd experiment, the electrical characterization as a function of temperature for the NW based device was done for which the treat chamber of the *JEOL STM* was used. The treat chamber of the *JEOL STM* has electrical and heating setups for the IV measurement of the NW device under UHV condition. Then SEM images for the heated device were investigated.

## 3.1 STM Setup

The apparatus used for STM setup is a *JEOL STM* setup which is shown in the *figure 3.1*. The setup consists of two chambers, the treat chamber and the STM chamber (analysis chamber).

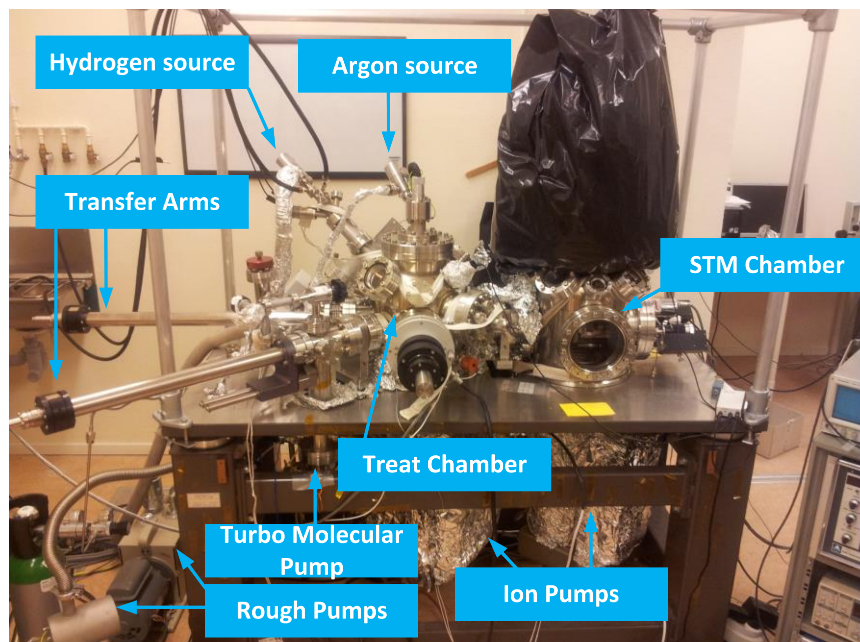



***Figure 3.1:*** *JEOL STM present in room C161 at Department of Physics, Lund University, Sweden.*

The treat chamber is used to prepare the samples and tips for the experiment while the STM chamber is used for the analysis of the sample. These two chambers have a base pressure of in the

$10^{-10}$ mbar range and are separated by a valve which protects the pressure of the STM chamber from the pressure of the treat chamber during the preparation of the sample or sputtering of the tip (section 3.2). There is also a load lock which is used to load the prepared sample from outside environment. The two transfer rods are used to transfer the sample or tip. An ion pump is common to both chambers while treat chamber and load lock have some extra pumps called Turbo Molecular Pump (TMP) and rough pump. The hydrogen source is used in H-cleaning (section 3.4), while an argon (Ar) source is used in tip preparation (section 3.2), as shown in *figure 3.1*.

When the tip or sample has been prepared (sections 3.2 and 3.4) outside UHV, then it is mounted in the transfer arm of the load lock. Then both turbo molecular and rough pumps attached to the load lock are allowed to run for almost 2 hours until the pressure in the load lock is almost equal to the base pressure of the treat chamber. With the help of the transfer arm the tip or sample is transferred to one of the storage positions in the treat chamber (4 sample positions and 3 tip positions). Then in the treat chamber the sample and the tip are further treated for the experiment.

## 3.2 STM Tip preparation

In any scanning probe technique one cannot expect good results without a good probe so the STM data is limited by a good tunneling tip. So for obtaining good STM images with atomic resolution the tip should be perfect. And preparing a perfect tip is one of the experimental key aspects of the STM. The resolution (all the important details of the image) is mostly depending on the radius of curvature of the tunneling tip. A perfect tip should be so sharp that there is only one atom at the apex as shown in *figure 3.2*.

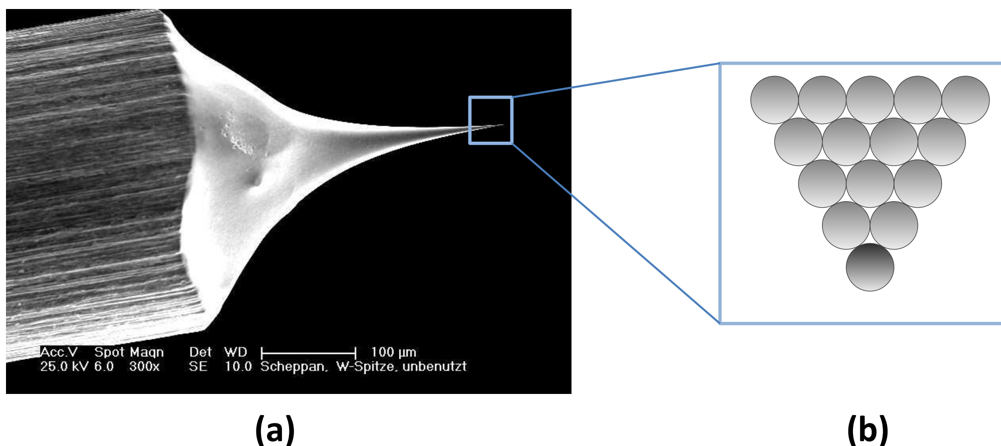



***Figure 3.2:*** *A perfect tip.* ***(a)*** *A very sharp tip [14].* ***(b)*** *Sketch of the atomic structure of a perfect tip apex.*

The chemical identity and the arrangement of the tip atoms closest to the sample surface determine the stability and resolution of the imaging. Both parameters are very difficult to control or quantify [12].

### 3.2.1: Tip shape/Arrangement of the tip atoms

In the Tersoff Hamann theory (ch. 2.2.1) the STM tip is described as a spherical potential well without any atomic features, like small clusters of three to four atoms or a single atom. To

avoid vibrations of the tip, the tip should not be too long and come to the point rapidly as shown in the *figure 3.2(a)*. Such a tip has a high resonance frequency, and practically tips with exponentially decreasing radii are easy to produce. Tips with several widely spaced mini tips which are close to the sample surface can lead to disjointed and confusing images. In special cases this can lead to double images which can be easily distinguished by the repetition of surface features of identical shape [12].

So in STM the quality of the tip is very important for scanning especially for non-flat surfaces. For the investigation of nanowires at the atomic level the tip should be atomically sharp in order not to get multiple features. If the tip ends in multiple micro tips, for example a double tip, each object will appear twice (or multiple times) in the image [12].

### 3.2.2: Tip material/Chemical identity of the tip atoms

The chemical identity of the tip atoms is an important factor in the performance of the STM. Atoms like Na have *s* valence orbitals while atoms like W have *d* valence orbitals. Therefore metals like Na have s-band electrons at the Fermi level while metals like W have d-band electrons at the Fermi level. So the tunneling performance of these two metals/materials will be different from each other by the fact that the d-band tip is more sensitive to small features on the sample surface than the s-band tip and has the higher resolution. The reason for the higher resolution is that the electrons in d-orbitals are more localized than the electrons in s orbitals, and that the tips are more sensitive because the tunneling matrix element is enhanced by the greater charge localization [12].

### 3.2.3: Tip etching

For the production of a sharp tip, as in our case, a tungsten wire of 0.25 mm diameter is electro-chemically etched using an 8% sodium hydroxide (NaOH) solution as electrolyte while a voltage is applied between the wire and a steel cathode. After the etching process, the tip is checked under the optical microscope to see whether we have got a sharp tip or not. If we have a sharp tip then we clean it with distilled water and isopropanol by holding the tip in such a way that the direction of the tip is in the direction of the flow of liquid so that the liquid should not hit the tip. If the tip is being hit then the sharp end of the tip may be damaged due to the impact of the cleaning liquid. Since the oxides cannot be cleaned with cleaning liquids the tip is then transferred to the treat chamber where it is sputtered with Ar ions. Therefore Ar gas is introduced into the treat chamber with a pressure of $2.5\times10^{-6}$ mbar and ionized in a sputter gun at energies of 2.5 kV and a filament current of 10 mA. The duration of sputtering is almost 20 to 25 minutes.

## 3.3 Problems with the JEOL STM and their overcoming

There were some problems with the *JEOL STM* which I should mention here in this part. The *JEOL STM* we were using for the experiment is a low temperature STM, so a cooling system with a cylindrical shaped cryostat is directly attached to the STM chamber. So acoustic resonances in the cryostat because of sounds from the surroundings will affect the STM images during scanning; therefore our STM is very sensitive to external sounds. These external sounds come when someone walks through the corridor talking or someone is wearing high heel shoes (which make much sound during walking) so these sounds make disturbance during the STM scanning. In order to overcome this problem we covered the cryostat first with Al foil, a blanket, and a plastic bag for vibration damping.

Another problem with the *JEOL STM* was that the *x* and *y* coarse movement didn't work properly especially when one wanted to move the tip from one area of the sample to another. In order to solve this problem the STM stage was taken out of the chamber and then taken apart and the mechanical parts of the *x* and *y* coarse positioning were cleaned with propanol in an ultrasonic bath. Then the STM was put back together.

One should be aware that for transferring a sample or tip in the STM chamber of the *JEOL STM*, one needs to bring the *x* and *y* coarse positioning back to the mean position after moving the tip. Otherwise it will be difficult to put the sample in the sample holder.

## 3.4 Sample preparation

In this thesis three experimental works were performed with three different setups. The different preparations of these samples are described in sections below.

### 3.4.1: Sample preparation for the surface studies in STM

In order to study surfaces, especially the surfaces of semiconductor samples, (in our case an InAs (111)B substrate and InAs NWs on InAs (111)B substrate by using the JEOL STM) one needs to go through several steps. In case of a flat surface analysis one needs to mount a sample in the sample holder and then prepare the surface for the STM in the treat chamber, but in case of NW surface studies one need to do some extra work along with mounting and cleaning. As it is not possible to image the surfaces of free standing NWs one needs first to transfer as-grown NWs from their growth substrate on a new substrate horizontally, so that most of the surface of a NW is exposed. Thereby the break off should be at the base of the NW so that the whole surface, meaning from top to base can be scanned. This is because the whole structure of a NW has interesting features in different axial positions along the NW [6].

In order to prepare the sample for STM surface studies we first clean all the equipment used to handle the sample and sample holder because we need a cleaned sample and clean environment inside the STM. After that we take a new substrate, e.g. InAs(111)B if one uses InAs nanowires, and cut it with a diamond cutter related to the size of the sample holder. Then we take the standing nanowires' substrate and put it very carefully on the desired area of the InAs(111)B substrate. After this, we press the NW sample gently several times, so that we can obtain some kind of milky area on the new substrate which indicates scattering light from the deposited NWs. After we have made sure that we have enough nanowires for scanning, we mount the sample on the sample holder for STM. The next step is to clean the sample from oxide contamination. To do so that we put the sample in the airlock of the STM chamber and run all the pumps for almost 2 hours. Then we open the valve to the treat chamber and transfer the sample, by using the transfer rod, from the airlock to position 2 or 4 in the sample storage stage of the treat chamber. Then we close the valve again.

### 3.4.2 Sample preparation for *I-V* spectra of NW devices by using JEOL *STM* setup

*Figure 3.3(a)* shows a number of NW based devices in which the NWs are deposited on a $SiO_2$/Si substrate, with predefined thick and medium sized Au contacts/pads and small lithographically defined contacts between the NWs and pre-defined contacts. Lithography was done after finding NWs with SEM or optical microscopy. The NW devices, which are investigated regarding their IV spectra, have been prepared at *Division of Solid State Physics, Department of*

*Physics, Lund University, Sweden*. A typical NW device is shown in *figure 3.3 (c)*. These devices can be connected to external voltage sources by external contacts. These external contacts can be made by Al bonding wires using a bondage machine (K&S 4523D) present in *Division of Solid State Physics*. For dealing with the bondage machine one needs a lot of expertise because of the small size of the devices and Au pads. Before making the external contacts the devices are checked for the conductivity by using the information given by the manufacturers of these devices. Then a device with good conductance is selected for the IV measurements.

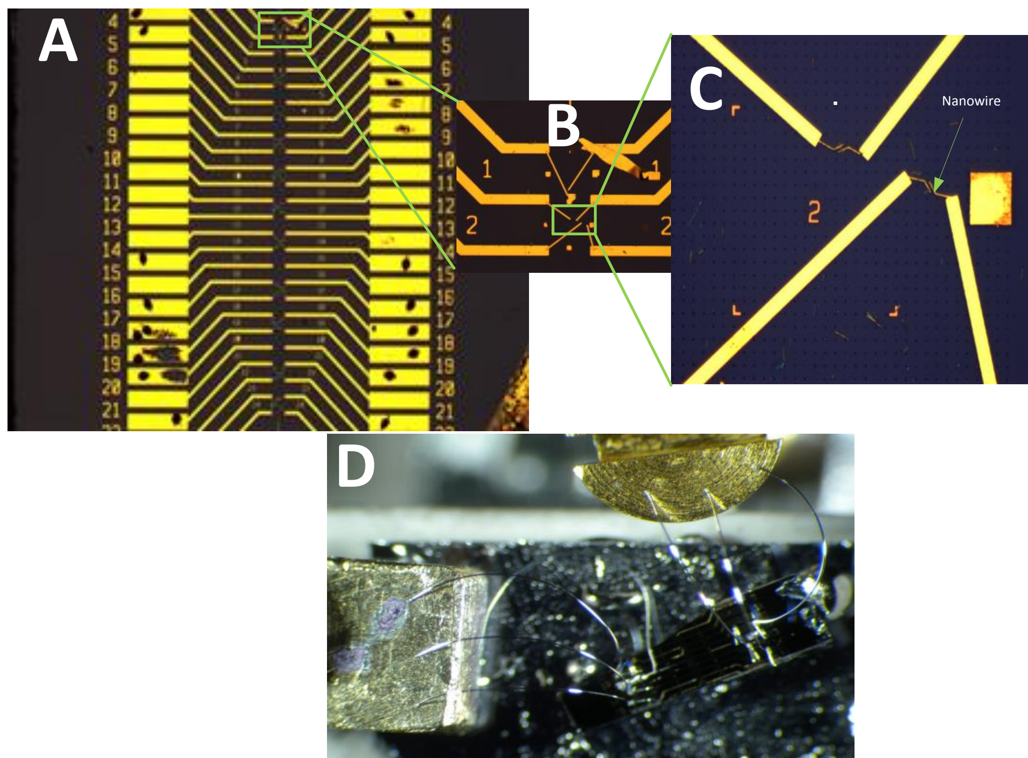



***Figure 3.3:*** *Optical microscope images for NW devices.* ***(a)*** *A substrate having 24 NW devices. Big Au pads are also shown which can be used to connect the NW devices to the external voltage source.* ***(b)*** *Smaller Au contacts to the NW.* ***(c)*** *Shows a nanowire connected to big Au pads through small contacts.* ***(d)*** *Shows the external contacts of the NW devices made by the Al wire bonding.*

### 3.4.3: Sample preparation for PEEM/LEEM

For the PEEM/LEEM studies the sample has been prepared by depositing a layer of gold on the outer sample surface while the center remains free. The layer of gold can be made by evaporating gold on the surface using a home built gold evaporator exposing the sample for some time with a mask covering the central, Au-free area, as shown in *figure 3.4*. The reason for the gold layer is that charge should not build up during the exposure of the sample to radiation. The time for the deposition of the gold is between 20 and 40 minutes.

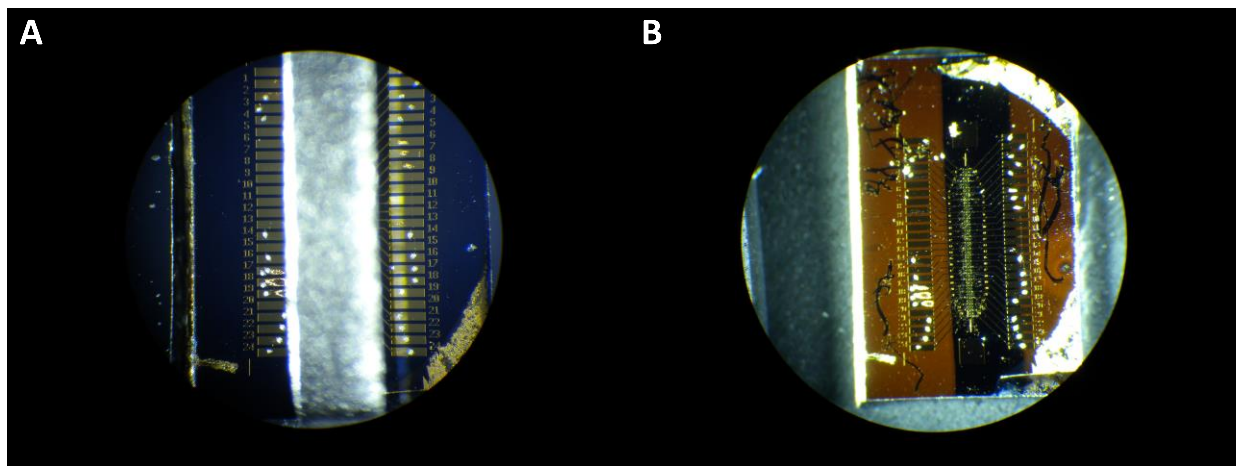



***Figure 3.4*** *shows the deposition of gold on a NW device for the PEEM/LEEM studies.* ***(A)*** *before gold deposition with a metallic strip to protect the central part of the NW devices from gold.* ***(B)*** *with gold layer except at the central part.*

### 3.4.4: Cleaning the Sample

When the III-V semiconductor nanowires are readily grown in the epitaxy chamber in the clean room and then taken out to the air, the air oxygen immediately attacks the surface creating oxides on the surface in a very short time. This oxide layer will act as an insulator creating problems during scanning the surface especially with the STM, because it inhibits the current from the metallic tip to the conductive surface of the III-V semiconductor substrates as well as nanowires.

One of the methods used in surface science to deoxidize the surface of any sample is annealing in which the sample is heated at high temperature until the clean surface is exposed. But the surface of a III-V semiconductor sample can be destroyed before we reach the temperature to deoxidize the surface; The surface III-V semiconductor materials will decompose because of the preferential evaporation of group V element leaving behind group III elements in the form of droplets [25-28]. So a method used to deoxidize the surface of III-V samples together with annealing is to expose the surface to reactive hydrogen atoms which react with the oxides. This makes the surface clean at a temperature where the atomic arrangement on the surface is not yet destroyed. The reactive hydrogen atoms or radicals can be achieved by passing molecular hydrogen gas through a hot filament called the hydrogen cracker. In our experiment the pressure used for the hydrogen molecules is $P_{Hydrogen}=2\times10^{-5}$ mbar while the current for the hydrogen cracker is $I_{Hydrogen-cracker}=5A$. This annealing is called hydrogen cleaning or simply H-cleaning.

In our experiment we used a rather simple home-built tungsten filament cracker shown in *figure 3.5*.

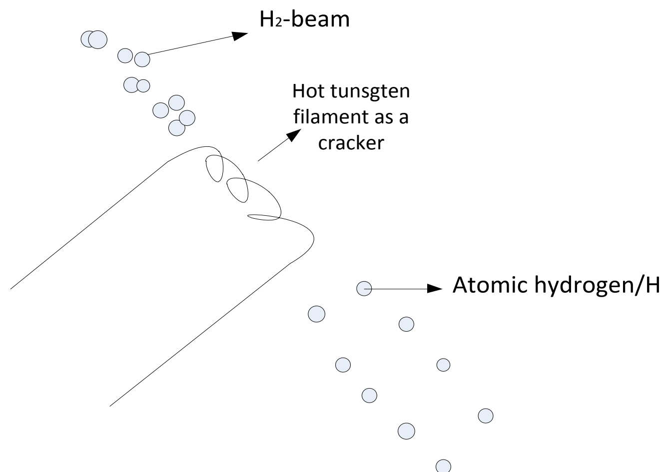



***Figure3.5:*** *The home-built hydrogen cracker used, made up from tungsten wire.*

By comparing the efficiency of our home built hydrogen cracker with other commercial hydrogen crackers then its efficiency is not that good. The amount of reactive hydrogen atom quantity is not efficient because there is mixture of hydrogen molecules and hydrogen atoms.

**Note**: The H-cleaning procedure is same for all three types of experiment i.e. cleaning surface but slightly different for IV measurements of the NW base devices.

## 3.5 Procedure to clean and measure the *I-V* curve for the Nanowire devices

1. First measure the NW *I-V* outside the vacuum, before transferring the device into the STM chamber. The reason to do this step is to make sure that the bonding wires are connected to the desired nanowire device and also that the device is ok for *I-V* measurement, because some of the devices are not working property.

2. Transfer the device into vacuum to measure the *I-V* curve at room temperature.

3. Heat the device along with hydrogen cleaning to 350°C for a time of 20 minutes.

4. Wait until the temperature of the device is down at room temperature again, which may take several hours.

5. Measure the IV curve in vacuum again.

6. Repeat steps 3 to 5 if no change occurs.

7. If still no changes have happened increase the annealing temperature by steps of 20°-30°C for heating (step 3) and follow steps 4 to 7 until you see a change in the *I-V* curve. .

8. Transfer the device to the load-lock and vent it. The reason to do this step is to check whether the observed change in *I-V* properties is because of oxygen reduction or because of heating.

9. Put the device back in vacuum and measure an *I-V* curve.

10. Repeat cleaning (heating) at the temperature last used, until the IV curve prior to venting is recovered, then

11. Further increase the temperature by 20°-30°C and repeat steps 7 to 11 accordingly, until the sample is destroyed.

## Precautions:

Some precautions should be taken during the preparation of the sample for *I-V* measurements and when performing the IV measurement. These precautions are

1. To avoid static charges, wear a grounding arm-wrist during the mounting and bonding of wires and measuring the *I-V*, because nanowires are sensitive to static charges.

2. When connecting the nanowires to the current amplifier, always ground that connection first to avoid static charges.

3. During the experiment for *I-V* measurement do not turn off and on any light because NWs are also sensitive to light and also because switching the light could induce electrostatic charges.

# Chapter 4: Results and discussion

In this chapter the experimental work has been divided into three different parts and discussed. The first part is about the STM images analyzed for the surface of an InAs(111)B substrate and InAs nanowires using *JEOL STM*. In second part the *PEEM*, *LEEM*, *MEM* images, and *PES* spectra of the InAs nanowire device are discussed. In the third part *I-V* data for InP and InAs nanowire devices have been discussed. For the second and third parts the SEM images for the heated devices are also discussed in order to see over all changes in the devices.

The reason of doing these experiments is that when we expose III-V semiconductor nanowires from the growth chamber to our environment then oxygen atoms (20-21% in earth's atmosphere) immediately attack the surface of III-V nanowires forming an oxide layer which becomes thicker and thicker with time. The native oxides on the surfaces of the nanowires can affect the conductance of the nanowire because these oxides create states on the nanowire surface. These surface states can affect the band bending and then the conductance of the device, an effect called Fermi level pinning. Mostly the atomic layer closer to the surface produces such type of band bending. As the diameter of the NW is in the range of nanometer so these oxide states will highly affect the conductance of the NW and NW based devices. Another point about the oxide layer is that it will act as an insulator especially when studying surfaces using STM. So the atomic level microscopy for the surface of III-V nanowires through STM will not be possible. So this native oxide layer should be removed in order to take the atomic level images and to see good conductance.

## 4.1: STM imaging of H-cleaned surfaces and NWs

In this part, the STM images taken in *JOEL STM* are shown and analyzed using *WS×M* software. The sample used for the analysis is an InAs(111)B substrate and InAs nanowires grown at *Division of Solid State Physics, Lund University, Sweden*.

### 4.1.1: InAs(111)B surface

*Figure 1a* and *1b* show the surfaces of an InAs(111)B substrate after 10 minutes of H-cleaning (section 3.4.4 chapter 3).

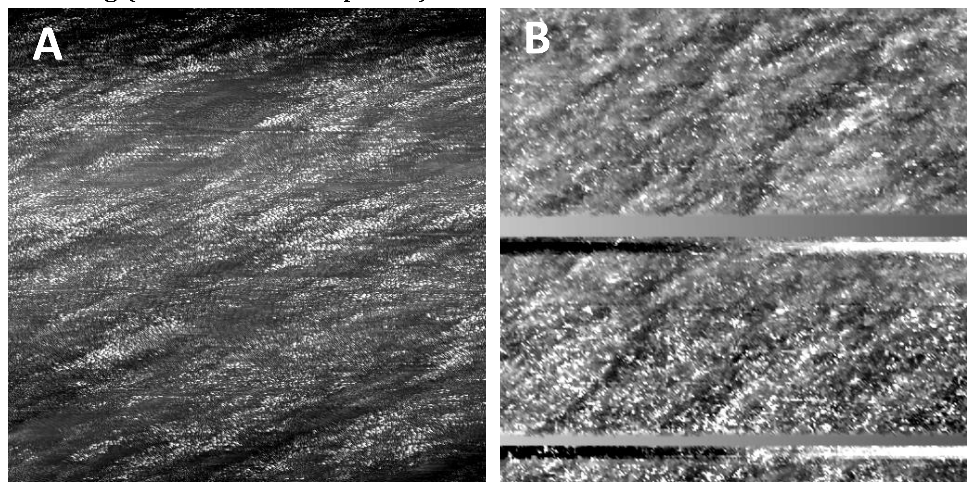



***Figure 4.1**: STM images of InAs(111)B surface but covered with native oxides (U=-2.5V, $I_{tunneling}$=25pA). **(A)** Area=200×200nm$^2$ and **(B)** Area=50×50nm$^2$.*

The annealing temperature for H-cleaning was T=380-390˚C while the current for heating the sample was $I_{heating}$=0.47A. From the images in *figure 4.1*, taken after the cleaning and subsequent

cool-down, it is clear that still we have native oxides on the surface and the surface is not yet clean. And one can see that the tip was unstable during scanning the surface and changed its properties several times, which is the indication that still we have oxides on the surface. So 10 minutes of H-cleaning is not enough time to clean the surface from oxides.

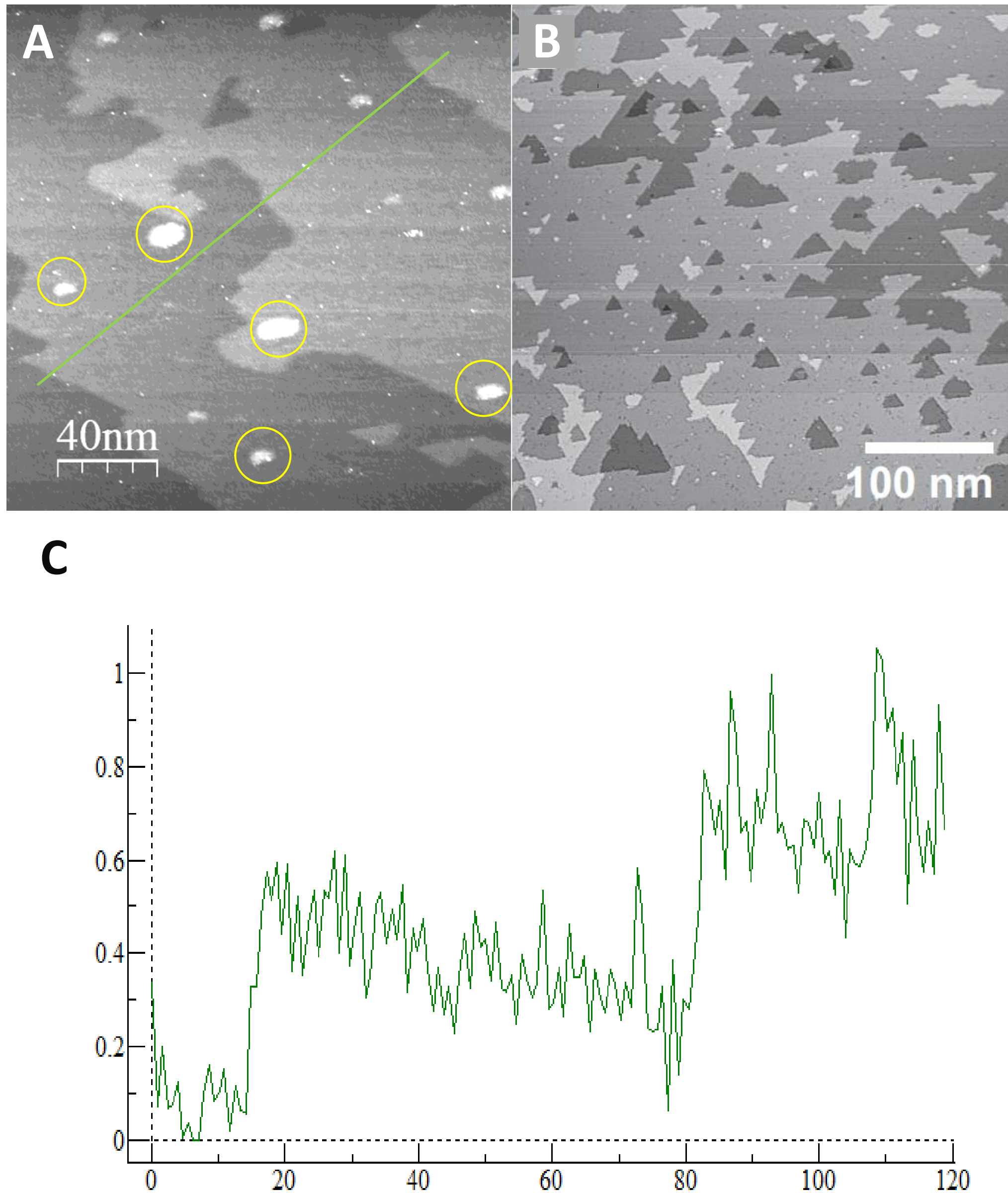



***Figure 4.2***: *STM images of InAs(111)B,* ***(A)*** *STM image of InAs(111)B (U=-2.5V, $I_{tunneling}$=25pA) 200×200nm²* *after 40 minutes of annealing at 400˚C in atomic hydrogen.* ***(B)*** *STM image of InAs(111)B (U=-2V) 390×390nm²* *after 40 minutes of annealing at 400˚C in atomic hydrogen [15].* ***(C)*** *shows the height profile of the green line in (A), with x and y axes in nm.*

The *figure 4.2* shows the result after 40 minutes of H-cleaning with annealing temperature of 380˚C-400˚C while the current for the sample heating is $I_{heating}$=0.48A. From the image it looks like the surface is clean with terraces and steps. We can also see drops marked with yellow circles

which might be indium droplets. Such indium droplets are expected to form when InAs is annealed at or above the temperature of thermal dissociations, leading to arsenic (As) out-diffusion, leaving In droplets on the surface. The clusters we can see here may be indications of initial In formation after that much heating.

The height of the terraces or steps is measured to about 4.2-5.5Å (*figure 4.2 (C)*) which is close to the theoretical value for the atomic layer-to-layer distance of InAs(111)B, which is 4.3Å [8]. The strong variation in height may be charges at steps influencing the apparent height or may be error during measurement.

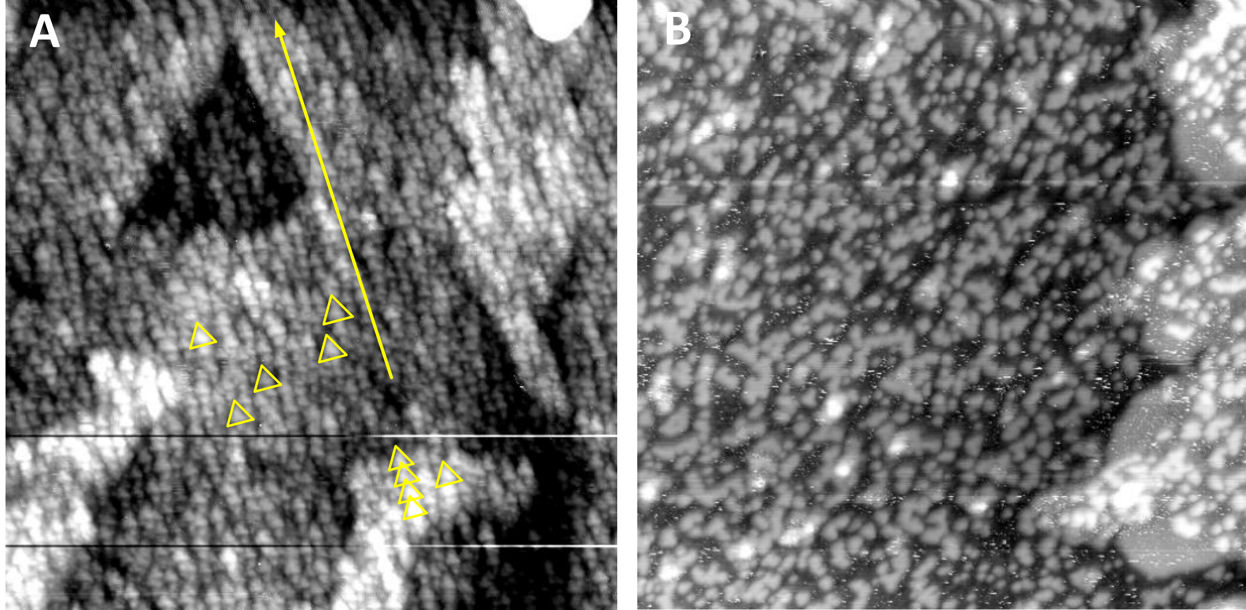



***Figure 4.3**: STM image of InAs(111)B, **(A)** (U=-1.8V, $I_{tunneling}$=80pA) 75×75nm² annealed up to 410˚C in atomic hydrogen. **(B)** (U=-2.6V,$I_{tunneling}$=80pA) 50×50nm² annealed up to 395˚C in atomic hydrogen for 30 minutes.*

*Figure 4.3 (A)* and *(B)* shows STM images for H-cleaned InAs(111)B surfaces which are smaller in size than *figure 4.2*. In the *figure 4.3 (A)*, an area of 75×75nm² is scanned with biased voltage of -1.8V and tunneling current of 80pA. The sample is cleaned for 55 minutes with annealing temperature of 380˚C-410˚C with heating current of $I_{heating}$=0.46A. In *figure 4.3 (B),* an 50×50nm² area is scanned after the surface was exposed to atomic hydrogen for 30 minutes along with an annealing temperature of 380-410˚C while the current for heating the sample was $I_{heating}$=0.45A. The parameters can be found in chapter 3.

In both the images of *figure 4.3* the surface looks free from oxides. *Figure 4.3 (A)* shows terraces and rows of small triangular shaped islands, as indicated by yellow triangles, having sizes of approximately 2nm while the height of each small island is around 5Å. The distance between each row is about 1-2nm and the direction of the rows is shown by the yellow arrow. *Figure 4.3 (B)* also shows another InAs(111)B sample having islands but not in rows.

The conclusion for these two STM Images is that we need atomic hydrogen for reducing the oxides on the surfaces. The home-built cracker used in this work has a cracker efficiency of about 5% compared to an efficiency of about 50% for commercial crackers. In order to reach the same

amount of atomic hydrogen with this home-built cracker, we need to increase the pressure of molecular $H_2$ by a factor of 10. This implies that we now have a large supply of $H_2$ at the surface during annealing. This $H_2$ is not cleaning the surface from oxide, but it might lead to a partial desorption of already cleaned InAs during annealing, leaving the observed small islands back on the surface.

### 4.1.2: InAs Nanowire surface studies

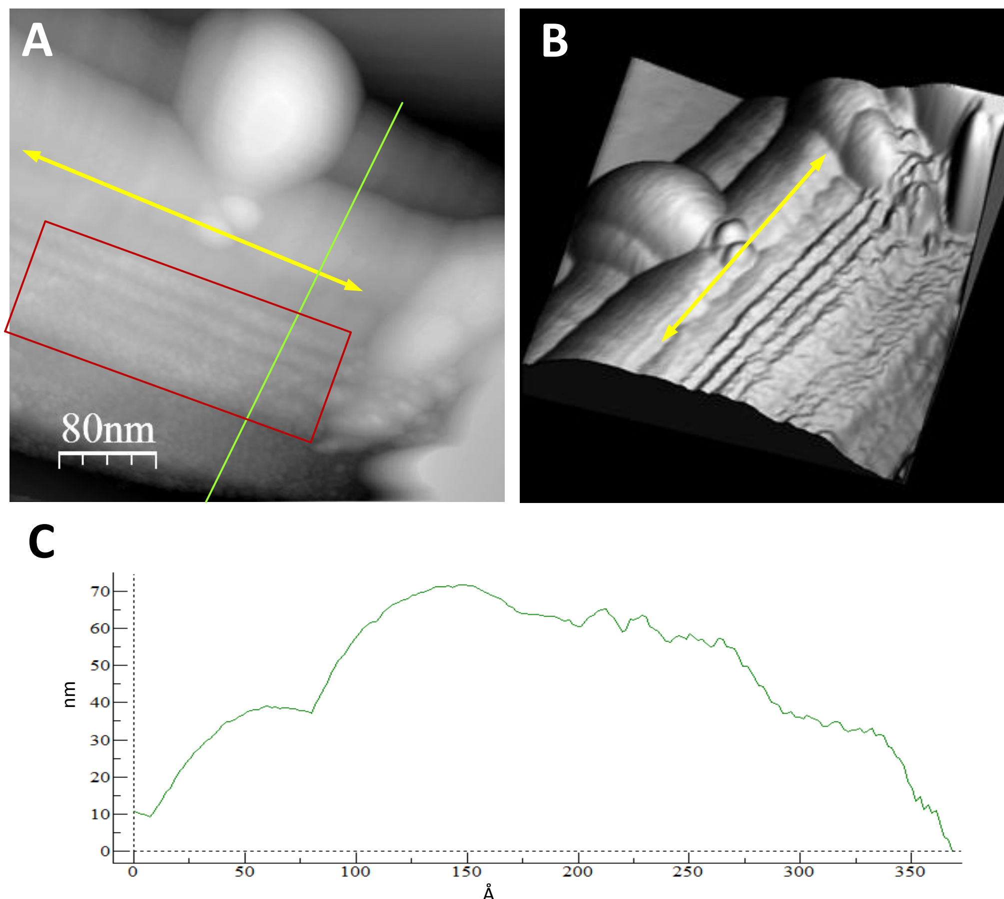



***Figure 4.4:*** ***(A)*** *A 400×400nm² STM image of the 50nm diameter wurtzite nanowire of InAs.* ***(B)*** *3D image of the nanowire.* ***(C)*** *the height profile for the NW.*

In *figure 4.4 (A)*, an STM image of a wurtzite nanowire with a diamter of *50 n*m is shown where the growth axis of the nanowire is marked by the yellow arrow. The green line marks the position of the height profile of the nanowire which is shown by *figure 4.4 (C)*. *Figure 4.4 (B)* shows the 3D image of the nanowire from the *figure 4.4 (A)*. The nanowire was cleaned under atomic hydrogen with an annealing temperature of 380-410°C for 35 minutes. In the image some large steps parallel to the nanowire growth direction can be seen, indicated by the red rectangle (*figure 4.4 (A)*). From the height profile which shows a height of almost 70nm it might be concluded that one NW is lying on top of another NW as the diameter of the NW is 50nm. And also double tip behaviour as can be seen at the lower part of the image below the red rectangle.

## 4.2: SPELEEM studies of NW device

In this part of the experiment we have studied a NW device while heating it up to *700˚C* using *Photo Emission Electron Microscopy* and *Low Energy Electron Microscopy (PEEM/LEEM)* at MAX-lab, Lund Sweden. The idea of performing this experiment is to find the temperature where the device undergoes structural changes that will stop the electrical performance. So for such an experiment we heated the device under UHV condition to high temperatures along with taking images for each temperature to see changes. In *figure 4.5*, the NW device used for the *PEEM/LEEM* studies is shown. The nanowire is lying horizontally on the surface of the substrate having external contacts indicated as in *figure 4.5(C)* by red arrow. The external contacts also have two defects from lithography especially near the nanowire, which are shown by yellow arrows in *figure 4.5 (C) & (D)*. These defects are the alloys of gold and nickel used for the contacts to the NW. Here in these devices nanowires consist of Indium Arsenide Antimonide (InAsSb) with 90% As and 10% Sb. The external contacts consist of a gold nickel (Au-Ni) alloy with 25 nm Ni at the bottom and 75 nm Au on top.

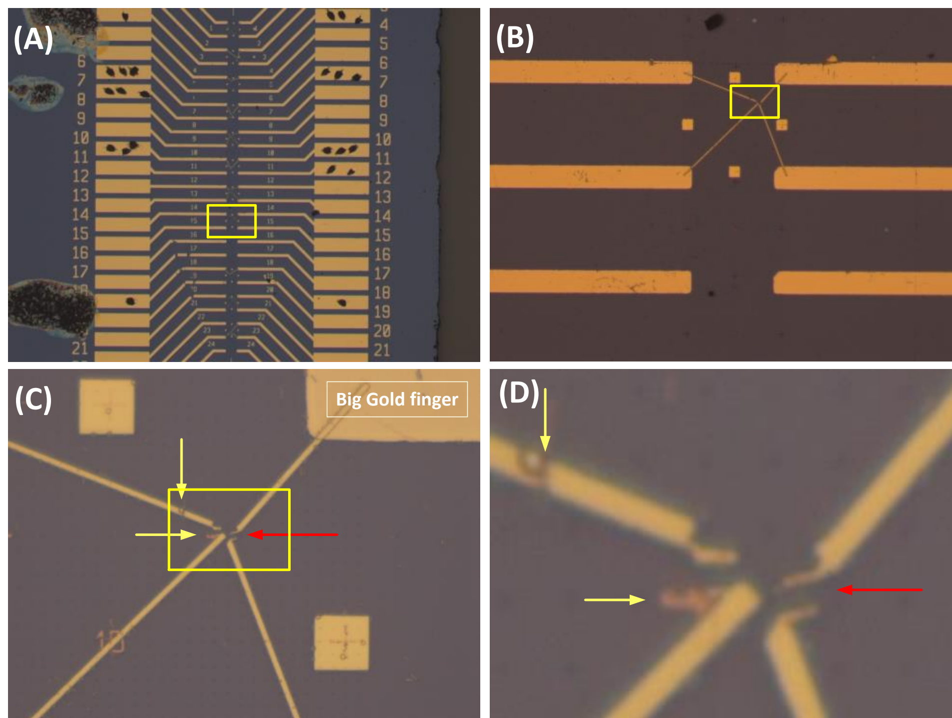



***Figure 4.5:*** *Optical microscope images for the NW devices used for the PEEM/LEEM studies.* ***(A)*** *An overview of the nanowire device sample.* ***(B)*** *Zoom in on the NW device 15 and its contacts of gold.* ***(C)*** *Further zoom-in on the NW device where defects from the manufacturing of the device are shown by yellow arrows, and a nanowire connected to gold contacts is shown by a red arrow. PES spectra are also obtained at the big gold finger.* ***(D)*** *The zoom-in of the device shown in yellow rectangle of figure (C).*

### 4.2.1: PEEM images during heating

In order to study the long-range surface features (like NWs, metallic contacts, the substrate etc.) of the device during heating in UHV, secondary electron X-ray photoelectron emission microscopy (SE XPEEM) was used. *Figure 4.6* shows SE XPEEM images when the temperature was ramped from room temperature to 700˚C. First a SE XPEEM image was taken at room temperature as a reference image (*figure 4.6 (A)*) and in the figure the defect in the rectangle appears bright

while the other defect does not. The defect in rectangle is clearly shown in SE XPEEM image of *figure 4.6 (A)* but not by optical image of *figure 4.5 (D).* After heating the device to 700˚C, the manufacturing defects in the rectangles shows structural changes as in *figure 4.6(B)*. No significant structural changes can be seen for the other contacts.

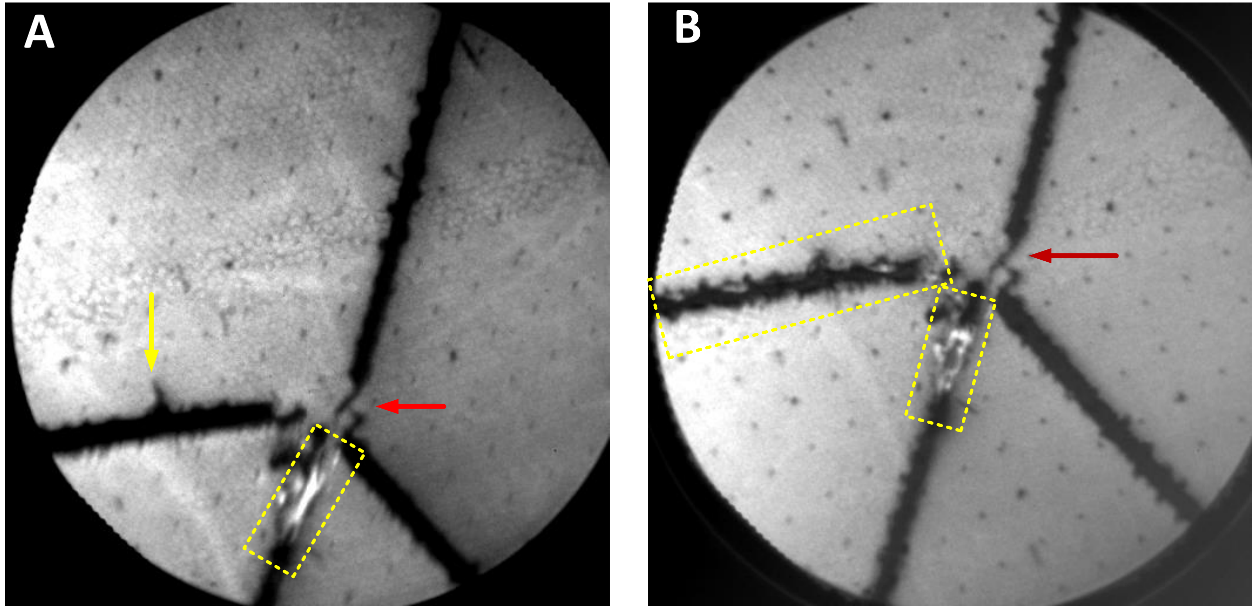



***Figure 4.6:*** *SE XPEEM images for the nanowire device heated to 700˚C.* ***(A)*** *SE XPEEM image (25µm) at room temperature before heating.* ***(B)*** *XPEEM image (25µm) when the NW device was heated to 700˚C, the images was taken immediately after heating.*

SE XPEEM images in *figure 4.7* show the NW device when the temperature was ramped from room temperature to 700˚C. At the temperatures of 310˚C, 362˚C, and 417˚C there are almost no changes in the appearance of the device *(figure 4.7B, C & D)*. But when the temperature has reached 460˚C there is a clear change especially at the defect at the metallic contact (yellow arrow) which is brighter than the rest of the contact *(figure 4.7E)*. Also the size of the defect is becoming smaller, which means that there is a structural change in the defective contact and it has separated from the contact, shown by the blue arrow. The contact is broken apart at the manufacturer defect and interrupted now at the position of the defect, which means that this device (with the defective contact) is not working anymore. We can also see the nanowire connected to contacts, as is shown by red arrow, which still appears structurally unchanged. At 490˚C the defect even more decreased in size *(figure 4.7F)*, and when the temperature is ramped to 525˚C the defect again starts increasing in size *(figure 4.7G)*. The defect is increasing further in size with the increase in temperature *(figure 4.7H, I & J)*. At 700˚C temperature the defect area with the bright appearance has reached its largest extension, shown by yellow and blue arrows *(figure 4.7K)*. The other contact which had a defect from the beginning (yellow arrow in *figure 4.6A*) is no more homogeneous but has some brighter areas, as shown by blue rectangle in *figure 4.7K*. The structural changes of the defects can cause electrical failure to the device because homogeneous defect free contacts are essential for keeping a working device even upon significant heating. There are no significant changes that can be seen at the NW itself and the good contacts even after heating to 700˚C. Also the

$SiO_2$ layer has become thinner, which can be seen by the clearer appearance of the regular dark spots underneath the $SiO_2$ (*figure 4.7 K*).

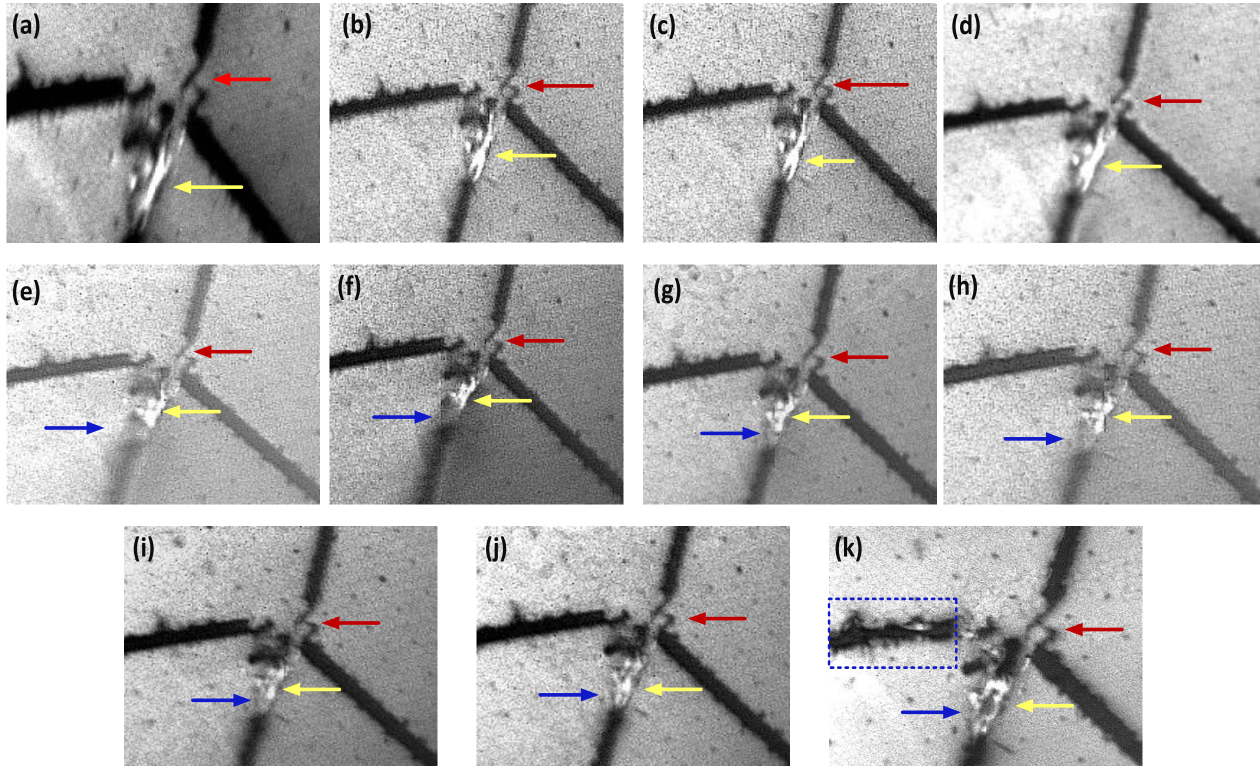



***Figure 4.7:*** *XPEEM secondary electron ($E_{photon}$=140eV) images for a NW device with Ni-Au contacts. A defect in one of the Ni-Au contacts due to the manufacturing process is shown by the yellow arrow while the NW is shown by the red arrow. The images have been taken at different temperatures ramped from room temperature up to 700˚C. The heating time is almost 2 minutes for each temperature.* ***(a)*** *NW device at room temperature and used as a reference image (Field of View, FOV=25μm).* ***(b), (c) & (d)*** *show images when the device is heated till 310˚C, 362˚C and 417˚C, respectively, with FOV=50μm which show almost no changes in the device.* ***(e) & (f)*** *At the temperature of 460˚C(e) and 490˚C(f) respectively, a gap has opened between the bright shining defect and the metallic contact as indicated by blue arrow. The Start Voltage is SV=0V for images (a) to (f).* ***(g)*** *to* ***(j)*** *show images with SV=0.89V for temperature=525˚C(g), SV=0.9V at temperature=555˚C(h), SV=2V at temperature=585˚C(i) and SV=3.1V(j) at temperature=620˚C, which has the same appearance as image (f).* ***(k)*** *At the final temperature of 700˚C the NW is still there, but the Au-Ni contact shows strong changes. The brighter part, which is the defect (yellow arrow, is now connected to the metallic contact so increased in size. Also the $SiO_2$ layer has become thinner, which can be seen by the clearer appearance of the regular dark spots underneath the $SiO_2$.*

We decrease the field of view (FOV) to 15 μm to further zoom in to the device using SE contrast of the XPEEM and the image is shown in the *figure 4.8*. The contacts having defects from the manufacturing process are less homogeneous than the contacts without defects.

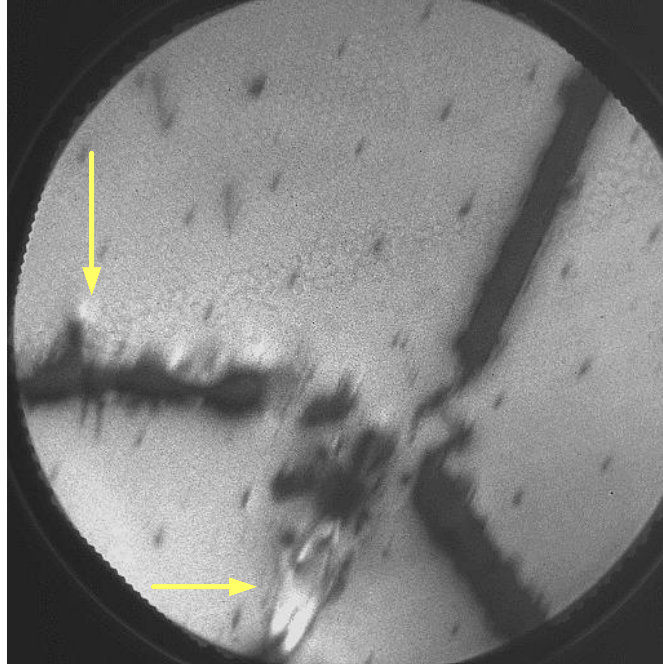


***Figure 4.8:*** *Secondary electron image when the device was heated to 700˚C and the changes at the Au-Ni contact can clearly be seen.* $E_{photon}$*=140eV, Starting Voltage, SV=0.32V and field of view, FOV= 15µm.*

After heating, core level XPEEM images of the NW device were obtained to check for the individual elements. The metallic contact consists of two layers, one layer of nickel (Ni) which forms the lower 25% of the contact and one of gold (Au) which forms the upper 75% of the contact. Nickel is used for homogeneous ohmic contact with semiconductor nanowire while gold is used as a protective layer. The substrate consists of silicon (Si). So core level electron XPEEM is used to identify the distribution of these elements. In addition, XPEEM was done at the valence band close to the Fermi edge, shown in figure *4.9(A)*. From the image it is proven that there are still metallic elements, but the contrast cannot distinguish between gold and nickel. Here one can see that also at the defects some metal is left, but there are smaller or larger gaps in the metal contact, interrupting the electrical circuit, as shown by yellow arrows. If one tunes the starting voltage to slightly higher values, one reaches an area within the valence band which is dominated by gold electrons. From the corresponding image (*figure 4.9 B*) and from the Au4f XPEEM images (*figure 4.9 C, D*) it is shown that the metal signal arises from gold, which thus is still at the top of the contact, while no specific nickel (Ni) signal could be found. Accordingly, we can exclude significant nickel diffusion but can conclude that the metal alloy of the contacts is still intact, at least on a larger scale. Also from the inverse contrast in *(D)*, there are some gaps (at the defects) and inhomogeneities in the contacts, even the 'good' one. The core level XPEEM images for Si2p show, however, that the contacts are partly contaminated by silicon, especially at the positions of the defects and no Si can be seen in good contacts and even at the NW position, and also something is covering the Si *(figure 4.9 E & F)*.

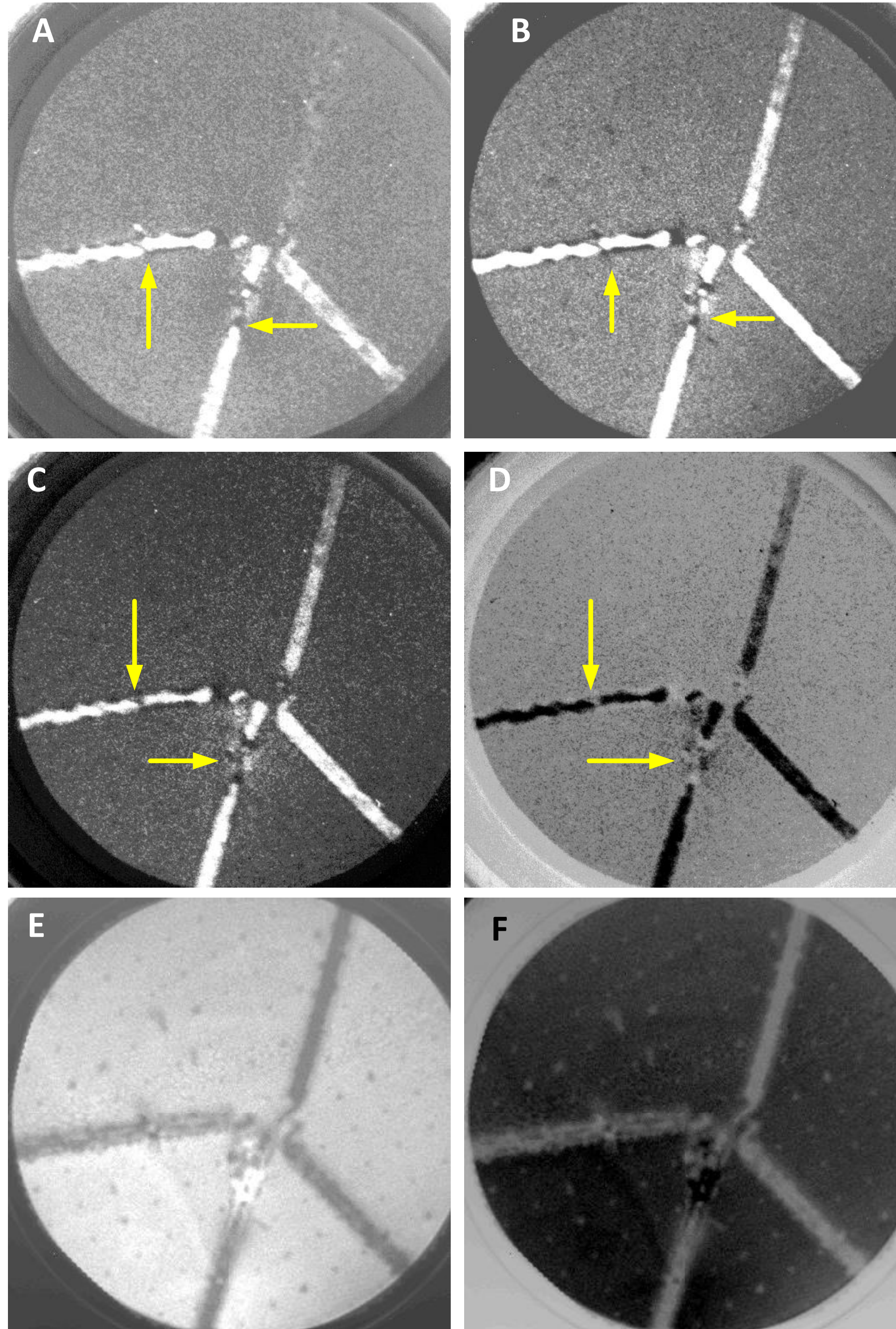



***Figure 4.9:*** *XPEEM images (Core-level electron contrast) for individual elements.* ***(A)*** *Valence band image (close to the Fermi edge) of the metal contact and the NW device.* $E_{photon}$*=70eV, Starting Voltage SV=64.5V and field of view, FOV= 25μm.* ***(B)*** *Valence band image at slightly higher energy, being sensitive to gold,* $E_{photon}$*=70eV, Starting Voltage SV=61.5 V and field of view, FOV= 25μm.* ***(C)*** *Gold 4f image with* $E_{photon}$*=200eV, Starting Voltage, SV=111.5 V and field of view, FOV= 25μm.* ***(D)*** *shows the invert image of image (C), from the image it is clear that we only have gold as protective layer on the contact.* ***(E)*** *Silicon-2p image,* $E_{photon}$*=140eV, Starting Voltage, SV=31.1V and field of view, FOV= 25μm.* ***(F)*** *The invert image of (E).*

In order to find the correct starting voltages for XPEEM images, micro-PhotoElectron Spectroscopy (μ-PES) was performed at the position of the big gold finger shown in *figure 4.5(C)*.

Since we have exposed the device till 700˚C, the PES spectra are also well suited to check whether all elements are still present and to investigate the chemical composition of the components. *Figure 4.10 (A)* shows a typical Au4f spectrum without additional peaks and shoulders. The difference between the two peaks due to the spin-orbit splitting is 3.7eV. *Figure 4.10 (B),* which is the PES Si2p spectrum shows that this is a strong Si peak, but the Selected Area Aperture (SAA) is larger than the Au finger so Si from the substrate can also be seen. *Figure 4.10C* is the valence band PES spectrum for the big gold finger and shows the correlating peaks to Au or Au-Ni. We don't show any Ni spectrum because Ni is covered by Au so we have no strong Ni signal, and also no In or As spectrum because the size of NW is very small compared with the SAA, so the As and In signals are too small.

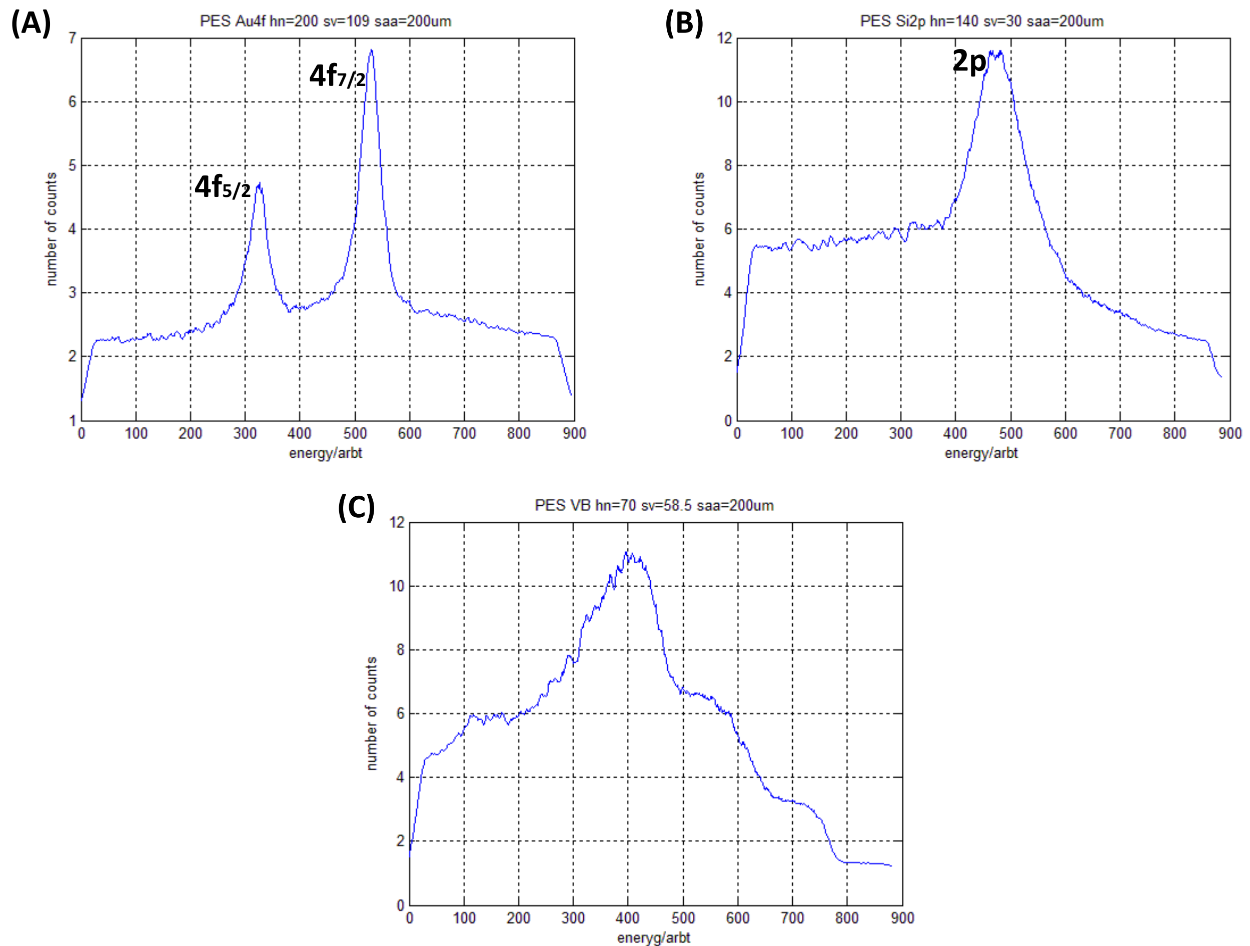



***Figure 4.10:*** *Photo Electron Spectra (PES) after heating to 700˚C, the selected area aperture is SAA=200μm.* ***(A)*** *PES for Au4f with hv=200eV, SV=109V.* ***(B)*** *PES for Si2p with hv=140eV and SV=30V.* ***(C)*** *PES for Valence Band (VB) with hv=70eV and SV=58.5V.*

For analyzing topography variations for the surface of the device, Low Energy Electron Microscopy (LEEM) and Mirror Electron Microscopy (MEM) were done. The difference between LEEM and MEM is that in LEEM there is interaction of LEEM electrons and surface atoms the contrast is dominated by work function differences, while for MEM low-energy electrons don't react with surface atoms, but get mirrored by electron density, so the contrast is mainly topography.

*Figures 4.11 (A) & (B)*, which are MEM images show the metallic contacts bright with darker edges, and also the NW with its contacts can be seen (red arrows). There are some nanowires without contacts, shown by the yellow arrows. The defects from the manufacturing process (black arrows) appear brighter than the metallic contacts. In the LEEM image *(figure 4.11 C)* the metallic contacts are bright and the NWs cannot be seen. The inhomogeneities in metallic contacts are also shown as well as the defective areas of the contact are shown by the dotted yellow box and black arrows.

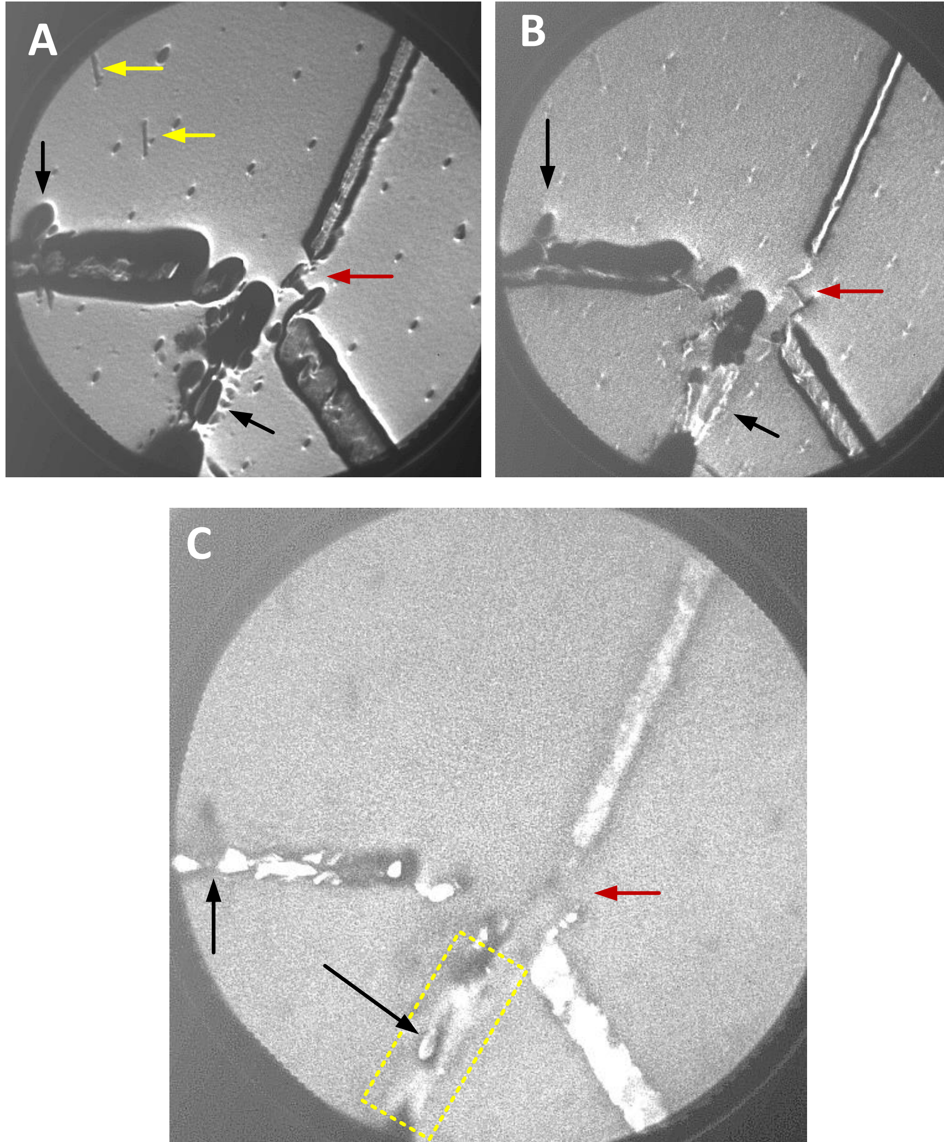



***Figure 4.11:*** *Low Energy Electron Microscopy (LEEM) and Mirror Electron Microscopy (MEM) images for the NW device heated up to 700°C with field of view, FOV=15µm.* ***(A)*** *MEM image for the NW device with SV=0.44V and objective lens current=1548.5mA. Yellow arrows show NWs without any contact, red arrow shows contacted NW device, while the black arrows show the defects from the manufacturing process.* ***(B)*** *MEM image for the NW device with SV=0.11V and objective lens current=1543.6mA.* ***(C)*** *LEEM image for the NW device with SV=1.77V and objective lens current=1548.7mA. The full extension of the defective area in one of the contacts is indicated by the dotted yellow rectangle.*

The conclusion for the LEEM and MEM studies is that the MEM shows that NWs and also thin contacts are still there; also non-contacted wires (yellow arrows, *figure 4.11A*) look still good, while in LEEM the contacts became inhomogeneous in work function.

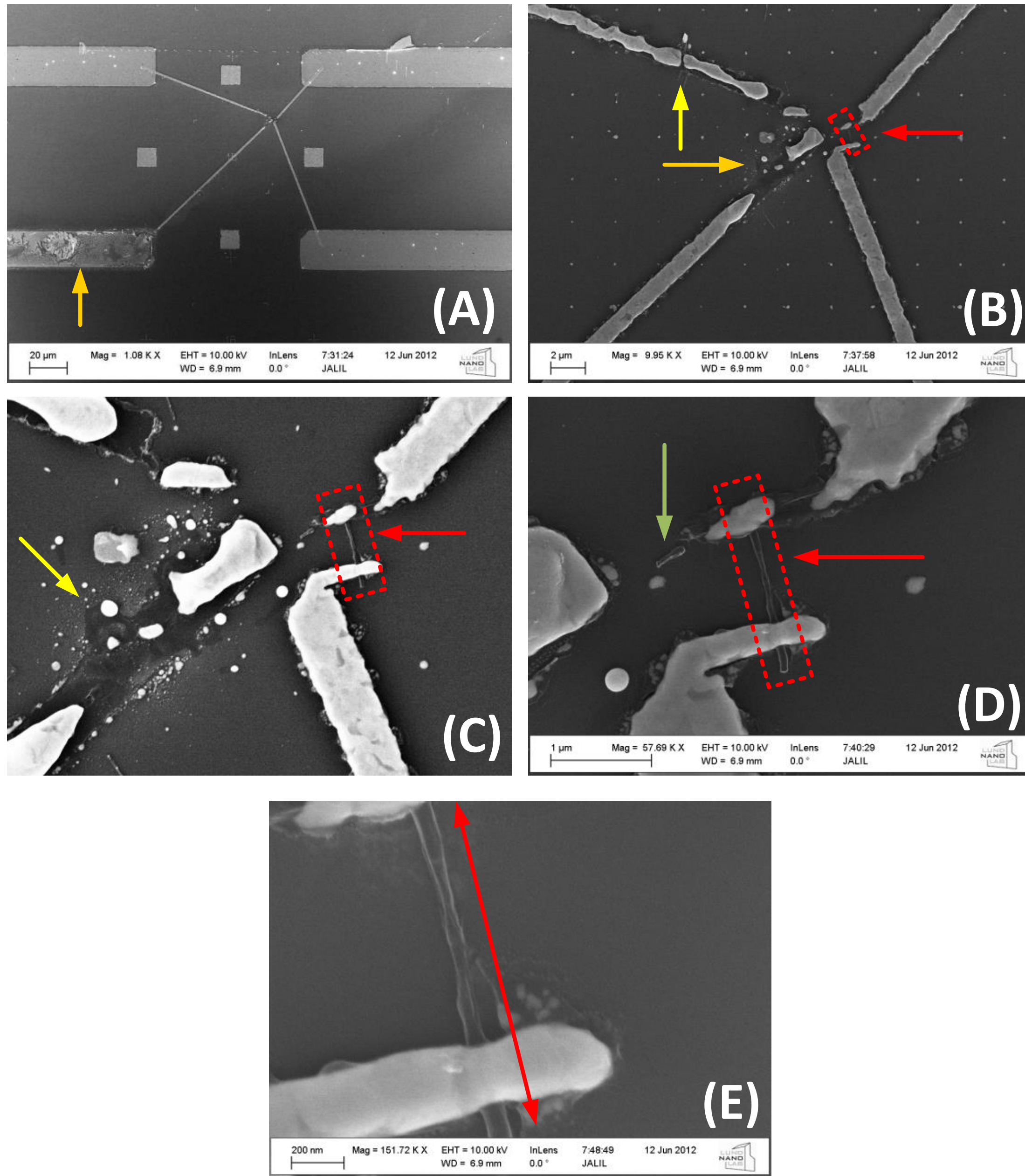



***Figure 4.12:*** *Scanning Electron Microscopy (SEM) images for the NW device heated to 700˚C in UHV condition.* ***(A)*** *shows the NW device with metallic contacts (big and small gold fingers). The bottom big gold finger shown by the yellow arrow is more damaged compared to others.* ***(B)*** *The damaged NW device where the contacts are broken is indicated by the yellow arrows.* ***(C)*** *The red arrow shows the position of the more intact NW. The defective metallic contacts are molten and spread throughout the area.* ***(D)*** *shows the place where the NW had been, by red arrow, but not the original NW anymore and its contacts, one of which is broken. The green arrow shows a feature which may be a broken part of the nanowire.* ***(E)*** *shows the place of the original NW.*

High resolution Scanning Electron Microscopy (SEM) topography was done for the NW device which shows more information about the changes of the devices after heating. It is shown that the metallic contacts which have defects from the manufacturing process are severely damaged by the heat (700˚C), much more than the initially defect-free contacts, so there is a strong change. Also one can see the traces of the original NW which might be group III In element because group V element As preferentially evaporates, so the NW is not homogeneous anymore.

Now the over-all summary of this section is that at higher temperature like 700˚C both the device contacts and the nanowire itself are damaged. At lower temperatures like 460˚C, the areas having defects from the manufacturing show changes but the protecting gold layer is still in good condition. The PEEM images still show the NW, which is also shown by the LEEM and MEM images. After 700˚C one can see strong changes in the contacts and these changes become more obvious by the SEM images. Also the NW is not homogeneous anymore and the $SiO_2$ layer has become thinner.

From the SE XPEEM technique, it is proven that the defects from the manufacturing process break at 460˚C which degrades the device quality. There are no significant changes in the NW itself and at the good contacts even at this temperature. Besides, the $SiO_2$ layer has become thinner at high temperature.

From the core level electron XPEEM technique, it is proven that not only defective metallic contacts but also the good ones are no more homogeneous and broken apart. Also the contacts are party contaminated by Si, especially at the positions of defective contacts, while no Si contamination can be seen at the NW positions.

From MEM, the NWs and the contacts are still there while from the LEEM it is shown that contacts are no more homogeneous.

High resolution SEM topography technique shows more information: the defective metallic contacts are severely damaged by high temperature, more than defect-free contacts. Also, there are only traces of the original NW, which might be indium.

So there are no chances for the NW devices to survive heating up to 700˚C but no significant changes at the moderate heating if the initial contacts have high quality.

## 4.3 *I-V* properties of nanowire devices

In this chapter the *I-V* data for nanowire devices are analyzed. The UHV condition is one of the essential parts for studying surfaces at the atomic level. In our case we used the treat chamber of the *JEOL STM*, described in chapter 3 (section 3.4.2), for electrical characterization. We have measured the conductance of the cleaned nanowire devices which changes as a function of temperature. We also compare the conductance of the cleaned nanowire devices with those of nanowire devices having an oxide layer. In the ideal case, cleaned nanowire devices have no native oxides left on their surfaces. These native oxides can be removed by exposing the surface of the nanowire to atomic hydrogen under annealing. Oxides on the surface of the nanowires can affect the conductance of the nanowire because these oxides can create states on the nanowire surface. These surface states can affect the band bending, an effect called Fermi level pinning.

The nanowire device sample is connected to electrical contacts on the STM sample holder by micrometer aluminum wires using a bonding machine, as shown in *figure 3.3* of *Chapter 3*. Two different nanowire device samples were studied, named *JWP11A* and *TP5-594b*, allowing to compare results for different nanowire materials.

### 4.3.1 Electrical characterization on n-doped InP NW device

We have first used an InP NW device sample-*JWP11A* for electrical characterization. *JWP11A* has low n-doped indium phosphide (InP) homogeneous nanowires while for the metallic contacts, gold (Au) and nickel (Ni) are used. The investigated device number is 24 in an array containing about 10 or 12 NW devices. The device was manufactured by *Jesper Wallentin* in the *Division of Solid State Physics, Department of Physics, Lund University*. First the integrity of the device is checked in air. After that, the device is transferred into the treat chamber of the *JEOL STM* for investigating the *I-V* characteristics.

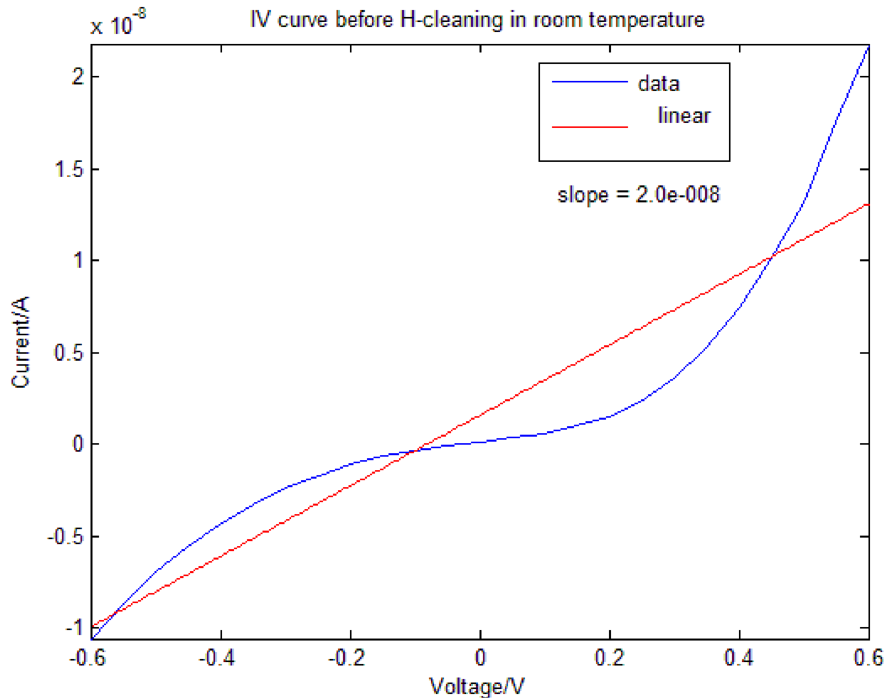



***Figure 4.13:*** *I-V curve for the NW device in UHV before H-cleaning. The slope of the curve which is the conductance of the device is $2.0\times10^{-8}$S.*

*Figure 4.13* shows the *I-V* curve of the nanowire device in UHV condition before any H-cleaning. The average slope of the *I-V* curve over the voltage interval from -0.6V to +0.6V, which defined as the conductance of the NW device is 20nA/V (nS). The sample had been investigated some months before under ambient conditions at the *Division of Solid State Physics*, where a current of 10 µA was obtained at a bias voltage of several volts. Our value is not in the same range, but showing that despite of a long storage time, the device is still alive and can be used for electrical characterization. Ideally the shape of the curve should be linear having Ohmic contacts but in *figure 4.13*, the shape of the curve is non-linear. This shows that the two metallic contacts at two sides of the NW which are defined by lithography have non-ohmic/Schottky contacts. Therefore the shape of the curve is non-linear and also asymmetric.

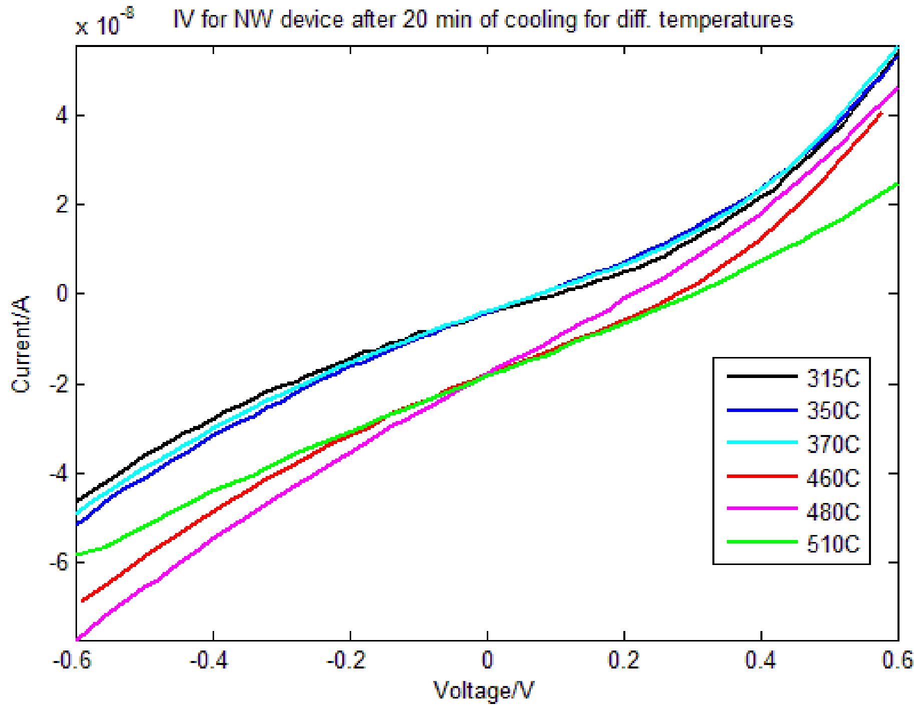



***Figure 4.14:*** *I-V curves for the NW device heated at different temperatures and then cooled down for 20 minutes prior to I-V measurement.*

*Figure 4.14* shows *I-V* curves of the device for different annealing temperatures. For each curve, the sample was cooled down for 20 minutes in UHV after the annealing before the *I-V* measurement. *Table 4.1* below shows the conductance for each *I-V* curve.

| Serial No. | Annealing Temperature [˚C] | Conductance [nA/V] |
|---|---|---|
| **1** | 25 (room temperature) | 20 |
| **2** | 315 | 86 |
| **3** | 350 | 90 |
| **4** | 370 | 90 |
| **5** | 460 | 125 |
| **6** | 480 | 165 |
| **7** | 510 | 82 |

***Table 4.1:*** *Measured conductances for different annealing temperatures.*

From the *figures 4.13, 4.14* and *table 4.1*, one can see that the conductance of the device after heating it up to 370˚C is higher than before any annealing, but not changing for annealing temperatures between 315˚C and 370˚C. Importantly, the shape of the *I-V* curve is still more or less the same as before any heating. After annealing the sample at 460˚C to 510˚C, the *I-V* curve becomes more and more linear but the average conductance decreases slightly. There are two reasons; the change in *I-V* shape means the changes at the NW contacts are minor for temperatures lower than 400˚C, and start increasing for temperatures between 400˚C and 460˚C, and change strongly for temperature of 460˚C and above. The second reason might be as in our case the InP NW is doped. Therefore when the temperature starts increasing the dopants start moving leaving their atoms. At

higher temperature, even the surface atoms start moving around which can cause the nanowire to melt and the result is shown in figure 4.18 C and D [16]. This can cause this conductance to decrease as for 510˚C.

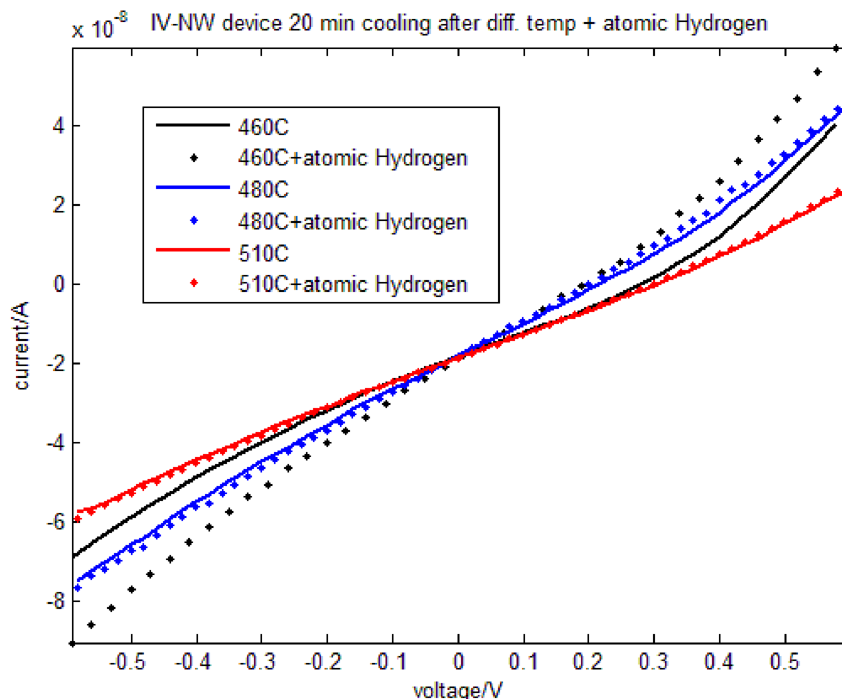
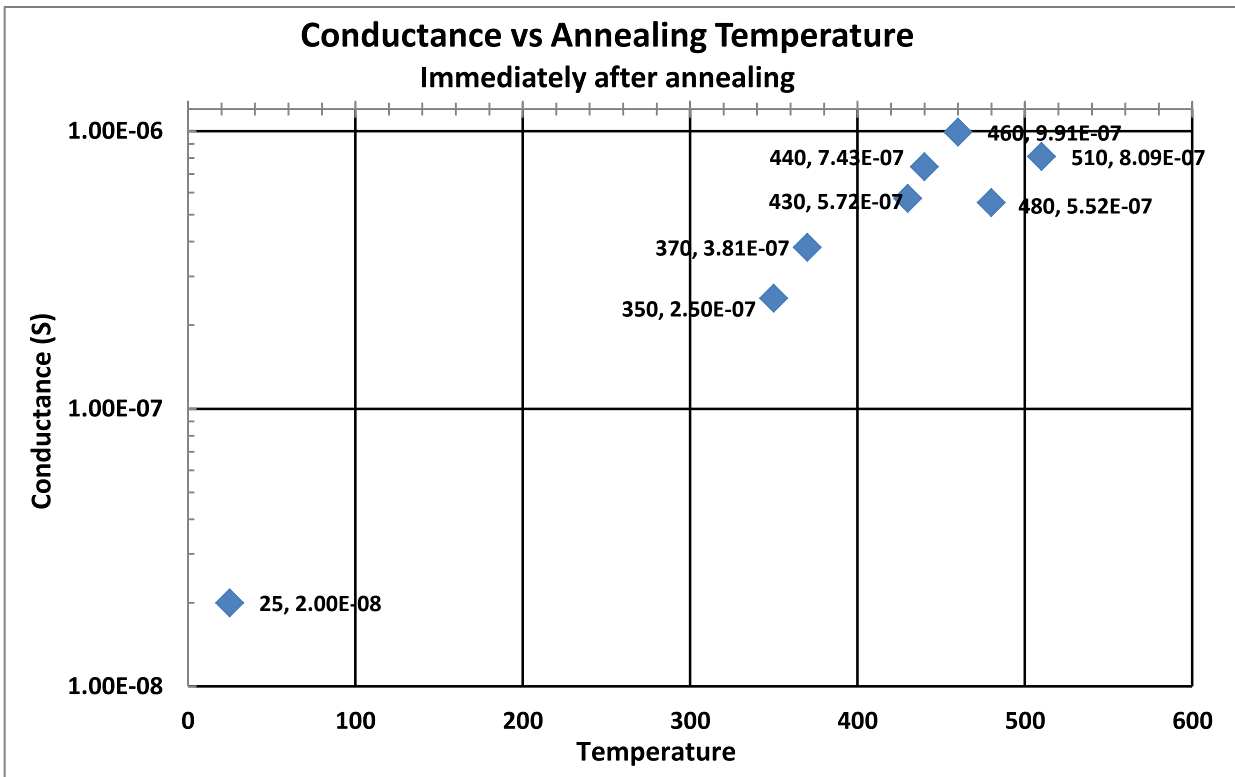



***Figure 4.15:*** *I-V curves for the NW device measured after annealing and cooling down for 20 minutes. The smooth lines show results from annealing in UHV, while the dotted lines show the results for annealing under atomic hydrogen background.*

*Figure 4.15* compares *I-V* curves of the device when it was annealed in UHV or under an atmosphere of atomic hydrogen. There is little or no change after annealing either under vacuum or with atomic hydrogen background, especially for higher temperatures. This shows that the presence of atomic hydrogen has very little influence on the shape of the *I-V* curve and the average conductance, in contrast to the annealing temperature which causes strong changes. Annealing alone does not clean the nanowires from their native oxides (at these temperatures); this is only reached together with atomic hydrogen. So we can conclude that the changes in *I-V* properties seen for our device are not coming from the presence or absence of the native oxide; in other words, cleaning the nanowires from its oxides has only minor influence here. Instead, the observed changes must come from changes regarding inner structure of the nanowire, or-more probably-from changes of the electrical contacts induced by annealing.



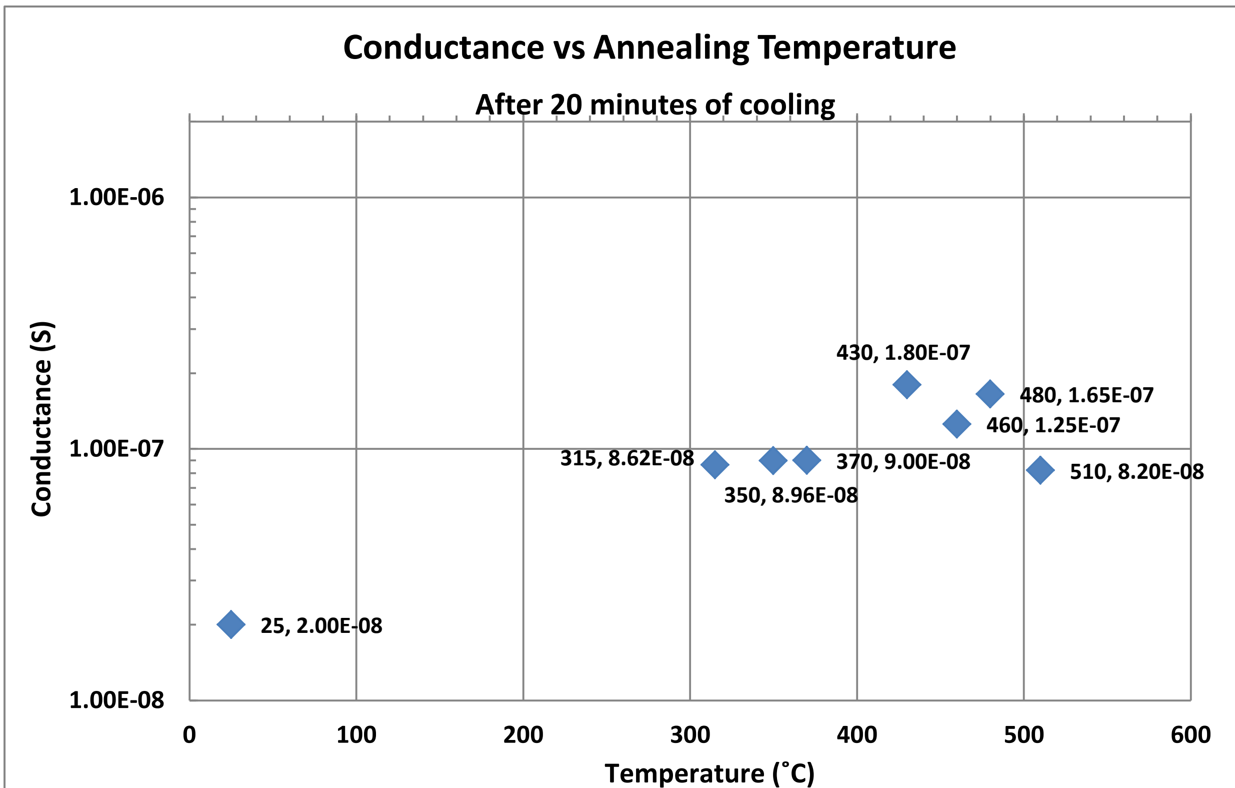




***Figure 4.16:*** *Conductance vs annealing temperature, conductance in logarithmic scale.* ***(A)*** *Conductance immediately after heating at various temperatures.* ***(B)*** *Conductivities after 20 minutes of cooling after heating at various temperatures.*

The average conductance of the NW device after annealing in UHV at different temperatures is summarized in *figure 4.16*. *Figure 4.16 (A)* shows the conductance immediately after annealing at various temperatures, while *figure 4.16 (B)*, the conductance after 20 minutes of cooling from different annealing temperatures. In both cases, the measured conductance generally increases with increasing annealing temperature, while the conductances measured directly after annealing are significantly higher than the conductances after some time of cooling.

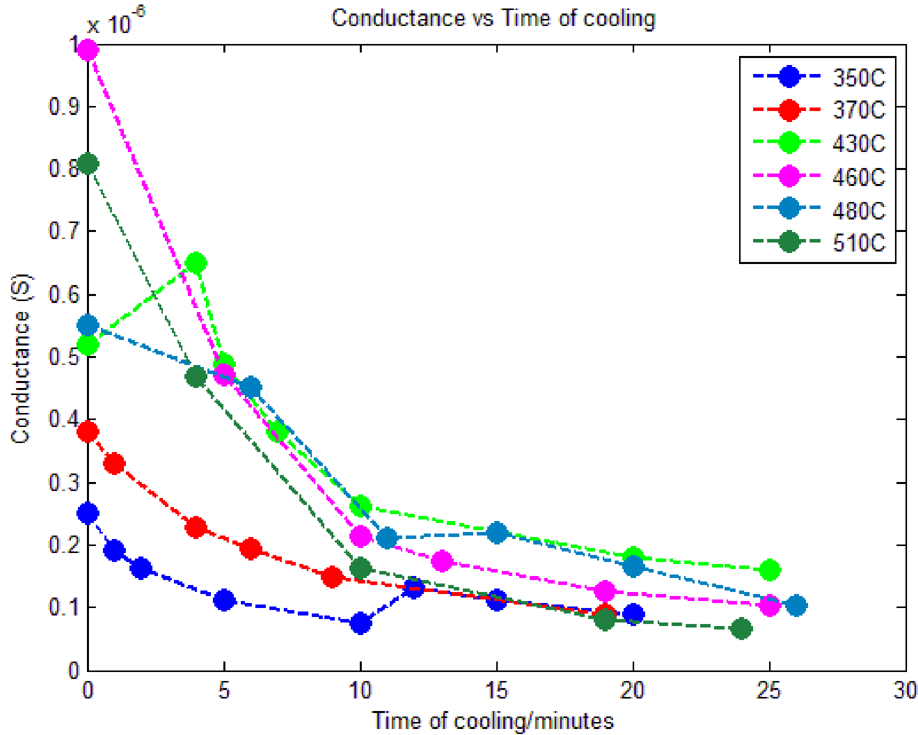



***Figure 4.17:*** *Average conductance of the NW device after different times of cooling from different annealing temperatures.*

*Figure 4.17* shows again the averaged conductance of the NW devices, obtained from the *I-V* curves, for different annealing temperatures. Here, *I-V* curves have been measured while the sample was cooling down, showing the decrease of device conductance over cooling time. The device conductance is decreasing more or less exponentially over the first 20 minutes and then saturating. In addition, the conductance generally increases with annealing temperature. This means that the measured conductance directly follows the temperature of the device. Such strong temperature dependence could be expected from the semiconductor nanowire materials. Also the existence of Schottky barriers at the metal-semiconductor interface of the contacts could explain the observed temperature dependence. This means that when the device is hot the conductance is high and when the device is becoming cold with time the conductance of the device is decreasing and a time will come when the conductance stay the same.

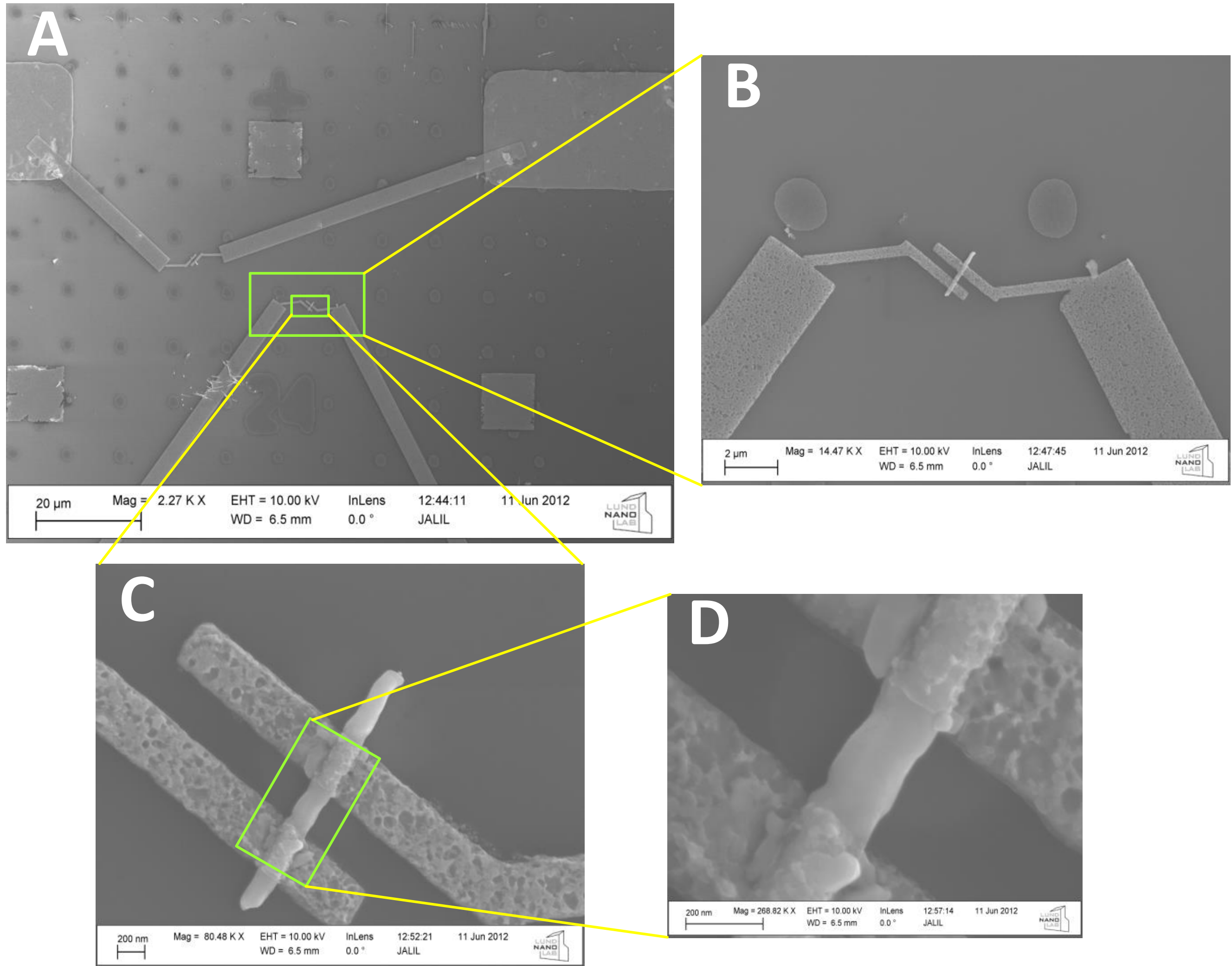



***Figure 4.18:*** *Shows SEM images for the NW device-24 heated to 510˚C.* ***(A)*** *An overview of the device,* ***(B), (C)*** *and* ***(D)*** *the device with the nanowire connected by metal contacts.*

*Figure 4.18*, shows SEM images for the NW device after heating it up to 510˚C. At a larger scale, the metallic contact still appear homogeneous, shown by *figure 4.18(A)*, but by zooming in, as shown in *figure 4.18 (B)*, *(C)* and *(D)*, it gets clear that the metallic contacts have cavities. The nanowire in *figure (C)* and *(D)* does not look nice anymore, but curved, as if it was molten.

To check the over-all effect to the metallic contacts because of heating optical microscopy is done and the images are shown in *figure 4.19* below. In this microscopy device number 13 is used which was the first device used for electrical characterization. But the *I-V* curves were not like for a real device which might be because of some personnel error in the connections. And the data for this device are not shown in this thesis.

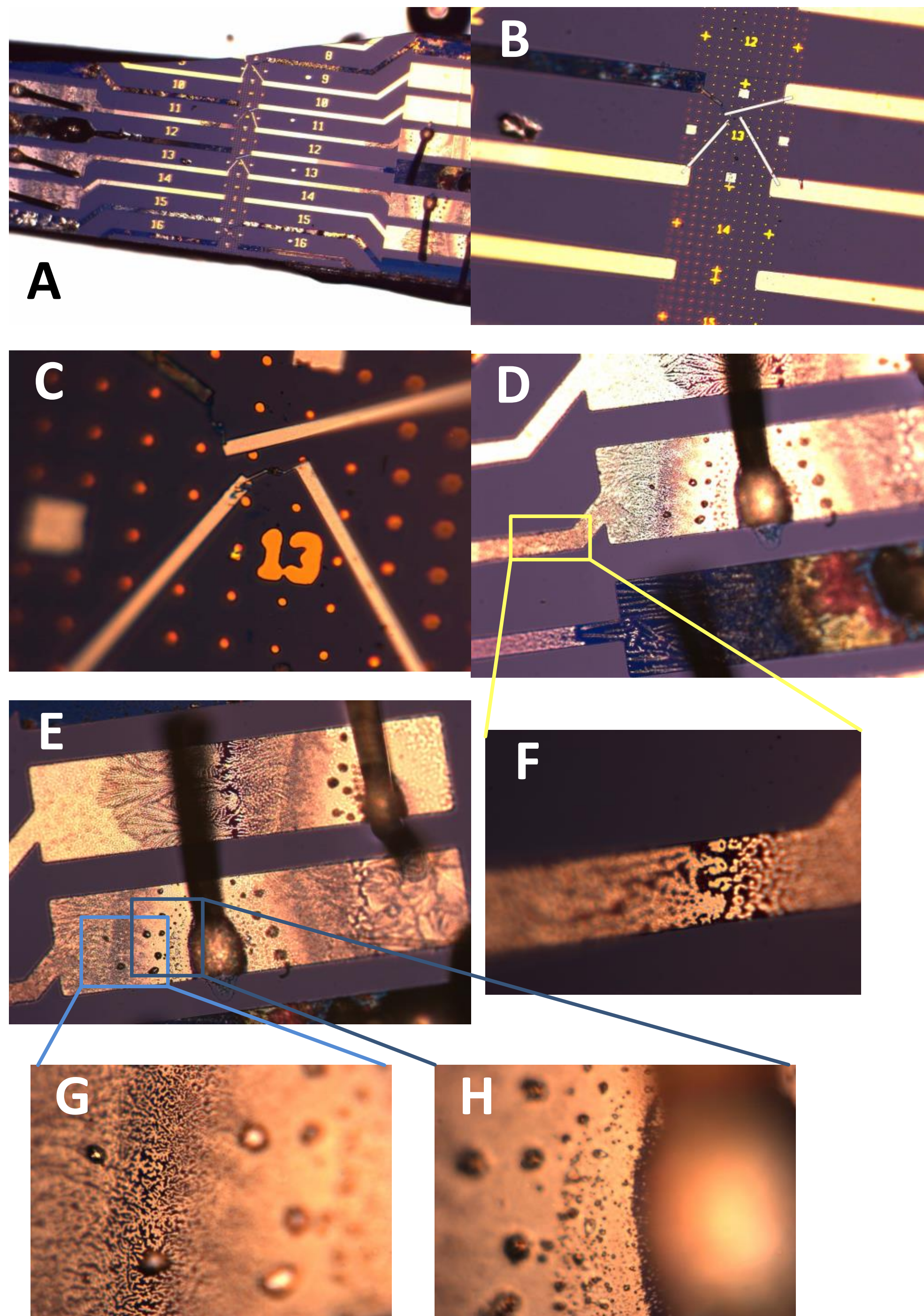



***Figure 4.19:*** *Optical microscopy images for NW device-13 heated up to 580˚C.* ***(A)*** *An overview of the device.* ***(B)*** *&* ***(C)*** *the NW area with Au contacts connecting NW.* ***(D), (E)*** *Show the big gold pads on to which aluminum wire is bonded.* ***(F), (G)*** *and* ***(H)*** *show the intermetallic compound of gold-aluminum formed after heating the device.*

When aluminum is bonded on gold pads and the device is heated at higher temperatures, then intermetallic compounds of gold-aluminum can form [17]. These intermetallic compounds of Au-Al are of different type and stoichiometry. Due to their pronounced appearance and unwanted occurrence, two common compounds have been called white plague ($Au_5Al$) or purple plague

($AuAl_2$). These intermetallic compounds occur at the contacts between two metals and have different properties than individual metals, i.e. gold and aluminum. Other gold-aluminum intermetallic compounds can also be formed. These intermetallic compounds are typically bad conductors of electricity and can cause mechanical interruption, as it has occurred for the contact shown in *figure 4.19 (F)*. When the temperature at the metallic junction starts increasing then inter-diffusion process takes place. This leads to formation of layers of intermetallic compounds having different compositions which can be from gold-rich to aluminum-rich, with different growth rates. Layers which are faster-growing and denser ingest a slower-growing layer which leads to the formation of cavities. Examples for these are shown in *figure 4.19 (G)* [17].

## 4.3.2 Electrical characterization on InAs NW device

We have used another NW device sample TP5 594b for electrical characterization. TP5 594b has un-doped Indium Arsenide (InAs) zincblende (ZB) twin-plane super-lattice NW grown by MOVCD. For the metallic contacts gold (Au) and nickel (Ni) are used, with 25nm thick Ni bottom layer and 75nm thick Au top layer. The investigated NW device is 5b in an array of 10 or 12 NW devices. The device was manufactured by Claes Thalender in *Division of Solid State Physics*, *Department of Physics, Lund University.*

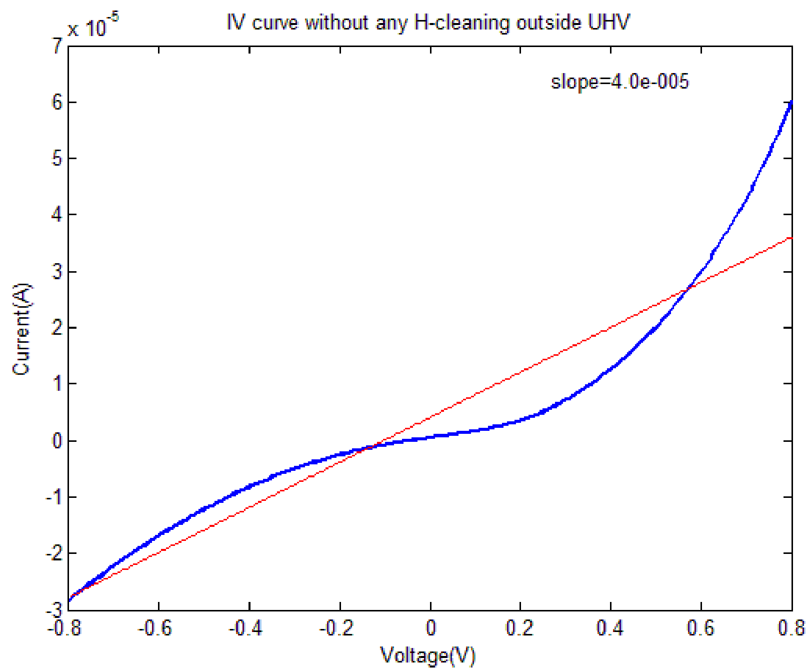



***Figure 4.20:*** *I-V curve for a NW device of sample TP5 594b before any H-cleaning and outside UHV. The red line is the linear curve while blue line is the I-V curve.*

The first electrical characterization was done outside the UHV (*figure 4.20*) to confirm whether the device is suitable for the electrical characterization inside UHV conditions. The average conductance from a linear fit of the curve, which is the slope of the IV curve $4.0\times10^{-5}$A/V, is within in the range of pre-characterization results performed in the division of *Solid State Physics* directly after processing the device. Also the shape of the *I-V* curve is asymmetric and non-linear because of

the two Schottky contacts at both sides of the NW. So the device is suitable for the electrical characterization inside UHV condition upon H-cleaning with different temperatures.

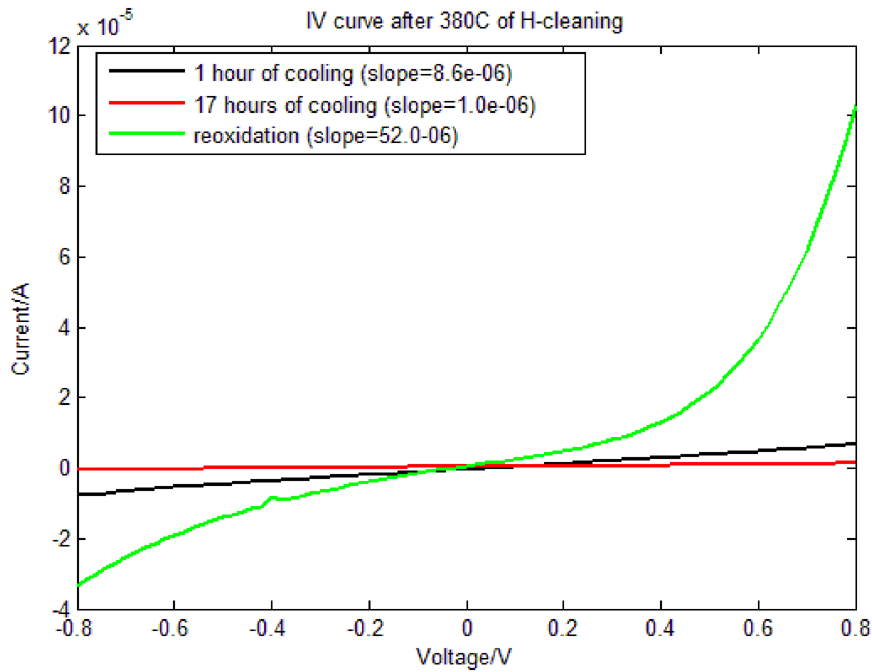



***Figure 4.21:*** *IV curve of the device after H-cleaning inside UHV at a temperature of 380˚C and after oxidation.*

After annealing to 380˚C under the presence of atomic hydrogen, the shape of the *I-V* curve has strongly changed towards the linear behavior. The average conductance has decreased by about one order of magnitude and further decreases while the sample is cooling down, as shown in *figure 4.21*. After cooling down, the sample was transferred into the load-lock of the STM setup and exposed to air for 10 minutes to 1 hour. After this, the *I-V* behavior is strongly changed again, coming very close to the initial device behavior prior to any H-cleaning. Also the shape of the curve is non-linear is similar to the shape before any H-cleaning (*figure 4.20*).

So the interpretation is that there is strong change upon cleaning. Besides with lower conductance might be the contacts become worse. After re-oxidation, the *I-V* curve is backed to original *I-V* curve and the contacts may be re-established.

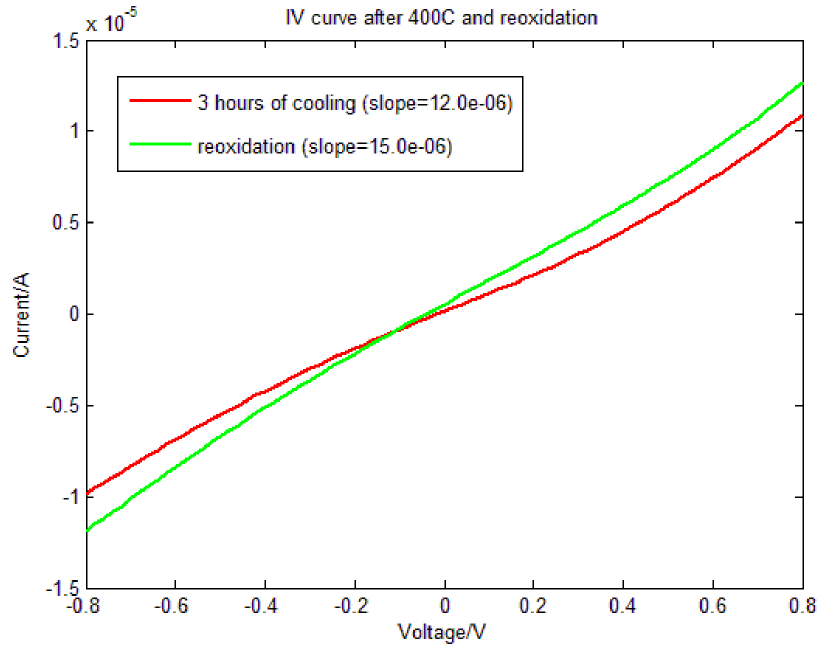



***Figure 4.22:*** *I-V curve of the device after re-oxidation with a temperature used for this cleaning at 400˚C.*

*Figure 4.22* shows the *I-V* curves when the device was heated to 400˚C for 2nd H-cleaning and then exposed to air for re-oxidation. The conductance for the re-oxidation is slightly higher than after 3 hours of cooling, shown by the *figure 4.22*. However comparing *figure 4.21* and *figure 4.22*, in second H-cleaning the conductance after re-oxidation is significantly lower than first H-cleaning, and also nearly linear *I-V* curve, showing that now the contacts of the device have irreversible changed.

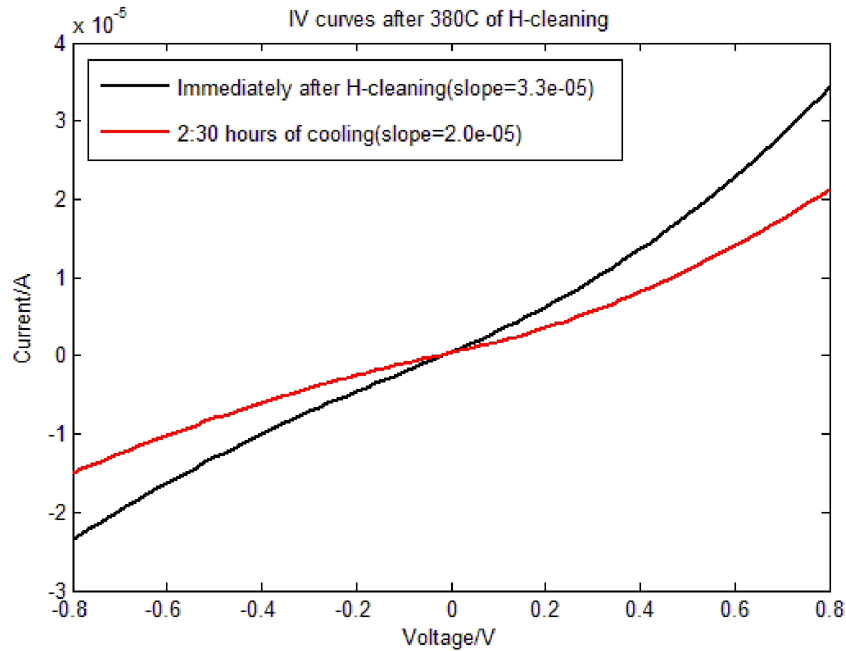



***Figure 4.23:*** *I-V curve of the NW device after H-cleaning inside UHV at a temperature of 380˚C.*

In the 3rd H-cleaning process, the device is again heated to 380˚C. Here the *I-V* curves measured immediately after H-cleaning and after 150 minutes of cooling have similar shapes. The conductance is higher for NW when it is hot, as already seen for NW device *JWP11A*.

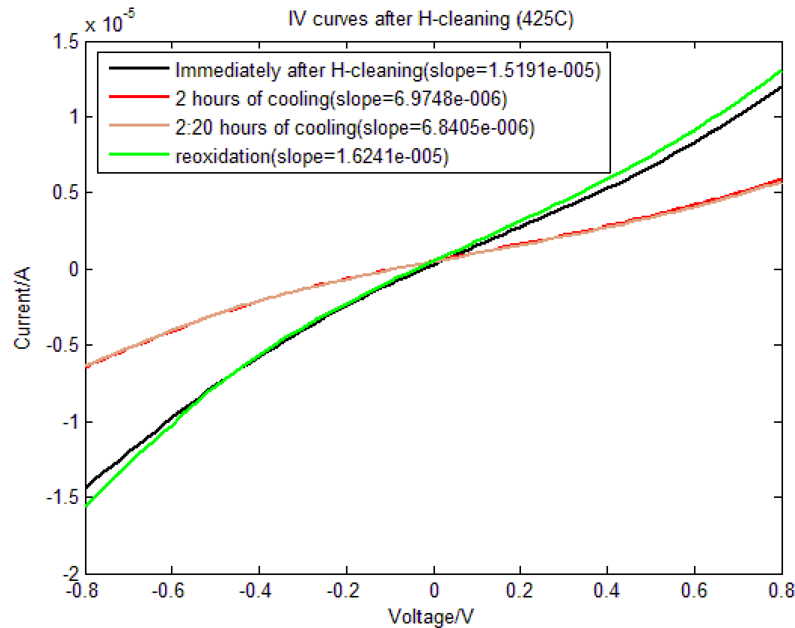



***Figure 4.24:*** *I-V curve of the NW device after H-cleaning and after re-oxidation with a temperature used for this cleaning of 425˚C.*

When the device is heated to 425˚C for the fourth H-cleaning, as shown in *figure 4.24*, the *I-V* curves and the conductance immediately after H-cleaning and after re-oxidation are almost the same. While the conductance as well as shape of the curves for 2h and 2:20h of cooling are the same. All conductance results are shown in *table 4.2*.

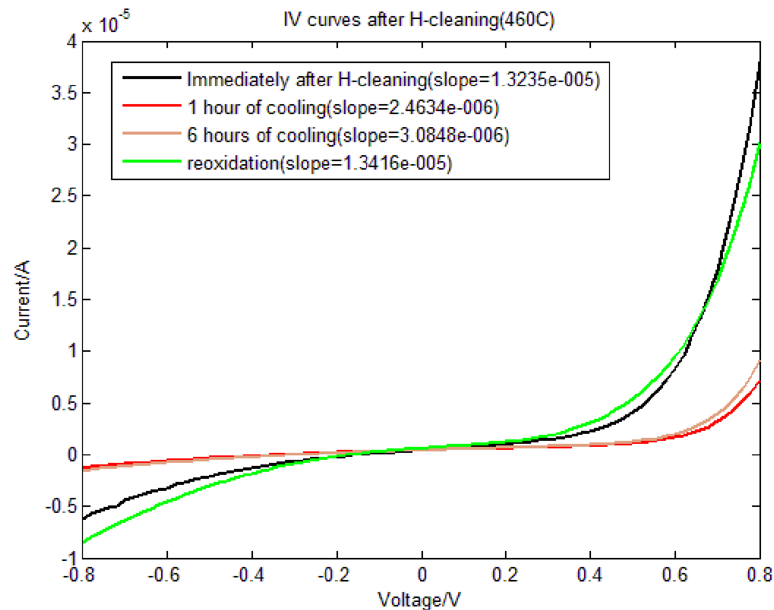



***Figure 4.25:*** *I-V curve of the NW device after H-cleaning and after re-oxidation with a temperature used for this cleaning of 460˚C.*

After the fifth H-cleaning when the device was heated to 460˚C, the shape of the *I-V* curve has been strongly changed, and almost has the same shape like that of the curve before any H-cleaning, although with a lower average conductances (*figure 4.20*). The conductances immediately after H-cleaning when the device is hot and after re-oxidation is almost the same and also the shapes of the curves. The saturation region for the *I-V* curve of the re-oxidation is smaller than the *I-V* curve of immediately after H-cleaning. The curves for 1 hour (red curve) and 6 hours (orange curve) of cooling have the same shapes and also the same conductance. Here we can say that the device shows a rectifying behavior which may be because the metallic contacts are changing again because of heating. So here the conductance of the hot device is higher than after 1 and 6 hours of cooling and strongly increase again upon re-oxidation. In *figure 4.25*, the device behavior was strongly changed compared to *figure 4.24.* So 460˚C is a temperature at which the contacts show strong change as was also have seen for the device *JWP11A*.

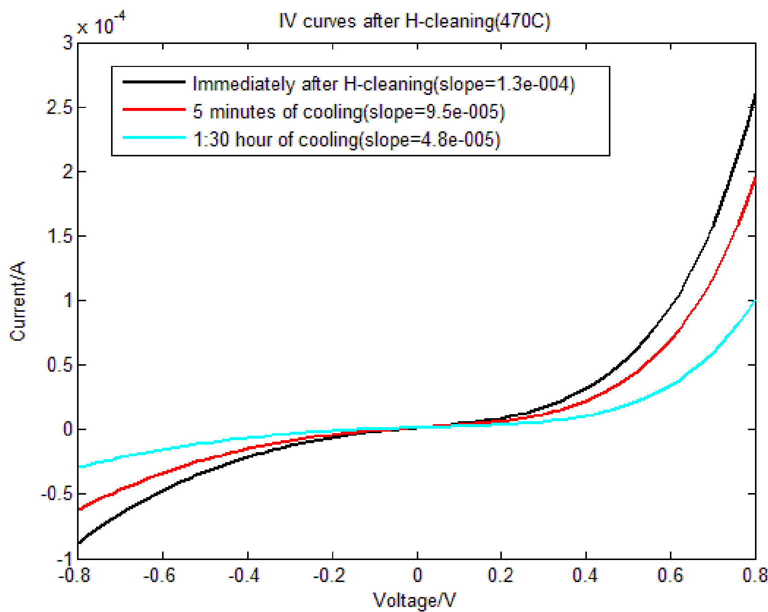



***Figure 4.26:*** *I-V curve of the NW device after H-cleaning inside UHV at a temperature of 470˚C.*

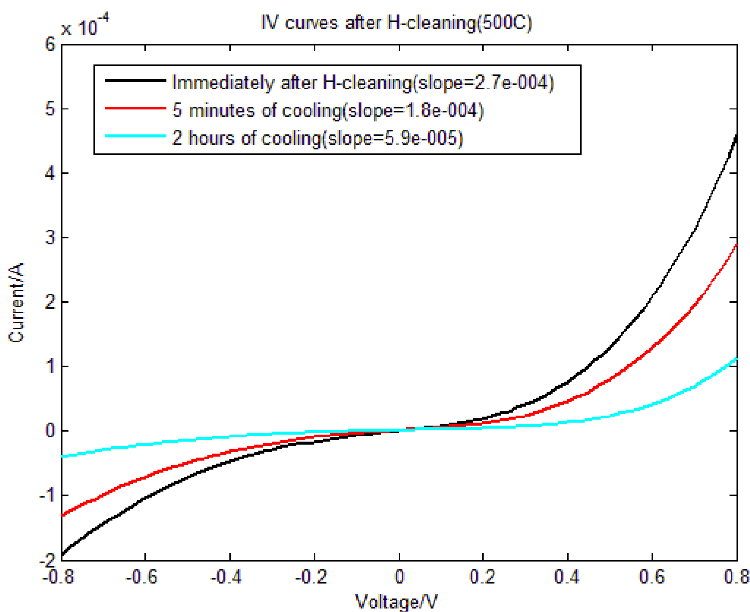



***Figure 4.27:*** *I-V curve of the device after H-cleaning inside UHV at a temperature of 500˚C.*

From *figures 4.26* and *4.27*, again one can see that the conductance for the hot device is higher, and when the device is becoming cooler, the conductance is becoming lower. So we can say that as good contacts give linear curve but bad contacts mean non-linear Schottky contacts. The results are shown in *figures 4.26* and *4.27*.

The conductances for each H-cleaning and re-oxidation steps are shown in the *table 4.2* below.

| H-cleaning with temperature[˚C] | Time of cooling[minutes] | Conductance[μA/V] |
|---|---|---|
| **Before H-cleaning** | 0 | 39.88 |
| **1st H-cleaning with 380˚C of temperature** | 60(1 hour) | 8.60 |
| | 1020(17 hours) | 1.06 |
| | Re-oxidation | 52.20 |
| **2nd H-cleaning with 400˚C of temperature** | 180(3 hours) | 11.965 |
| | Re-oxidation | 14.58 |
| **3rd H-cleaning with 380˚C of temperature** | 0 | 32.86 |
| | 150(2:30 hours) | 20.24 |
| **4th H-cleaning with 425˚C of temperature** | 0 | 15.19 |
| | 120(2 hours) | 6.97 |
| | 140(2:20 hours) | 6.84 |
| | Re-oxidation | 16.24 |
| **5th H-cleaning with 460˚C of temperature** | 0 | 13.24 |
| | 60(1 hour) | 2.46 |
| | 360(6 hours) | 3.08 |
| | Re-oxidation | 13.42 |
| **6th H-cleaning with 470˚C of temperature** | 0 | 130.73 |
| | 5 | 95.44 |
| | 90(1:30 hours) | 48.08 |
| **7th H-cleaning with 500˚C of temperature** | 0 | 272.5 |
| | 5 | 177.43 |
| | 120(2 hours) | 59.03 |

***Table 4.2:*** *Results of H-cleaning for the device with temperatures, related time of cooling and conductance.*

The conductance before any H-cleaning is 40μA/V which strongly decreases upon the first H-cleaning with a temperature of 380˚C, and further decreases when the sample is cooling down. But the conductance is higher after re-oxidation, even higher than before H-cleaning.

After the second H-cleaning at a temperature of 400˚C the conductance has strongly decreased again. This time it only slightly increases when the cold sample is re-oxidized.

After the third H-cleaning with a temperature of 380˚C the conductance has slightly increased and remains high also upon cooling down.

The conductance after the fourth H-cleaning has a similar behavior as after the second H-cleaning. But the conductance immediately after the fifth H-cleaning is higher than after 1 hour and 6 hours of cooling. Also the conductance after re-oxidation is the same as the conductance immediately after H-cleaning. For the sixth and seventh H-cleaning the behavior of the

conductances are similar to the conductance of the fifth H-cleaning, meaning that the conductance is higher for higher temperature while decreasing when the temperature is decreasing. The conductances are plotted against heating and cooling steps in a semi-logarithmic plot in *figure 4.28*.

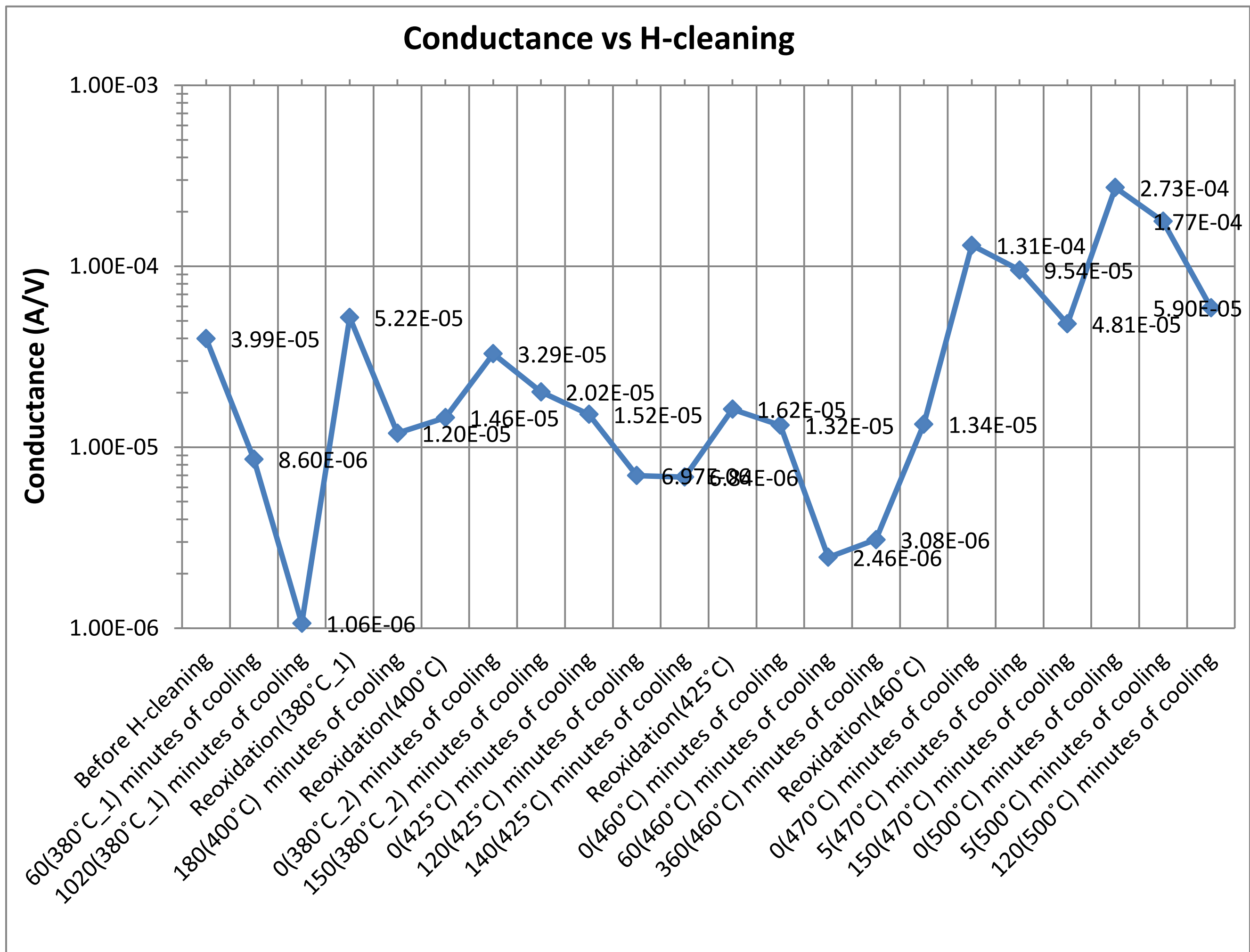



***Figure 4.28****: Conductance vs different H-cleaning.*

The discussion for this part of the result is that for the cleaning at 380˚C strongly changes the contacts worse. The re-oxidation step brings the *I-V* curve back to original contact behavior. Cleaning at 400˚C again changes the contacts, but now the re-oxidation does not bring back the IV behavior so it means that the contacts have changed irreversibly. The next strong change happens at 460˚C, where the conductance goes down and the *I-V* shape changes again. At 500˚C the conductance rises again, but now the device is already severely changed and probably the structure is damaged. Hence, the shape of the *I-V* curve is nonlinear before any heating and this non-linear behavior of the device is because of the Schottky contacts. For the temperature of 380˚C and less than 460˚C there is linear behavior in the IV curve but at 460˚C again there is non-linear behavior.

## 4.3.3: Comparison of n-doped InP NW device with InAs NW device

**JWP11A:**

Annealing n-doped InP NW device (JWP11A) till 370˚C and temperature less than 370˚C shows high conductance compared to conductance before any annealing while the shape of the *I-V* curve was non-linear and asymmetric. There is a strong change for the annealing temperature of 460˚C not only for conductance but also for the shape of the IV curve. Conductance is high and the shape of the *I-V* curve is more linear. The conductance for annealing temperature of 480˚C becomes higher and the shape of *I-V* curve is more linear than 460˚C. But at temperature of 510˚C the conductance has become lower while the shape of the *I-V* curve is much linear. Cleaning has only minor effect on the *I-V* properties of JWP11A especially for higher temperatures.

**TP5 594b:**

For InAs NW device (TP5 594B), the annealing temperature of 380˚C has decreased the conductance compared to conductance before any H-cleaning while the shape of *I-V* curve is same i.e. non-linear and asymmetric. At 400˚C the conductance as well as the shape of the *I-V* curve has changed, now the conductance is higher than H-cleaning at 380˚C and curve more linear. May be this is the temperature where the NW got cleaned because InAs NWs can be cleaned at temperature above than 360˚C. The shape of the *I-V* curve has remained almost same for temperatures lower than 460˚C but becomes non-linear again at 460˚C. The *I-V* curve shape remains the same as the *I-V* curve shape at 460˚C but the conductance increases for temperatures 460˚C and higher.

The H-cleaning temperature for InP NW is between 400˚C and 420˚C while for InAs NW is between 360˚ and 400˚C. For InP NW device, the strong changes occur for temperatures above than 370˚C and are between 400˚C and 460˚C shown by the *figure 4.14* and *table 4.1.* For InAs NW device, the temperature for H-cleaning is between 360˚C and 400˚C, and the changes occur at the temperature of 400˚C shown in *figure 4.22*. Further exposure to atomic hydrogen on the cleaned surfaces for temperatures above than 460˚C does not affect the *I-V* properties of both the devices except the temperature. Also the *I-V* curve for InAs NW device is more non-linear than the InP NW device for temperatures of 460˚C and above, whiles the *I-V* curve for InP NW device becomes linear for 510˚C.

# Chapter 5: Conclusion and outlook

## 5.1: Conclusions

High resolution STM, SEM, and SPELEEM experiments were performed for the investigation of surface chemistry of InAs(111)B substrate, InAs nanowires, and InAs nanowire based devices. In addition, the electrical properties of InP and InAs nanowires based devices were studied in the UHV chamber of the STM.

Using STM for the surface studies of InAs(111)B and InAs nanowires, it is shown that for cleaning the surfaces from oxides the home-built hydrogen cracker is not a perfect choice because its efficiency of 5-10% is much lower than that of a commercial cracker. And by increasing the $H_2$ pressure to reach the necessary amount of atomic hydrogen, there is high supply of $H_2$ at the surface during annealing which leads to partial desorption of already cleaned InAs, leaving the observed small islands back on the surface. Nevertheless, surface cleaning at a temperature of 380˚C-410˚C for the time of 30-40 minutes with atomic hydrogen exposure using the parameters given in section 4.1 leads to the complete removal of the surface oxides.

From SPELEEM as well as SEM studies it is proven that at higher temperature like 700˚C both the device contacts and the nanowire itself are damaged. At lower temperatures like 460˚C, the areas having defects from the manufacturing show changes but the protecting gold layer is still in good condition. The PEEM images still show the NW, which is also shown by the LEEM and MEM images. After 700˚C one can see strong changes in the contacts and these strong changes become more obvious by the SEM images. Also the NW is not homogeneous anymore and the $SiO_2$ layer has become thinner.

From the IV characterization of InP (n-doped) and InAs nanowires based devices in the UHV chamber of the STM it is proven that there are strong changes at temperatures of 380˚C and 460˚C. The conductance is high before any H-cleaning as well as immediately after annealing (when the device is still hot) while decreasing during cooling, but when re-oxidized the conductance again increases. The shape of the IV curve is nonlinear before any heating and this non-linear behavior of the device is because of the Schottky contacts. For the temperature of 380˚C and less than 460˚C there is linear behavior in the IV curve but at 460˚C again there is non-linear behavior.

## 5.2: Outlook

The results do however provide a solid foundation for the future studies related to III-V nanowires and nanowire based devices, as a basic understanding of the surface chemistry and electrical properties. There are few important improvements to the apparatus which would give it the capability for more accurate and meaningful results.

- The commercially built hydrogen cracker will give a good pressure of $H_2$ an extra supply of $H_2$. Therefore no partial desorption of already cleaned III-V surfaces should occur.
- For the better performance of the nanowire based devices the lithographically made metallic contacts should be given extra importance. Because the electrical degradation (as a

function of temperature) of the device also depends of the defects present in the metallic contacts.

- The aluminum (Al) wire which is used to bond the device to external contacts should be replaced by gold (Au) wire. Which might give improved IV characteristics of the nanowire based devices even after annealing.

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