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Surface Chemistry and Electrical Properties of Nanowire Devices

Nanotechnology is generally considered as a key technology for the future of electronic and LEDs as well as from medical point of view. Different research fields of science are involved in nanotechnology, with semiconductor physics playing an important role. Using different fabrication techniques nanometer sized electronic and photonic devices can be made from different semiconductor materials.

One dimensional rod-shaped nano-crystal structures, called nanowires, have tremendous applications. The growth and characterization of single crystalline semiconductor nanowires and nanowire based devices are major areas of research at Lund University. Nanowires have diameters in tens of nanometer (nm) range and lengths up to several micrometers (μm). III-V hetero-structure semiconductor nanowires consist of atoms from groups III and V in the periodic table. They have direct band gap and high electron mobility, so can be used both for high speed devices and photonics.

The surfaces of the III-V semiconductor nanowires are important because of their large surface-to-volume ratio, as surface atoms are more exposed to the environment compared to bulk atoms. Therefore the surfaces of these semiconductors are very sensitive to oxides. These native oxides create surface states which affect band bending, limiting the conductance of the nanowire devices. So these native oxides should be removed without changing the surface structure of the sample. In order to clean the surfaces of the III-V substrate and nanowires from the native oxides, the sample under study is exposed to atomic hydrogen during annealing. With this approach we can clean the surfaces of most III-V semiconductors at temperatures below thermal dissociation of the surface.

However, until now it has not been studied how such cleaning procedures will affect the performance of nanowire devices. Surface sensitive characterization techniques like Scanning Tunneling Microscopy (STM), Photo Emission Electron Microscopy (PEEM), Low Energy Electron Microscopy (LEEM) and Scanning Electron Microscopy (SEM) contribute a lot to the research by obtaining information not only about the surface but also about electrical properties for nanowires and nanowire based devices.

In this thesis, the changes of the surface structure and conductance of planar InAs, InAs nanowires and n-doped InP nanowires during cleaning have been studied with STM, PEEM, LEEM and SEM. The surface oxides of InAs(111)B substrate and InAs nanowires, are successfully removed by H-cleaning. At moderate temperatures there is only a tiny effect of the H-cleaning on the conductance of the nanowire device, but at temperatures above 500˚C the metallic contacts change strongly, which then considerably affects the device conductance. The most pronounced changes are because of chemical reactions of Aluminum wires which are used to connect the device externally with the metallic-(gold) contacts of the device, and because of some defects which have already been incorporated during the lithographic device processing.

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