LUND UNIVERSITY

Master Thesis of Physics Department

IV-Characterization of high-k (Al_2O_3/HfO_2) films on InGaAs substrate

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Abstract

Metal oxide semiconductor (MOS) capacitor was fabricated on the InGaAs substrate with Al_2O_3/HfO_2 gate oxide. InGaAs is one of the promising candidates for advanced applications which require the lower power supply and high frequency. The high-*k* films (Al_2O_3/HfO_2) were formed by atomic layer deposition (ALD) as an alternative to silicon dioxide (SiO_2) to proceed the scaling of oxide to lower values of equivalent oxide thickness (EOT). To reduce the high leakage current HfO_2 has been processed as a gate oxide while Al_2O_3 was used as an interlayer to improve the interface quality of high-*k*/InGaAs.

The constant voltage stress (CVS) and ramped voltage stress (RVS) techniques were used to analyze the reliability of gate oxide in terms of stress induced leakage current and soft & hard breakdown. The analyzed conduction mechanism through high-*k* oxide represents the thermal dependence at high temperature but it was not fitted with PF-model neither with Schottky model. However, band to band tunneling was observed at lower temperature. Time to breakdown 6.13×10^2 s was also measured at 4.5 V constant voltage stress. Breakdown field of Al_2O_3 with oxide thickness 0.5 nm and HfO_2 with oxide 4.5 nm thickness was observed by ramped voltage stress (RVS) technique. Under the positive applied bias the breakdown field for HfO_2 and Al_2O_3 was 9.5 MV/cm and 26.4 MV/cm respectively. Similarly, under negative bias breakdown field for HfO_2 and Al_2O_3 was 6.1 MV/cm and 17.2 MV/cm respectively.

Acknowledgement

All praises to Almighty ALLAH, the most merciful, beneficent and compassionate who blessed my ability, strength and knowledge to complete this research project. All respect and regard to Holy prophet Hazrat Muhammad (P.B.U.H) for enlightening our conscience and paving us on right path with the essence of faith in ALLAH.

I am very grateful to my supervisor Prof. Lars-Erik Wernersson who provides me the opportunity to work on this research project.

I would also like to express my deepest appreciation to Guntrade Roll for her countless encouragement and guidance to keep me on the right track.

I am really thankful to my parents, brothers and sisters for their motivation and always prayer for my success. Finally special thanks to my friends for their help to complete this project.

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List of abbreviations

Notation	Description
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
BTBT	Band to Band Tunneling
ALD	Atomic Layer Deposition
PVD	Physical Vapor Deposition
CVD	Chemical Vapor Deposition
RTP	Rapid Thermal Processing
EOT	Equivalent Oxide Thickness
IV	Current Voltage
FN	Fowler Nordheim
DT	Direct Tunneling
TAT	Trap Assist Tunneling
PF	Poole Frenkel
SILC	Stress Induced Leakage Current
CVS	Constant Voltage Stress
CVR	Ramped Voltage Stress
PMA	Post Metallization Annealing
AHI	Anode Hole Injection

List of symbols

Notation	Description
E_a	Activation energy
E_f	Fermi energy
E_c	Conduction band energy
E_v	Valance band energy
E_i	Intrinsic energy
E	Electric field
V	Applied voltage
V_{ox}	Voltage drop across oxide
d	Separation
m^*	Effective mass
n_i	Intrinsic carrier concentration
Φ_B	Barrier height
Φ_t	Height of trap well
t_{bd}	Time to breakdown
k	dielectric constant
D_{it}	Density of interface traps
J_{FN}	Fowler Nordheim current density
J_{DT}	Current density through direct tunneling
χ	Affinity of an electron
A^*	Effective Richardson constant
e	Electronic charge, 1.60×10^{-19} C
$\hbar$	Reduced Planks constant: 1.054×10^{-34} J-s
k	Boltzmann’s constant, 1.38×10^{-34} J/K or 8.62×10^{-5} eV/K
ε_i	Permittivity of free space, 8.85×10^{-14} F/cm

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1. Introduction

1.1 Introduction

The complementary metal oxide semiconductor (CMOS) made from silicon having silicon dioxide (SiO_2) as an outstanding dielectric has been dominating in electronics industry for decades. The significant development in electronics industry was observed due to scaling of metal oxide field effect transistor (MOSFET). The scaling of transistors was made by the Moor's law which states that the number of transistors is roughly doubled every two years [3]. The main objective of scaling is to increase the number of transistors per chip by shrinking their horizontal and vertical dimensions. The aggressive downscaling of MOSFETs leads to low power consumption equipment like personal computer, tablets and mobile etc. But due to ultra large downscaling of CMOS devices the thickness of SiO_2 has been reduced to 14 Å which results in high gate leakage current through ultra-thin oxide [1]. The high gate leakage current enhances the power consumption and reduces the oxide reliability [2]. One possible solution to continue the scaling for longer time and also to reduce the power consumption is to change the transistor's structure with alternative materials.

The key advantage of Si was an excellent interface with SiO_2 having only few electronic defects. III/V semiconductors such as GaAs and their related compound materials have much higher electron mobility than Si and Ge as shown in table (1) [3]. InGaAs is one of the promising candidates among many compound semiconductors because of its light affective mass which leads to high electron mobility and high on-currents [4]. The higher carrier mobility of III-V semiconductors leads to faster complementary metal oxide semiconductor logic operations at lower power supply [5]. Also band structure engineering of III-V semiconductors provides more flexibility in designs with respect to Si and Ge [3].

Table 1: *Electrical properties of semiconductors regarding to electron mobility, hole mobility and band gap* [3].

Electrical Properties	**Si**	**Ge**	**GaAs**	**$In_{0.53}Ga_{0.47}As$**
Electron effective mass (m^*/m_o)	0.98	1.64	0.067	0.041
Electron Mobility ($Cm^2V^{-1}S^{-1}$)	1500	3900	8500	12000
Hole Mobility ($Cm^2V^{-1}S^{-1}$)	470	1900	400	300
Band Gap (eV)	1.12	0.67	1.42	0.74

The high-k oxides were introduced as alternative gate dielectrics to SiO_2 to enhance the electrical performance of MOS devices. By using high-k oxides the gate leakage current decreases exponentially while keeping the same capacitance [1].

$$C = \frac{\varepsilon_0 \, k_{sio_2} \, A}{t_{ox}} = \frac{\varepsilon_0 \, k_{high-k} \, A}{t_{high-k}} \quad (1)$$

Equation (1) shows the equivalent capacitance through low-k and high-k oxides [6], where C represents capacitance, A is the area, ε_0 the permittivity of free space, $k\text{-}SiO_2$ is dielectric constant of SiO_2, $k_{high\text{-}k}$ is dielectric constant of high-k films, t_{ox} is the thickness of SiO_2 and $t_{high\text{-}k}$ represents the thickness of high-k dielectrics.

As compared to other semiconductors the main advantage of Si was the high quality natural grown SiO_2 gate oxide [1]. On the other hand high-k oxides were deposited by the atomic layer deposition having poor interface quality with compound semiconductors [7]. More research is needed to decrease the high-k/compound semiconductor interface defects to resolve reliability issues.

After the brief introduction, the second chapter presents the theoretical and experimental backgrounds of metal oxide semiconductor devices. In the processing chapter the detailed fabrication process was discussed. In the last part of this project characterization of processed sample was made by analyzing the leakage current, stress induced leakage current, time to breakdown and hard breakdown field for Al_2O_3 and HfO_2.

2. Theoretical and experimental background

2.1 Ideal MOS capacitor structure

The metal oxide semiconductor (MOS) capacitor is the heart of metal oxide field effect transistor (MOSFET). A MOS capacitor is a two terminal device. Generally, it is processed by growing an oxide film on top of semiconductor substrate and then depositing the metal on the oxide layer to form the contacts called gate electrode as shown in Fig (2). The oxide film is sandwiched between the gate and the semiconductor substrate.

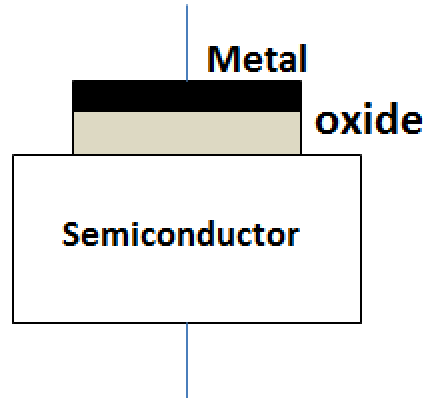

Figure 1: *MOS capacitor structure represents the gate electrode, oxide as an insulator and semiconductor as substrate.*

By appropriate applying bias the energy bands in the semiconductor bends upwards or downwards from the oxide-semiconductor interface due to the electric field induced across the oxide.

$$E = \frac{V}{d} \tag{2}$$

In equation (2) E represents the magnitude of electric filed, V is the applied bias and d is the thin film thickness [3].

The Fermi level position depends on the applied bias, therefore the concentration of electrons and holes regarding to applied voltage can be described as in equation (3) & (4) [3].

$$n = n_i e^{\frac{E_i - E_f}{kT}} \tag{3}$$

$$p = n_i \, e^{\frac{E_f - E_i}{kT}} \tag{4}$$

In equation (3) & (4) n and p describe the density of electron and holes, where k is the Boltzmann's constant, T is temperature, n_i is the intrinsic carrier concentration and E_i & E_f is the intrinsic energy and Fermi energy, respectively.

The band diagram of a MOS capacitor with n-type substrate represents the distribution of charges under the applied biases.

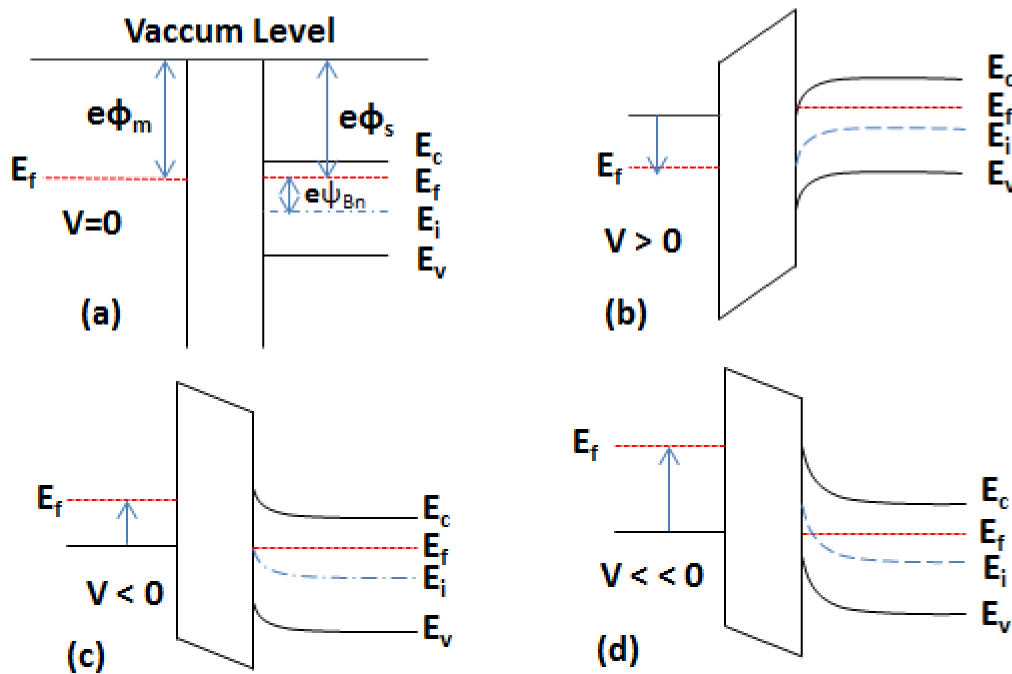

Figure 2: *Energy band diagram of MOS capacitor with n-type semiconductor, (a) Flat band, (b) Accumulation layer of majority carriers (electrons), (c) Depletion region of ionized donors and (d) Inversion layer of minority carries (holes) [8].*

Fig (2a) shows an n-type semiconductor with metal work function $e\phi_m$ and semiconductor work function $e\phi_s$. The metal work function is defined as the energy required to inject an electron from metal to conduction band of oxide [3]. In equilibrium the metal work function is equal to semiconductor work function known as flat band condition ($\phi_m = \phi_s$) [8]. Therefore, the barrier ϕ_m seen by carriers to move from the metal to conduction band of oxide is equal to the barrier ϕ_s seen by carriers to move from n-type semiconductor to conduction band of oxide are equal.

Under the positive bias regarding to n-type semiconductor, the metal Fermi level is shifted downward which indicates the positive charge density increases at the metal surface. To satisfy charge neutrality, an equal amount of negative charges will be accumulated near the oxide-semiconductor interface. The conduction-band edge is closer to Fermi level at oxide-semiconductor interface than in bulk material which indicates the accumulation of negative charges at the oxide-semiconductor interface. The induced electric field will bend the conduction and valance band of semiconductor downwards at oxide-semiconductor interface as shown in Fig (2b). As the metal work function is equal to the semiconductor work function, the induced electric field tilts the conduction and valance band of oxide [8].

When small negative voltage is applied on the top of metal gate, the Fermi level of metal moves upward and lies above the equilibrium position as shown in Fig (2c). Therefore the

concentration of electrons increases on metal surface and a depletion region is formed due to the repulsion of electrons from semiconductor surface and positive donor ions are left behind. The induced electric field will bend the conduction and valance band of the semiconductor towards the semiconductor oxide interface. The density of electrons (majority carriers) at the oxide-semiconductor interface decreases as compared to bulk of n-type semiconductor due to bending of conduction and valance bands towards semiconductor oxide interface [8].

Under sufficient negative applied bias on the gate electrode, the electron density on metal surface increases as the Fermi level of metal shifts upward. Therefore the density of minority carriers (holes) increases which implies a larger induced space charge region and even more band bending occurs [3]. Consequently, at the oxide semiconductor interface the density of minority carriers (holes) is much higher than the majority carriers (electrons). Therefore with sufficient negative applied bias n-type semiconductor would behave like p-type semiconductors at semiconductor-oxide interface known as inversion [3].

2.2 High-*k* films

Dielectrics or electrically insulated materials are used in integrated circuits and also for gate oxides. Dielectrics have been divided into two categories regarding to the *k*-values. The dielectrics which have *k*-values lower than 5 are known as low-*k* oxides such as SiO_2 and those which have *k*-values higher than 5 are called high-*k* oxides such as HfO_2 [1].

Equivalent oxide thickness (EOT) is the electrical thickness of silicon dioxide to get same capacitance as the high-*k* material being produced with relatively higher thickness as shown in equation (5) [1].

$$t_{ox} = EOT = \left(\frac{3.9}{k}\right) t_{high-k} \qquad (5)$$

To introduce the high-*k* oxides is not as easy as it seems to be. For successful introduction of high-*k* dielectrics, it must satisfy some elementary conditions.

The value of new dielectric must be high enough to continue the scaling for number of years and to maintain the band offset, the band gap must be over than 5 eV to avoid the Schottky emission [9]. The gate oxide having only few active bulk defects and it would be in direct contact with substrate. The electrical interface quality in terms of roughness and in the absence of interface defects should be high. There are only few high-*k* dielectrics that satisfy the selected criteria such as Al_2O_3 and HfO_2 [9].

2.2.1 Al_2O_3/HfO_2 gate stack

A bi-layer is the composition of two high-*k* films and it can be processed according to the need of MOSFET. HfO_2 and Al_2O_3 bilayer gate oxide is a promising combination for InGaAs to reduce the high leakage current and also to enhance the substrate interface quality with high-*k* oxides. In order to maintain the high performance of MOS devices, density of interface trap (D_{it}) should be low at a high-*k*/InGaAs interface. The higher D_{it} causes the

degradation of drive current and sub threshold swing [4]. The dielectrics constant of HfO_2 (k = 25) has the ability of down scaling for number of years but the interface quality of HfO_2/InGaAs is poor as compared to SiO_2/Si [9].

In order to improve the interface quality of HfO_2/InGaAs, the Al_2O_3 interfacial layer should have been grown between HfO_2 and InGaAs. The potential barrier height of gate oxide has changed due to formation of Al_2O_3 with larger band gap (8.8 eV) between HfO_2 and InGaAs. Therefore the leakage current should be reduced due to higher barrier. Also the interface quality of high-k/InGaAs would be improved due to insertion of inter-layer Al_2O_3 having very low D_{it} [10].

2.3 Conduction mechanism

The leakage current through stacked gate Al_2O_3/HfO_2 is strongly dependent on applied bias and might be also dependent on temperature. Different conduction processes could be considered to evaluate the accurate leakage current for different dependences as shown in Fig (3).

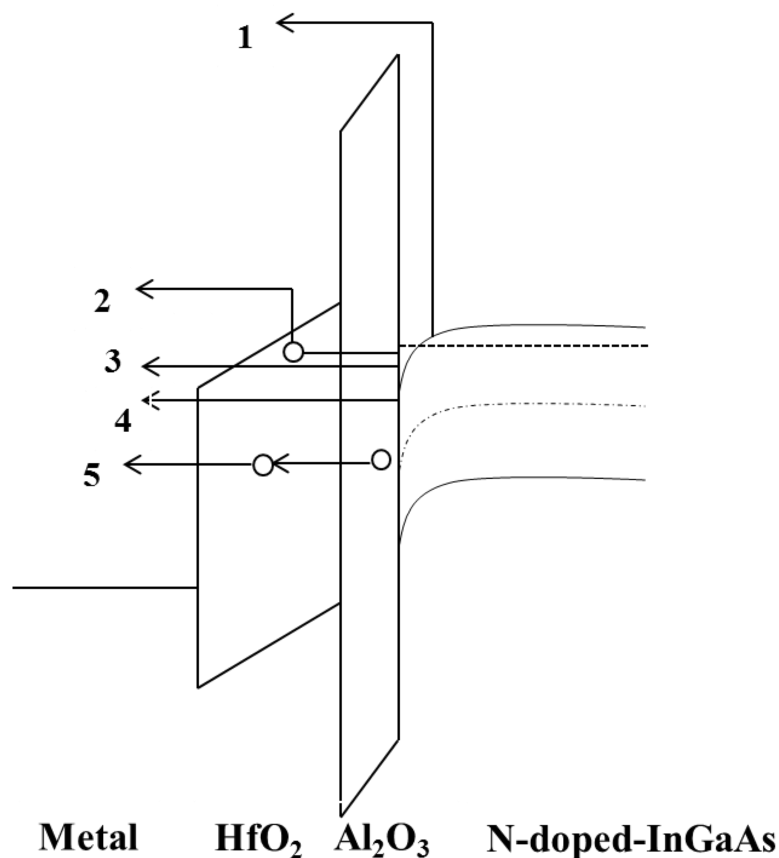

Figure 3: *Conduction mechanisms through HfO_2/Al_2O_3: (1) Schottky emission, (2) Poole Frenkel emission, (3) Fowler Nordheim tunneling, (4) Direct tunneling, (5) Trap assisted tunneling [11].*

2.3.1 Band to band tunneling

In Fig (3) conduction mechanism-3 to-5 represent the tunneling leakage current. Tunneling is purely a quantum mechanically phenomenon by which carrier wave functions have finite probability to penetrate through a potential barrier. It strongly depends on the applied bias and it is almost independent of temperature. Under the influence of high electric field coupled with low oxide thickness, the gate oxide tunneling current has been observed due to tunneling of carriers from gate to semiconductor and also from semiconductor to gate through the potential barrier. The probability of the tunneling current depends on the oxide thickness, the potential barrier height and also on the oxide structure [12]. There are two types of tunneling regarding to band to band tunneling known as Fowler Nordheim tunneling and direct tunneling.

The induced electric field bends the energy bands of lightly n-doped-InGaAs. The band bending has been observed under the electric field and voltage drop across the oxide resulting in thinning of oxide. In Fig (3) conduction mechanism-3 shows tunneling of electrons through a triangular barrier called Fowler Nordheim tunneling. The equation (6) represents the Fowler Nordheim tunneling when the voltage drop across oxide is greater than potential barrier height (ϕ_B) [25].

$$J_{FN} = \frac{q^3 E_{ox}^2}{16\pi^2 \hbar q \phi_B} exp\left(-\frac{4\phi_B{}^{\frac{3}{2}}\sqrt{2m^*}}{3\hbar q E_{ox}} \right) \tag{6}$$

In equation (6) J_{FN} represents the Fowler Nordheim current density [2] , E_{ox} is the electric field across oxide, q is the electric charge, ϕ_B is the potential barrier height, m^* is the effective mass of an electron and $\hbar$ is the reduced Planck's constant.

Usually in ultra-thin oxides (14 Å) direct tunneling dominates. In Fig (3) conduction mechanism-4 represent the direct tunneling in which electrons are tunneling through trapezoidal barrier.

$$J_{DT} = \frac{q^3 E_{ox}^2}{16\pi^2 \hbar \phi_B} exp\left(-\frac{4\phi_B{}^{\frac{3}{2}}\sqrt{2m^*}}{3\hbar q E_{ox}} \left[1 - \left(1 - \frac{V_{ox}}{\phi_B} \right)^{\frac{3}{2}} \right] \right) \tag{7}$$

The current density (J_{DT}) through direct tunneling can be found by using equation (7) [2]. Direct tunneling is observed when the voltage drop (V_{ox}) across the oxide is smaller than the barrier height. Therefore electrons start tunneling directly through the forbidden gap of oxide.

2.3.2 Trap Assisted Tunneling (TAT)

Trap assisted tunneling (conduction mechanism-4) depends on the density of traps in the bulk of dielectrics shown in Fig (3). Defects in the oxide give rise to the tunneling mechanism based on two or more traps. These traps are generated due to high field stress. As the density

of traps increases, the TAT leads to stress induced leakage current. TAT can be observed at very low electric field when tunneling probability of the carrier through complete barrier is low [13].

Hopping and Poole Frenkel emission represent the trap assisted conduction mechanism. Hopping conduction is due to jumping of electrons from filled tarps to empty ones and mostly occurred in trap rich high-k oxides [14].

2.3.3 Poole Frenkel emission (PF)

Electrically active defects and impurities give rise to localized electronic states in forbidden gap of oxides. These electronic states can act as charge trapping in MOS devices. When electrons get trapped in localized states cannot move freely. The emission of electrons from the traps depends on the applied bias and also on the temperature [11]. In high electric field electrons need less thermal energy to get out of trap well. At zero field the barrier height represents the trap depth.

In fig (3) conduction process-2 represents thermal emission of electrons from the traps to over the barrier so called Poole Frenkel (PF) emission [11]. Hopping causes more defects across the oxide. Therefore leakage current through Poole Frenkel emission is also increasing due to high oxide defects [11]. The band bending is affected due to electric interaction between charged carriers and trapped centers [26]. Consequently, the barrier height is lowered which makes the conduction possible.

$$J_{PF} = CE_{ox}\, exp\left[\frac{-q\left(\phi_t - \sqrt{qE/\pi\varepsilon_i}\,\right)}{kT}\right] \quad (8)$$

In equation (8) C is the function of trapping centers, E_{ox} is the electric field across oxide, ϕ_t is the height of trap well, ε_i is the permittivity of insulator [11].

2.3.4 Schottky emission

The conduction of charged carriers over the barrier called is Schottky emission (conduction mechanism-1). Schottky emission is a type of hot carrier's emission. Therefore it is strongly dependent on temperature and also on the electric field. Schottky emission is possible when the barrier height of oxide is less than the voltage drop across the oxide. The Schottky emission can be reduced with assistance of dielectric materials which have larger band gap like Al_2O_3.

$$J = A^{*}T^{2} exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right] \quad (9)$$

In equation (9) A^* represent the effective Richardson constant, ϕ_B is the barrier height, E is electric field, ε_i insulator permittivity, k is the Boltzmann's constant and T is the temperature [11].

2.4 Defects and degradation mechanism

Usually atomic configurations are produced due to deficiency or excess of oxygen known as impurities [9]. The carriers get trapped in available vacancies due to different structural defects with dangling bonds and it changes the band structure. Thermally grown SiO_2 on Si have only few bulk traps because of its low coordinate number but high-*k* on III/V have many intrinsic defects because bonding of high-*k* oxide material cannot relax as easily as SiO_2 can [1]. The generation of bulk and interface traps also increases by electrical stress.

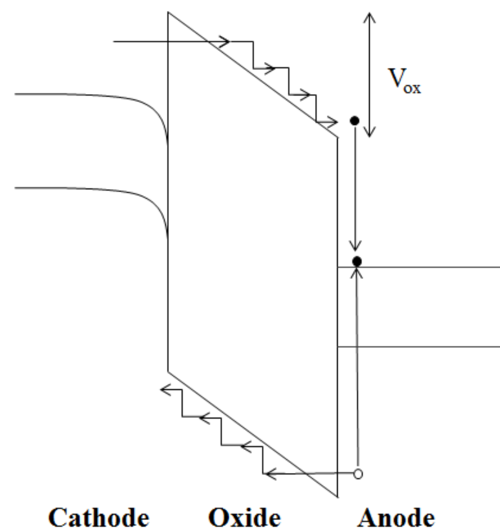

Figure 4: *Anode hole injection model describes the degradation mechanism [2].*

The anode hole injection (AHI) describes the physical process of electron injection into oxide under the high field as shown in fig (4). The AHI fitted well with experimental data at high field stress also known as $1/E$ model [24]. The injected electrons are tunneling through the conduction band of oxide via Fowler Nordheim tunneling or Direct Tunneling. At the oxide-metal interface they fall into anodes conduction band by losing their excess energy. The electron-hole pairs are generated in the anode through impact ionization. At the anode some of electrons are able to elastically transfer their energy to deep level valance band electrons [2]. The transmission of this energy promoted the valance band electron to the anode conduction band. Once the electron reaches the conduction band, it will generate the hot hole. The generated hole can tunnel back into oxide, increasing the current density though hole-induced trap generation. Once the trap has been created, the more hot holes are generated which leads more damage across oxide [15].

2.5 Stress induced leakage current (SILC)

Under the high electrical stress the gate leakage current is increasing due to formation of defects in gate oxide known as stress induced leakage current (SILC). It can be observed at low electric field and it is generally attributed to trap assisted tunneling [23]. As the stress time is increasing the SILC is also increasing as shown in Fig (6). Therefore SILC is the starting point of wear-out of the oxide before the soft breakdown and hard breakdown [16]. The stress induced leakage current in terms of damage across the oxide can be observed by periodic interruption.

2.6 Breakdown

The modeling of breakdown depends on the density of traps. The oxide breakdown depends on the area of dices, voltage drop across oxide, and stress conditions [17]. In the percolation model the generated defects are characterized by a sphere known as neutral electron traps as shown in Fig (5). The bunch of small traps is collectively called a cluster. When the density of traps is sufficiently large then it starts overlapping and makes a conduction path from one interface to another interface of oxide [17].

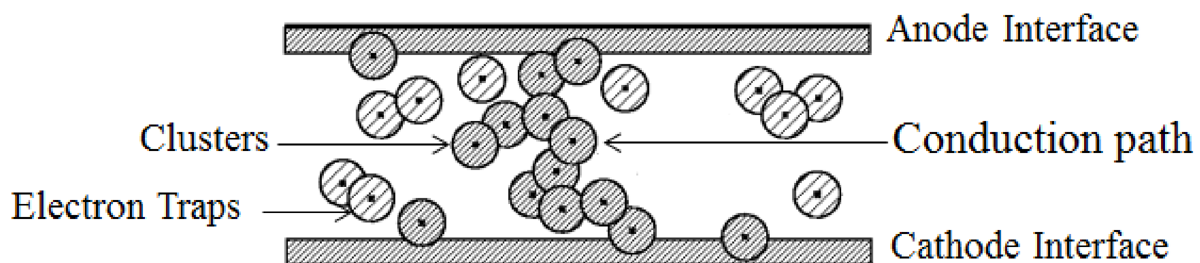

Figure 5: *Percolation model for oxide breakdown [17].*

2.6.1 Soft breakdown

Under the applied stress voltage leakage current increases due to generation of traps which forms a weak localized conduction path between anode and cathode [17]. In soft breakdown the leakage current is some order of magnitude smaller than in hard breakdown as shown in Fig (6). Generally, in soft breakdown the whole oxide would not be worn-out. Therefore in the bilayer case it is suggested that may be one layer of oxide shows breakdown but the other layer does not show conducting behavior.

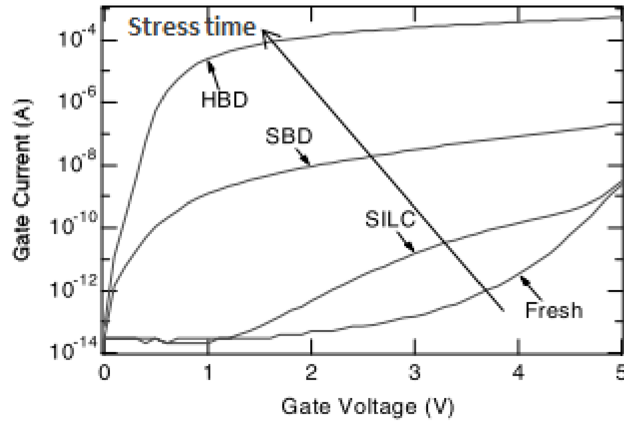

Figure 6: *Gate leakage current as function of applied gate voltage represents comparison between fresh device leakage, SILC, soft and hard breakdown [17].*

2.6.2 Hard breakdown

The second type of breakdown is called hard-breakdown also known as post-breakdown. Hard breakdown can be characterized by large change in leakage current due to high damage across the oxide as shown in Fig (6). Unlike the soft breakdown, hard breakdown completely destroys the oxide structure. During the soft breakdown once the conduction path has been formed, its leads to more generation of traps and thermal damage. Therefore cyclic process of thermal damage leads to final oxide breakdown called hard breakdown [18].

3. Fabrication

The metal oxide semiconductor fabrication has been made by using the III/V semiconductor to analyze the high-*k*/InGaAs interface. High-*k* films (HfO_2 and Al_2O_3) were grown by atomic layer deposition to reduce the high leakage current and to improve the high-*k*/InGaAs interface quality. Metallization was made by using titanium (Ti) and gold (Au).

The processing of metal oxide semiconductor capacitor has been made according to the following steps.

- Preparation of the InGaAs surface
- Deposition of high-*k* films (Al_2O_3/HfO_2)
- UV-Lithography
- Metallization (Ti/Au)

3.1 Preparation of the InGaAs surface

Cleaning of InGaAs was carried out to get high process reliability. The purpose of wafer cleaning was to remove the unwanted material without damaging the substrate. For ultrasonic cleaning the sample was immersed in acetone and isopropyl alcohol (IPA) for three minutes each to remove the dust particles from the InGaAs surface. After that the wafer was rinsed in solution of hydrochloric acid (HCl) for 10 s to remove the native oxides.

We had made a dummy gate on the wafer by using resist XR1546-006. Actually this step was not necessary for MOS capacitors; it was just to make the interface comparable to MOSFET devices. For high temperature treatment rapid thermal processing (RTP) was used in the presence of oxygen for 1 hour at 350 $^{\circ}$C. The dummy gate was removed by hydrofluoric acid (HF) and followed by ozone cleaner. In UV-ozone cleaner system (UVOH-150) oxygen turned into ozone by UV-radiation. The interaction of high intensity UV-light with substrate removed the organic contaminants from the surface. In order to achieve high quality InGaAs interface the sample rinse in solution of $(NH_4)_2S$ for 20 minutes to minimize the surface state densities [19].

3.2 Deposition of High-*k* films (Al_2O_3/HfO_2)

Atomic layer deposition (ALD) is a promising technique to deposit the high quality thin films on substrate. In ALD the substrate surface was exposed in vacuum chamber in the presence of two alternating precursors to create the self-saturated chemical reactions. The cyclic process of ALD is schematically shown in Fig (7).

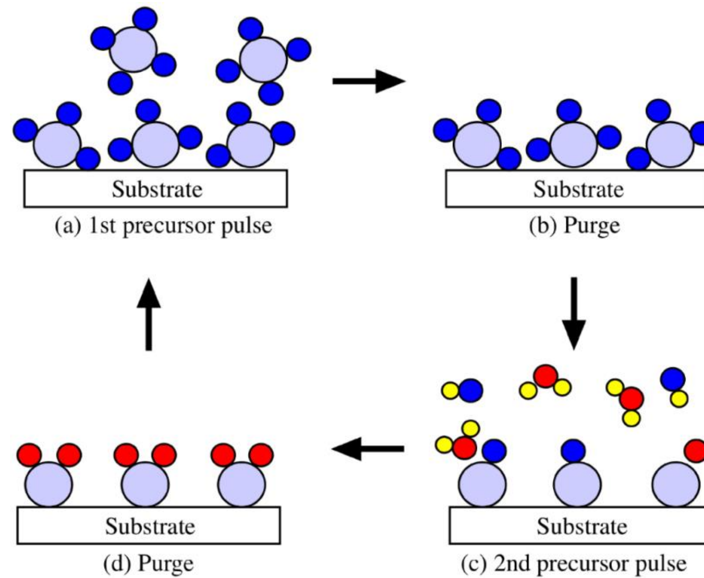

Figure 7: *Schematic represents the ALD cyclic process [20].*

One complete cycle represents one-layer of the compound on the substrate. The number of precursor cycles controlled the oxide thickness. In each cycle deposition continues to defined saturation point. Therefore, it is a self-limiting process to deposit the uniform and conformal films with precise controlled oxide thickness. The Cambridge Nano-Tech Savannah 100 system was used to deposit the high-*k* (Al_2O_3/HfO_2) films on the InGaAs.

3.2.1 Al_2O_3 deposition

First the Al_2O_3 film was deposited by using the tri-methyl aluminum (TMAl). The Al precursor was used to deposit the Al molecules and H_2O was used as the oxygen precursor. Al molecules are chemisorbed onto the substrate and form one mono layer. The excess of reactants are purged out of the growth chamber before exposing the substrate to second precursor. Second precursor undergoes an exchange reaction with the first adsorbed reactant and forms a solid molecular film. The by-products or physisorbed on the surface are removed by the purging of N_2. The growth rate of Al_2O_3 monolayer is around 1 Å per cycle [21]. The deposited Al_2O_3 thickness was 0.5 nm at 300 $^{\circ}$C with 5 cycles of Al.

3.2.2 HfO_2 deposition

For the deposition of HfO_2 Tetrakis [dimethylamido] hafnium was used as Hf precursor and water vapor was used as oxidizer. Similarly, first the substrate surface is exposed and Hf precursor molecules were adsorbed. The weakly adsorbed molecules were desorbed from surface and removed from chamber by the purging of N_2. After the removal of by products, the substrate surface was exposed to the second precursor and starts the chemical reaction. The one monolayer formed due to chemical reaction of water vapor with adsorbed Hf molecules. The thickness of oxide was 4.5 nm after deposition of 50 cycles at 120 $^{\circ}$C.

3.3 UV-Lithography

Ultraviolet-lithography is an optical technique used in fabrication to transfer the geometric pattern from photo-mask to thin layer of photo sensitive materials. The mask aligner MJB4 was used as photolithography.

Fig (8) shows the sequence of photolithographic process. After the deposition of high-*k* oxides (Al_2O_3/HfO_2) the sample was coated with photo resist first LOR-10B and then S1813 as shown in Fig (8b). Positive photo-resist is ultraviolet sensitive compound was distributed equally on the wafer and spun by the high speed spinner. Then the wafer was soft baked to improve the adhesion and to drive the solvents out of resist [22]. Fig (8c) illustrates the exposure of photo resist with UV-light. Before the exposure of photo resist, it is insoluble in developer solution.

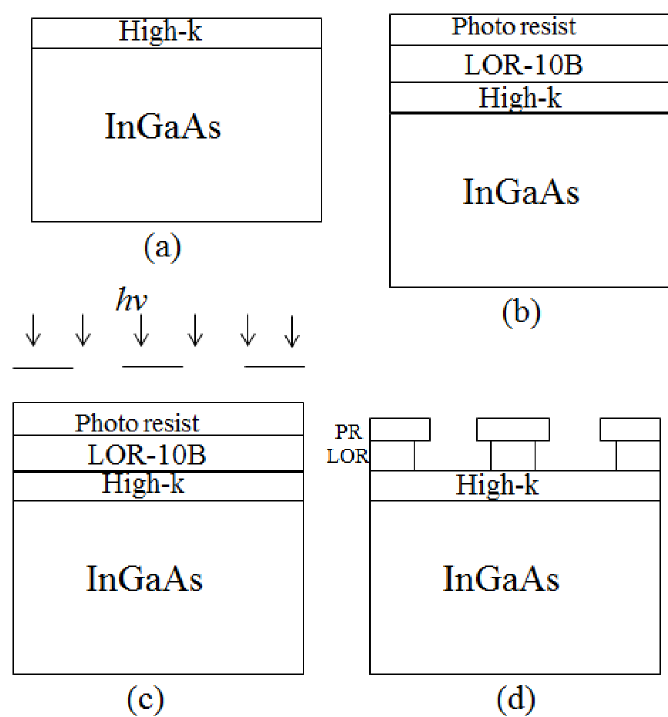

Figure 8: *Photolithographic process, (a) substrate with high-k oxide, (b) application of LOR-10B and S1813 photoresists, (c) exposure of photoresist with UV-light, (d) after development.*

After the exposure to the radiation, the exposed positive photosensitive compound adsorbs the UV-light and breaks its long polymer into small parts that become soluble in the developer solution. The exposed positive resist area was removed from the developed holes as shown in Fig (9d) [22].

3.4 Metallization (Ti/Au)

The deposition of metal layers on the top of wafer surface is known as metallization. Metals with high conductivity are used for fabrication of semiconductor devices. For successful metallization, conductors have to fulfill some preliminary properties.

- Conductors have low resistivity to construct high speed devices with low power consumption.
- Having smooth surface for high resolution patterning process.
- High electromigration resistance to enhance the reliability.
- Low film stress for better adhesion to underlying substrate.

There are three most common methods to deposit the metal layers, physical vapor deposition (PVD), chemical vapor deposition (CVD) and electrochemical. In this project PVD technique has been used to deposit titanium (Ti) and gold (Au) on the wafer substrate. In an evaporator the Ti and Au boats were heated above the melting point with resistance heating and sample holder stays on the top of boats as shown in Fig (9). The evaporated atoms travel at high velocity and deposited on the entire sample surface

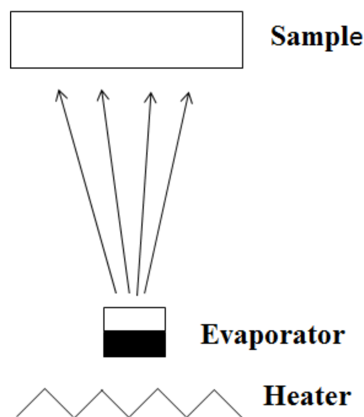

Figure 9: *Block diagram of evaporator.*

Compared to gold, titanium adheres well to high–k oxides. Therefore Ti with thickness 1 nm was used as an interlayer between high-*k* and gold. The thickness of deposited gold layer was around 2000 nm to make better contact with probes.

3.4.1 Lift-off

LOR-10B resist was used to create the clear separation between the deposited metal layers on the developed holes and unwanted metal layers deposited on photo resist shown in Fig (10a). After the metallization the sample was rinsed in acetone for 1 hour to dissolve the resist. Furthermore removal 1165 was used to get rid of all resist residuals. Fig (10b) represents the deposited metal on top of high-*k* oxide as gate electrode.

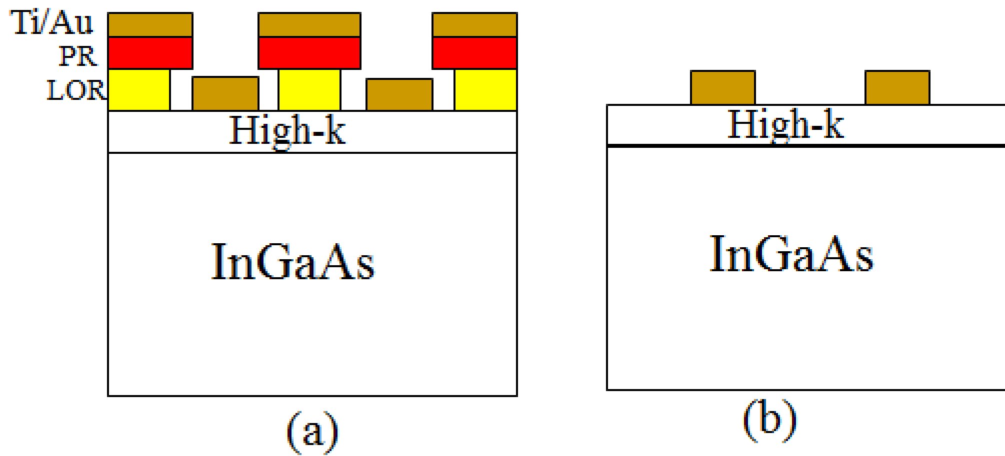

Figure 10: *(a) Deposition of metal layers (Ti/Au) by PVD, (b) LOR-10B was dissolved with unwanted metal layers.*

After the lift-off post metallization annealing (PMA) was carried out used at 350 $^{\circ}$C for 5 minutes in N_2/H_2 to decrease the interface trap density.

Fig (11) represents the optical image of processed sample with deposition of high-*k* films (Al_2O_3/HfO_2) and metallization (Ti/Au) on InGaAs substrate.

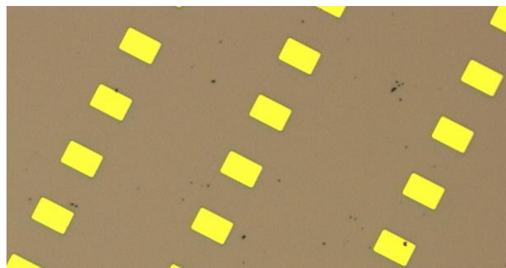

Figure 11: *Top view of fabricated sample (metallization/high-k/InGaAs).*

4. Experimental results and Discussion

This chapter is about the measurements scheme to characterize the high-*k* oxide (Al_2O_3/HfO_2) on InGaAs substrate. The current voltage curves were measured by Keithley and Agilent parameter analyzer to investigate the conduction mechanism through oxide. Probe tips were used to contact the sample. Different techniques were used to analyze the gate leakage, stress induced leakage and breakdown of oxide under positive applied bias.

4.1 Leakage current

The gate leakage current was measured as function of applied gate voltage on 10-dices across the sample at room temperature 300 K. The area of each device was 2364.15×10^{-8} cm^2. Fig (12) shows the small variation in leakage current across the sample.

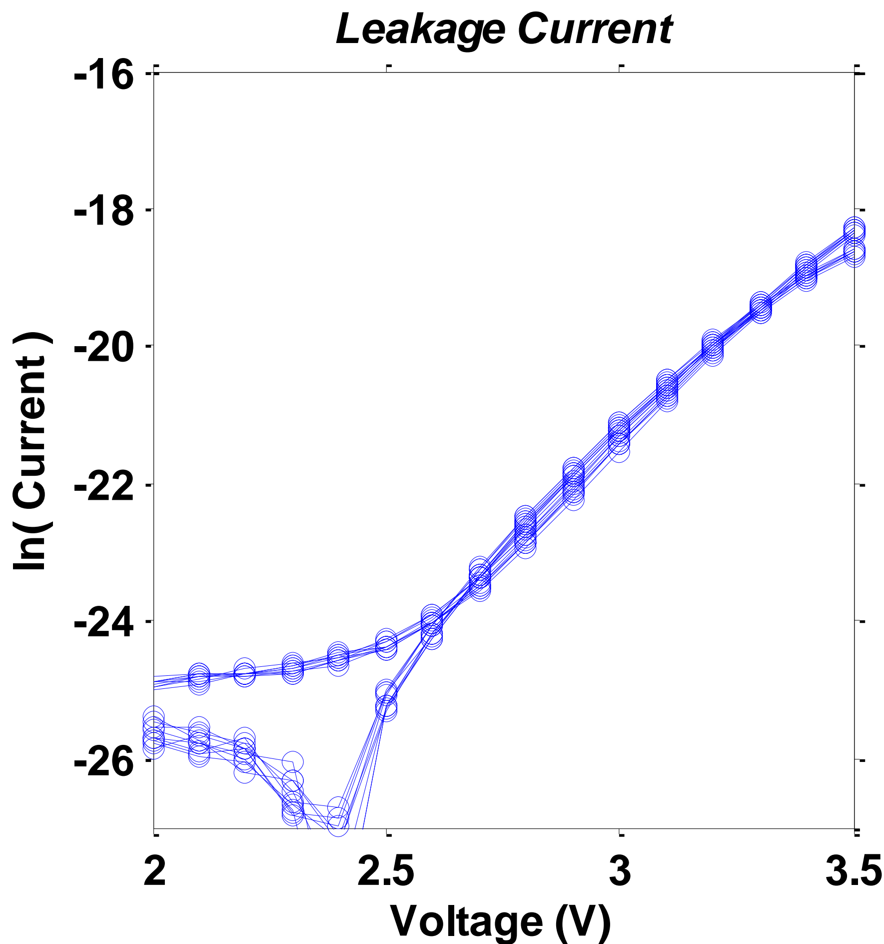

Figure 12: *Leakage current was measured on 10-devices at room temperature.*

Out of ten-dices one dice was picked as a reference dice to characterize conduction mechanism though bilayer Al_2O_3/HfO_2 gate oxide.

Figure (13) shows the current density as function of applied gate voltage. The current-voltage (*I-V*) curves were measured at 0 $^{\circ}$C, 25 $^{\circ}$C, 40 $^{\circ}$C, and 70 $^{\circ}$C temperature to evaluate their

dominant dependence. The maximum applied gate voltage is 3.5 V to avoid any permanent damage across the oxide.

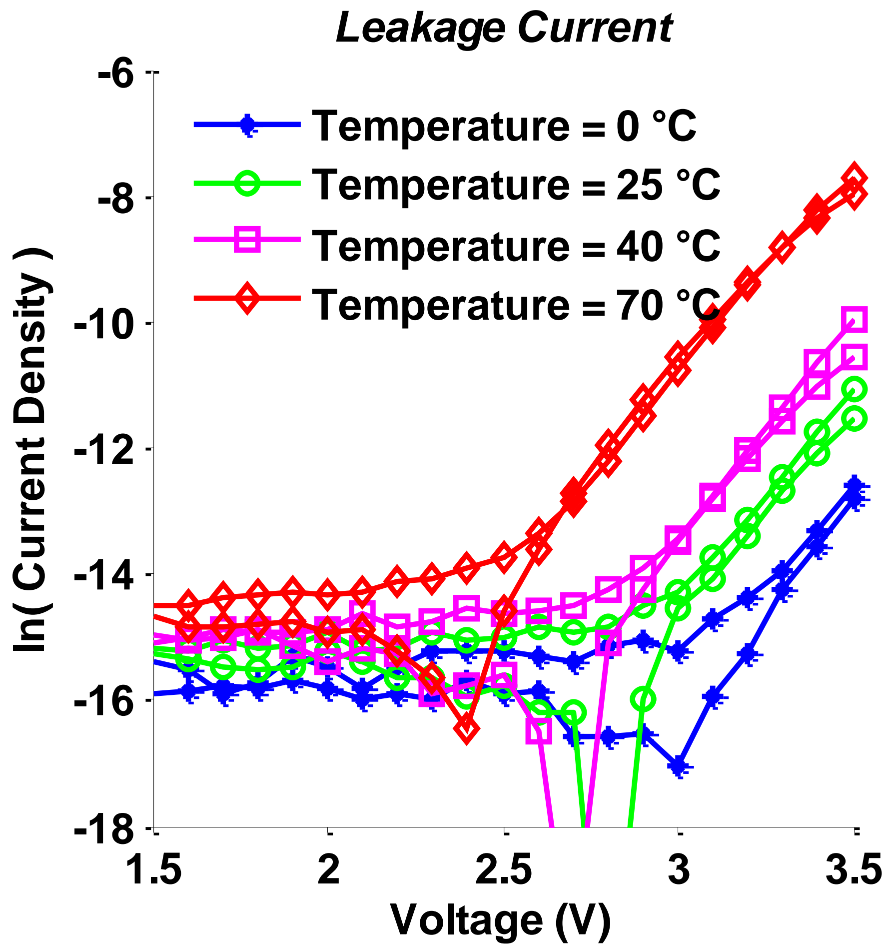

Figure 13: *Logarithmic gate current density versus applied gate voltage at different temperatures.*

As shown in Fig (13) from 1.5 V to 2.5 V, the leakage current stayed constant. The constant leakage current was due to system noise limit. It was observed that after the 2.6 V as the applied bias is increasing the leakage current density through gate oxide is also increasing.

In order to examine responsible degradation mechanism different models were considered by following the theoretical background.

After tunneling through the thinner oxide (Al_2O_3), the electrons have finite probability to being trapped in thicker oxide (HfO_2). High-*k* oxides have more defects than low-*k* oxides such as SiO_2 [1]. An Arrhenius plot is often used to analyze the thermal effects on the emission rate of electrons from traps. Equation (10) describes the slope of logarithmic plot of *J/V* versus inverse of *kT* known as activation energy [11].

$$Activation\ energy = \frac{ln[J/V]}{1/kT} \tag{10}$$

Fig (14) shows that the leakage current density was increasing at high temperature which suggested the thermal nature of emission of electrons from the traps. This might be due to Poole Frenkel or Schottky emission (Equation 8 & 9). But at the lowest temperature 273K the leakage current was not fitting with linear models. It was also observed that at lowest temperature deviation from the linear model was increasing as applied bias is increasing. Therefore it was suggested that at higher temperature the electrons have more probability to escape from the traps than tunneling through the remaining part of HfO_2 while at lowest temperature, might be some tunneling was involved.

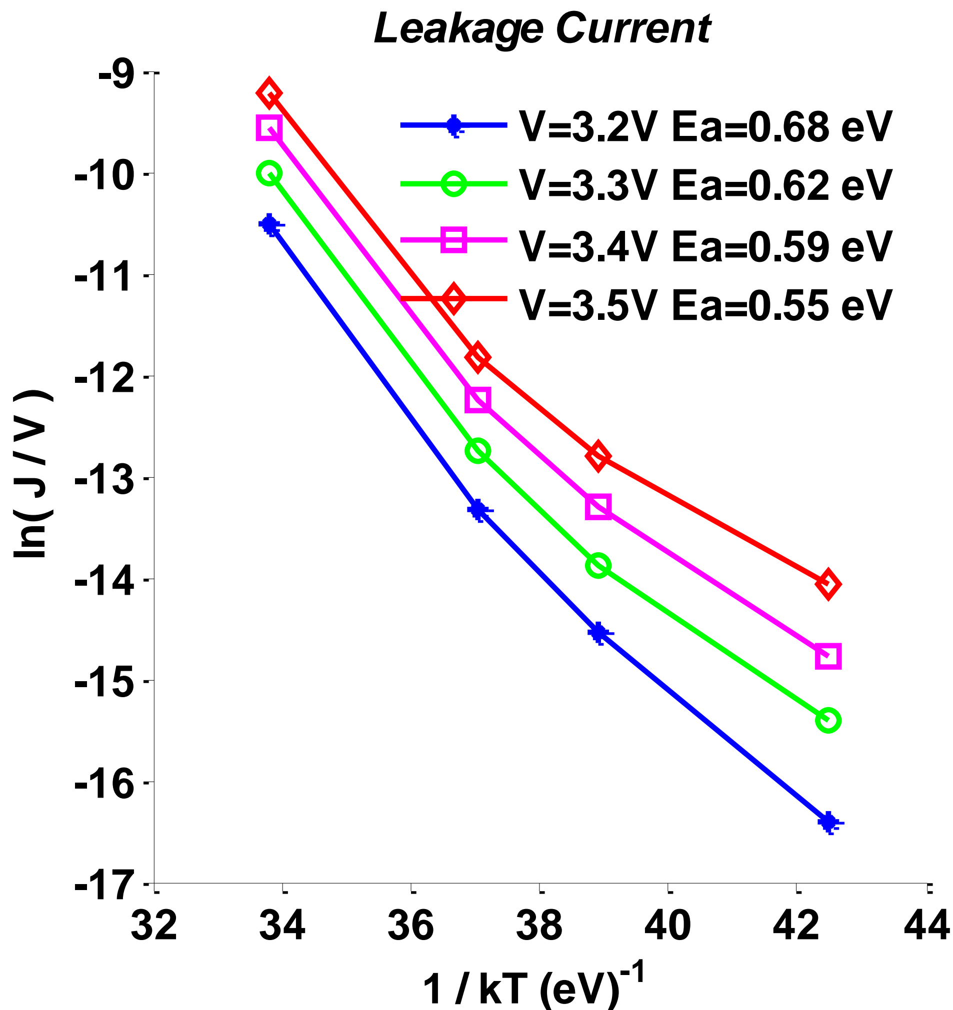

Figure 14: *Arrhenius plot shows thermal dependence of leakage current at higher temperature.*

Fig (15) describe that extracted activation energy was decreasing as the applied bias is increasing which suggest the electric field dependence. Under the high electric field the barrier height of trap-well is reduced. Therefore at high biases trapped electrons need less energy to become free than at lower bias.

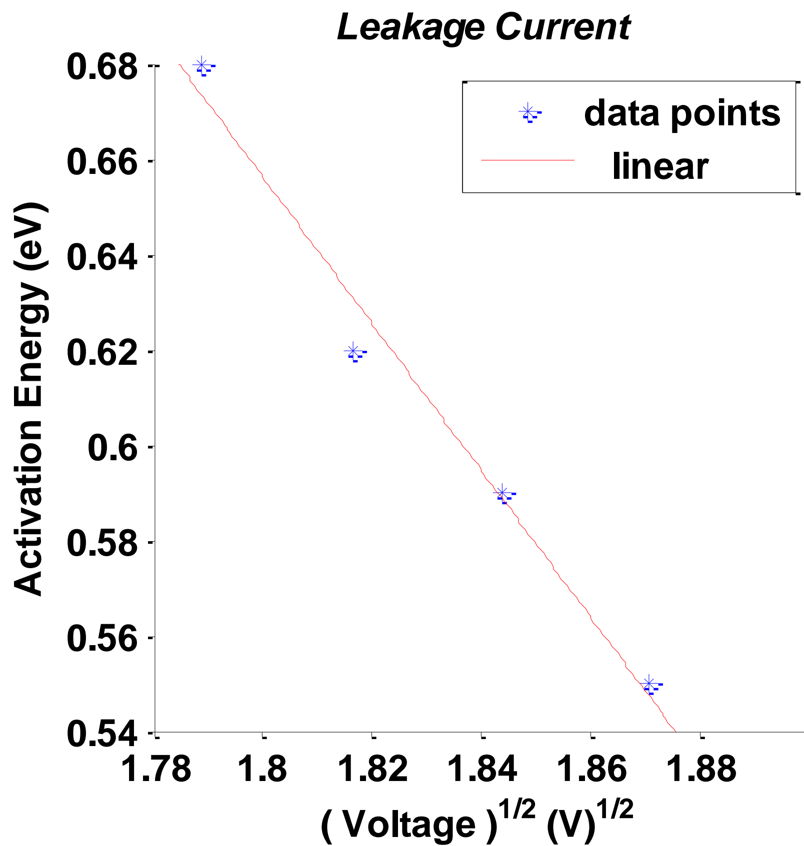

Figure 15: *Activation energy versus square root of applied bias.*

The barrier height of trap corresponding to activation energy was determined by extrapolating the square root of applied bias as shown in Fig (16).

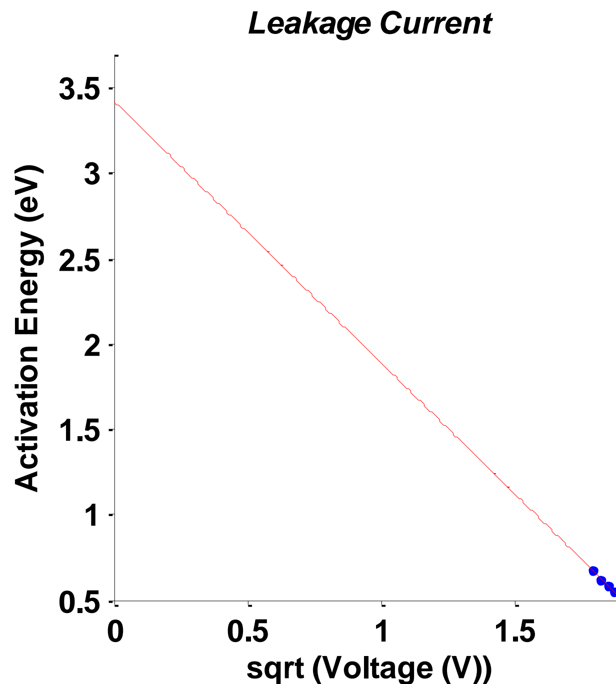

Figure 16: *Extrapolation of square root of applied bias at zero voltage represents the energy of trap.*

The measured activation energy was higher than the theoretical values of Poole Frenkel and Schottky emission. It seems that experimental data was not fitted with Poole Frenkel neither with Schottky emission. The generation was also not fitted because the band of gap of InGaAs is only 0.74 eV. One possible suggestion is that might be some hole current is also involved.

Under high applied bias band to band tunneling was considered to evaluate the corresponding leakage mechanism at lower temperature (0 °C). Fig (17) shows the leakage current density over the square of applied gate voltage versus the inverse of applied gate voltage (equation 6 & 7). Experimental data showed that leakage current density increases under the high electric filed across the oxide.

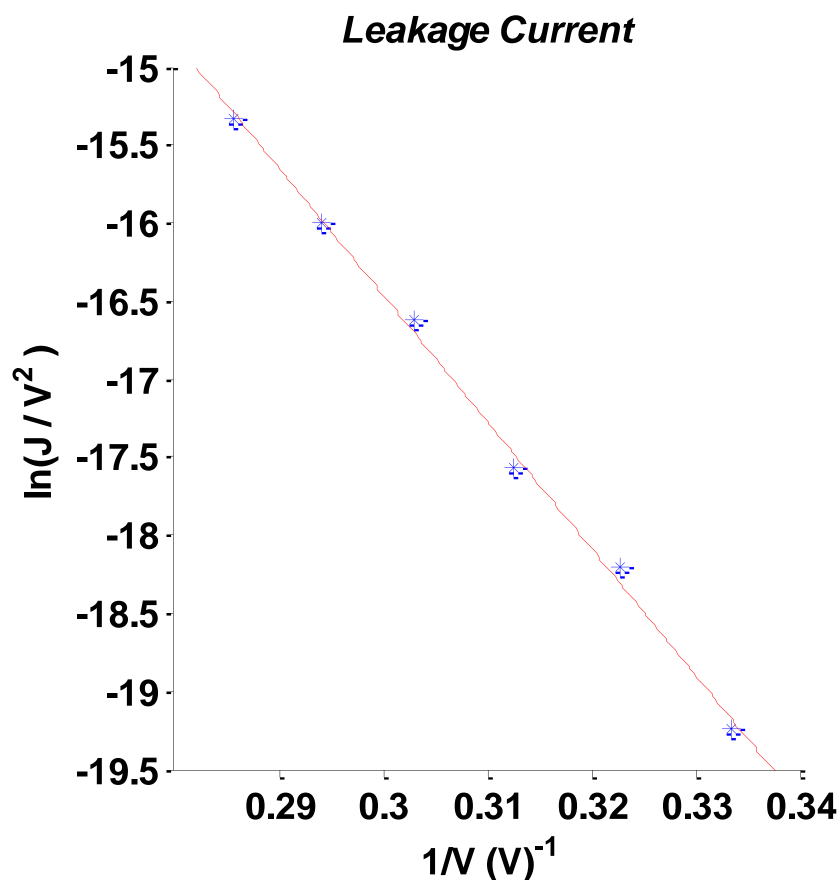

Figure 17: *Band to band tunneling plot through Al_2O_3/HfO_2 film at 0 °C*

The observed leakage current was due to the tunneling of electrons which could be direct tunneling or Fowler Nordheim tunneling depending on the oxide thickness and voltage drop across the oxide. The electric field across the Al_2O_3 was more than electric field across the HfO_2 due to effect of different dielectric constants. The high voltage drop across thinner oxide (Al_2O_3) results in more electrons tunneled through oxide and having less possibility of being trapped in thinner oxide. Since the thickness of Al_2O_3 was 0.5 nm, the leakage current through Al_2O_3 was due to direct tunneling. The linearity at high bias the leakage current is due to the band to band tunneling mechanism.

4.2 Stress induced leakage current (SILC)

To investigate the reliability of stack Al_2O_3/HfO_2 with InGaAs electrical properties were observed under the constant voltage stress (CVS). Fig (18) represents the measurement scheme under constant voltage stress (4.5V) with periodic interruption from 0 V to 3 V to monitor the oxide degradation.

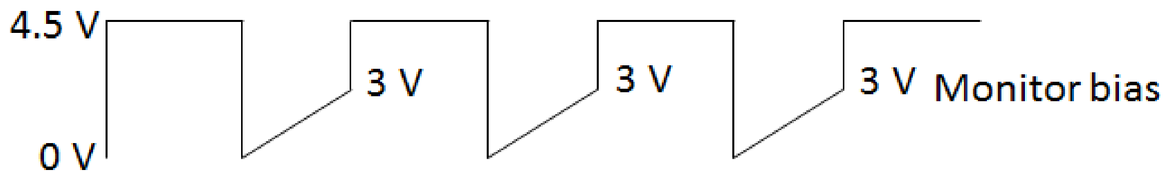

Figure 18: *Measurement scheme to investigate the oxide degradation under 4.5 V constant voltage stress with perodic interuption from 0 V to 3 V.*

One of the major reliability issues of nano technology is the stress induced leakage current (SILC). It can be observed at low stress voltages due to defects generation or charge trapping. Usually SILC comes before the onset of soft or hard breakdown of oxide.

Fig (19) shows the raw data of SILC under the constant voltage stress (4.5V). To characterize the damage across oxide measurements were interrupted from 0 V to 3 V for every 30 s.

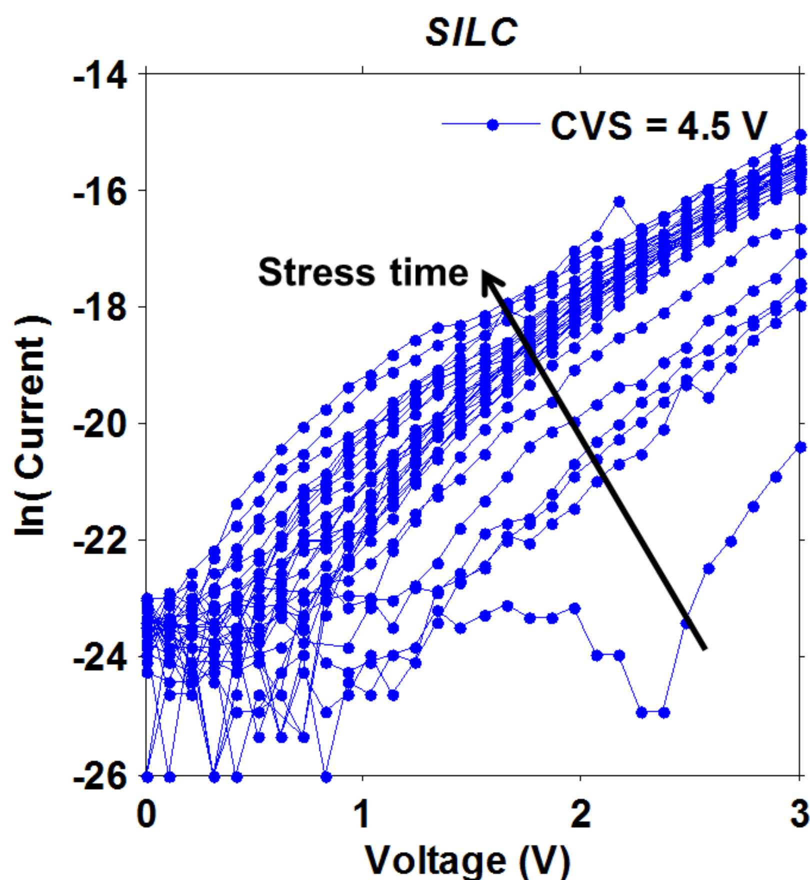

Figure 19: *The stress induced leakage current increases as applied stress is increasing.*

In the interval 0 V to 0.5 V applied bias mainly nosie was observed. Above 0.5 V applied bias leakage current was increasing gradually due to generation of new traps. It was also observed that leakage current was increasing as stress time was increasing even at same applied bias. Therefore damage across the oxide increases with stress time.

Fig (20) represents the logarithmic current thorugh gate oxide as function of stress time. Stress induced leakage current was observed from 0 s sec to 200 s. Atfer 200 s leakage current was staurated due to high damage across the oxide. Therefore no more new defetcs was created and fluctuation of the carriers due to trapping and detrapping indicates the soft breakdown which is less destructive than the hard breakdown.

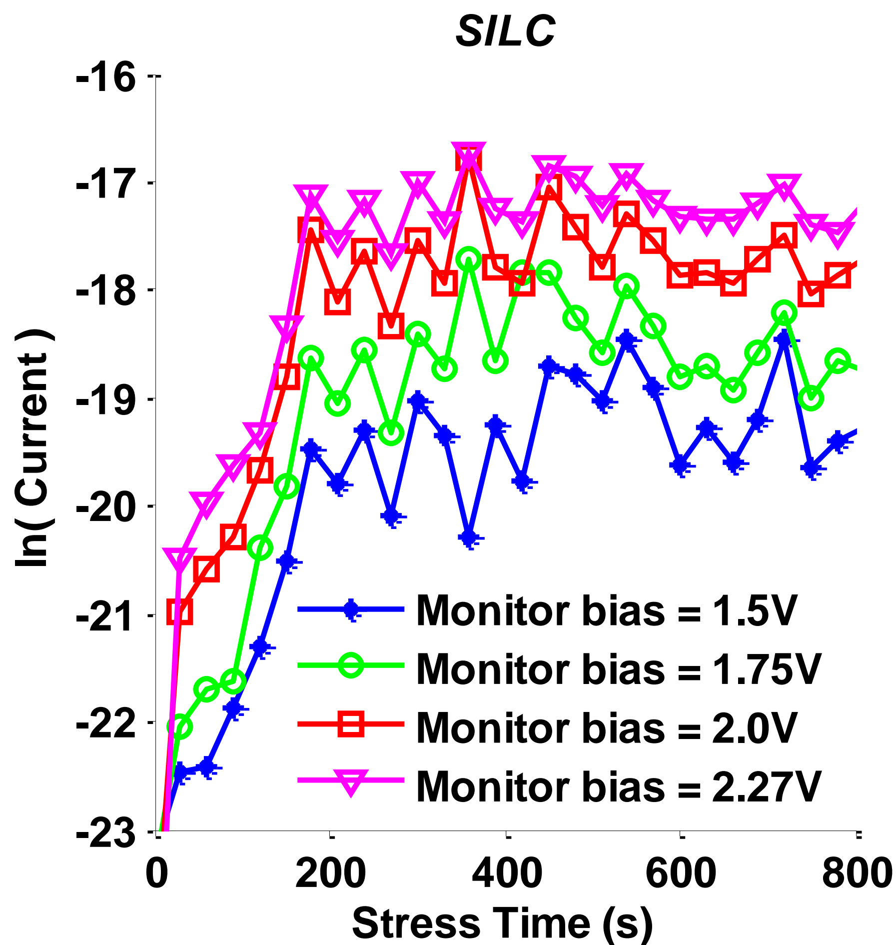

Figure 20: *SILC increases gradually up to 200 s and then saturates.*

4.3 Time to breakdown

Constant voltage stress is a measurement technique to investigate the dielectric strength in terms of time to breakdown (t_{bd}). The gate current has been monitored under the constant voltage stress. The variation in gate current reflects the damage across the oxide due to trapping of electrons and holes as shown in Fig (21)

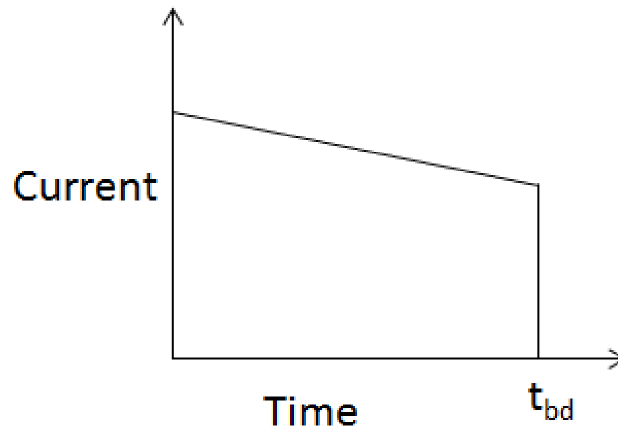

Figure 21: *Under CVS gate leakage current was decreasing due to trapping of carriers until breakdown has occurred.*

Fig (22) represents the time to breakdown under the CVS. To examine the breakdown across the oxide we have measured the gate current on 30 devices as function of time to breakdown. The constant voltage stresses 4.5 V, 4.75 V and 5 V was applied on 10-dices each to measure the average time to breakdown. The extracted average breakdown time for 4.5 V, 4.75 V and 5 V is shown in table (2).

Table 2: *Represents the average time to breakdown under the CVS stress with estimated uncertainty.*

Applied stress	Average time to breakdown	Estimated uncertainty
4.5 V	613 sec	± 55.8 sec
4.75 V	165 sec	± 11.8 sec
5 V	58.5 sec	± 92.8 sec

where 55.8 s, 11.8 s and 92.8 s were the uncertainties of time to breakdown for 4.5 V, 4.75 V and 5 V CVS respectively.

In Fig (22) experimental data showed that time to dielectric breakdown has logarithmic linear dependence with applied voltage stress. A low stress voltage needs longer time to introduce the sufficient damage for breakdown of gate oxide.

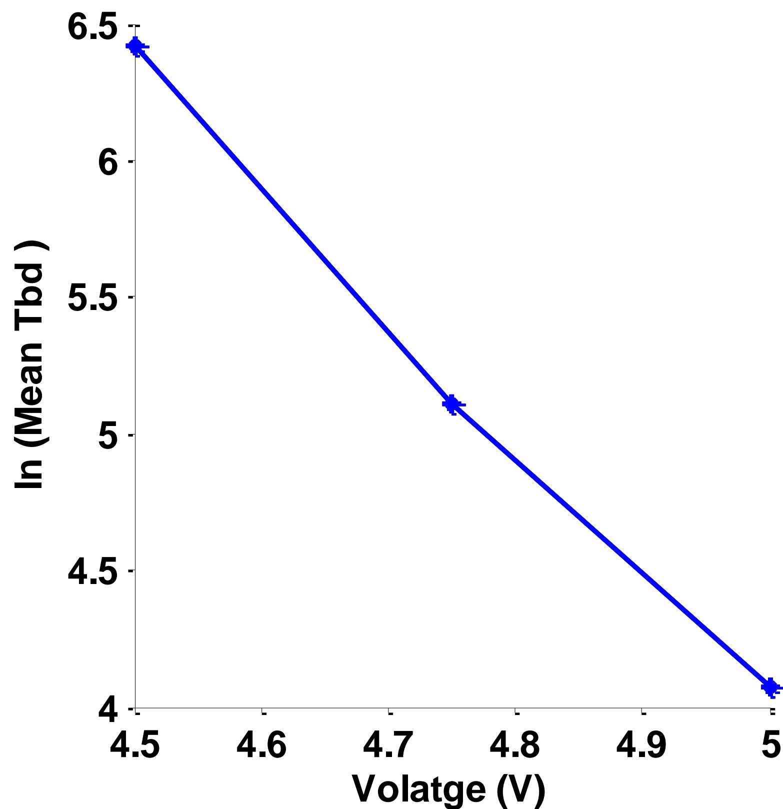

Figure 22: *Representation of logarithmic average time to breakdown as function of applied CVS.*

4.4 Breakdown voltage

The purpose of ramped voltage stress measurements was to evaluate breakdown voltage instantly. Breakdown voltage was the point at which high-*k* (Al_2O/HfO_2) showed conducting behavior under the applied the stress voltage.

Ramped voltage stress (RVS) is a time saving technique to measure the breakdown statistics. In this method current was measured across the oxide as function of applied gate voltage. To measure the average breakdown, measurements were taken on 10-dices under positive applied bias and 20-devices under negative applied bias. It was observed that as the applied voltage was sweeping from 0 V to several volts, the electric field was increasing across the oxide.

Fig (23) shows the experimental result of the breakdown voltage measurements. Under positive applied bias 0 V to 2.8 V, the leakage current was increasing very slowly due to trap assisted tunneling. Above the 2.8 V leakage current was increasing due to band to band tunneling or might be some overlying mechanism was involved. At higher biases leakage current was also influenced by increasing amount of traps. When density of traps was reached at critical value then traps made a direct conducting path from anode to cathode by

overlapping each other. When the conduction path has formed the high-*k* oxide completely lost its insulting properties.

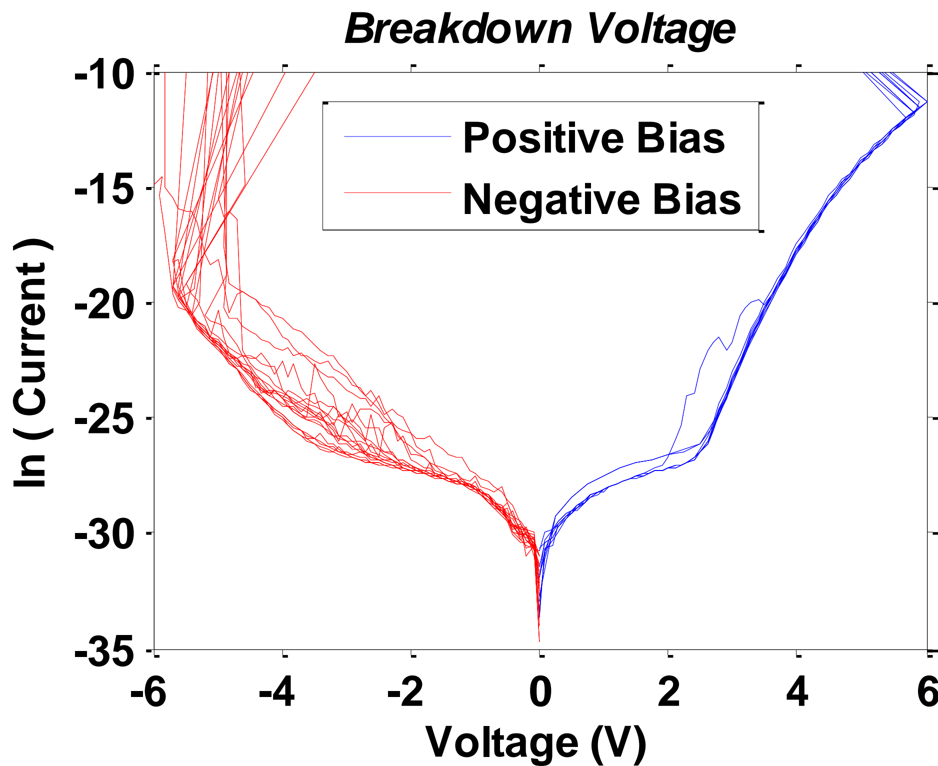

Figure 23: *Logarithmic current versus applied gate voltage showed the breakdown voltage under the positive and negative applied bias.*

At 5.87 V the current jumped to high level and passed a pre-set current limit (1mA) and that was the breakdown point. Therefore 5.87 V ± 0.13 V was the average breakdown voltage for 10-dices under positive bias, where 0.13 V was the estimated uncertainty.

Fig (24) represents band diagram at positive applied bias 5.87 V. Breakdown field for HfO_2 was 9.5 MV/cm with oxide thickness 4.5 nm and for Al_2O_3 26.4 MV/cm with oxide thickness 0.5 nm.

Figure 24: *Under positive applied bias electrons are injecting from substrate to high-k.*

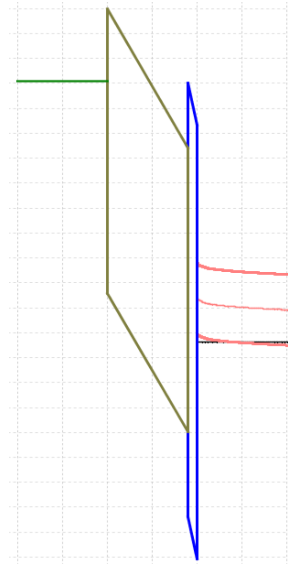

Figure 25: *Under negative applied bias electrons are injecting from metal to high-k.*

Fig (25) represents band diagram under the negative applied bias. At sufficient negative bias the high-*k* (Al_2O_3 & HfO_2) oxide lost the conducting behavior. Therefore under negative bias 5.22 V ± 1.38 V was the measured average breakdown voltage for 20-dices with uncertainty 1.38 V. The observed average breakdown voltage under the negative bias was lower than under the positive bias. At -5.22 V the measured breakdown field for HfO_2 was 6.1 MV/cm with oxide thickness 4.5 nm and for Al_2O_3 17.2 MV/cm with oxide thickness 0.5 nm.

Summary

The processed structure is schematically shown in Fig (26). HfO_2 and Al_2O_3 were grown on InGaAs substrate by atomic layer deposition with oxide thickness 4.5 nm and 0.5 nm respectively. Titanium with thickness 1 nm and gold with 2000 nm was deposited by evaporator. After the lift-off post metallization annealing was used to reduce the interface trap density.

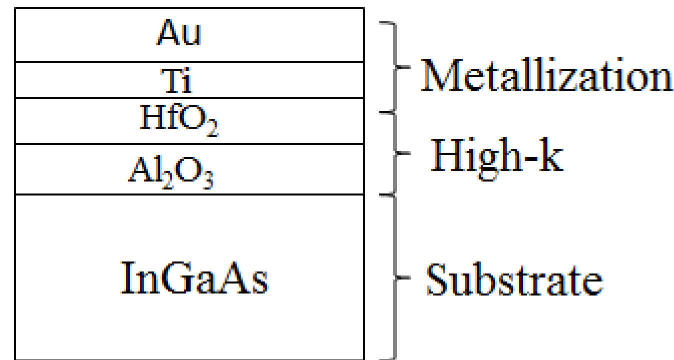

Figure 26: *Structure of MOS capacitor, n-type InGaAs has epitaxially grown on the InP substrate, high-k films by atomic layer deposition and metallization by evaporator.*

In this project we have characterized the gate stack Al_2O_3/HfO_2 on InGaAs substrate to investigate the conduction mechanism, stress induced leakage current and soft & hard breakdown. The leakage current was measured at different temperatures and biases to examine their dominant dependence. Under the high positive applied bias the observed leakage current was due to band to band tunneling at lower temperature. At higher temperature the leakage current was strongly dependent on the temperature. The measured activation energy was higher than the theoretical values of Poole Frenkel model and Schottky model. The stress induced leakage current was measured at 4.5 V constant voltage stress with periodic interruption to observe the damage across the oxide. Under the constant voltage stress initially stress induced leakage current was increased due to generation of new defects. Once high damage formed across the oxide, SILC was saturated which indicates the soft breakdown. The time to breakdown was measured under different constant voltage stresses. The ramped voltage stress technique was used to investigate the breakdown field for Al_2O_3 and HfO_2.

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