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Industrial Electrical Engineering and Automation

High Voltage Pulsed Power Converters for the ESS Linear Accelerator

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Abstract

Material science has become an important research area in order to fulfill today's requirements on lighter, cheaper and more sustainable materials. The European spallation source is a research center based on the world's most powerful neutron source, which will enable new possibilities to evaluate material properties down to an atomic level. The linear accelerator (Linac), accelerates with help of electromagnetic fields, protons to a speed of 96.2 % of the light. Due to high power and the pulsing nature of the accelerator an extremely advanced electrical supply is required. This master´s thesis comprises a concept topology for solving the impact of such pulsed power supplies on the AC grid power quality.

The electrical supply consists of two series connected stages, which will be stacked in modulators. The first stage is a low voltage grid connected capacitor bank charger, the second stage converts the power to a high voltage pulsing pattern. This project comprises the first stage (the capacitor charger) which consists of an Active Front End in series with a DC/DC-converter. The main objectives are to fulfil the international standards regarding power quality, where main focus will be on flicker, low frequency harmonics emission and unitary power factor. In order to fulfill these goals with pulsating loads connected, a completely new developed power control introduced. Mathematical models have been derived in order to verify the functionality and to tune all the developed controls. A complete final implementation is done with the help of Matlab Simulink to more in-depth verify the different control parameters. This implementation is also used to check that the international standards are met. Complete calculations of power losses are also presented with evaluation of results and possible improvements.

Together with the limitations, goals of the degree project and basic equations are derived in this report. The topology is shown to be extremely effective with very good results in terms of output voltage quality (capacitor charging voltage) and on flicker and low frequency harmonics impact on the grid. Almost every effects due to the pulsing output nature are totally erased seen from the grid side.

Acknowledgments

During the thesis there has been a couple of persons encouraging, helping with constructive inputs and making this master thesis possible that deserves a special thanks.

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Table of Contents

CHAPTER 1

1 Introduction

1.1 The European Spallation Source

The European Spallation Source (ESS) is an international research institution built by at least 17 European countries, with Sweden and Denmark as host nations. It will be located in Lund, Sweden, where it will be a research center based on the world's most powerful neutron source [1]. The project will enable new opportunities for improving material science research with positive impact on our everyday lives. With today's new requirements on lighter, cheaper and environmentally sustainable materials, the research has to go down to atomic levels in order to study the materials properties. This becomes possible with neutron research so that material science can develop and improve all the thousand products that are used in people's life [2].

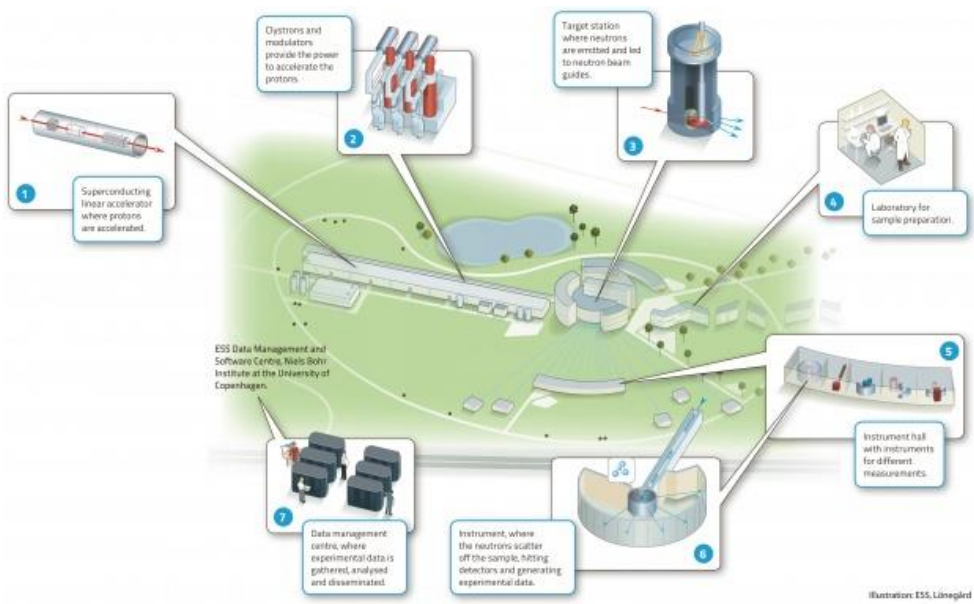

Figure 1.1: An illustrative picture of ESS research facility together with the accelerator and its main components [3].

ESS will also be the first sustainable research facility in the world, It will set a new standard for large scale research facilities and put Europe in the lead of sustainable development. Four key concepts will ensure ESS to be carbon dioxide neutral:

Responsible – Requires that the facility uses as little energy as possible.

Renewable – Requires that all energy must derive from renewable sources.

Recyclable – Requires that as much surplus heat as possible is recycled.

Reliable – Critical systems like the cooling and power systems must be reliable to secure the facility's operational availability for the researchers. [4]

1.2 The accelerator and how it works

The ESS research facility is designed around a linear proton accelerator (Linac), Figure 1.2. With a peak power of over 100 MW, pulse length of 2.86 ms and a repetition rate of 14 Hz it will be the most powerful neutron source worldwide [5]. The principle for the accelerator is as following; by heating hydrogen gas with rapidly varying electromagnetic fields at the ion source and striping the plasma from electrons, protons are created. From the ion source protons are guided under vacuum by beam pipes and accelerating structures into the accelerator beam line. The accelerating structures are also distributed along the Linac and accelerate the protons forward with electromagnetic fields. At the first approximately 50 meters protons travel at low speed in order to properly guide and focus the beam with magnets around the beam pipes. After that, superconductive cavities accelerate the protons to 96.2 % of the speed of light before they hit the target. At the target, neutrons will be created by a spallation process and detected at the experimental stations [6].

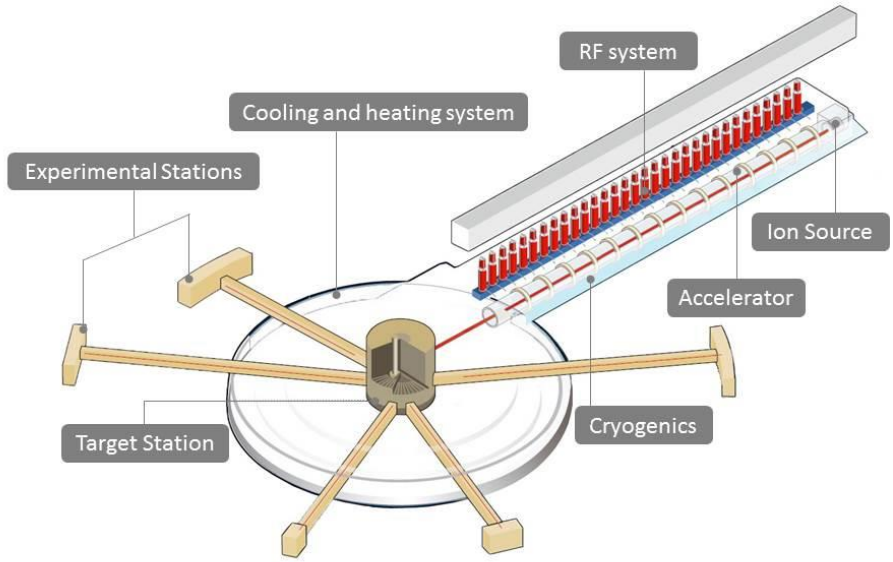

Figure 1.2: Illustrative picture showing the accelerator concept with its main components [7]

1.2.1 Ion source

Hydrogen gas is lead in to the ion source, where the hydrogen is turned into plasma by heating up the gas with rapidly varying electromagnetic fields. The plasma is stripped of its electrons, leaving the protons which are injected into the accelerator [7].

1.2.2 Accelerator

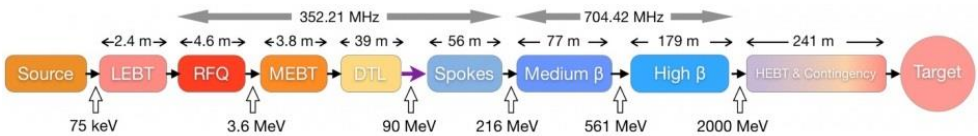

Figure 1.3: The ESS accelerator overview with its main stages [8].

In the accelerator protons pass through a large number of cavities. The first cavities are the Low Energy Beam transport (LEBT) section and the Radio Frequency Quadrupole (RFQ) where the beam of protons is bunched and accelerated up to 3.6 MeV. At the Medium Beam Transport (MEBT)

section is the beam characteristics diagnosed and optimized for further acceleration in the Drift Tube Linac (DLT). After this there are 26 spoke cavities followed up by 36 Medium Beta Linac and 87 High Beta Linac that are superconducting and accelerates the protons up to 2000 MeV [9]. After the high beta section the proton beam will have an average power of 5 MW and a diameter of about 2 mm. The beam is then transferred through the superconducting High Energy Beam Transport (HEBT) section and will after this section hit the target. At the target, protons have a speed up to 96.2% of the light when it hits the tungsten [10].

1.2.3 Cryogenics

Cryogenics is the science and technology of phenomena below a temperature of 120 K [11]. The cavities are superconducting because of the high currents required to generate the magnetic and electrical fields. In order to reach this phenomena, liquid helium is used as cooling, which cools the cavities down to a temperature near the absolute zero. This will reduce the power consumption of the accelerator drastically [7].

1.2.4 Target station

The target station is the facility where the high-energy neutrons are released when the protons hit the tungsten target. The collision of tungsten nuclei and the protons will scatter or throw off a collection of neutrons that are assembled into beams directed to the experimental stations [12].

1.2.5 Experimental stations

The assembled high-energy beams with neutrons are directed to the experimental stations, where the material sample is investigated. Each station is uniquely calibrated for particular scientific studies [7].

1.2.6 Cooling and heating system

The cooling system is another large part of the accelerator and the target. In order to optimize the heat recovery efficiency, parts of the accelerator operate at three different temperature levels, 20˚C, 40˚C and 80˚C. The chosen cooling temperature is dependent on the maximum operating temperature level for the components. This will require complex cooling systems and well dimensioned heat exchangers. Due to the recyclable target in ESS key concepts the estimated 200GWh of surplus energy also needs to be taken care of [13].

1.2.7 RF system

In order to generate the electromagnetic fields in the cavities for beam acceleration, radio frequency (RF) power source are required. The radio frequency system converts AC grid power to RF power at either 352 or 704 MHz, which is the required frequency for different sections of the accelerator [14]. In order to supply the accelerator with an average power of 5 MW, 4 % of duty cycle and a repetition rate of 14 Hz the RF system must supply over 123 MW in peak power [15].

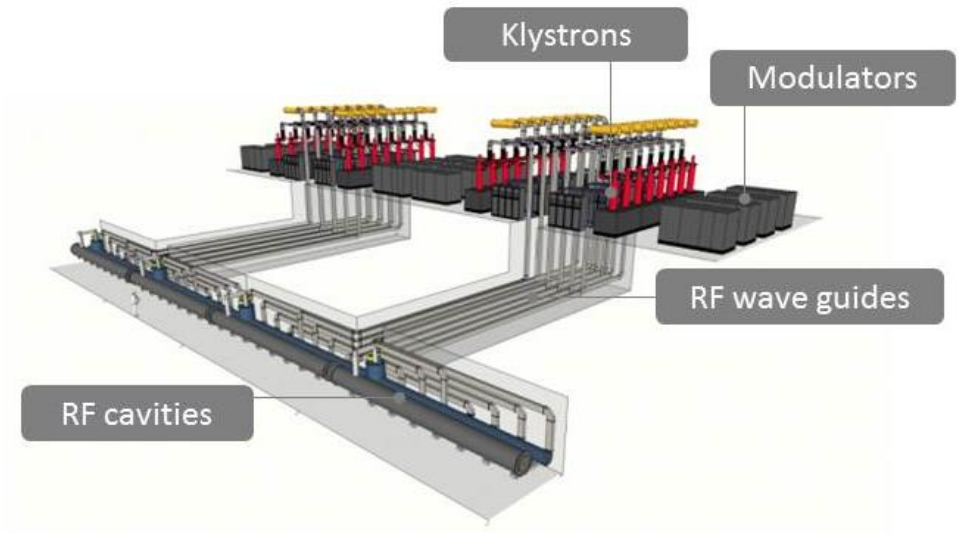

Figure 1.4: Illustrative picture of the RF sources together with its main components [16].

1.2.7.1 Modulators

The modulators are electrical power converters that transform the AC power from the low voltage grid into high voltage pulse power that supplies the klystrons. The modulators will consist of two parts, where the first part is connected to the grid and charges capacitor banks at low voltage. The second part transforms the low voltage DC power from the capacitor banks into 3.5 ms long pulses at high voltage (~100 kV) that supplies the klystrons [14, 15].

1.2.7.2 Klystrons

The klystrons convert electrical power into RF power. A low power signal generator generates RF signals at a frequency of 704.42 MHz or 352.21

MHz, which amplifies the RF signal to the cavities [15]. The modulators supply the klystrons with electrical power.

1.2.7.3 RF wave guides

The RF wave guides are conduits that transmit and guide RF power from the Klystrons to the RF cavities [15].

1.2.7.4 RF cavities

The RF cavities generate magnetic and electrical fields that accelerate and guide the beam. In order to generate the electrical and magnetic field the RF cavities are supplied with RF power from the klystrons [15].

1.3 Project overview

The RF power sources will require several high precision high voltage power modulators rated for peak voltages and currents of 115 kV and 100 A. These will work under a pulsing nature with a pulse length of 3,5 ms and a repetition rate of 14 Hz. The project comprises the first part of these converters, which is the part between the AC-grid and the capacitance bank. Because of the connection to the low voltage AC-grid and the high power pulsing nature of the accelerator, the converter topology together with the control loops need to be designed and dimensioned in such a way that international standards on power quality are met. With the chosen topology, see Figure 1.5, using advanced control loops, a flicker-free and sinusoidal current absorption connection with unitary power factor is made possible. The approach will also have a high efficiency and a modular based parallel formation, which will make a hypothetical expansion easily managed. Because of the low voltage connection and operation, all the components of this power conversion stage can be chosen from the conventional market and the structure will not require inclusion in oil tanks for insulation reasons [17] [15].

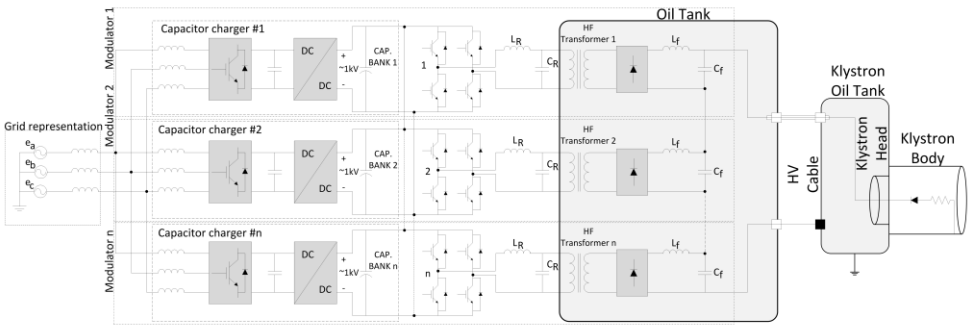

Figure 1.5: Block diagram of the new modulator concept.

The concept (Figure 1.5) is that several modules are stacked, which will decrease the power transferred through a single system. It's possible to have n modules in parallel, where each of them is phase shifted in terms of switching to reduce the harmonics and interferes in the system. The first step of the modulator consists of a grid connected capacitor charger, where an AFE and a DC/DC step down converter control the voltage with high precision over the capacitor bank. After the capacitor bank an H-bridge converts the DC-voltage into a high frequency (~15 kHz), three level AC square wave. The high frequency transformer submerged in an oil tank transforms the voltage in a one to one relation and provide a galvanic isolation. Because of high frequency, the transformer size is drastically reduced. Before the klystron body the voltage is rectified into pulses and filtered at high voltage in a separate oil tank.

1.4 Goals of the degree project

The main objectives of this Master of Science project are:

- In depth study and mathematically derive analytical modeling of an AFE and a DC/DC step down converter as a capacitor bank charger.
- Develop control/regulation loops for the AFE with the following specifications:
    - The current absorbed from the grid shall be sinusoidal.
    - The reactive power absorbed from the grid shall be reduced in order to minimize the power quality impact, particularly the flicker
    - The DC-link voltage shall be constant according to a specified level.
- Develop control/regulation loop for the DC/DC step down converter with the following specifications:

    - The power drawn from the DC-link shall be constant when pulsing, therefore investigating flicker problem in the AC-network.
    - The output voltage over the capacitance bank shall according to the specification have reached the given level before the next pulse arrives.
- Find optimal parameters for the controller/control loops at different power modes.
- Dimension the system and find optimal parameters for all the components including the output capacitance bank at the DC/DC converter.
- Derive mathematical expressions and calculate power losses for the AFE and the DC/DC step down converter. Compare losses at different switching frequencies and different power modes.
- Simulate the full system and verify that the different control algorithms work as expected. The performance with respect to the requirements from the IEC, international standards on flicker and low frequency harmonics emission shall also be verified according to the IEC 61000-3-3 and ICE 61000-3-2.

1.5 Limitations

Since the time scope for the thesis is limited, focus has mainly been on simulating one of the three parallel connected capacitor chargers in the modulators in Figure 1.5. Practical implementation possibilities have not been evaluated but a discussion of possible ways will be included in further work subchapter. Due to a well establishment of Matlab/Simulink at the university the simulations are developed on this platform, where SimPowerSys is used for modeling the electric circuit. Implementation in other software packages such as MathCad, SABER, LTSpice, etc. has not been evaluated. The simulated models are ideal in terms of noise and losses, active components are considered ideal as well and nonlinearities are not included.
In terms of control has main focus been on steady state operation of the capacitor charger. Limited number of control possibilities are evaluated, this because of strict requirements in terms of harmonics, flicker, constant active power and high precision. The final thesis will include one control methodology that will be evaluated in depth for AFE and two methods for the DC/DC-converter. Optimization of parameters, dimensioning and losses will be done for three different power levels.

CHAPTER 2

2 Power converters basic theory

Power electronic converters are a modern technology in comparison to the conventional electrical theory that was mostly discovered in the 19th century. In the early 20th century, electricity was considered as luxury, today it is more considered as something important that is necessary for a global development and is used in almost every household.

Electric energy is nowadays converted to and from other energy sources in many situations. The development of power electronics, as from the 60's, has deeply contributed to advancement of electric energy conversion according to the needs of different loads and applications. A key element of modern switch-mode power electronics is the power semiconductors that form the switching cells and allow for regulation of electrical variations and power flow. Examples of such semiconductors are diodes, transistors and thyristors in various configurations. The typical form of electricity is a DC or an AC, with for example a frequency of 50 Hz and 400 V in the Swedish electrical grid. With help of power electronics this type of electric energy can be transformed to the required specification for controlling motors, power supplies, CFL (Compact Fluorescent Lights) or modulators to a Linear Particle Accelerator (LPA) as in this case [18, 19]. Regarding efficiency, the power electronic structure allows up to 99 % in extremely good cases [20].

In this chapter the main components and general calculations for behavior of power converters is described. The configuration of PE can vary a lot but in this part the focus will mainly be on the basics of components and functions that are chosen for this application. Fundamental control, power losses calculation and dimensioning theory will also be presented.

2.1 Switching basics

The principle in PE is built on switching. In a discrete environment with fast switching between different states the desired output can be obtained, after filtering the harmonics. The switching semiconductor that is mainly used for these applications can alter between two states – "on and off", but also vary between many more states in a constellation in sub-converters (multi-level converters; interleaved converters). Switching structure is built on a triangular carrier wave in comparison with a reference signal. The outcome of this is a modulation wave that is in average the wanted quantity. In a switching circuit everything needs to be considered in average, but with a high switching frequency it can in some cases be deliberated as continuous. Due to the switching a lot of harmonics is created that always needs to be under consideration. In Figure 2.1, a switching example during a couple of micro-cycles is illustrated [19].

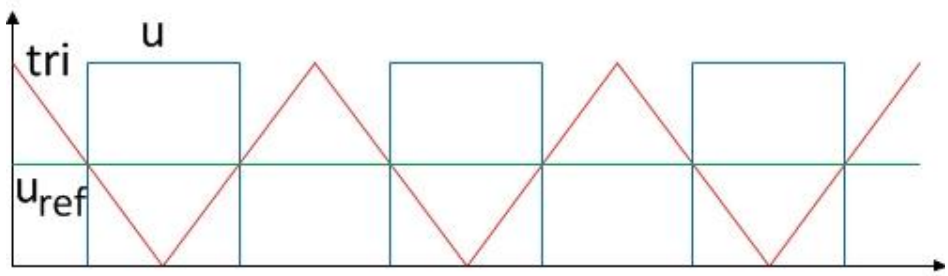

Figure 2.1: Triangular wave (red) interacts with the reference signal (green) creating the PWM (blue).

2.2 Power electronic components

In case of a PE solution there is demands in switching between different states or levels of voltage. This is made possible with active semiconductor elements such as transistors and diodes.

2.2.1 The IGBT

A transistor optimized for PE can switch up to several kV and conducting a high current up to several kA without demanding too much supplied current on the gate is called IGBT. This transistor has the characteristic and efficiency of a FET-transistor on the gate and the characteristics of BJT between collector and emitter which allows high power conduction. The IGBT is constructed to work under extreme conditions with currents and voltages up to 1 200 A and 3 000 V respectively and switching time under 1 microsecond. When the IGBT is conducting there is a small voltage drop

between collector and emitter and when it's not conducting there are small leakage currents that are considered negligible [19]. In Figure 2.2 the symbol and indications for an IGBT is presented.

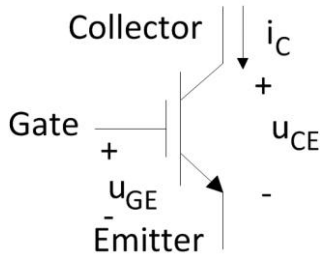

Figure 2.2: Structure of an IGBT.

2.2.2 The diode

The diode required in PE is a fast switching type for high frequencies, rated for high levels of current and voltages (up to several kV, kA). When the diode is forward biased there is a small voltage drop proportional to the current. In the case of reversed biased diode the conduction is almost totally blocked and the leakage current is negligible [19]. In Figure 2.3 the symbol for a diode is presented. The main challenge in the construction of such diodes is in obtaining fast reverse recovery time (passage from conduction to blocking stage), therefore minimizing the power losses due to recovery energy.

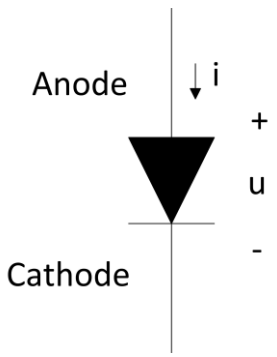

Figure 2.3: Structure of a diode.

2.3 Basic PE – The buck converter

The Buck converter is a traditional DC/DC step down converter. With a steady DC-voltage provided on the input side, a switched voltage is

generated on the output. By controlling the transistor in a specific way and creating a PWM-square wave, the average output voltage is proportional to the desired reference.

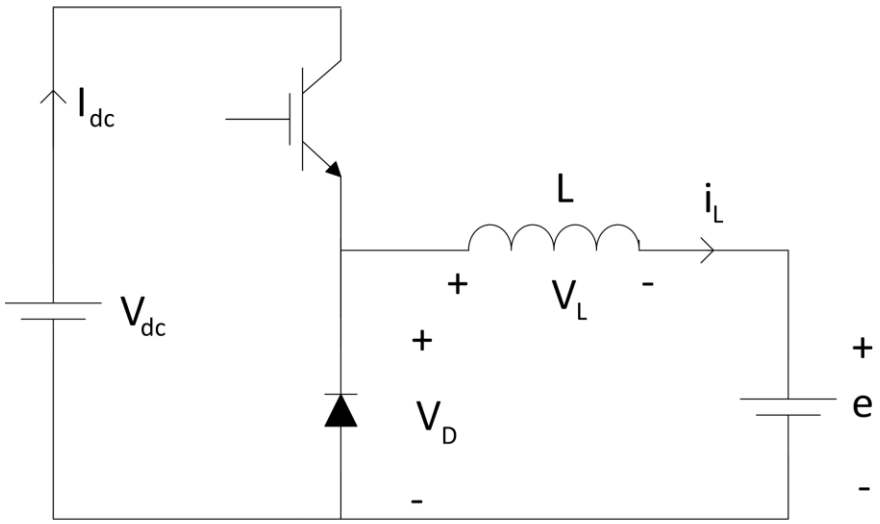

Figure 2.4: Basic schematic of a conventional buck-converter.

With usage of the circuit in Figure 2.4 the output voltage will look as in Figure 2.5. Definition of the duty-cycle is expressed by (2.1). This duty-cycle corresponds to the ratio between time of conduction for the transistor in respect to the switching time.

$$D = \frac{V_{avg}}{V_{dc}} = \frac{t_p}{T} \tag{2.1}$$

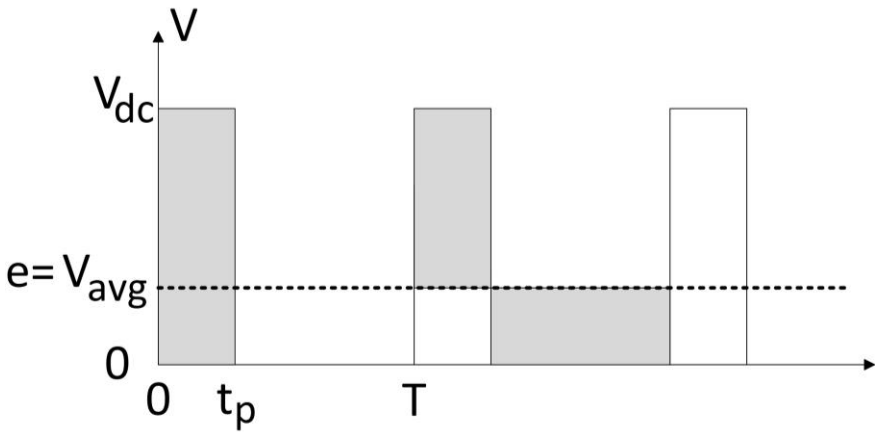

Figure 2.5: Waveform of output voltage from a buck-converter with its average voltage as dashed line.

2.4 Estimation of converter losses

The power losses in semiconductors are derived in two parts; one for the conduction losses and one for the switching losses. Losses due to blocking-state are negligible.

$$E_{T/D}(T_{sw}) = \int_{T_{sw}} p_s(t)dt = E_{T,on}(T_{sw}) + E_{T/D,off}(T_{sw}) + E_{T/D,cond}(T_{sw}) \quad (2.2)$$

Where $E_{T,on}(T_{sw})$ is the required energy for turning on the transistor per switching period, $E_{T/D,off}(T_{sw})$ energy for turning off the transistor and diode per switching period and $E_{T/D,cond}(T_{sw})$ the energy loss during conduction for one switching period. Calculations of the different parts are based on datasheet information for the semiconductors. The specified losses in datasheets are experimentally determined with inductively clamped current and are valid for AFE and DC/DC etc. [18]

2.4.1 Switching losses

Energies for turn-on ($E_{T,on}$) and turn-off ($E_{T/D,off}$) are taken from the datasheet for the respective component. These are provided for a specific test voltage ($V_{DC,n}$) and current ($I_{L,n}$) and depend on rise and fall times. To get the appropriate values they are scaled with the actual voltage (V_{DC}) and

current (I_L). Note that the turn-on energy for the diode is not included because it's very low and therefore considered to be negligible [18].

$$E_{T,on} = \frac{E_{on,n}}{V_{DC,n} \cdot I_{L,n}} \cdot V_{DC} \cdot I_L \tag{2.3}$$

$$E_{T/D,off} = \frac{E_{off,n}}{V_{DC,n} \cdot I_{L,n}} \cdot V_{DC} \cdot I_L \tag{2.4}$$

Considering the energy loss per cycle and switching period (T_{sw}), the average power losses over a switching cycle is calculated.

$$P_{T,on} = \frac{E_{T,on}}{T_{sw}} = \frac{E_{on,n}}{T_{sw}} \cdot \frac{V_{DC} \cdot I_L}{V_{DC,n} \cdot I_{L,n}} \tag{2.5}$$

$$P_{T/D,off} = \frac{E_{T,off}}{T_{sw}} = \frac{E_{off,n}}{T_{sw}} \cdot \frac{V_{DC} \cdot I_L}{V_{DC,n} \cdot I_{L,n}} \tag{2.6}$$

Further analysis will be presented in chapter 3, 4 and 6 for practical calculation.

2.4.2 Conduction losses

For a semiconductor there is a specific conduction IV-characteristic. This characteristic can be linearized in order to obtain the internal voltage drop ($V_{T/D0}$) and the resistance ($R_{T/D}$) for the semiconductor based on values from the datasheet. This approximation is remarkably accurate and often used [18].

$$E_{T/D,cond} = V_{T/D(on)} \cdot I_L \cdot t_{cond} \tag{2.7}$$

$$V_{T/D(on)} = V_{T0/D0} + R_{T/D} \cdot I_L \tag{2.8}$$

With the help of the energy loss per cycle (2.7), forward voltage characteristic (2.8) and switching time (T_{sw}) the average conduction power losses are calculated (2.9).

$$P_{T/D,cond} = \frac{E_{T/D,cond}}{T_{sw}} = V_{T/D(on)} \cdot I_L \cdot D_{T/D} = I_L{}^2 \cdot D_{T/D} \cdot R_{T/D} + I_L \cdot D_{T/D} \cdot V_{T0/D0} \tag{2.9}$$

Where I_L is the conducting current, t_{cond} is the time of conduction and $D_{T/D}$ the duty-cycle.

Further analysis will be presented in chapter 3, 4 and chapter 6 for practical calculation.

2.5 Grid filtering

In an ideal case the grid voltage is expected to be perfectly sinusoidal. Unfortunately this isn't true for the real world. In the real world there is external impact in terms of disturbances creating unwanted harmonics. If a harmonic grid voltage would enter a regulation-loop it may create an unstable system. To prevent this, a low pass filter is often constructed and implemented.

A low pass filter attenuates disturbances with high frequencies. The variable, τ, defines the cut-off frequency (f_c) for the system. Equation (2.10) is an example of a first order low pass filter [21].

$$G(s) = \frac{1}{1 + s\tau}, \qquad f_c = \frac{1}{2\pi\tau} \tag{2.10}$$

This filter affects the phase and amplitude for certain frequencies differently. The Bode diagram shown in Figure 2.6 illustrates this effect.

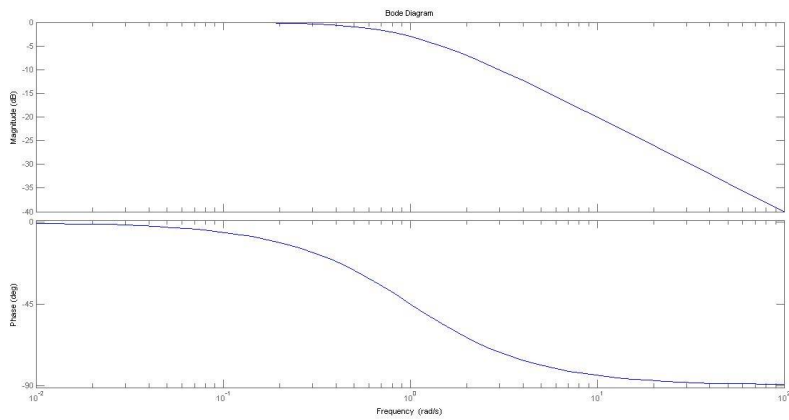

Figure 2.6: Illustration of a Bode amplitude and phase plot with equation (2.10) for τ=1.

When a signal passes through a low pass filter with a certain frequency its affected amplitude and phase can be calculated exactly with mathematical expressions [21].

$$|G(s)| = \frac{1}{\sqrt{1 + (\omega\tau)^2}} \tag{2.11}$$

$$\arg\big(G(s)\big) = -\arctan(\omega\tau) \tag{2.12}$$

2.6 Control

When having a dynamic system with input variables a controller is constructed to manipulate the input so that the output will follow a requested reference. With help of a physical model the nature's behavior can be identified. For electronic purpose, physical models are mainly the basic equations for electronics. The most conventional controller is a PI-controller.

2.6.1 PI-controller

The PI-controller consists of two parts, a proportional and an integral part. Basic structure of the PI-controller that is used to control the system is presented (2.13).

$$G(s) = K \cdot \left(e(s) + \frac{e(s)}{sT_i}\right) \tag{2.13}$$

Where K is the proportional gain, e(s) the error and T_i is the integral gain.

2.6.1.1 P-part

The proportional part of the controller returns a value proportional to the error and an unwanted proportional part produces a stationary error (2.14) [22].

$$e(s) = \frac{(u(s) - u_0(s))}{K} \tag{2.14}$$

Where $u(s)$ is the controller output signal and $u_0(s)$ is the controller output signal with no stationary error.

I-part

The integral part of the controller eliminates the remaining part of the stationary error. By integrating the error it contributes with a value proportional to the magnitude of the error accumulated over time [22].

2.7 Dimensioning of passive components

Electrical circuits constructed needs dimensioning of components to work properly. In this part basic dimensioning of passive components are discussed. Dimensioning is based on the relation between voltage and current for an inductance (2.15) and a capacitance (2.16) [21].

$$v_L = L\frac{di_L}{dt} \tag{2.15}$$

$$i_C = C\frac{dv_c}{dt} \tag{2.16}$$

For a DC/DC step down converter the inductance is dimensioned with a predefined current ripple. With Figure 2.4, (2.15), (2.1) and the approximations $di_L \approx \Delta i_L$, $dt \approx \Delta t$ the formula (2.17) is derived [18].

$$L = \frac{(V_{dc} - e) \cdot D \cdot t_s}{I_{ripple}} \tag{2.17}$$

Where t_s is the switching time of the converter, D the duty cycle and I_{ripple} the current ripple.

In the same way the dimensioning of capacitance with a predefined voltage ripple can be calculated. With Figure 2.4, (2.16), (2.1) and the approximations $dV_c \approx \Delta v_c$, $dt \approx \Delta t$ the formula (2.18) can be derived [18].

$$C = \frac{\bar{I}_0 \cdot (1 - D) \cdot t_s}{V_{drop}} \tag{2.18}$$

Where t_s is the switching time, D the duty cycle, V_{drop} the voltage drop and $\bar{I}_0$ the average current going into the capacitance.

CHAPTER 3

3 Active Front End

The main purpose of the conversion is to transform the source power at the AC side to a controllable DC load power. The traditional way of using diode or a tyristor rectifier for AC to DC conversion induces large current harmonic contents on the grid. Individual current harmonics and Total Harmonic Distortion (THD) may then exceed limits in the international standards regarding EMC and power quality. A possible solution to reduce the harmonics is to introduce passive components such as inductors and capacitors in conjunction with the rectifier. But with these components come cost, size and other disadvantages. Another way of improving the waveforms is to use an AFE, a traditionally diode rectifier together with an IGBT placed in parallel with each diode (see Figure 3.1). The power quality is improved and the current waveforms are sinusoidal shaped [23].

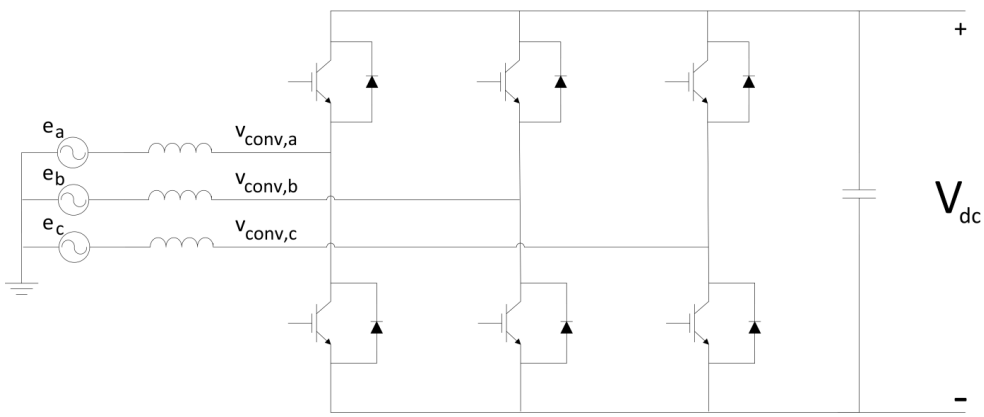

Figure 3.1: Active front end electrical circuit with an AC input and a DC output.

3.1 Characteristics

The AFE is controlled with a PWM and converts power from AC to DC or vice versa. Due to the possibility of controlling the power in both directions through the AFE together with reactive and active power individually, it's possible to adjust the power factor [23].

$$Power\ Factor = \frac{P}{\sqrt{p^2 + Q^2}} = \cos(\varphi) \tag{3.1}$$

Equation 3.1 is valid for sinusoidal currents and defines the ratio between the apparent power in the circuit and the load power. As a result of the equation, shall the reactive power Q ideally be set to zero in order to achieve ideal power factor. The apparent power through the AFE is calculated by [19]:

$$\vec{S} = \vec{V_s} \cdot \vec{I_s^*} = \frac{V_s^2 \cdot e^{j\pi/2} - V_{conv} \cdot e^{j(\delta + \frac{\pi}{2})}}{\omega \cdot L_{conv}} \tag{3.2}$$

Active and reactive power can be separated (3.3), (3.4):

$$Re\{\vec{S}\} = P = \frac{V_{conv} \cdot V_s}{\omega \cdot L_{conv}} \cdot \sin(\delta) \tag{3.3}$$

$$Im\{\vec{S}\} = Q = \frac{V_s^2}{\omega \cdot L_{conv}} \cdot \left(1 - \frac{V_{conv} \cdot \cos(\delta)}{V_s}\right) \tag{3.4}$$

In order to control the AFE a carrier wave, in this case a triangular wave is compared with a reference wave creating a modulation signal (see Figure 2.1). The reference wave is a sinusoid in steady state (3.5).

$$m_a(t) = \hat{m}_a \cdot \sin(\omega \cdot t - \delta) \tag{3.5}$$

By increasing or decreasing the phase δ or the magnitude $\hat{m}_a$ it's possible to control both the active and reactive power through the AFE. An expression that describes the relation between voltage input of the converter as a function of $\hat{m}_a$ and DC-link voltage V_{dc} is presented (3.6).

$$V_{conv} = \hat{m}_a \cdot \frac{V_{dc}}{2 \cdot \sqrt{2}} \tag{3.6}$$

Together with equation 3.3, 3.4 and 3.6 it's possible to express P and Q as a function of $\hat{m}_a$ and δ.

$$P(\hat{m}_a, \delta) = \frac{V_{dc} \cdot \hat{m}_a \cdot V_s}{2 \cdot \sqrt{2} \cdot \omega \cdot L_{conv}} \sin(\delta) \tag{3.7}$$

$$Q(\hat{m}_a, \delta) = \frac{V_s^2}{\omega \cdot L_{conv}} \cdot \left(1 - \frac{V_{dc} \cdot \hat{m}_a \cdot \cos(\delta)}{2 \cdot \sqrt{2} \cdot V_s}\right) \tag{3.8}$$

The relationship in equation 3.7 and 3.8 is visualized in Figure 3.2.

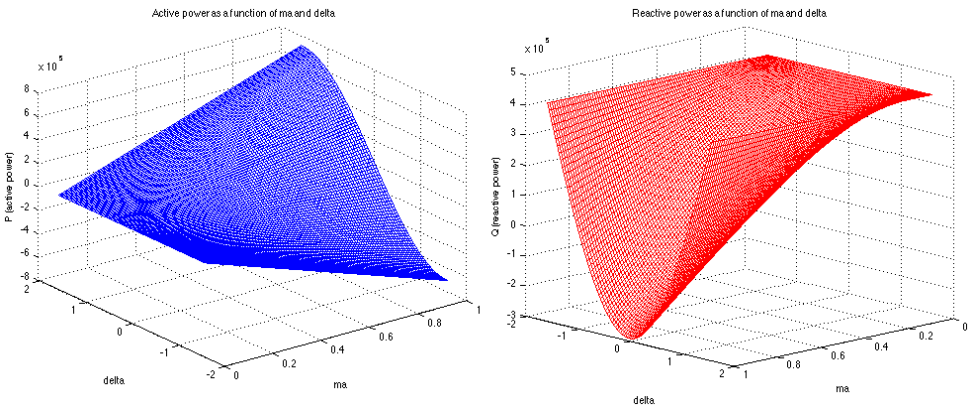

Figure 3.2: 3d plot of equation 3.7 to the left and 3.8 to the right. The values for $_{Vdc}$ is 1100 V, V_s is 230 V and L_{conv} is 0.4 mH.

3.2 Control

The AFE is an active three phase rectifier and can be controlled by feedback loops. In order to simplify the control, transformations are established from the 3-phase AC representation to a two vectored rotating frame. In the dq frame the controller is optimized by derived models together with decoupling of variables.

3.2.1 Clarke transformation

The Clarke transformation is used to transform a vectored three-phase system in space to two-coordinated system denoted alpha beta. Both current and voltage vectors are transformed using the same transformation.

The transformation (3.9) can be derived from the vector diagram (Figure 3.3).

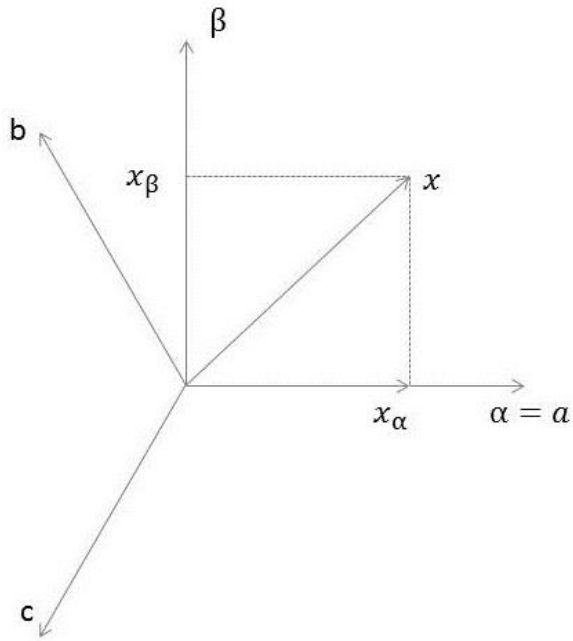

Figure 3.3: Vectors for three-phase system (a, b, c) and (alpha, beta).

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.9}$$

The invers transformation gives:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{3.10}$$

The Clarke transformation can be simplified (3.11) by assuming a symmetrical load in a balanced three-phase system.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \end{bmatrix} \tag{3.11}$$

3.2.2 Transformation from α,β to d,q

In the traditional Park transformation the angle theta is defined as the angle difference between direction alpha and the vector d. In this case the angle theta is instead defined as the angle between alpha and voltage vector (vector q). The main reason for not keeping the traditional park transformation is the earning of not needing to calculate the flux. The flux is the integral of the voltage vector, which is a heavy operation and physically doesn't exist in a grid-connected system. It would therefore only cost extra computational power to first integrate the grid voltage and then use the Park transformation instead of using this transformation directly on the existing voltage vector.

The transformation (3.12) can be derived from the vector diagram (Figure 3.4).

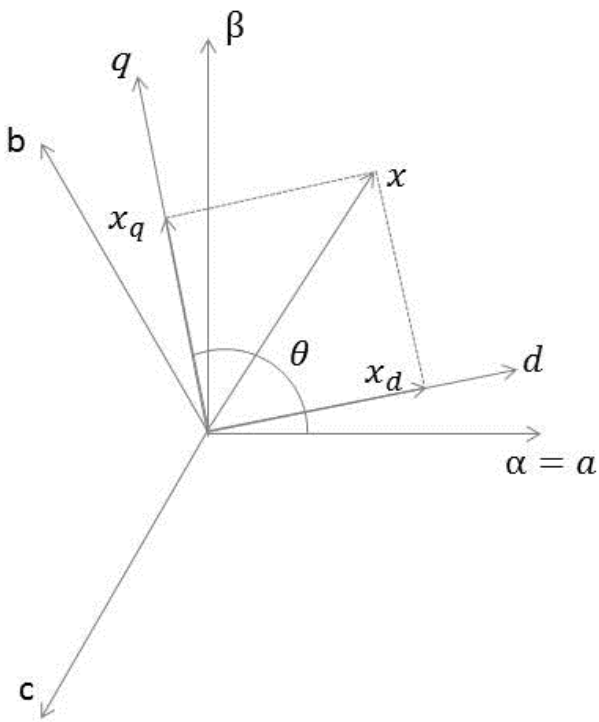

Figure 3.4: Vectors for three-phase system (a, b, c), (alpha, beta) and (d,q).

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{3.12}$$

The corresponding inverse transformation is:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ -\cos(\theta) & \sin(\theta) \end{bmatrix} \cdot \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{3.13}$$

Calculation of the angle theta can be a difficult operation because it´s requiring arctangent. Therefore a more efficient way of determining the sin(θ) (3.14) and cos(θ) (3.15) is chosen with help of trigonometric equations based on the assumption that voltage and q-vector is aligned.

$$\sin(\theta) = \frac{v_\beta}{\sqrt{v_\alpha^2 + v_\beta^2}} \tag{3.14}$$

$$\cos(\theta) = \frac{v_\alpha}{\sqrt{v_\alpha^2 + v_\beta^2}} \tag{3.15}$$

3.2.3 Adaption of α,β to d,q transformation with grid voltage filter

A first order grid filter is good for attenuating disturbances, but unfortunately it affects the measurement. The phase and amplitude is changed, which will have a negative affect on the control system. To prevent this a compensation for the low pass-filtered voltage measurement is implemented. By plotting the bode-diagram the affected phase and magnitude can be determined depending on chosen cut-off frequency.

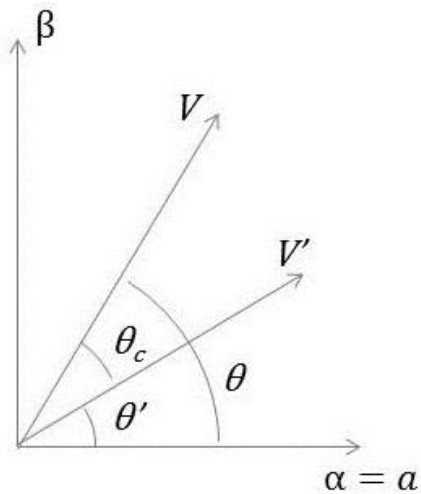

Figure 3.5: Voltage vector diagram where V is the real voltage vector and V' is the filtered voltage vector.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{1}{|G(2\pi f)|} \cdot \begin{bmatrix} \frac{\cos(\theta)}{\cos(\theta')} \cdot {x_\alpha}' \\ \frac{\sin(\theta)}{\sin(\theta')} \cdot {x_\beta}' \end{bmatrix} \tag{3.16}$$

Transformation from measured quantities to actual values before filter is presented in equation 3.16, where $|G(2\pi f)|$ is the absolute value of the transfer function for a first order low pass-filter (2.11).

The angle θ is not known but it can be computed with help of the transfer function (2.12). The affected angle $\theta_c = \arg(G(2\pi f))$ for a specific frequency, f, makes the angle implicitly know. By the trigonometry of Figure 3.5 the relation (3.17) can be derived:

$$\theta = \theta_c + \theta' \tag{3.17}$$

From trigonometric equations the expression of sinus (3.18) and cosinus (3.19) of angle θ is finally presented with well-known terms.

$$\sin(\theta) = \frac{1}{\sqrt{{x'_\alpha}^2 + {x'_\beta}^2}} \cdot \left(x'_\beta \cdot \cos(\theta_c) + x'_\alpha \cdot \sin(\theta_c)\right) \tag{3.18}$$

$$\cos(\theta) = \frac{1}{\sqrt{x'^{2}_{\alpha} + x'^{2}_{\beta}}} \cdot \left(x'_{\alpha} \cdot \cos(\theta_c) - x'_{\beta} \cdot \sin(\theta_c)\right) \tag{3.19}$$

3.2.4 Model of the AFE converter

A way of modeling a modulator and an active rectifier is by a first order system with a gain and a delay [24].

$$G_c(s) = \frac{K_c}{1 + sT_c} \tag{3.20}$$

The transfer function (3.20) describes the system where K_c represents the gain and T_c represents the time constant.

$$K_c = \frac{V_{dc}}{2 \cdot \hat{V}_{tri}} \tag{3.21}$$

Equation 3.21 describes the relation between K_c, the magnitude of the triangular wave $\hat{V}_{tri}$ and V_{dc}(visualized in Figure 3.6).

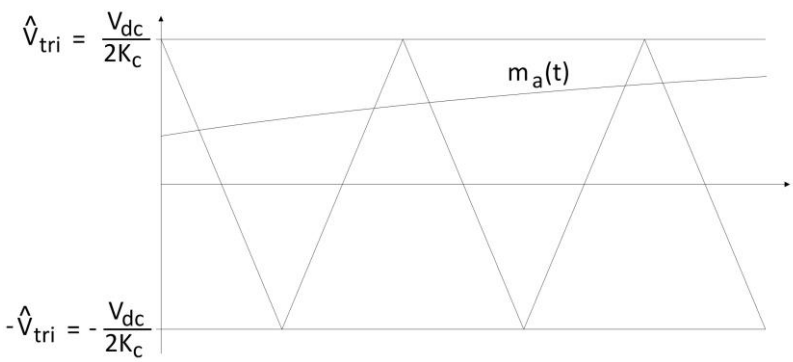

Figure 3.6: The relation between $\frac{V_{dc}}{2}$ and $\hat{V}_{tri}$ where the difference is the gain K_c.

Based on the switching, the average delay T_c is half a switching period of T_s [24].

$$T_c = \frac{1}{2 \cdot f_s} \tag{3.22}$$

3.2.5 Model of the control loops

In order to control the AFE, a mathematical analysis needs to be done. The goal is a constant DC-link voltage with an optimized power factor. An overview of the implementation with transformations, PWM and control of the system can be viewed in (Figure 3.7).

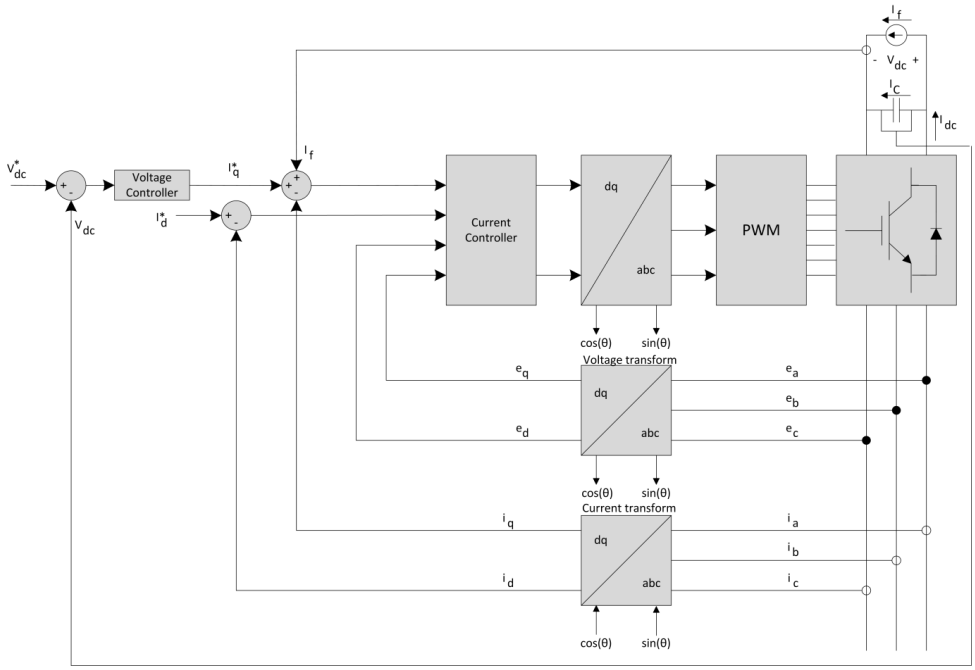

Figure 3.7: Block diagram with an overview of the AFE control system.

3.2.6 Current controller

The physical part of the system can be described as a simplified model with input and output components (see Figure 3.8).

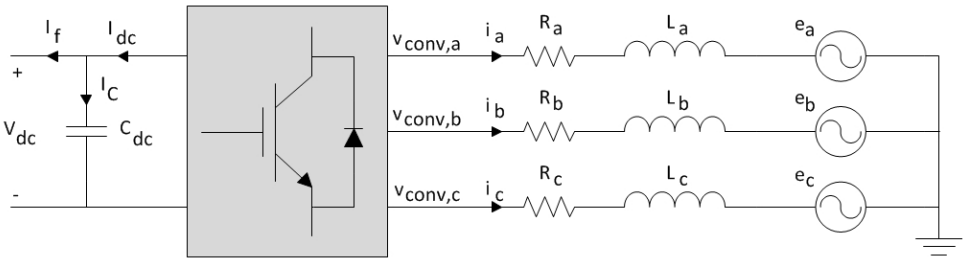

Figure 3.8: Simplified illustration of the AFE circuit with detailed input and output components.

By KVL analysis of the model at the AC-side in Figure 3.8 the following relations are obtained:

$$\begin{cases} v_{conv,a} = R_a \cdot i_a + L_a \cdot \dfrac{di_a}{dt} + e_a \\ v_{conv,b} = R_b \cdot i_b + L_b \cdot \dfrac{di_b}{dt} + e_b \\ v_{conv,c} = R_c \cdot i_c + L_c \cdot \dfrac{di_c}{dt} + e_c \end{cases} \tag{3.23}$$

Due to symmetry reasons the line resistances and inductances are of the same magnitude in all three phases, $L_{conv} = L_a = L_b = L_c$ respective $R_{conv} = R_a = R_b = R_c$. The voltages $v_{conv,a}$, $v_{conv,b}$ and $v_{conv,c}$ are the modulation voltages of each phase to the converter and e_a, $e_b$and e_c represent the voltage of the AC source and i_a, i_b and i_c represent the phase currents.

By using the transformation from a, b, c- to d, q-frame the equation 3.23 is transformed into two DC-quantities [18]:

$$\begin{cases} i_d = \dfrac{u_d - e_d + \omega \cdot L_{conv} \cdot i_q}{R_{conv} \cdot (1 + s\tau)} \\ i_q = \dfrac{u_q - e_q - \omega \cdot L_{conv} \cdot i_d}{R_{conv} \cdot (1 + s\tau)} \end{cases} \tag{3.24}$$

The time constant at the input is $\tau = \frac{L_{conv}}{R_{conv}}$.

Equation 3.24 is the result of the transformation, where the d-part and the q-part are dependent on each other.

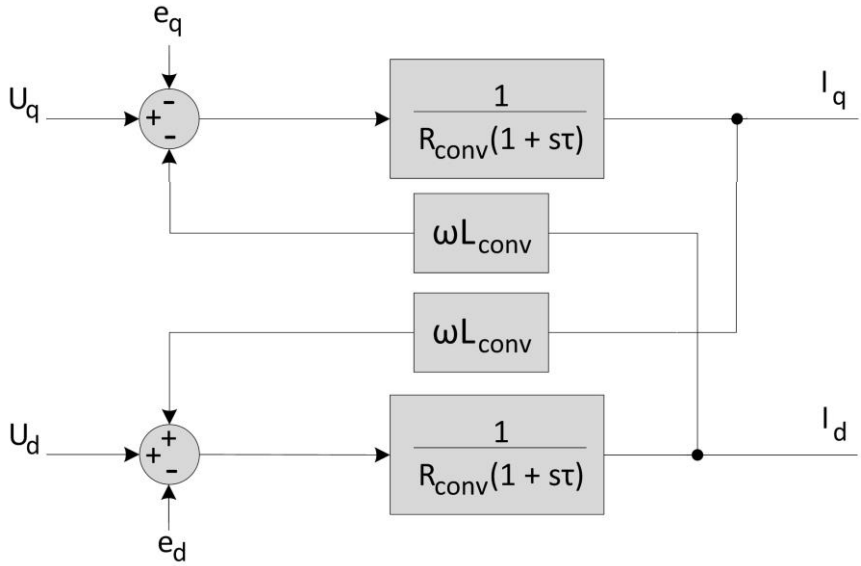

Figure 3.9: Block diagram representation of the rectifier in d,q frame with coupling.

The rectifier has a coupling between the d and q part (see Figure 3.9), which will make the current control of the system difficult. By designing the controller with a feed forward compensation (see Figure 3.10) it is possible to decouple the system and control the currents independently [25].

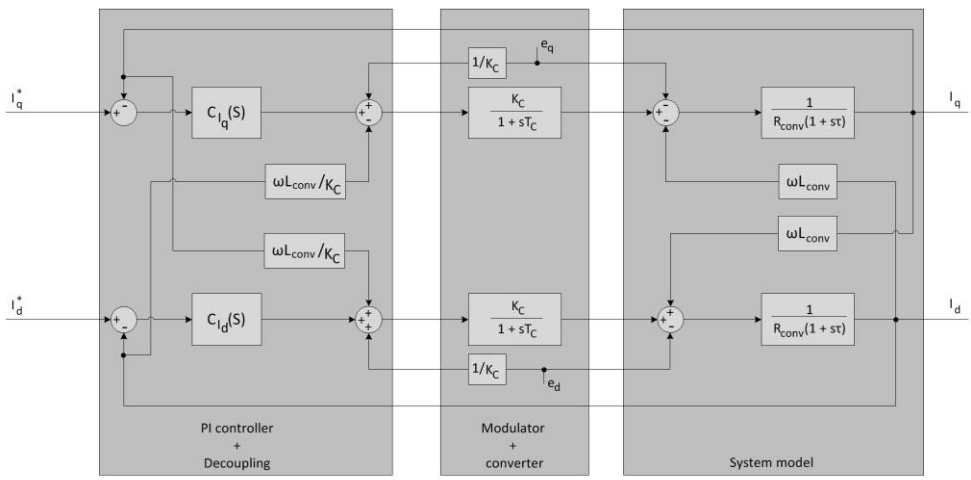

Figure 3.10: Block diagram showing control and decupling, modulator and converter and system model of the AFE.

Due to the decoupling it is possible to independently control active and reactive power and optimize the power factor, where the d-part represents reactive power and the q-part active power. In Figure 3.10 the first part shows the controller and the decoupling, because of this the system can be represented as two separate systems, see Figure 3.11.

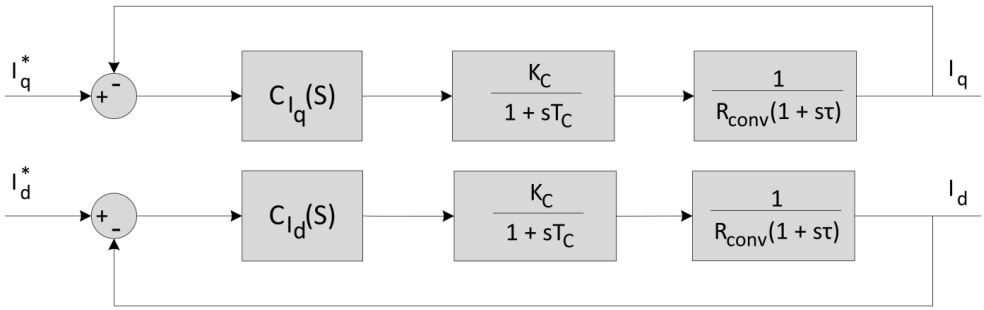

Figure 3.11: Block diagram showing the two decoupled systems.

The first blocks, $C_{I_q}(s)$ and $C_{I_d}(s)$, in each part of the system in Figure 3.11 describes the controller. To control the system a PI controller is used (relation described in equation 3.25) with a proportional part and an integrating part to remove the stationary error.

$$C_{i,q}(s) = \frac{1 + sT_{zi}}{sT_{pi}} \tag{3.25}$$

Implicitly the proportional gain for the current controller is $K_i = \frac{T_{zi}}{T_{pi}}$ and the integral gain is $\frac{1}{T_i} = \frac{1}{T_{pi}}$. The control parameters are chosen in such a way that the controller together with the system is a compromise between speed and robustness.

$$T_{zi} = \tau = \frac{L_{conv}}{R_{conv}} \tag{3.26}$$

By analyzing the decoupled system in Figure 3.11, the control parameter T_{zi} (3.26) is chosen in such a way that one pole is canceled and thereby decreasing the complexity of the system to control (Figure 3.12).

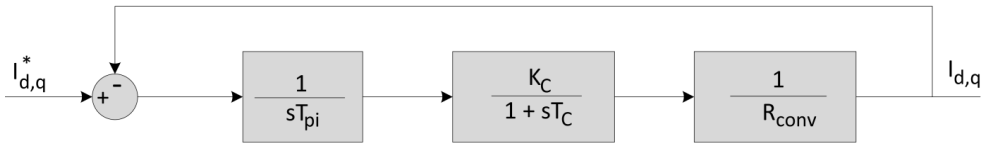

Figure 3.12: Simplified block diagram of the system with chosen T_{zi} inserted.

The second order closed loop transfer function of the system in Figure 3.12 is:

$$G_{I_{d,q}}(s) = \frac{\frac{K_c}{T_{pi} \cdot T_c \cdot R_{conv}}}{s^2 + s\frac{1}{T_c} + \frac{K_c}{T_{pi} \cdot T_c \cdot R_{conv}}} \tag{3.27}$$

The denominator in equation 3.27 is compared with the standard form of a second order closed loop system and put to zero for identification of poles (3.28) [22].

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{3.28}$$

Identification of the components gives the following relations:

$$\begin{cases} 2\xi\omega_n = \frac{1}{T_c} \\ \omega_n^2 = \frac{K_c}{T_{pi} \cdot T_c \cdot R_{conv}} \end{cases} \tag{3.29}$$

By choosing the parameter ξ to $\frac{1}{\sqrt{2}}$, the highest possible bandwidth without an amplitude response over $0\ dB$ is achieved. By solving (3.29) the expression for T_{pi} is achieved (3.30).

$$T_{pi} = \frac{2 \cdot K_c \cdot T_c}{R_{conv}} \tag{3.30}$$

3.2.7 Voltage controller

The parameters for the current controller, T_{zi} (3.26) and T_{pi} (3.30), inserted in (3.27) in the previous section gives a second order

closed loop transfer function (3.31).

$$\frac{I_q(s)}{I_q^*(s)} = \frac{1}{2 \cdot s^2 \cdot T_c^2 + 2 \cdot s \cdot T_c + 1} \tag{3.31}$$

Due to the choice of ideal power factor, $I_d^*(s)$ is set to zero. The second order term in the denominator polynomial of (3.31) is neglected due to a lower bandwidth in the voltage controller [24].

$$\frac{I_q(s)}{I_q^*(s)} = \frac{1}{1 + 2 \cdot s \cdot T_c} \tag{3.32}$$

In the a,b,c to d.q transformation with amplitude invariance used as a base, it is implied that $I_{dc} = i_q$. The AFE DC-link voltage is then controlled by cascade coupling the current controller with a voltage control loop. This is illustrated in a block diagram in Figure 3.13.

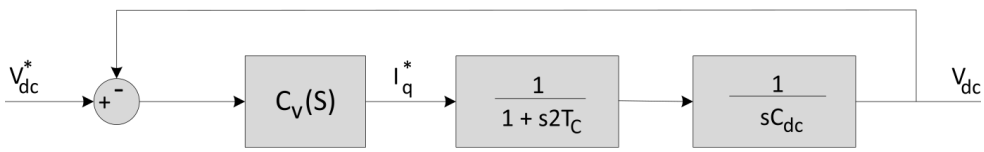

Figure 3.13: Block diagram with voltage controller in cascade with current controller.

The controller $C_v(s)$ is a PI controller (3.33)

$$C_v(s) = \frac{1 + sT_{zv}}{sT_{pv}} \tag{3.33}$$

From the block diagram in Figure 3.13 the open loop transfer function is derived.

$$G_{o_v}(s) = \frac{1 + s \cdot T_{zv}}{s^2 \cdot T_{pv} \cdot C_{dc} \cdot (1 + 2 \cdot s \cdot T_c)} \tag{3.34}$$

Due to the double pole in the origin, the slope at low frequencies is -40 dB/decade. In order to achieve system stability the zero $\left(\omega_1 = \frac{1}{T_{zv}}\right)$ shall be positioned before the unit gain cross over (ω_c) and the controller

pole $\left(\omega_2 = \frac{1}{2 \cdot T_c}\right)$ after ω_c so that the slope at the cross over is -20dB/decade [24]. The relationship for parameters and properties of the open loop transfer function is illustrated as a bode diagram in Figure 3.14.

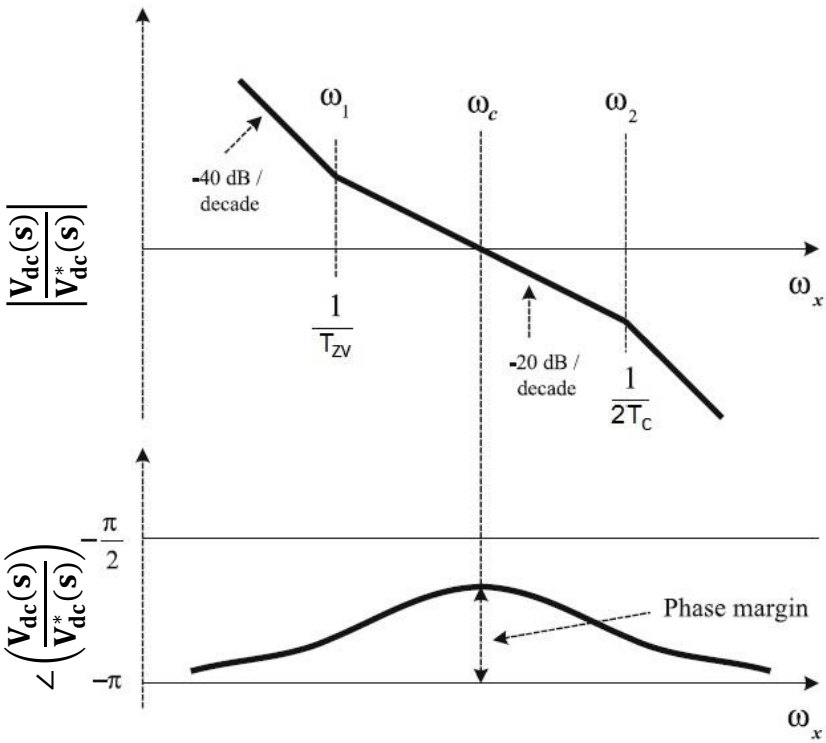

Figure 3.14: An illustrative figure of the bode plot for voltage controller design [24].

As illustrated in Figure 3.14 a possible way of choosing the desired cross over frequency (ω_c) is to take the geometrical mean of the two frequencies, ω_1 and ω_2 [24].

$$\omega_c = \frac{1}{\sqrt{2 \cdot T_c \cdot T_{zv}}} = \frac{1}{a \cdot 2 \cdot T_c} \rightarrow T_{zv} = a^2 \cdot 2 \cdot T_c \tag{3.35}$$

Equation 3.35 describes the relation between T_{zv} and T_c where a is a constant larger than 1. The control parameter T_{pv} is derived by setting the gain of the open loop transfer function (3.34) to 1. [24]

$$\left|\frac{V_{dc}(s)}{V_{dc}^{*}(s)}\right|_{\omega_x=\omega_c} = 1 = \frac{\sqrt{1+(\omega_c \cdot T_{zv})^2}}{\omega_c^2 \cdot C_{dc} \cdot T_{pv}\sqrt{1+(\omega_c \cdot 2 \cdot T_c)^2}} \tag{3.36}$$

By using equation 3.34 and 3.35 in expression 3.36 the following relation is derived.

$$T_{pv} = \frac{4 \cdot a^3 \cdot T_c^2}{C_{dc}} \tag{3.37}$$

The parameter a is decided by applying the rule of thumb for the phase margin and compromise between speed and stability, suitable phase margin $\varphi_m \in [45{,}60]$ [22].

3.3 AFE power losses

The current waveforms through the AFE are as mentioned before sinusoidal which will cause the duty cycle to vary over time.

$$I_{L_{conv}}(t) = \hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t) \tag{3.38}$$

$$D(t) = \frac{1}{2} \cdot (1 - \hat{m}_a \cdot \sin(\omega \cdot t + \varphi - \delta)) \tag{3.39}$$

Where the $I_{L_{conv}}(t)$ is the current from the ac side into one of the rectifier arms and $D(t)$ is the duty cycle for the corresponding transistors or diodes.

3.3.1 Conduction losses

Due to the high switching frequency of the transistors, current and duty cycle is approximated to be continuous over a 50 Hz period. There are two possibilities of conduction in a one phase active rectifier bridge. Either the transistor T_1 or the diode D_2 conducts during the positive part of the period. During the negative period the transistor T_2 or the diode D_1 conducts.

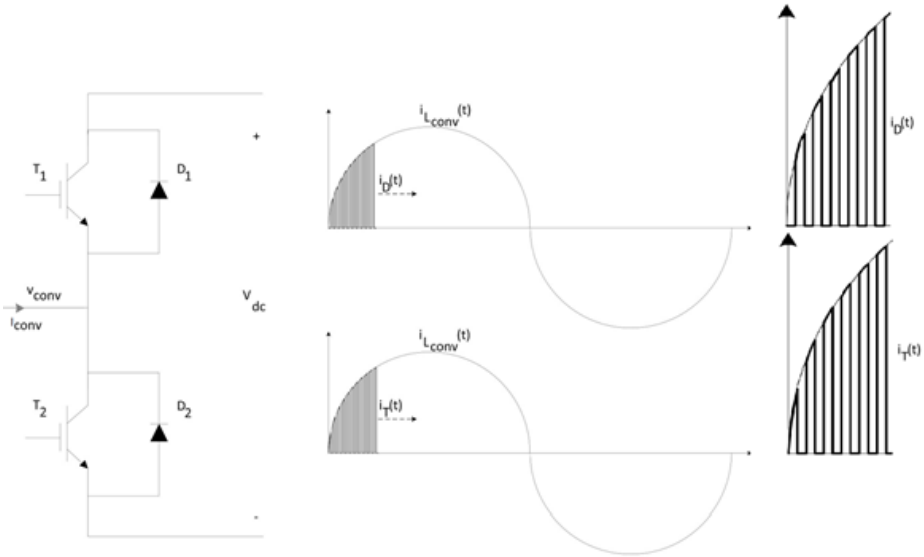

Figure 3.15: The left picture shows one arm of the active rectifier, the right illustrates the current during switching over a part of a sinus period for diode (top) and transistor (bottom).

The equation for average conduction losses in a transistor is defined (3.40) with use of the general equation for instantaneous losses in a semiconductor (2.9).

$$\langle P_{tran,con} \rangle = \langle I_{L_{conv}}^2(t) \cdot D(t) \rangle \cdot R_{on} + \langle I_{L_{conv}}(t) \cdot D(t) \rangle \cdot V_{fo} \tag{3.40}$$

The transistor conduction losses are given by (3.40) and the two average parts for this equation are given by (3.41) and (3.42). The average parts are calculated over half a period of the sinus wave, due to symmetric reasons. Further calculations and expressions are presented in appendix.

$$\langle I_{L_{conv}}^2(t) \cdot D(t) \rangle = \frac{1}{T_{50Hz}} \int_{t_1}^{t_2} \left(\hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t) \right)^2 \cdot \frac{1}{2} \cdot (1 - \hat{m}_a \cdot \sin(\omega \cdot t + \varphi - \delta)) dt \tag{3.41}$$

$$\langle I_{L_{conv}}(t) \cdot D(t) \rangle = \frac{1}{T_{50Hz}} \int_{t_1}^{t_2} \hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t) \cdot \frac{1}{2} \cdot (1 - \hat{m}_a \cdot \sin(\omega \cdot t + \varphi - \delta)) dt \tag{3.42}$$

The equation for average conduction losses in a diode are defined (3.43) with the use of the general equation for instantaneous losses in a semiconductor (2.9). Since $D(t)$ is the percentage of time when the transistor is conducting power to the load, $(1 - D(t))$ is the percentage of time when the diode is conducting power to the load.

$$\langle P_{diode,con} \rangle = \langle I_{L_{conv}}^2(t) \cdot (1 - D(t)) \rangle \cdot R_{on} + \langle I_{L_{conv}}(t) \cdot (1 - D(t)) \rangle \cdot V_{fo} \tag{3.43}$$

The diode conduction losses are given by (3.43) and the two average parts for this equation is given by (3.44) and (3.45). Further calculations and expressions are presented in appendix.

$$\langle I_{L_{conv}}^2(t) \cdot \big(1 - D(t)\big) \rangle = \frac{1}{T_{50Hz}} \int_{t_1}^{t_2} \big(\hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t)\big)^2 \cdot \frac{1}{2} \cdot (1 + \cdot \sin(\omega \cdot t + \varphi - \delta)) dt \tag{3.44}$$

$$\langle I_{L_{conv}}(t) \cdot \big(1 - D(t)\big) \rangle = \frac{1}{T_{50Hz}} \int_{t_1}^{t_2} \hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t) \cdot \frac{1}{2} \cdot (1 + \hat{m}_a \cdot \sin(\omega \cdot t + \varphi - \delta)) dt \tag{3.45}$$

3.3.2 Switching losses

The switching losses are based on the characteristic of the semiconductor and the datasheet specifies switching energy losses for a given current and voltage magnitude, where the voltage is set to V_{dc}.

$$\langle I_{L_{conv}} \rangle = \frac{1}{T_{50Hz}} \int_{t_1}^{t_2} \hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t)\, dt \tag{3.46}$$

The average current is calculated over half a period for one component, due to symmetric reasons as mentioned before. An IGBT requires energy for both turn on and turn off, meanwhile the diode requires only energy for turn off due to its characteristic (chapter 2.4.1).

3.4 Electromagnetic compatibility (EMC)

The AFE is connected to the low voltage grid and has to fulfill international standards regarding power quality. Main focus is on fulfilling the low harmonic distortion and flicker according to the IEC standards.
The ESS modulators are rated for extremely high power and currents which are outside the range of IEC standards. Due to this and to ensure low grid impact the strictest standards are applied for equipment with rated currents below 16A.

3.4.1 Flicker - IEC 61000-3-3

The IEC 61000-3-3 concerns standards regarding voltage fluctuations, voltage changes and flicker on applications connected to the low voltage grid.

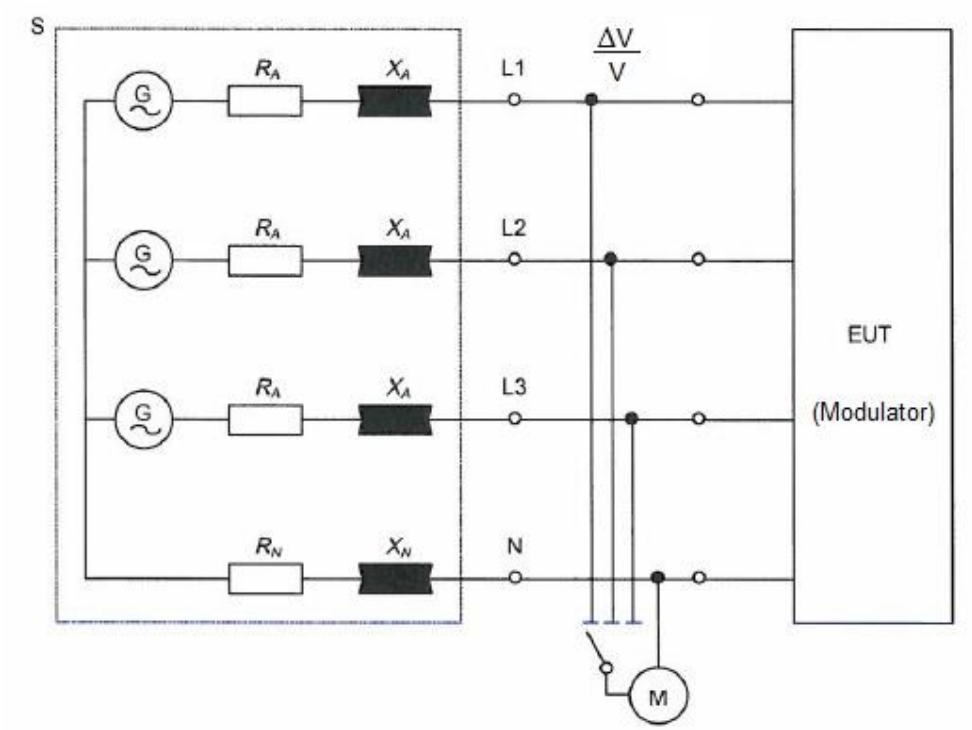

Figure 3.16: Reference network for a three-phase supply [26].

In Figure 3.16 is the test set up for the three-phase application where:
EUT equipment under test (modulator)

M measuring equipment
G voltage source
S supply source consisting of the supply voltage generator G and test impedance Z with the following elements which include the generator impedance.

([26], p. 31)

V is the nominal peak value of the voltage.
ΔV is the difference between nominal peak voltage and measured peak voltage.

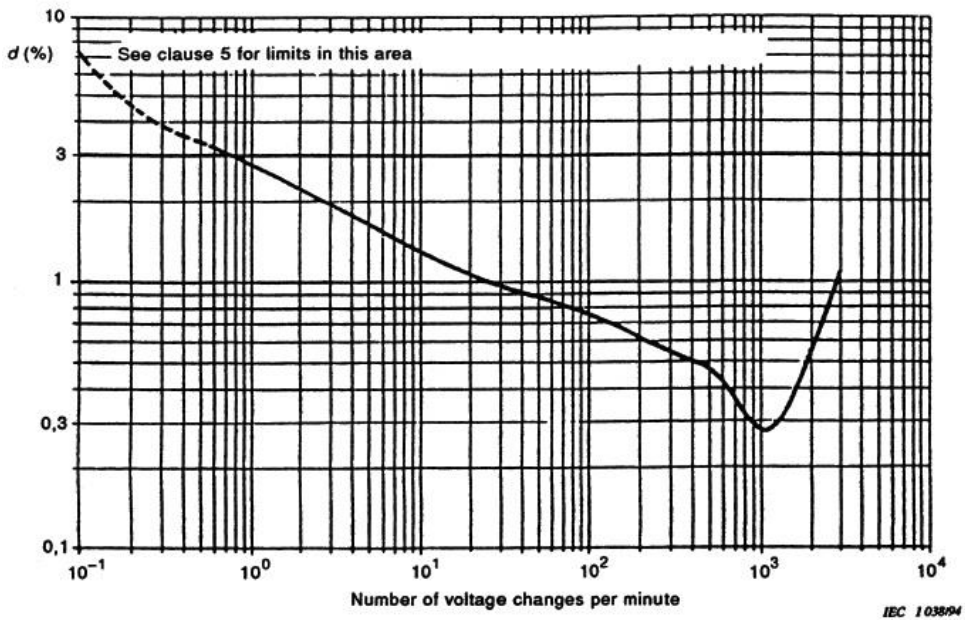

Figure 3.17: The flicker level in percent as a function of number of voltage changes per minute [26].

For this type of application it is important to check the relative steady state voltage change, d_c, which is the ratio between the difference in peak voltages at the measurement points (Figure 3.16) and nominal peak voltage. The maximum relative steady state voltage change shall not exceed the limits given in the diagram in Figure 3.17 [26].

3.4.2 Low harmonic current – IEC 61000-3-2

The IEC 61000-3-2 concerns the limitation of current harmonics injected into the low voltage grid.

Harmonic order n	Maximum permissible harmonic currrent expressed as a percentage of the input current at the fundamental frequency %
2	2
3	$30 \cdot \lambda$ *
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3
* λ is the circuit power factor	

Figure 3.18: Limits for the harmonic current in percentage **[27]**.

The injected current harmonics are measured by doing an FFT analysis of the current wave forms when the application is in operating mode. At startup and shut down, the 10 first seconds is not taken into account and the FFT measurement of the current shall be performed during 1,5 seconds [27].

CHAPTER 4

4 DC/DC-converter with a pulsed load

The DC/DC step down converter is traditionally a conversion structure allowing power conversion from a DC-voltage input to an output load, having the output average voltage that is equal or lower than the input voltage. With a LC-filter on the output the signal is smoothened and can therefore be considered as a flat DC level [18]. The problem in this case is the pulsed load, which will imply high power fluctuations on the grid. With the assumption that the time between pulses and duration of them are known, construction of a smart power control will be feasible. This power control´s mission is to reduce the impact from the switched output load. Due to low energy storage in components, the power output on the DC/DC-stage will be the same as input power if losses are neglected. This chapter covers the theory behind controllers that can solve pulsed load power fluctuations. In short terms a new-developed power control loop concept is put in cascade with a current controller. The electric structure for a DC/DC converter can be seen in Figure 4.1, where the transistor and diode switch for alternating time periods depending on the duty-cycle.

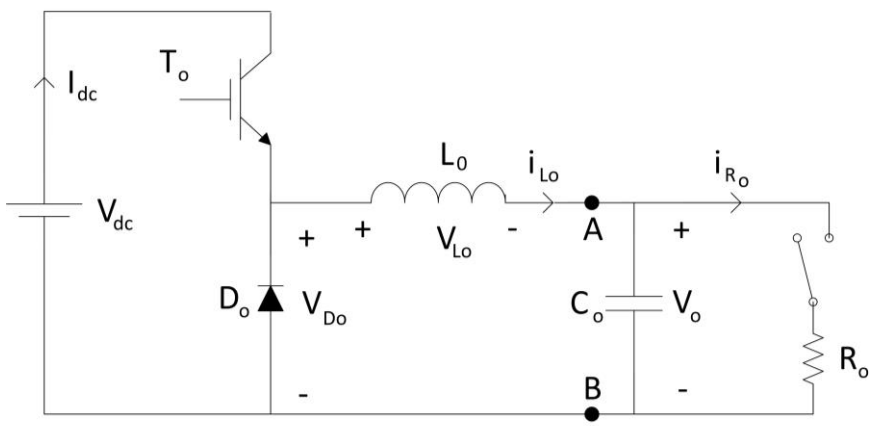

Figure 4.1: Schematic of a DC/DC step down converter with a pulsed load.

4.1 Characteristics

The DC/DC is controlled with PWM and since the levels are DC only active power matter. To achieve constant input power to the converter, output current, I_{Lo}, and output voltage, V_o, will be controlled in a way to make the power, P_{AB}, constant. In order to make this work, the product of current and voltage has to be constant in every point due to the electric power law. The output power is equal to the input power and therefore the following relation is valid (4.1) [21]. An illustrating picture of how a constant power source can supply a high power pulsing load is shown in Figure 4.2.

$$P_{AB} = V_o \cdot I_{L_o} = P_{dc} = V_{dc} \cdot I_{dc} \tag{4.1}$$

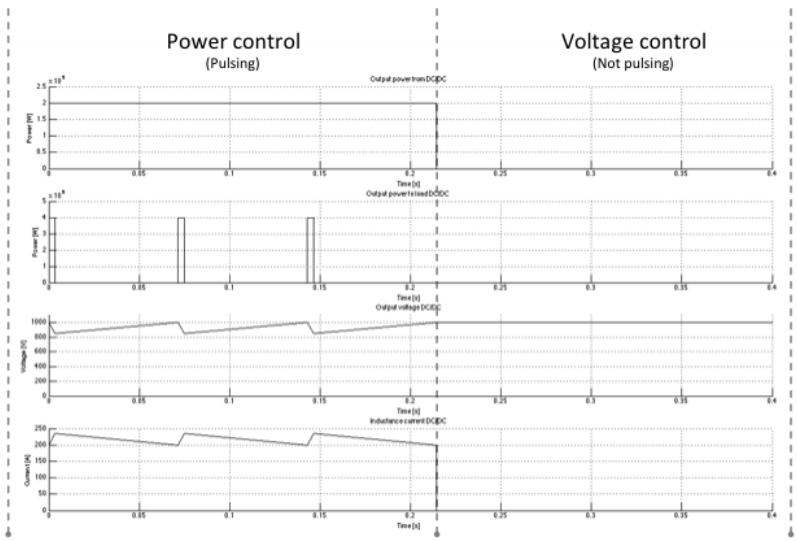

Figure 4.2: Characteristics for a constant power DC/DC-converter and graphs for load power, output voltage and inductance current.

Due to pulsing nature of the output load, output voltage will drop to a certain level depending on dimensioning of the output capacitance. The enormous amount of power that will be fed to the load, in the pulsing period, will create this voltage drop and is almost impossible to counter. If this phenomenon should be encountered, an unrealistically big output capacitance would be needed. Therefore this voltage drop is accepted and controlled in a linear way to obtain constant power.

In order to control the DC/DC conventionally a triangular carrier wave is compared with a reference level that creates the pulsing pattern. Where the triangular wave amplitude is stretching from zero to input DC-level, the reference level is chosen depending on desired output level. Notate that the output DC-level is lower or equal to the input DC-level. Deeper knowledge about characteristics for switching is found in Chapter 2.1.

4.2 Control

By looking at the characteristics for switching, it can be understood, that adjustment of the PWM-reference will control the average voltage level over the diode. When demanding a specific current level on the DC/DC-converter output a current control loop needs to be implemented [18]. Furthermore a voltage or a power control loop in cascade with the current control loop is needed to control the voltage level or power level on the output. In the normal situation, the power control will be in use to control power to the output. If the output stage under some circumstance will stop pulsing, the voltage control takes over and acts as a safety to not exceed high voltage levels. The voltage control will also be used to ensure that correct voltage level is held when the pulsing eventually starts again. In this chapter, an approach for controlling this system is presented and regarding the power control, two types will be described and evaluated. The final choice of power control type will then be presented in chapter 5 with clear motivations.

4.2.1 Model of converter

An easy way of modeling the converter is by a first order delay (4.2). The calculation and update of new values will be finished in average between two sampling periods. The delay is there for half a switching period (4.3).

$$G_c(s) = \frac{1}{1+sT_c} \tag{4.2}$$

$$T_c = \frac{1}{2 \cdot f_s} \tag{4.3}$$

4.2.2 Model of system

The complete high-level principle of the control approach and system is shown in Figure 4.3.

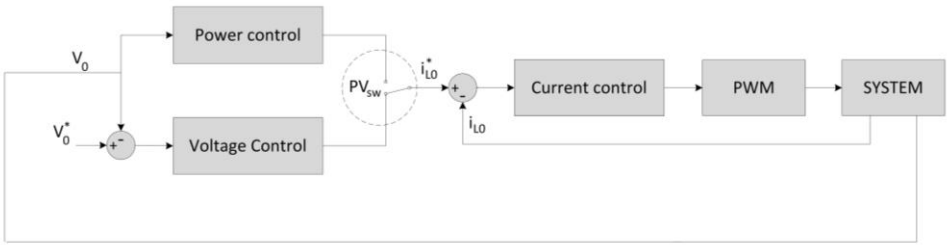

Figure 4.3: A block diagram representation of the power control, voltage control, simplified switch between them, current control, PWM and the system.

Based on KVL analysis of the circuit in Figure 4.1, a representation of the system can be constructed in frequency domain (4.4).

$$V_{D_o}(s) - sL_o \cdot i_{L_o}(s) - V_o(s) = 0 \tag{4.4}$$

With help of (4.4) an expression for the current can be derived (4.5).

$$i_{L_o}(s) = \frac{V_{D_o}(s) - V_o(s)}{sL_o} \tag{4.5}$$

When having a capacitance, C_o, on the output port the voltage can be calculated (2.16), in frequency domain (4.6).

$$V_{c_o}(s) = \frac{i_{C_o}(s)}{sC_o} \tag{4.6}$$

4.2.3 Model of current control

In order to eliminate stationary errors and create a current controller with desired performance, a PI-controller with feed forward of the output voltage is used (4.7).

$$C_i(s) = K_i \cdot \left(T_i + \frac{1}{s}\right) \tag{4.7}$$

The block diagram in Figure 4.4 contains a mathematical description of the system (4.2, 4.3, 4.5 and 4.6) and the current controller (4.7) together with a feed-forward of the output voltage. The open loop transfer function (4.8) and closed loop transfer function (4.9) is derived from the block diagram in Figure 4.4 to make good estimations of the control parameters.

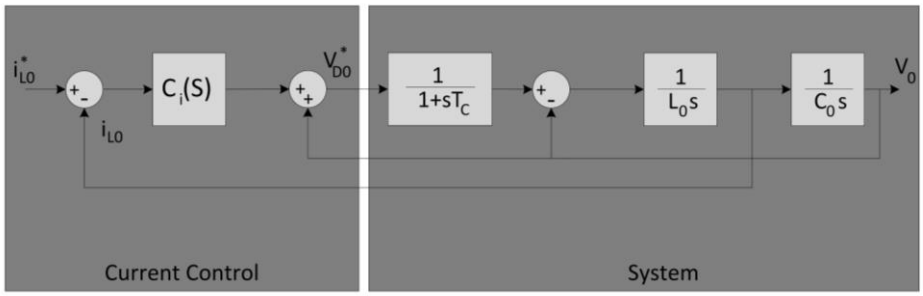

Figure 4.4: A block diagram representation of the current control in interaction with the system.

$$G_{o_i}(s) = \frac{i_{L_o}}{i_{L_o}^* - i_{L_o}} = \frac{sK_iT_i + K_i}{s^3L_oT_c + s^2L_o} \tag{4.8}$$

$$G_{c_i}(s) = \frac{i_{L_o}}{i_{L_o}^*} = \frac{sK_iT_i + K_i}{s^3L_oT_c + s^2L_o + sK_iT_i + K_i} \tag{4.9}$$

4.2.4 Model of voltage control

To create a voltage controller an additional PI-controller is used in cascade with the current controller. This voltage controller (4.10) will set the reference for the current controller and needs to be relatively slow compared to the current controller, this to work in a stable and desired way.

$$C_v(s) = K_v \cdot T_v + \frac{K_v}{s} \tag{4.10}$$

To determine parameter values for the voltage controller the closed loop transfer function for current control (4.9) is used. This is a third order system that is approximated to a first order system in order to simplify calculations (4.11).

$$G_{c_i}(s) = \frac{I_q(s)}{I_q^*(s)} = \frac{1}{1 + 2 \cdot s \cdot T_c} \tag{4.11}$$

The block diagram in Figure 4.5 contains a simplified description of the system with current control (4.11), the voltage controller (4.10) and output voltage over capacitance (4.6). The open loop transfer function (4.12) and

closed loop transfer function (4.13) is derived from the block diagram in Figure 4.5 to make good estimations of the control parameters.

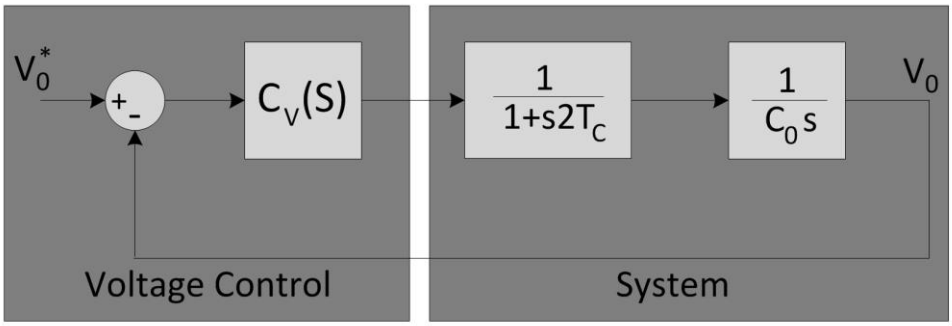

Figure 4.5: A block diagram representation of the voltage control in interaction with the system.

$$G_{o_v}(s) = \frac{sK_vT_v + K_v}{s^3C_oT_c + s^2C_o} \tag{4.12}$$

$$G_{c_v}(s) = \frac{sK_vT_v + K_v}{s^3C_oT_c + s^2C_o + sK_vT_v + K_v} \tag{4.13}$$

4.2.5 Model of power control type 1

Making a control for the power is quite a challenge. The approach described in this subchapter is based on a predictor and a proportional corrector. The output voltage is used to update the power control in specific periods when the load is switching. A schematic picture of this methodology and structure can be seen in Figure 4.6.

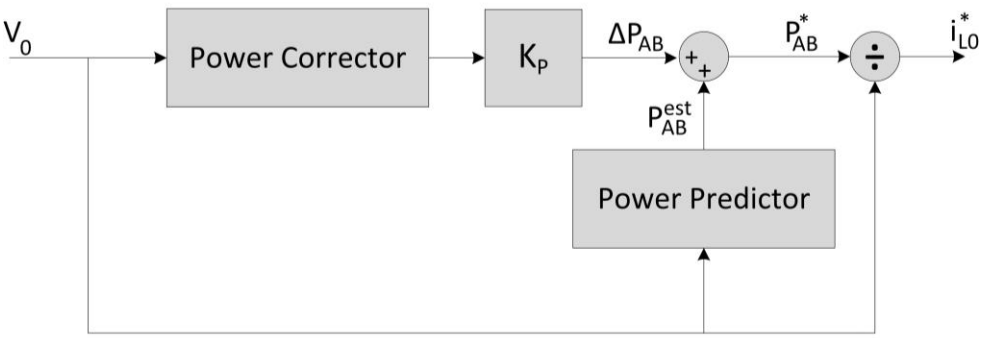

Figure 4.6: A block diagram representation of the type 1 power control structure with a power predictor and corrector.

With help of the energy equation for a capacitance (4.14) and knowing the time between discharges, Δt, the power required to charge the output capacitance is derived (4.15) [21].

$$E_{C_o} = \frac{1}{2} \cdot C_o \cdot {V_{C_o}}^2 \tag{4.14}$$

$$P_{C_o} = \frac{E_{C_o}}{\Delta t} \tag{4.15}$$

When the power at the output is drawn in a pulsed formation, it is hard or almost impossible to keep the voltage level on the output capacitance. The discharge will be exponentially but over a short period of time in respect to the time constant (τ=RC), due to this the discharge can be approximated to linear. After discharge to the low voltage level, V_o^{min}, the capacitance needs to be charged up to a reference level, V_o^{max}, so that it will be ready for next pulse. This needs to be done in a linear way to make the power (product of voltage and current) constant (Figure 4.7).

Figure 4.7: Voltage ripple for a perfect period on the DC-output.

In order to make this work a constant power reference needs to be determined. The constant power level is hard to decide because of the unknown characteristic of the pulsing load. Before and when the first pulse arrives, there will be an initial guess for the power reference based on the expected voltage drop. After the first cycle this power prediction reference will be evaluated in time t_1. Where (4.16) estimates the power by measured voltage drop (V_o^{min}), reference voltage level that shall be reached to the next pulse (V_o^{max}), time until next pulse and capacitance value. An update of the power prediction is immediately done after calculation in t_1.

$$P_{AB}^{est} = \frac{1}{2 \cdot (t_2 - t_1)} \cdot C_o \cdot (V_o^{max^2} - V_o^{min^2}) \tag{4.16}$$

Due to imperfections in a real circuit an implementation with only a prediction term will not be sufficient. Therefore the following approach with a correction term needs to be implemented, this to erase the errors from these imperfections. When a pulse arrives in t_2, the voltage can either be above or below the reference. In the case when voltage level is below the reference, the measured value $V_0(t_2)$ is used to calculate the power correction, see Figure 4.8 for the cycle. In the other case when voltage level is above the reference (if no voltage control loop were implemented), the measured value $V_0(t_2)$ would also be used to calculate the power correction, see Figure 4.9.

Figure 4.8: Voltage waveform for a period when reference level isn't reached on the DC-output at t_2.

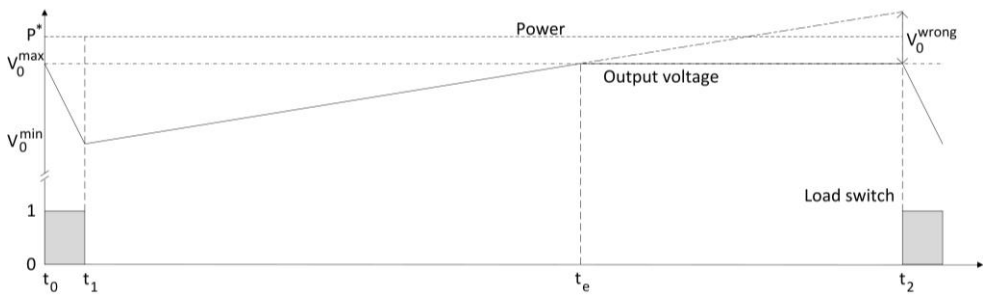

Figure 4.9: Voltage waveform for a period when reference level is reached too early on the DC-output.

Due to the voltage control loop, the voltage level will be limited to a given reference and must be estimated (Figure 4.9). By extrapolating the linear voltage curve a good approximation is done (4.17), where V_o^{ext} is the extrapolated voltage in t_2.

$$V_o^{ext} = V_o(t_2) = V_o^{min} + \frac{V_o^{max} - V_o^{min}}{t_e - t_1} \cdot (t_2 - t_1) \quad (4.17)$$

As mentioned before the measured value $V_o(t_2)$ can either be a voltage under (Figure 4.8) or above (Figure 4.9) the V_o^{max} reference in t_2. With help of this variable a power correction term is calculated and added to the power reference with a proportional controller, which is calculated and updated immediately in time t_2 for the next cycle (4.18).

$$\Delta P_{AB} = K_p \cdot \frac{1}{2 \cdot (t_2 - t_1)} \cdot C_o \cdot (V_o(t_2)^2 - V_o^{max\,2}) \quad (4.18)$$

Where K_p is the gain of the proportional controller.

4.2.6 Model of power control type 2

This type of controller is constructed in a way where the perfect voltage waveform in Figure 4.7 is mimicked. As an outcome of this the power will be constant at the output and the purpose is fulfilled. By using the control theory in section 4.2.4 for voltage control together with an input reference constructed as a ramp function, this behavior will be achieved. The ramp voltage reference will more in detail follow the positive slope (t_1 to t_2) in Figure 4.7. After a pulse (t_1), the output voltage (V_o^{min}) will be measured and by knowing the reference voltage (V_o^{max}) a straight-line function can be calculated. The expression used as reference for the output voltage is presented in (4.19).

$$V_o^*(t) = V_o^{min} + \frac{V_o^{max} - V_o^{min}}{t_2 - t_1} \cdot t \quad (4.19)$$

During the discharge time (t_0 to t_1) the output voltage (V_o) will as mentioned before be hard or impossible to control, due to the big amount of power that will be fed through the circuit. During this time the output capacitance will almost itself supply the output load with power. The current fed from the grid will not be of a big impact. A negative reference slope is therefore too fast and not possible to follow with a controller and can be neglected. If the voltage control now constructed to control the power is optimized to follow the slope perfectly, constant power will be obtained.

In order to decide which implementation of type 1 and type 2 that will be the best for this type of application, simulations will be done. Notation can be done regarding only evaluating two alternatives for the power control even though this is a completely new field in power electronics. Under the development other versions of the power control were investigated with no greater success and are therefore not presented in this report. An evaluation of the two types will be done in the simulation chapter, chapter 5.

4.3 DC/DC dimensioning of passive components

With use of equations from chapter 2.7 a complete dimensioning of the DC/DC can be done. Equation 2.17 is used for inductance dimensioning and (2.18) is used for capacitance dimensioning. The parameters needed in (2.17) and (2.18) are calculated below.

When dimensioning the inductor an acceptable current ripple, $I_{L_o}^{percent}$, is defined. With a constant power, P_{AB}, the average current can be determined (4.20) and the current ripple is calculated by (4.21). These equations are based on the assumption that $V_{L_o} = L_o \cdot \frac{dI_{L_o}}{dt} \approx 0$ since the inductor is small and also the current ripple.

$$\bar{I}_{L_o} = \frac{P_{AB}}{\frac{V_o^{max} + V_o^{min}}{2}} \tag{4.20}$$

$$I_{L_o}^{ripple} = \bar{I}_{L_o} \cdot I_{L_o}^{percent} \tag{4.21}$$

The output voltage is changing between pulses and an average duty-cycle will therefore be used:

$$\overline{D} = \frac{\frac{V_o^{max} + V_o^{min}}{2}}{V_{dc}} \tag{4.22}$$

Regarding dimensioning of the capacitance, the voltage ripple is defined by (4.23). The duty-cycle is defined from characteristics of the output load and the switching frequency as well. With this information and the equation for average current through the circuit (4.20), a determination of output capacitance can be done (2.18).

$$V_o^{drop} = V_o^{max} - V_o^{min} \tag{4.23}$$

4.4 DC/DC power losses

Power losses for the DC/DC are based on the approximation that variations from switching characteristics in the converter are neglected. Because the switching frequency in the converter is much higher than the switched output load, this is a very good estimation. Currents and voltages can therefore be derived into continuous perfect waveforms. Two scenarios are evaluated, one describing the voltage curve when output load is sinking power (4.24) and the other when the load is not sinking power (4.25).

$$V_o(t) = V_o^{max} - \frac{V_o^{max} - V_o^{min}}{t_1 - t_0} \cdot t, t \in [t_0, t_1] \tag{4.24}$$

$$V_o(t) = (V_o^{min} - \frac{(V_o^{max} - V_o^{min}) \cdot t_1}{t_2 - t_1}) + \frac{V_o^{max} - V_o^{min}}{t_1 - t_0} \cdot t, t \in [t_1, t_2] \tag{4.25}$$

$$I_{L_o}(t) = \frac{P^*}{V_o(t)}, t \in [t_0, t_2] \tag{4.26}$$

4.4.1 Conduction losses

The equation for average conduction losses in a transistor are defined (4.27) with the use of the general equation for instantaneous losses in a semiconductor (2.9).

$$\langle P_{tran,con} \rangle = \langle I_{L_o}^2(t) \cdot D(t) \rangle \cdot R_{on} + \langle I_{L_o}(t) \cdot D(t) \rangle \cdot V_{fo} \tag{4.27}$$

The duty-cycle (4.28) is defined as the time when transistor is conducting power to load, in respect to the diode.

$$D(t) = \frac{V_o(t) + L_o \cdot \frac{dI_{L_o}(t)}{dt}}{V_{dc}} \tag{4.28}$$

The transistor conduction losses are given by (4.27) and the two average parts for this equation are given by (4.29) and (4.30). Further calculations and expressions are presented in appendix.

$$\langle I_{L_o}^2(t) \cdot D(t) \rangle = \frac{1}{T} \cdot \int_{t_0}^{t_2} \left(\frac{P^*}{V_o(t)} \right)^2 \cdot \frac{V_o(t) + L_o \cdot \frac{dI_{L_o}(t)}{dt}}{V_{dc}} dt \tag{4.29}$$

$$\langle I_{L_o}(t) \cdot D(t) \rangle = \frac{1}{T} \cdot \int_{t_0}^{t_2} \left(\frac{P^*}{V_o(t)} \right) \cdot \frac{V_o(t) + L_o \cdot \frac{dI_{L_o}(t)}{dt}}{V_{dc}} dt \tag{4.30}$$

The equation for average conduction loss in a diode is defined (4.31) with the use of the general equation for instantaneous losses in a semiconductor (2.9). Since $D(t)$ is the percentage of time when the transistor is conducting power to the load, $(1 - D(t))$ is the percentage of time when the diode is conducting power to the load.

$$\langle P_{diode,con} \rangle = \langle I_{L_o}^2(t) \cdot (1 - D(t)) \rangle \cdot R_{on} + \langle I_{L_o}(t) \cdot (1 - D(t)) \rangle \cdot V_{fo} \tag{4.31}$$

The diode conduction loss is given by (4.31) and the two average parts for this equation is given by (4.32) and (4.33). Further calculations and expressions are presented in appendix.

$$\langle I_{L_o}^2(t) \cdot \big(1 - D(t)\big) \rangle = \frac{1}{T} \cdot \int_{t_0}^{t_2} \left(\frac{P^*}{V_o(t)} \right)^2 \cdot (1 - \frac{V_o(t) + L_o \cdot \frac{dI_{L_o}(t)}{dt}}{V_{dc}}) dt \tag{4.32}$$

$$\langle I_{L_o}(t) \cdot \big(1 - D(t)\big) \rangle = \frac{1}{T} \cdot \int_{t_0}^{t_2} \left(\frac{P^*}{V_o(t)} \right) \cdot (1 - \frac{V_o(t) + L_o \cdot \frac{dI_{L_o(t)}}{dt}}{V_{dc}}) dt \tag{4.33}$$

4.4.2 Switching losses

The switching losses are based on the characteristic of the specific semiconductor. The datasheet specifies the switching energy losses for a given current and voltage magnitude. Average current (4.34) and voltage (4.35) in this circuit is used for normalization of these values. The

expression used for normalization of turn-on energy is (2.5) and for the turn-off energy (2.6).

$$\langle I_{L_o}(t)\rangle = \frac{1}{t_2-t_0}\int_{t_0}^{t_2}\left(\frac{P^*}{V_o(t)}\right)dt \tag{4.34}$$

$$\langle V_{dc}\rangle = V_{dc} \tag{4.35}$$

CHAPTER 5

5 Matlab/Simulink implementation

In order to verify that the requirements on control and dimensioning of the system are fulfilled, simulations have been done, where Simulink has been the chosen simulation tool. To derive the required control parameters, the implementation is separated in two parts. One part is a mathematical implementation which is done with continuous blocks. This to minimize the execution time when determining the control parameters. The other part is a discrete physical implementation done with Simscape/SimPowerSystems components and controls implemented with standard blocks.

At first the capacitor charger is separated into two systems, the DC/DC and the AFE, this to decrease the complexity and execution time. When desired control and dimensioning of the two separate systems are fulfilled, the full system is simulated at different scenarios. The main goal is to fulfill the international grid standards on flicker, low harmonic distortion together with optimized power factor.

As a starting point some parameters have been set initially as a guideline and a way of simplifying the implementation:

- The simulation components are ideal, no losses are included.
- The grid voltage is set to a standard 400 V three phase grid.
- The DC-link voltage is 1100 V with a maximum ripple of 5 %.
- The average power through the system is 200 kW.
- The output voltage from the DC/DC is 1000 V when the load switches, with a precision of better than 1 %.
- The output voltage drop is 15 % when the output load is pulsed.
- The output load pulse frequency is 14 Hz with 5 % duty-cycle.
- The transistor switching frequency is set to 7.5 kHz.
- The mean current ripple of the DC/DC output is 5 %.
- The discrete clock frequency for the controller is 4 MHz.
- The sampling frequency of the I/O-measurement ports is 200 kHz.

- The discrete physical system has a sampling frequency that is 200 times larger than the switching frequency in order to be considered as continuous.

5.1 Simplifications and impact

The physical part of the system is based on the Simscape/SimPowerSystems-library and is as far as the block components allows ideal. This implies that no losses are included in the Simulink model. Due to mathematical modeling the sensor delays and possible lack of sensor precision are not included. The rise and fall time for diodes and transistors are neither included.

Because the combination of different sampled discrete systems the time for simulation is mostly dependent on the smallest step size, the complexity and number of elements in the model. Since the models are quite complex and contains many elements it takes a lot of time to simulate short scenarios. Due to this, the simulations are executed until steady state has been certainly reached. The phase angles, integral values, capacitance voltage, etc. are initially set to optimized values. This also to reduce execution time, in reality this type of concept will be valid due to pre-charging of capacitors.

5.2 System parameters

To implement the model in Simulink some general parameters are required for the system. These parameters are defined in this subchapter and will be final through this chapter.

Table 5.1: General system parameters for simulations.

Notation	**Description**	**Value**
$V_{a,b,c}$	Grid voltage	400 V
V_{dc}	DC-link voltage	1100 V
V_{dist}	Amplitude of grid disturbances	32.5 V
f	Grid frequency	50 Hz
f_s	Transistor switching frequency	7.5 kHz

f_{R_o}	Output pulse frequency	14 Hz
f_c	Cut-off frequency of the grid filter	50 Hz
f_{dist}	Frequency of grid disturbances	325 Hz
ω	Angular frequency	314.16 rad/s
T_s	Physical system sampling time	330 ns
P_{peak}	Peak power	4 MW
$I_{L_o}^{percent}$	Current ripple in DC/DC output inductance	5 %
D_{R_o}	Output pulse width	5 %
F_{sc}	Sampling frequency control	4 MHz
F_{sio}	Sampling frequency I/O-ports	400 kHz
F_s	Sampling frequency discrete system	200*fs Hz

5.3 AFE implementation

The AFE implementations are separated in two parts, one mathematical simulation part and one with a physical representation of the system. In this subchapter the system parameters are calculated and verified. The chapter also comprises the controller implementation together with the physical system and a switched load, without taking into account the flicker and low harmonics. In order to simplify the understanding of the design, the same parameters are used through this chapter.

5.3.1 Dimensioning parameters

The dimensioning parameters presented in Table 5.2 are based on the requirements on flicker and low harmonic current content.

Table 5.2: Dimensioning parameters used for simulation of the AFE.

Notation	Description	Value
L_{conv}	Input converter inductance	0.4 mH
R_{conv}	Input converter resistance	1 mΩ
C_{dc}	DC-link capacitance	5 mF

5.3.2 Control parameters

Parameters for the current controller are calculated based on the parameters in Table 5.1 and Table 5.2 together with equation (3.26) and (3.30). The parameters for the voltage controller are optimized by mainly looking at the phase margin, this is done in subchapter 5.3.3.3.

Table 5.3: Current control parameters used for simulation of the AFE.

Notation	Description	Value
K_c	Converter gain	550
T_c	Converter delay	67 μs

5.3.3 AFE mathematical model

The AFE is controlled by a current control loop in cascade with a voltage control loop. This is done in order to control both the current and voltage. The current control loop is simulated first and then the outer voltage control loop is added.

5.3.3.1 Current controller

The mathematical model for the closed current control loop is set up in the frequency domain. Focus is mainly on achieving reactive power compensation together with a system that follows a given current reference. The system is modeled with an ideal three phase input that is transformed to the d,q-frame, this to control the currents independently. There is also a PI-controller together with a grid voltage feed forward and decoupling of system. The saturation for modulation output and the anti-windup for the

PI-controllers are based on the maximum vector length of the d,q parameters.

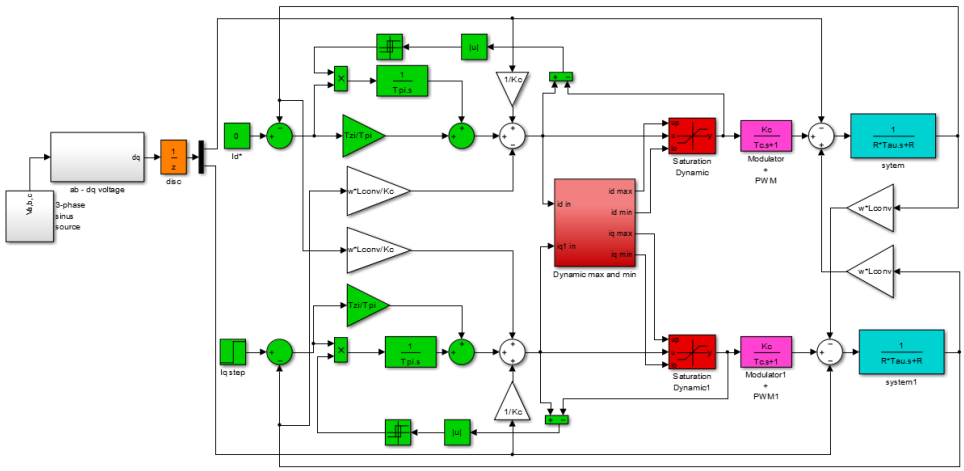

Figure 5.1: The mathematical system of current controller with system.

By inserting the parameters from Table 5.1, Table 5.2 and Table 5.3 the bode-diagram for the system (Figure 5.1) is achieved (Figure 5.2).

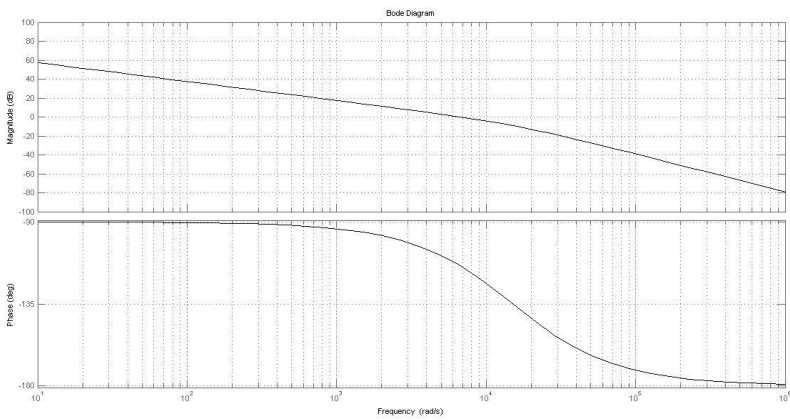

Figure 5.2: Bode diagram for the AFE current controller, with optimized parameters in open loop.

5.3.3.2 Voltage controller

The closed loop voltage controller is also modeled in the frequency domain. It consists of the current controller together with the system, modeled as a

first order transfer function (3.32). This together with the PI-controller, feed forward of the load current and a model of the DC-link capacitance. The step-response of the absolute current controller and of the simplified first order system is compared to ensure valid approximation (Figure 5.4).

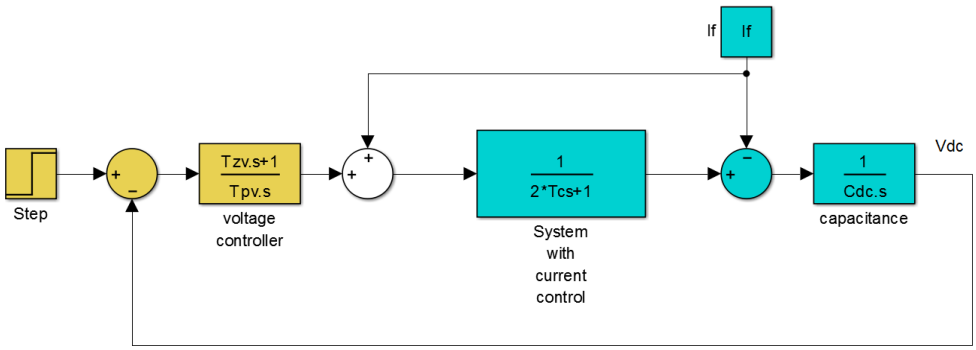

Figure 5.3: The mathematical system of voltage controller with system.

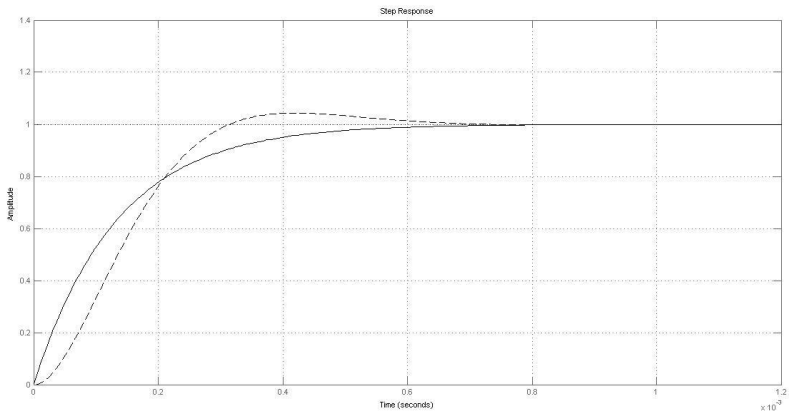

Figure 5.4: Step response of first order simplified current controller with system (not dashed) and absolute current controller with system (dashed).

5.3.3.3 Calibration of control parameters for voltage controller

The parameters from Table 5.1 and Table 5.2 are inserted into the equations for T_{zv} (3.35) and T_{pv} (3.37). In order to determine these parameter values the open-loop transfer function (3.34) bode diagram is plotted, Figure 5.5. The parameter a is determined by choosing the phase margin as mentioned

before, subchapter 3.2.7, to a value that combines speed and stability, the phase margin φ_m is chosen to 60˚.

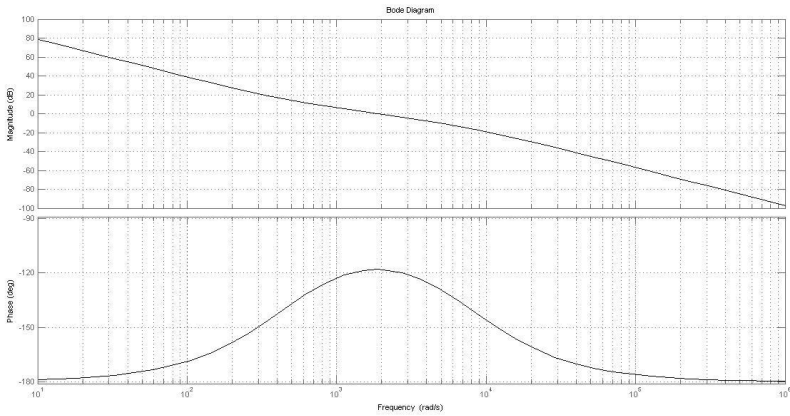

Figure 5.5: Bode diagram for AFE voltage controller in open loop, a=4.

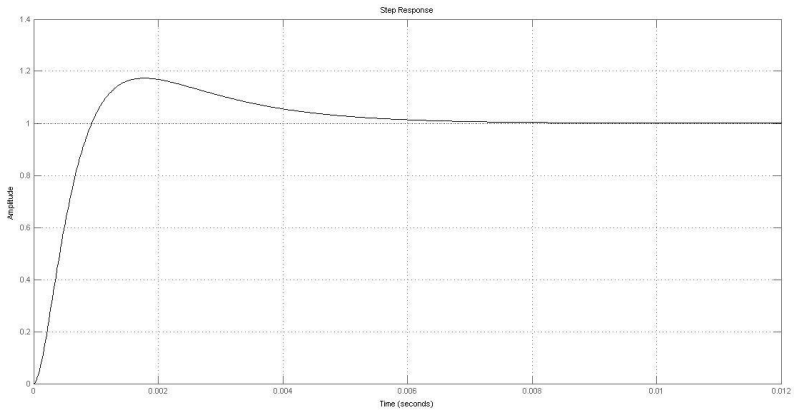

Figure 5.6: Step response for AFE voltage controller, a=4.

Table 5.4: Calibrated parameters for voltage controller.

Notation	**Description**	**Value**
a	Gain	4
T_{zv}	Voltage control	0.0021

	gain	
T_{pv}	Voltage control gain	2.2756e-04

5.3.4 Implementation in Simulink

A complete overview of the simulation system can be viewed in Figure 5.7. The sampling block works as I/O-ports sampling delays and discretization which would exist in a real implementation on a NI Compact Rio platform, etc. On the AC-side of the AFE a 3-phase low voltage grid is connected, a capacitance in parallel with a switched load is connected to the DC-link. Blocks fulfilling functions for control and PWM are investigated more in the following subchapters.

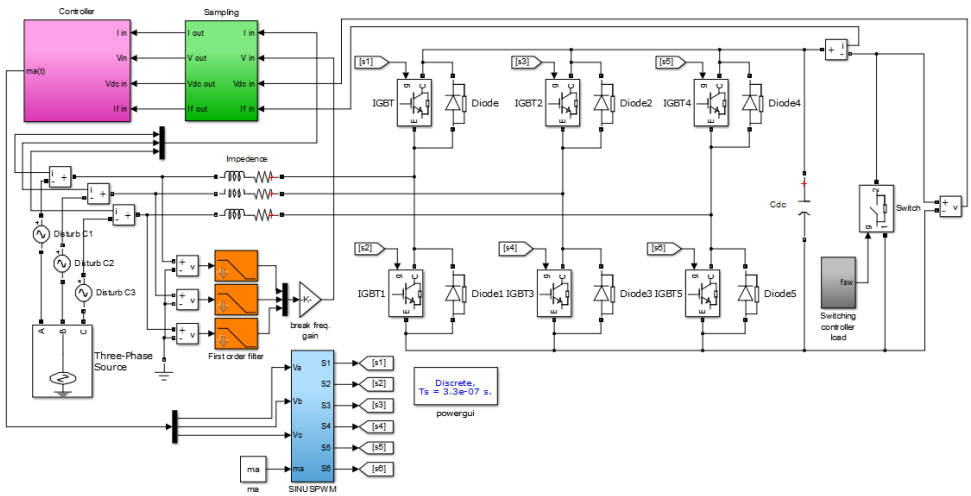

Figure 5.7: AFE simulation model overview.

5.3.4.1 PWM

In order to control the AFE, PWM-signals are created for each pair coupled transistors, where one signal per transistor pair is inverted. Dead-time generations are implemented to avoid short circuits in the system. The dead-time is usually integrated in the transistor drivers, and in this case set to the sampling frequency of the physical system, T_s.

5.3.4.2 Current controller

The current controller implementation (Figure 5.8) is basically the same as the mathematical model in chapter 5.3.3.1. The major difference is that discretization and the feed-forward of I_f are implemented.

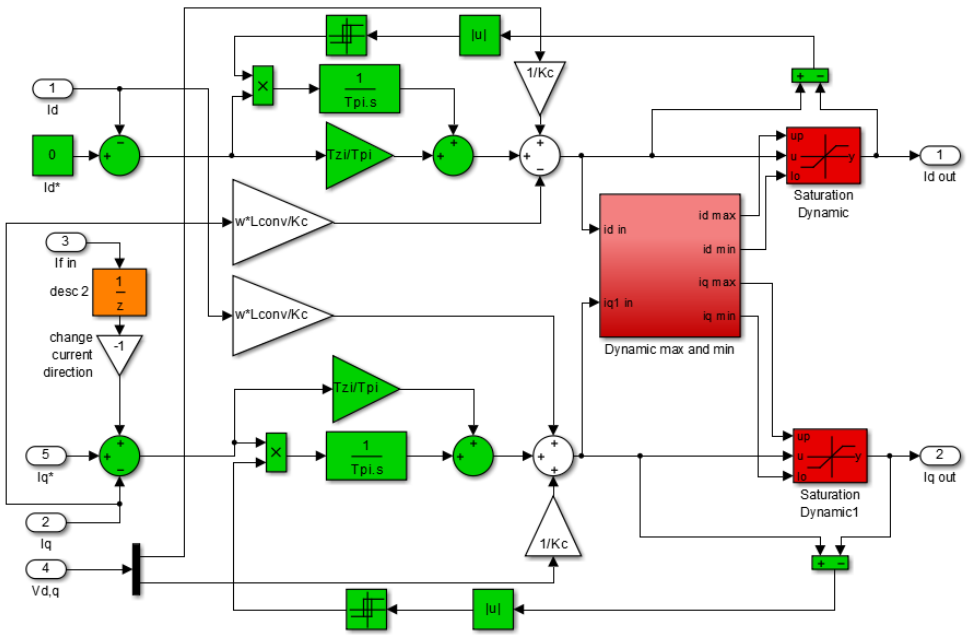

Figure 5.8: Current controller for the AFE.

5.3.4.3 Voltage controller

The voltage controller is the outer loop in the cascade coupled system and consists of a PI-controller. The saturation for the integral part is based on the maximum output current that is allowed for the system. Due to the current measurement direction, the output sign is changed.

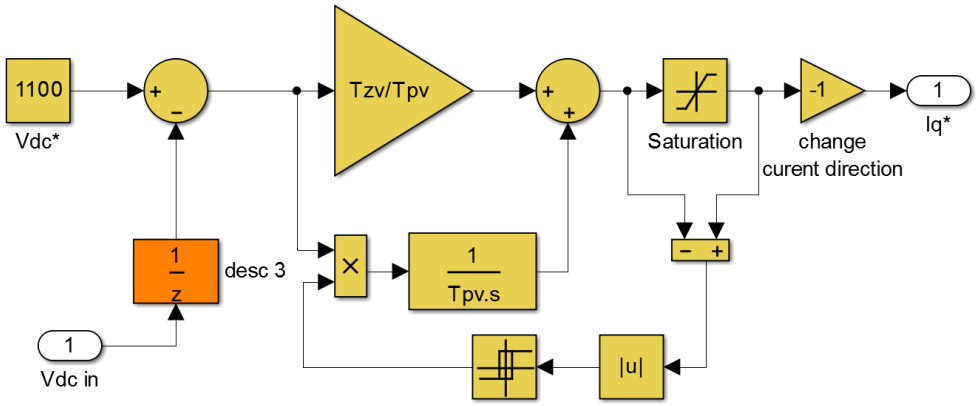

Figure 5.9: Voltage controller for AFE**.**

5.3.4.4 Transformation

The transformation block is based on the equations from AFE chapter 3.2, amplitude invariance is used as a basis for the transformation. Due to phase and amplitude impact from the grid filter compensation is done to achieve correct values, more in detail subchapter 2.5.

5.3.4.5 Grid measurement filter

Due to harmonics and flicker on the grid the input signal is filtered. This is done by three low pass filters, one for each phase that damps the noise. Transformations are based on grid voltage measurement and therefore compensation for this is done.

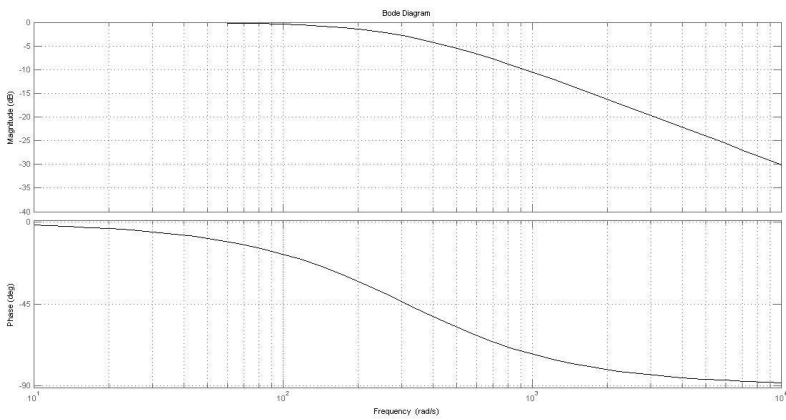

Figure 5.10: Bode plot of 50Hz filter.

From (2.11) and (2.12) the gain and phase impact for a cut-off frequency of 50 Hz is calculated:

$$\tau = \frac{1}{2 \cdot \pi \cdot f_c} \tag{5.1}$$

$$|G(s)| = \frac{1}{\sqrt{2}} \tag{5.2}$$

$$\arg\big(G(s)\big) = -45^{\circ} \tag{5.3}$$

5.3.4.6 Output load

The switching characteristic of the DC/DC is represented initially as a constant load, which sinks the same amount of power in average (200 kW). The output resistance is calculated for a given DC-level, power and the DC/DC output voltage.

$$\begin{cases} P = V_{dc} \cdot I_f \cdot D \\ V_{dc} = R_{dc} \cdot I_f \end{cases} \rightarrow R_{dc} = \frac{V_{dc}^2}{P} \cdot D = \frac{1100^2}{200 \cdot 10^3} \cdot \frac{1000}{1100} = 5.5\Omega \tag{5.4}$$

Table 5.5: Constant equivalent DC-link load.

Notation	**Description**	**Value**
R_{dc}	DC-link resistance	5.5Ω

The current I_f is switched and to ensure a good feed-forward to the controller a mean value is constructed.

5.3.5 Results from implementation

A restriction for the AFE is that the DC-link voltage should maximally differ 5 % from the reference. Another restriction is that the power factor should be optimized when the system is in steady state. Looking at Figure 5.11 and Figure 5.12, the average power is 200 kW. The DC-link voltage is dropping 2 % in the start and has a voltage ripple of 0.2 % at steady state. The input currents on the AC-side are sinusoidal shaped with the transistor

switching ripple on top of the 50 Hz fundamental. A summary of the results from implementations can be seen in Figure 5.11 and Figure 5.12.

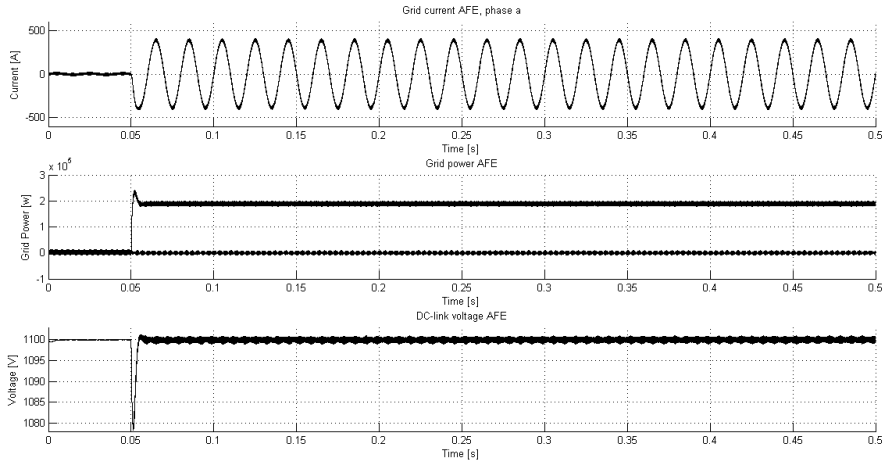

Figure 5.11: Plots from simulations with output quantities; grid current, power from grid (Q @ ~ 0 kW, P @ ~ 200 kW) and DC-link voltage.

Due to possible disturbances on the grid a disturbance-source is implemented on each phase to represent this. The impact of the DC-link voltage is the reduced due to the grid filters and remains constant and stable (Figure 5.12).

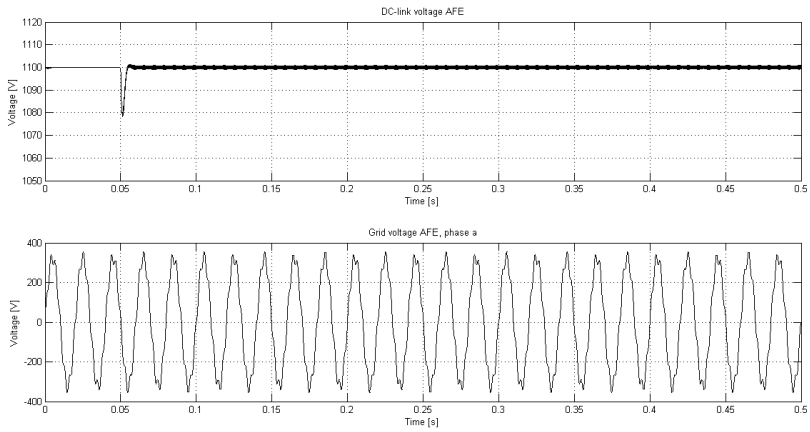

Figure 5.12: Plots from simulations with output quantities; DC-link voltage, grid voltage with disturbances @ 325 Hz, 32.5 V.

5.4 DC/DC implementation

The DC/DC implementations are separated in two parts, as for the AFE, one part with a strict mathematical model and one part with a physical representation of the system. System control parameters and dimensioning are via these models calculated and verified. This subchapter also comprises an implementation of the control and a physical system with the output load modeled as a switch, representing the pulsing power drawn. When simulating the DC/DC-converter a solid DC-voltage source is assumed on the input, represented as an ordinary DC-voltage source. The simulation parameters are based on equations from subchapter 4.3 and system parameters defined in Table 5.1.

5.4.1 Dimensioning parameters

In this chapter are the dimensioning parameters calculated with help of the theory described in subchapter 4.3. The inductance dimensioning from this subchapter is though not a guaranty for good current ripple all the time, since it is based on average values. To ensure that the current ripple is limited, all the time, the most critical situation must be evaluated. This critical situation occurs when the load is switched on and sinks power, where the current magnitude is determined. To get the converter output current to ripple on this change, the inductor must be dimensioned for four times this magnitude as a rule of thumb. The inductance calculated for this purpose is defined as L_{check} and expressed in equation (5.5).

$$L_o^{check} = \frac{V_{dc} - \bar{V}_o}{4 \cdot \frac{I_{L_o}^{max} - I_{L_o}^{min}}{t_1 - t_0}} \tag{5.5}$$

The smallest inductor is chosen, under the restriction that the basic current doesn't ripple over restraining conditions, $I_{L_o}^{percent}$. Calculation of inductances from (2.17) and (5.5) will generate $L_o = 1.8\,mH$ and $L_o^{check} = 4.5\,mH$ where the smallest inductance is chosen, $L_o = 1.8\,mH$.

Table 5.6: Calculated dimensioning parameters for simulation models (*Calculated under section 5.4.4.5).

Notation	Description	Value

C_o	Output capacitance	97.7mF
L_o	Output inductance	1.8mH
R_o*	Switched output load resistance	214mΩ

5.4.2 DC/DC mathematical model

This model is set up with help of the system model in frequency domain (4.5) and equation for capacitor voltage (4.6). It is a model of the current control with feed forward of the output voltage in cascade with a voltage controller. The converter is modeled as a delay, which is described in (4.2.1). Further details can be investigated in chapter 4.2. Anti-windup is implemented to prevent unrealistic output values.

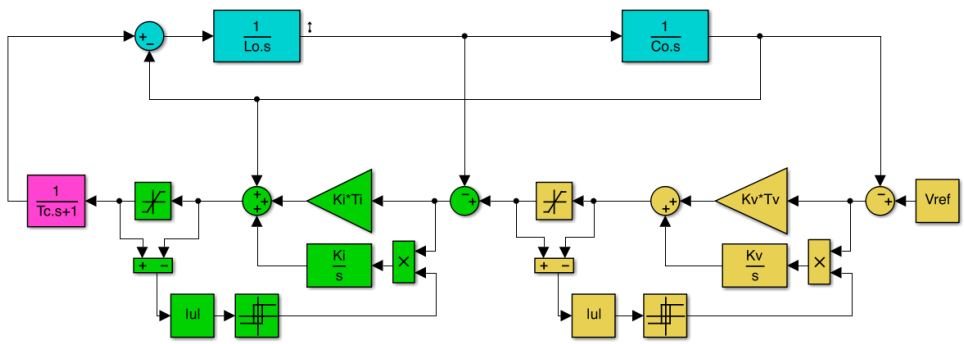

Figure 5.13: Mathematical model of current and voltage control system.

5.4.3 Calibration of control parameters

To calibrate control parameters for both the current controller and voltage controller, bode-diagrams are used. A phase margin φ_m of 60 degrees is the criterion for the systems to be considered both stable and fast enough. Corresponding step responses are also checked to make sure the system is stable.

5.4.3.1 Calibration of current controller

Parameters calibrated for the current control system can be seen in Table 5.7.

Table 5.7: Calibrated parameters for current control.

Notation	Description	Value
K_i	Gain	5
T_i	Gain	3

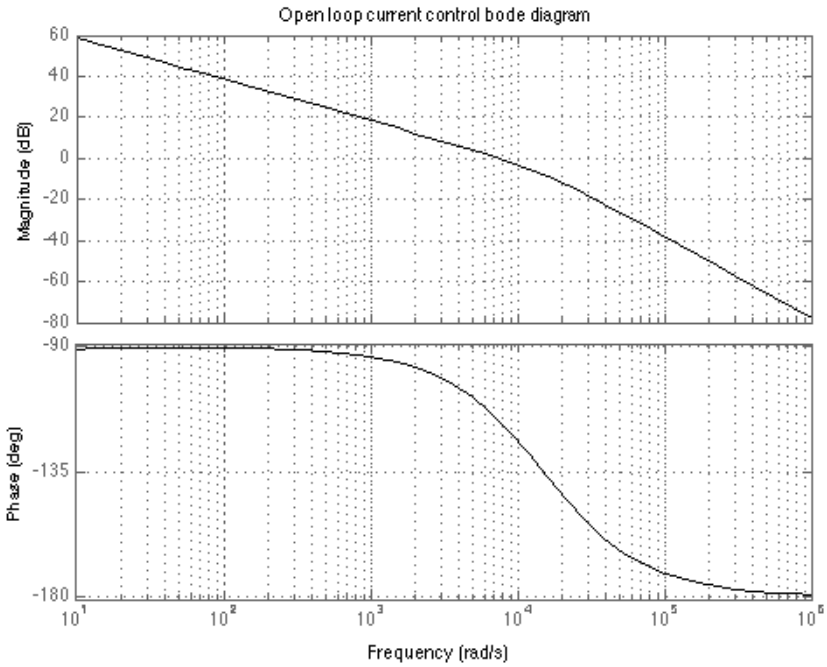

Figure 5.14: Bode diagram of the open loop current control system with a phase margin of 60 degrees.

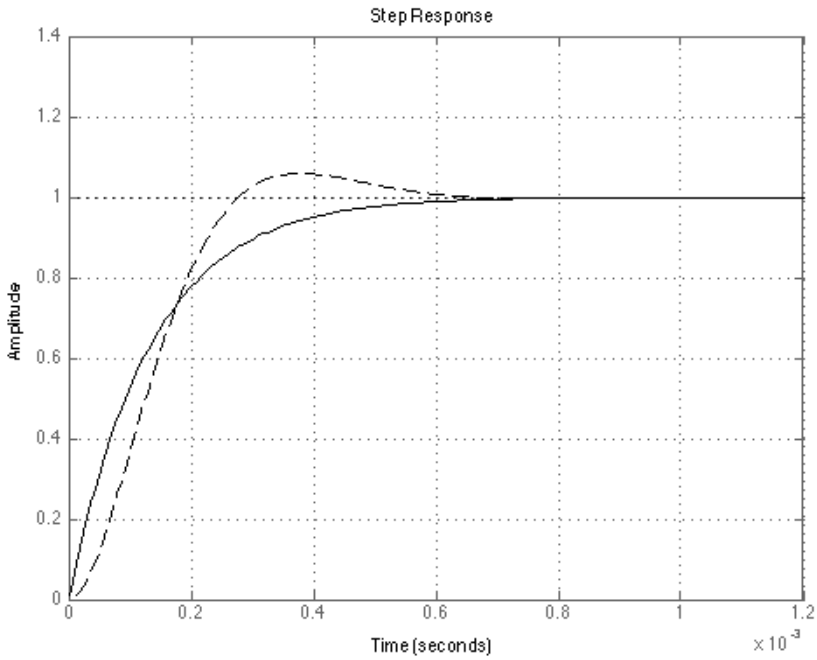

Figure 5.15: Step response for the current control (dashed line) and an approximated first order version of this control (non-dashed line).

5.4.3.2 Calibration of voltage controller

An approximation of the current control as a first order system is used to simplify transfer functions and validation of parameters (4.11). The step-responses can be seen in Figure 5.15. Parameters calibrated for the voltage control system from Bode-diagrams in Figure 5.16 and step-response in Figure 5.17 can be seen in Table 5.8.

Table 5.8: Calibrated parameters for voltage control.

Notation	**Description**	**Value**
K_v	Gain	0.5
T_v	Gain	9

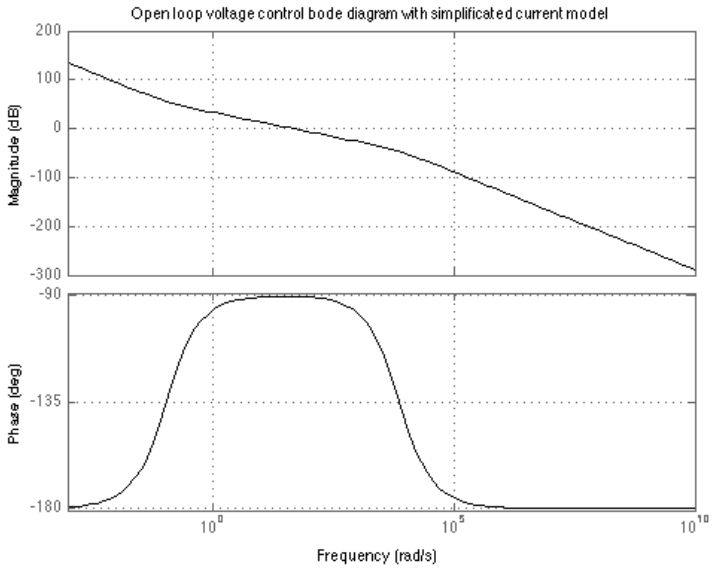

Figure 5.16: Bode diagram of the open loop voltage control system with a phase margin of at least 60 degrees.

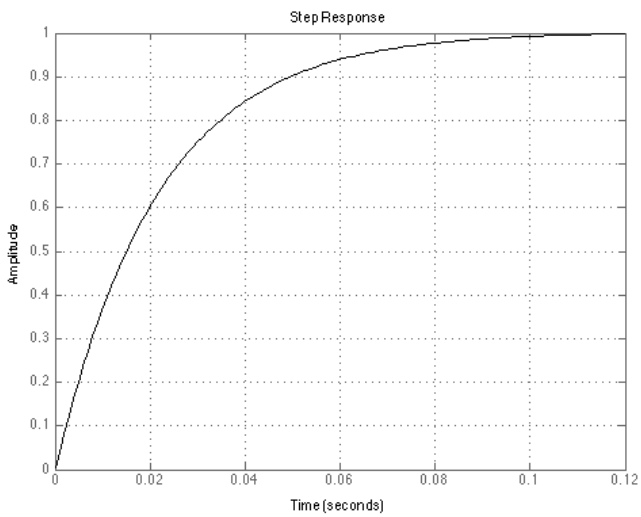

Figure 5.17: Step response of the mathematical voltage model with calibrated parameters.

Notation can be done regarding the phase margin to be almost around 90 degrees in voltage controller. When reducing the phase margin to a level

that is closer to 60 degrees, Figure 5.16, saturation is reached and therefore such parameters should be avoided.

5.4.4 Implementation in Simulink

A complete overview of the simulation system can be viewed in Figure 5.18. The sampling blocks are working as I/O-ports sampling delays and discretization which would exist in a real implementation on a NI Compact Rio platform, etc. On the output a switch with resistive load in series connected to a pulse generator is used for simulation of the pulsing power. Blocks fulfilling functions for control and PWM are investigated more in the following subchapters.

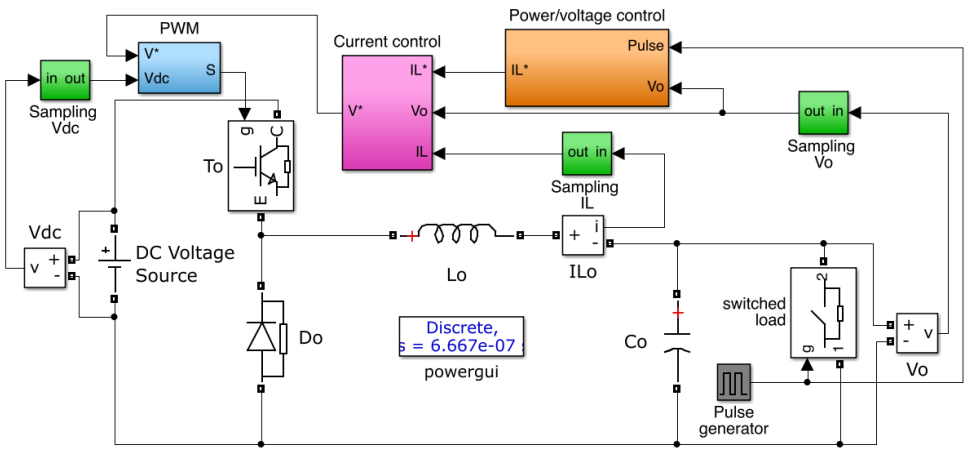

Figure 5.18: Extraction from simulation model of the complete DC/DC simulation system.

5.4.4.1 PWM implementation

The PWM implementation is constructed with a discretized DC-voltage representing the discrete time in a controller. The reference voltage is compared with a triangular wave creating switched pattern for the transistor.

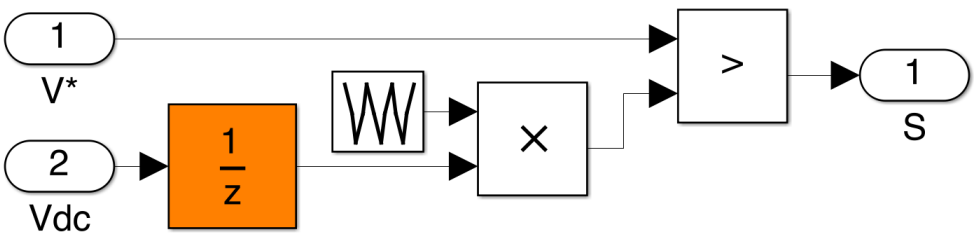

Figure 5.19: Extraction from simulation model of the PWM structure.

5.4.4.2 Current control implementation

The current control is very similar to the mathematical model shown in subchapter 5.4.2. Apart from the mathematical model a discretization of feed forward output voltage and inductance current are implemented.

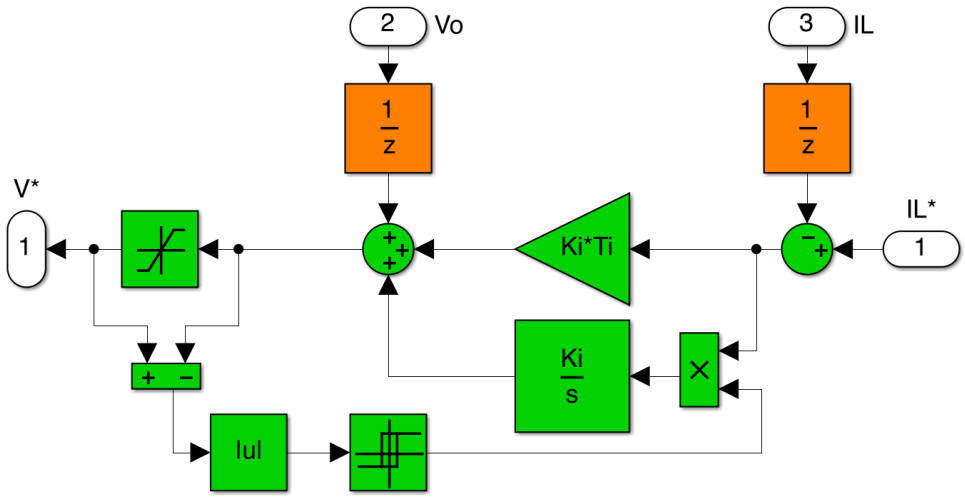

Figure 5.20: Extraction from simulation model of the current control structure.

5.4.4.3 Voltage and power control implementation, type 1

The voltage control implementation is done in the same way as for the mathematical model (5.4.2). The difference is the implementation of power control. A hysteresis checks if the output voltage is high or low and then controls a switch making the decision between power- or voltage-control. Voltage measure-block helps to construct and declare the lowest voltage point when drawing power and also to determine the maximum voltage reached in a cycle. These values are then used for calculation of the power prediction and correction described in subchapter 4.2, the equations are placed in blocks denoted f(u) in Figure 5.21.

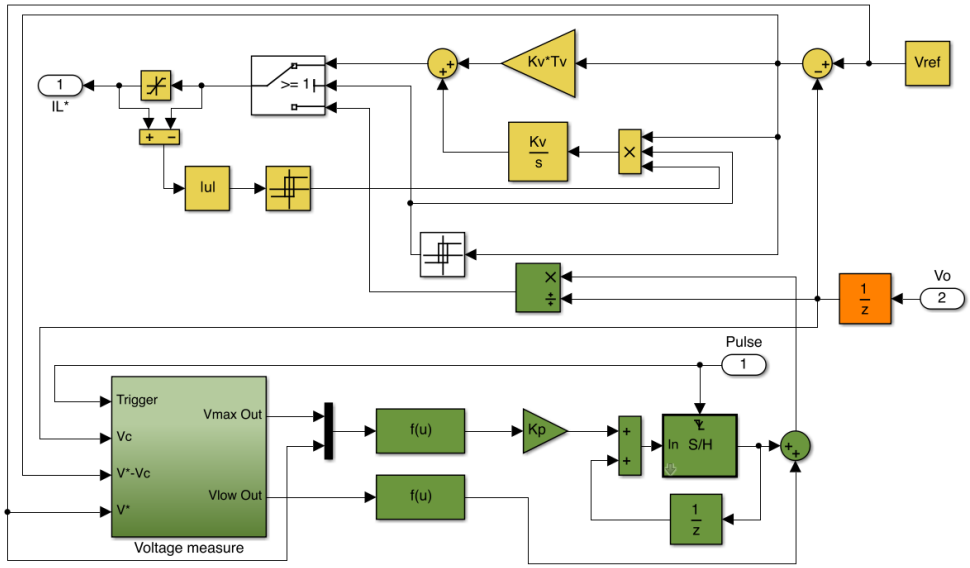

Figure 5.21: Extraction from simulation model of the voltage and power control type 1.

5.4.4.4 Voltage and power control implementation, type 2

Voltage implementation in type 2 is identical with the one for type 1 (5.4.4.3) and are therefore not further explained. A hysteresis will also check if voltage is high or low but in this case switch input reference between the constant V_o^{max} and ramp function (4.19). Voltage measure-block helps to construct and declare the lowest voltage point when drawing power and also to determine elapsed time since most recent pulse. These values are then used as inputs to (4.19).

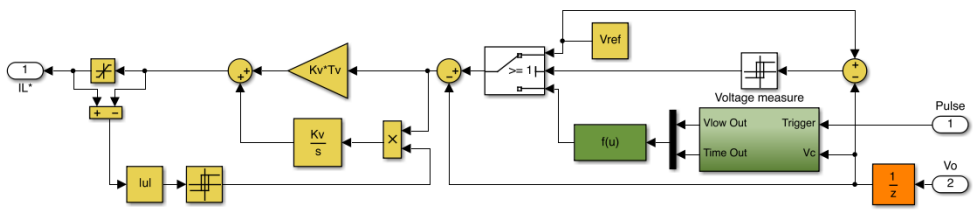

Figure 5.22: Extraction from simulation model of the voltage and power control type 2.

5.4.4.5 Pulsing power output implementation

The objective is to sink a peak power of 4MW to a load through the DC/DC. With an average voltage of 925V on the output, the resistance for simulation can be calculated (5.6). Notation can be done regarding the

somewhat confusing symbol of the switched load (Figure 5.23), Simulink symbol is not correct because the resistance is in series.

$$R_o = \frac{\bar{V}_o^{\,2}}{P_{peak}} = 0.214\ \Omega \tag{5.6}$$

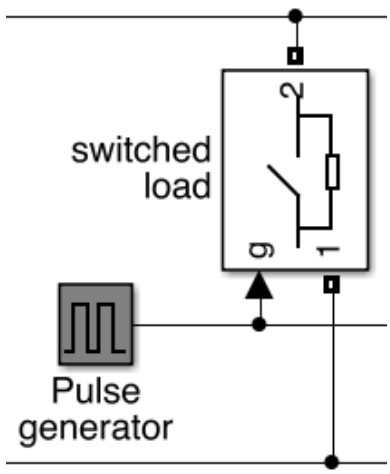

Figure 5.23: Extraction from simulation model of the switched output load.

5.4.5 Results from implementation

A restriction for the DC/DC-converter is that the output voltage should maximally differ 1 % from the reference when load is pulsing. Another restriction is that a constant supplied power should be fed into the system in steady state. A summary of the results from the DC/DC simulations can be seen in Figure 5.24 for power control type 1. Looking at the different graphs the average power drawn when pulsing is 200 kW and a close to perfect voltage change between 850 V and 1000 V is obtained. Accuracy on the output voltage is better than 0.1% starting from the first pulse and approximately 0.01 % in steady state after 3 pulses, which is remarkably good. Ripple on power is unfortunately something that can't be eliminated due to the switched environment. The current ripple will be reflected on the power, which has the same percentage of ripple and period as the current. In this case the current and also the power ripple are 5 % and 7.5 kHz as specified in the simulation parameters.

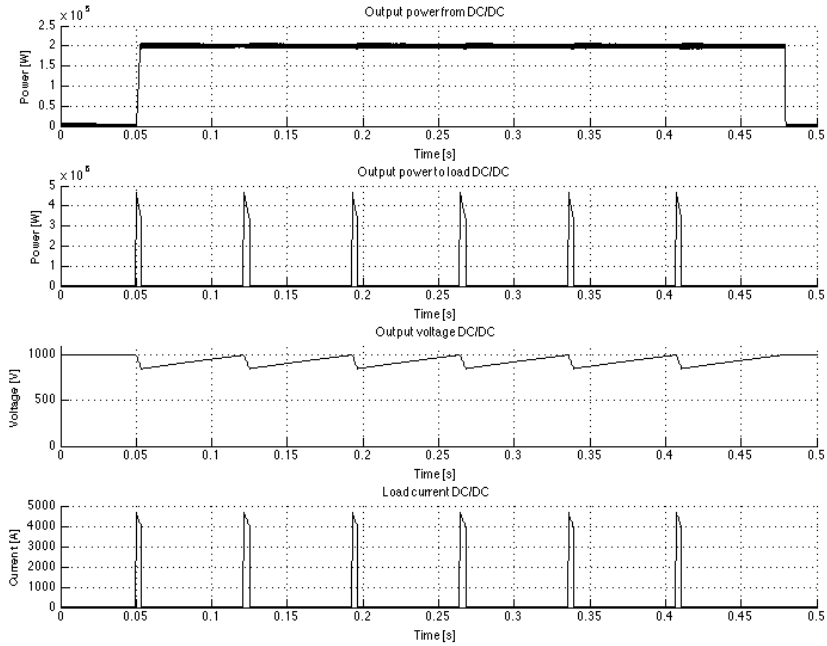

Figure 5.24: Plots from simulations with output quantities; power from DC/DC, power to load, output voltage and load current.

The summary of results from implementation with power control type 2 can be seen in Figure 5.26 at the output voltage ripple it looks almost perfect between 850 V and 1000 V. Accuracy on the output voltage meets the criterion, less than 0.5 % starting from the first pulse and is reduced over time. Unfortunately a couple of imperfections can be observed when looking at the power. The fluctuations in power are in worst case almost 75 % in respect to the average power of 200 kW. This fluctuation occurs when the load is switched on and off. Because of the changed reference level for the voltage control in this situation, a couple of milliseconds delay is present before adapting. This can be verified by looking at the voltage ripple in detail, where the voltage has a non-linear behavior in the beginning and ends up with a stationary error (Figure 5.25). If the stationary error should be eliminated, control parameters would have to be chosen in a way that makes the system unstable and are therefore not implemented. All these things reflect back on the power with a big impact.

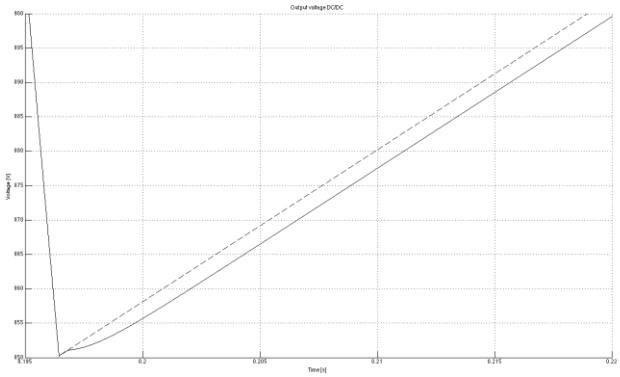

Figure 5.25: Zoomed plot of output voltage (non-dashed) and the reference for output voltage (dashed) according to power control type 2.

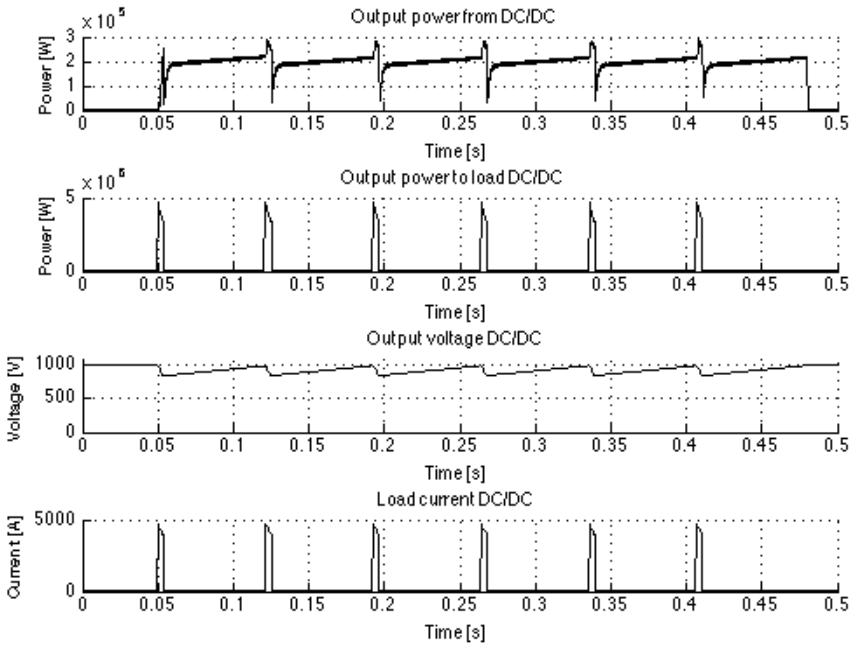

Figure 5.26: Plots from simulations with output quantities; power from DC/DC, power to load, output voltage and load current (type 2 power control).

By comparing the two power controls, type 1 is the absolute best and most preferable. The output voltage accuracy in type 1 is better than in type 2

already from the start and the power stays perfectly around 200 kW with not more deviation than the current ripple. By these evaluations power control type 1 is the only one treated further on.

5.5 Full system implementation

The two systems, AFE and DC/DC, is in this chapter put together into one system. The system shall still be able to fulfill the requirements on precisions together with optimal power factor and constant power. In this chapter flicker and low harmonic distortions are discussed as a part of the dimensioning. Components and control parameters will be chosen to fulfill the requirements and IEC-standards. A non-ideal grid as voltage supply will be introduced to simulate a more realistic scenario. The full system implementation includes setups for three different power levels, 200 kW, 100 kW and 50 kW.

5.5.1 Dimensioning of a realistic grid

In conventional transformer datasheets there is a parameter describing the transformer's characteristic when short-circuited. The percentage is the fraction of nominal voltage level that the transformer should have at its input to reach nominal current when short-circuited. This percentage is often around five percent, $u_{cc} = 5\ \%$, and the nominal voltage is $V_N = 230\ V$.

The rated transformer power, S_N, is in the case of ESS distribution network 250 kW. Nominal current through the three phases is calculated by (5.7).

$$I_N = \frac{S_N}{\sqrt{3} \cdot 400} = \frac{250kW}{\sqrt{3} \cdot 400} = 360.8\ A \tag{5.7}$$

Short circuit test condition:

$$u_{cc} \cdot V_N = \omega \cdot L \cdot I_N \tag{5.8}$$

Valid grid inductance to be used:

$$L_{grid} = \frac{u_{cc} \cdot V_N}{\omega \cdot I_N} = \frac{0.05 \cdot 230 \cdot \sqrt{3} \cdot 400}{2 \cdot \pi \cdot 50 \cdot 250 \cdot 10^3} = 101\ \mu H \tag{5.9}$$

5.5.2 Simulation parameters

At the different power levels the dimensioning of the system will change, which will impact the control parameters. The phase margin is kept to at least 60 degrees in all controllers, for AFE subchapter 5.3.2 and DC/DC subchapter 5.4.2.

Table 5.9: Calculated dimensioning parameters used for simulation of the full system.

Notation	**Value @ 200 kW**	**Value @ 100 kW**	**Value @ 50 kW**
L_{conv}	0.4 mH	0.8 mH	1.6 mH
R_{conv}	1 mΩ	1 mΩ	1 mΩ
C_{dc}	5 mF	2.5 mF	1.25 mF
L_o	1.8 mH	3.6 mH	7.2 mH
R_o	0.214 Ω	428 mΩ	856 mΩ
C_0	97.7 mF	48.9 mF	24.5 mF

Table 5.10: The control parameters used for simulation of full system.

Notation	**Value @ 200 kW**	**Value @ 100 kW**	**Value @ 50 kW**
T_{zi}	0.4	0.8	1.6
T_{pi}	73.3	73.3	73.3
a	4	4	4
T_{zv}	0.0021	0.0021	0.0021
T_{pv}	2.2756e-04	4.5511e-04	9.1022e-04
K_i	5	5	5

T_i	3	3	3
K_v	0.5	0.5	0.5
T_v	9	9	9

The system parameters are kept the same as previous implementations in DC/DC and AFE.

5.5.3 Full system simulation

The AFE and the DC/DC is connected and simulated at three different scenarios. A complete overview of the simulation system can be viewed in Figure 5.27. The system is initially put at steady state.

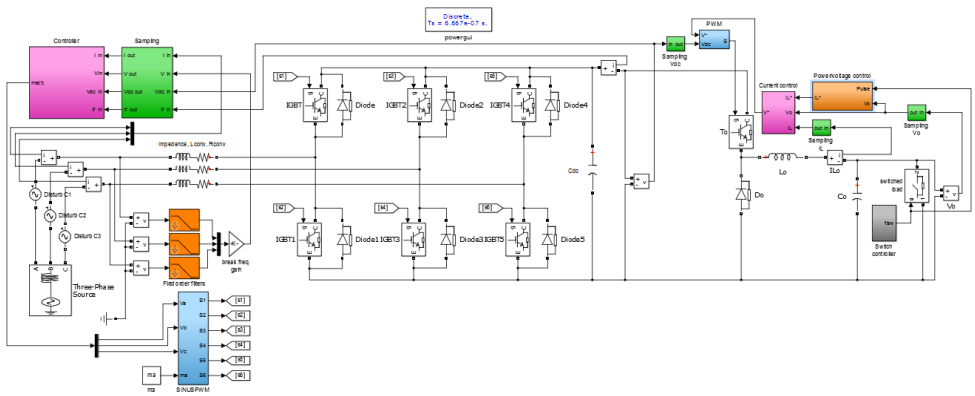

Figure 5.27: Extraction from simulation model of the complete full system.

5.5.4 Results from implementation

When the full system is simulated, the same restrictions apply for all three scenarios. The main results of these simulations are presented in Figure 5.28-5.36. By evaluating the figures, following results are achieved for all three scenarios:

- The current absorbed from the grid is sinusoidal shaped with a high frequency switching ripple on top.
- The power is constant with reactive power compensation, when the output load is pulsing.
- The output voltage precision is better than 0.1 % at the first pulse and better than 0.01% at steady state.

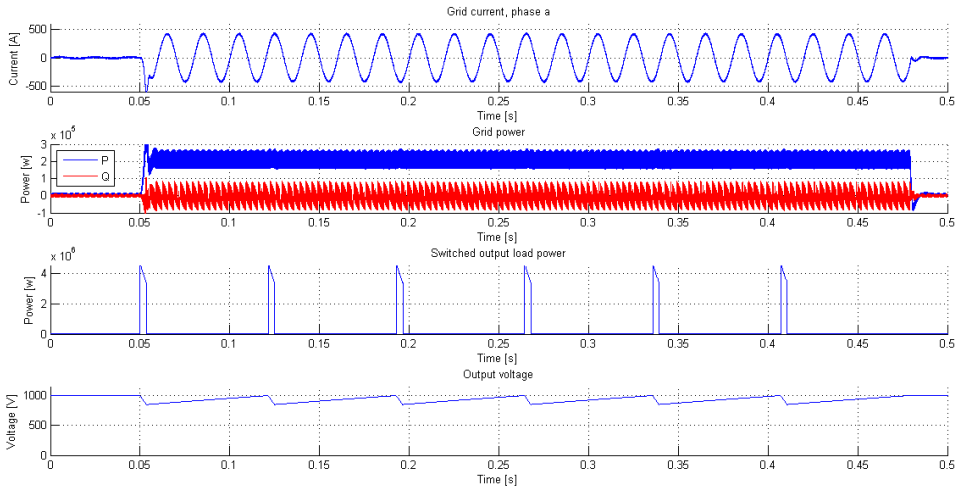

Figure 5.28: Plots from 200 kW simulations with output quantities; Grid current in phase a, active and reactive grid power, switched output load power, output voltage.

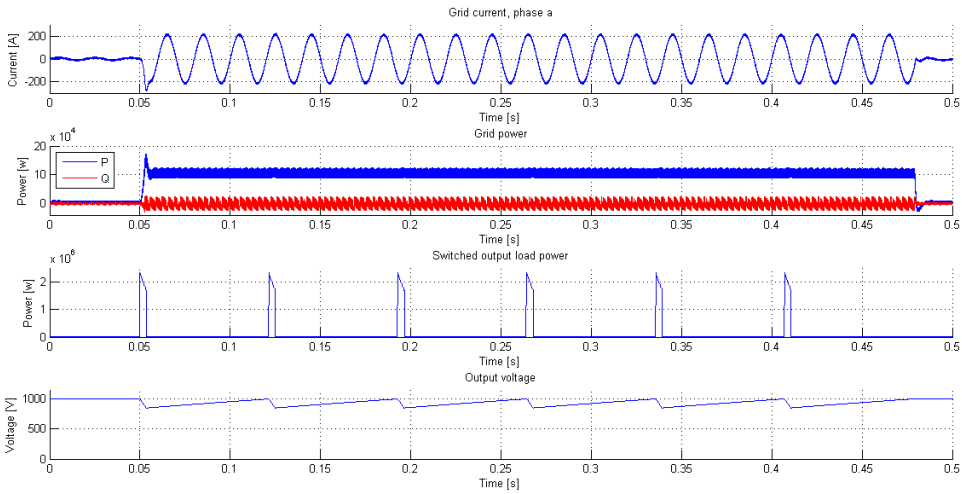

Figure 5.29: Plots from 100 kW simulations with output quantities; Grid current in phase a, active and reactive grid power, switched output load power, output voltage.

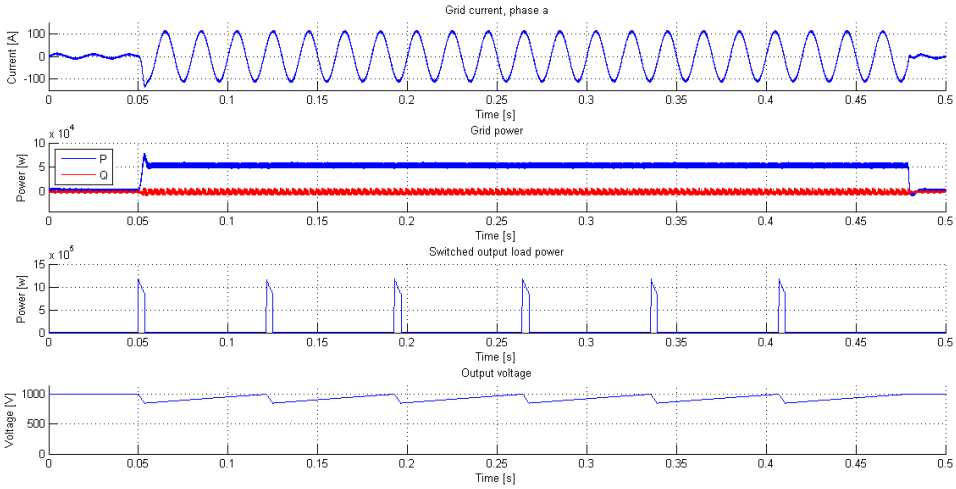

Figure 5.30: Plots from 50 kW simulations with output quantities; Grid current in phase a, active and reactive grid power, switched output load power, output voltage.

5.5.4.1 Low harmonic current

An FFT analysis of the line current is performed in one of the phases only, due to symmetry reasons. The FFT analysis is done with the internal "power_fftscope"-function in Matlab. The function will provide a graph with the harmonics compared to the 50 Hz fundamental frequency.

Due to long execution time for short simulation scenarios, the analysis is done when the system is in steady state (time between 0.05 s and 0.45 s) for three sinus periods instead of during a 1.5 s period required by the standard. For more information see chapter 3.4.2.

Table 5.11: The low harmonic current for phase a in the full system.

Power level / **Harmonic order**	**Harmonics @ 200 kW**	**Harmonics @ 100 kW**	**Harmonics @ 50 kW**
2	0.8 %	0.11 %	0.07 %
3	0.06 %	0.11 %	0.05 %
5	0.16 %	0.2 %	0.16 %

7	0.18 %	0.1 %	0.09 %
9	0.02 %	0.04 %	0.03 %
11 ≤ n ≤ 39	< 1.5 %	< 1.5 %	< 1.5 %

The harmonic content is presented in Figure 5.31-5.36, where the 10 first harmonic orders are presented in a separate graph. The higher harmonic orders (Harmonic order > 10) are shown in a frequency diagram where the limit is marked with a dashed line.

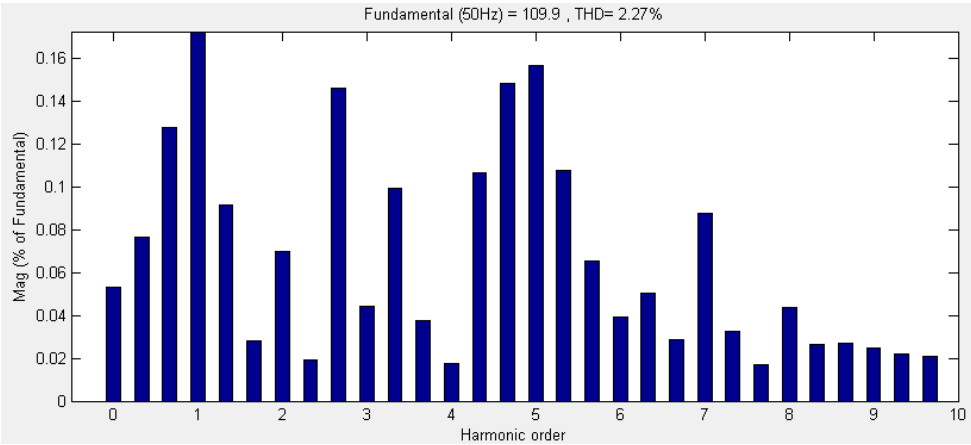

Figure 5.31: Low harmonic current content for 50 kW in phase a.

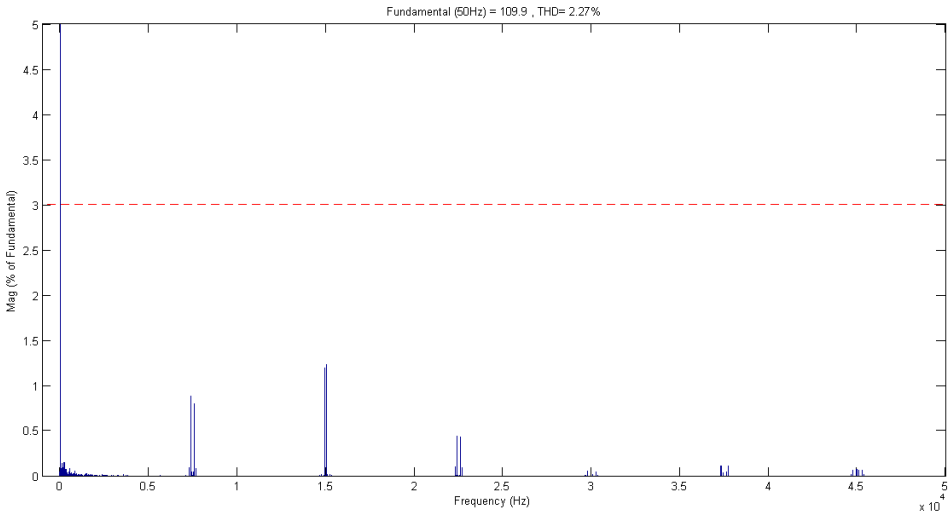

Figure 5.32: Harmonics up to 50 kHz in phase a for 50 kW, together with the limit from the standard for harmonic order $11 \leq n \leq 39$ (marked as a dashed line).

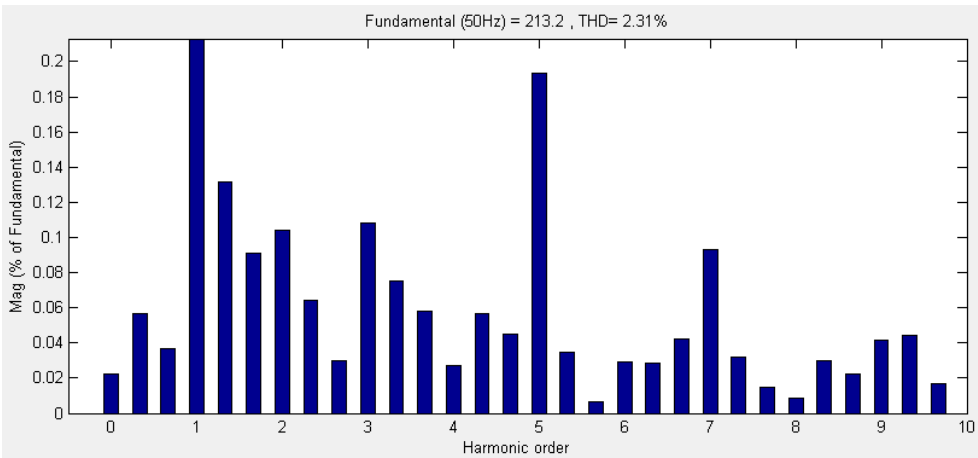

Figure 5.33: Low harmonic current content for 100 kW in phase a.

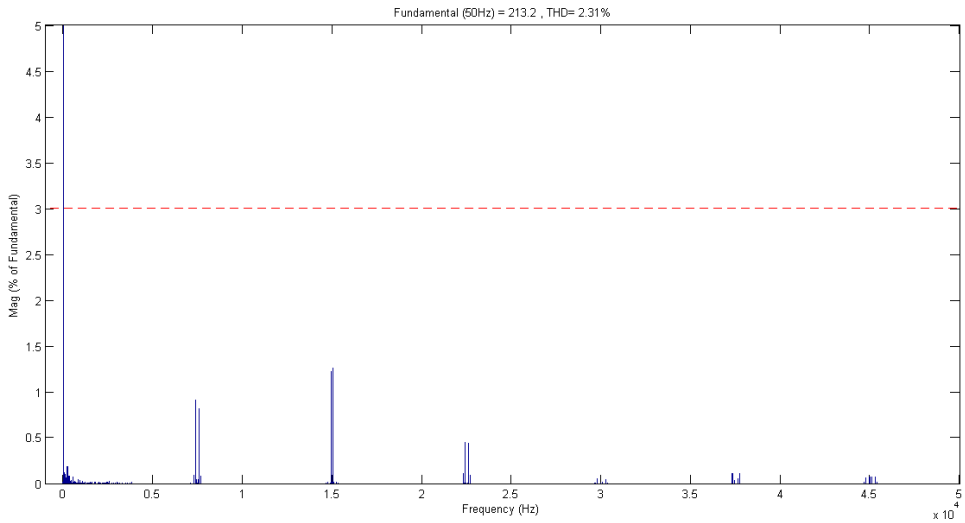

Figure 5.34: Harmonics up to 50 kHz in phase a for 100 kW, together with the limit from the standard for harmonic order $11 \leq n \leq 39$ (marked as a dashed line).

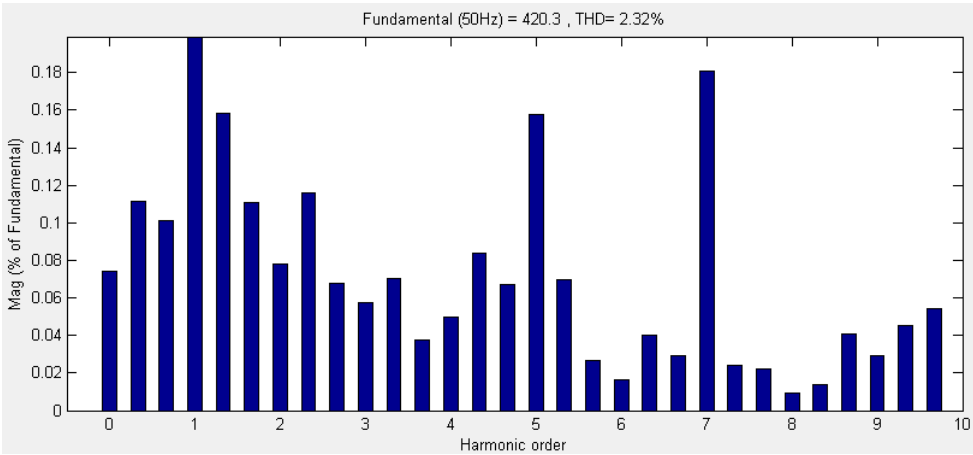

Figure 5.35: Low harmonic current content for 200 kW in phase a.

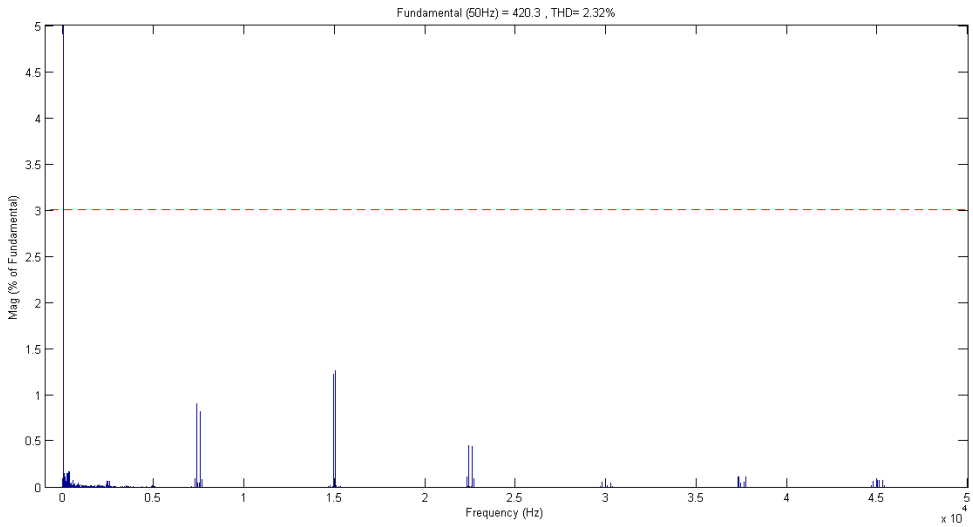

Figure 5.36: Harmonics up to 50 kHz in phase a for 200 kW, together with the limit from the standard for harmonic order $11 \leq n \leq 39$ (marked as a dashed line).

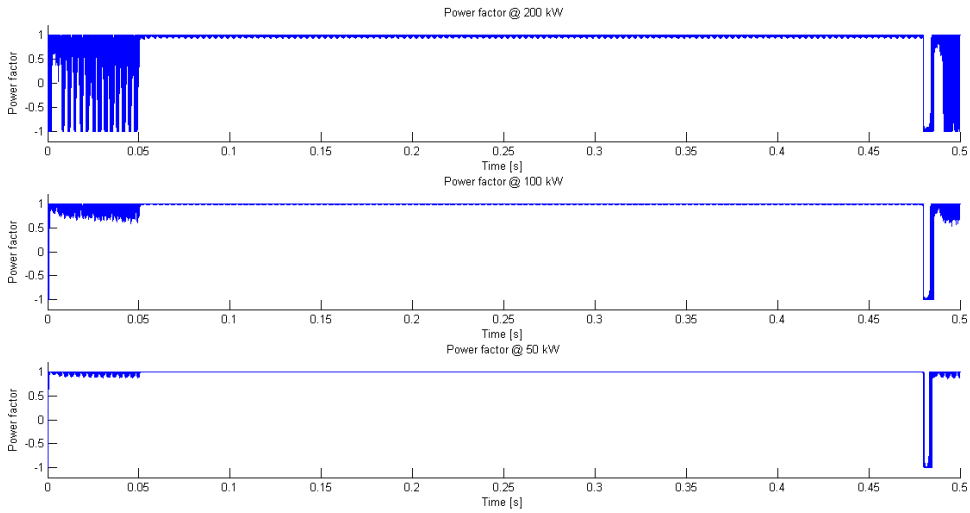

Figure 5.37: Power factor for the three rated power levels.

5.5.4.2 Flicker level

The flicker level is measured by taking the maximum voltage level difference in all three phases and compare with the grid peak voltage $\widehat{V}_{a,b,c} = 325\ V$.

$$\max\left(\frac{\Delta V}{\hat{V}_{a,b,c}}\right) < 0.3\ \%\ @\ 14\ Hz \tag{5.10}$$

Equation (5.10) shall be fulfilled, where ΔV is the voltage difference between minimum and the maximum voltage level at the measurement points, see Figure 3.16. In order to verify the full functionality for the three rated power levels, measurements are done during the following scenario:

1. No pulsing output load.
2. Pulsing output load.
3. No pulsing output load.

The results on flicker levels for the three different power levels can be seen in Table 5.12. These results are derived from the information in Figure 5.38-5.40, where the time in steady state is the only time range considered.

Table 5.12: Flicker level for the three rated power levels.

Power level	**Flicker level**
200 kW	0.059 %
100 kW	0.019 %
50 kW	0.0078 %

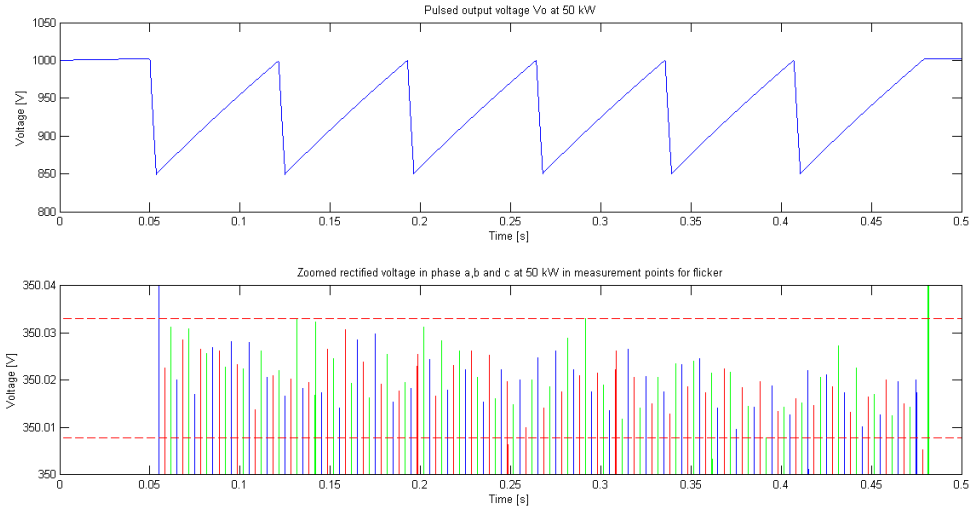

Figure 5.38: Rectified voltage levels in all the three phases at 50 kW, with the maximum and minimum voltage peaks (dashed lines).

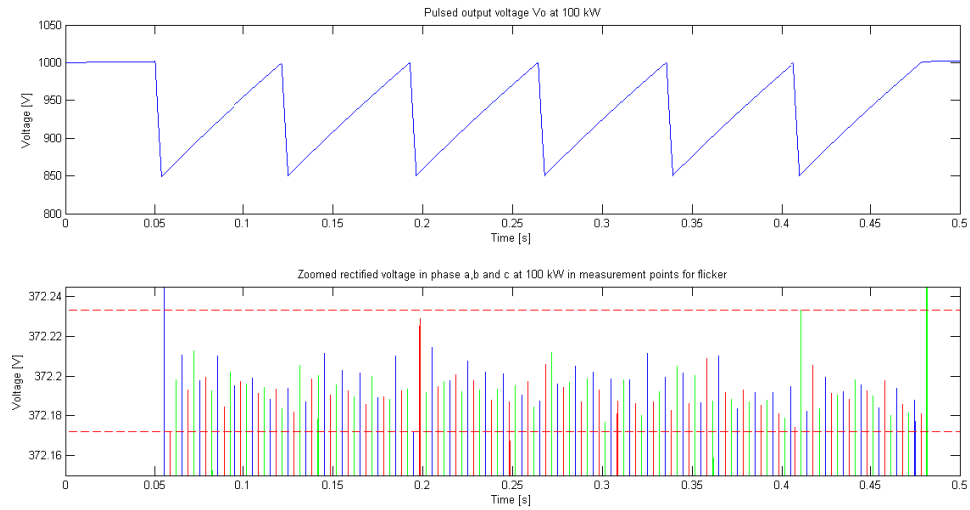

Figure 5.39: Rectified voltage levels in all the three phases at 100 kW, with the maximum and minimum voltage peaks (dashed lines).

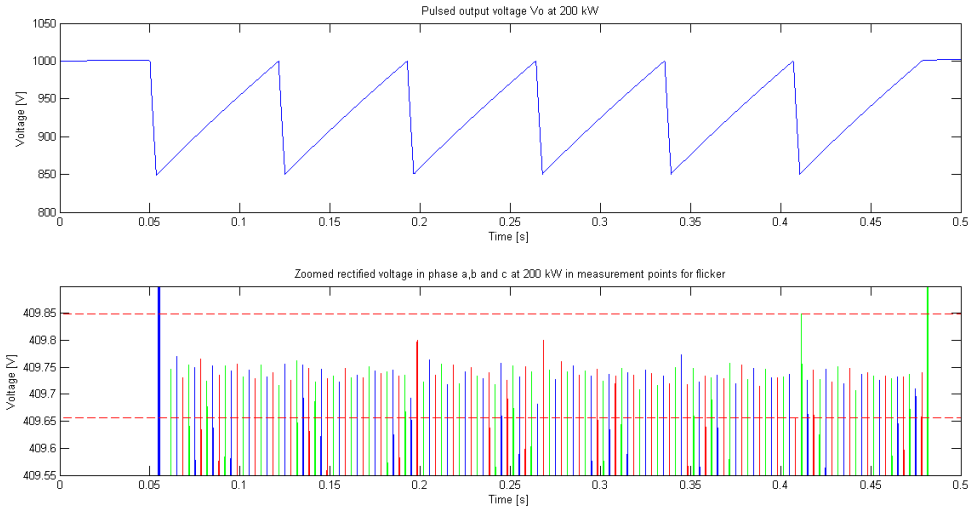

Figure 5.40: Rectified voltage levels in all the three phases at 200 kW, with the maximum and minimum voltage peaks (dashed lines).

CHAPTER 6

6 Losses

Today, environmental thinking is a matter of common sense, for protection of todays living creatures and in order to pave the way for coming generations. From the introduction in this report it can be understood that ESS cares about the environment. This chapter will therefore focus on calculating losses for the complete system and hopefully obtain efficiencies that correspond to requirements. Because of the systems high power rating, every part of percent in efficiency is important. The AFE- and DC/DC-converter is considered as two independent stages in the complete system and therefore these efficiencies will be estimated separately and multiplied for a complete result in the end. For estimation of losses there are two ways, the first is to simulate and calculate the difference in input power and output power, the second is to use mathematical calculations. Due to the lack of flexibility in the simulation methodology, the mathematical version with its fast and flexible calculation possibilities is chosen. The mathematical solution is also remarkably accurate and often the methodology used in industries and described in many literature. With help of common components datasheet information and matching them for this application the estimations are done.
As a starting point some parameters have been set as a guidelines and a way to simplify the implementation:

- The grid is set to a standard 400 V, 50 Hz three phase grid.
- The DC-link voltage is 1100 V
- The average transferred active power is 200 kW and no reactive power.
- The output voltage ripple on DC/DC is, as specified, exactly 15 % in respect to the maximum output voltage of 1 kV.
- The component dimensioning follows Table 5.6.
- The switched output load frequency is 14 Hz
- The transistor switching frequency is set to 7.5 kHz
- The current ripple of the DC/DC is 5 %.

- The transistors and diodes characteristics follow datasheet for SKM400GB176D (see appendix).
- The gate resistance on semiconductors is 10 Ω.

6.1 Simplifications and impacts

When calculating the losses a couple of estimations need to be done. Characteristics in datasheets regarding switching losses aren't provided in exact terms for this interpretation. Therefore an interpolation and manipulation of curves from the datasheet information in Matlab is arranged. Regarding the curve representing switching energy as a function of current, a third order polynomial has been chosen and for the switching energy as a function of resistance, a first order polynomial. In Figure 6.1 the interpolated plots are provided and scaled for a voltage level of V_{dc} = 1100 V.

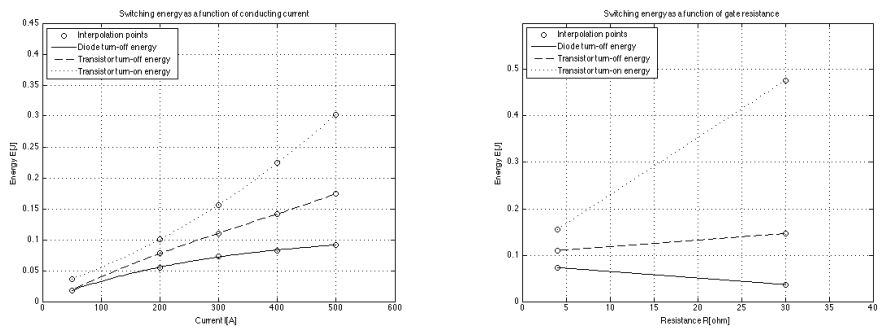

Figure 6.1: Plots of interpolated information from datasheet with correction for voltage-level.

Since there is an apparent impact from the gate resistance on the switching losses, a compensation for gate resistance also needs to be done. Values in the left picture in Figure 6.1 are scaled to correct values and are illustrated in Figure 6.2, with a change of gate resistance from 4 Ω to 10 Ω.

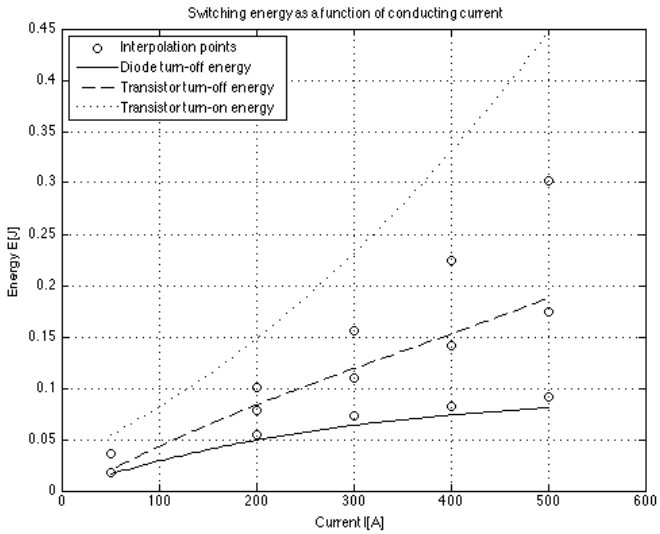

Figure 6.2: Plot of interpolated information from datasheet with correction for gate resistance to Rg = 10 Ω.

Regarding losses in inductances and capacitances these are neglected based on the assumption that they are relative low compared to the losses from transistors and diodes. The same is assumed regarding stray-losses and impact from dead-time generation for transistors. For calculation of the more exact amount of losses in a PE-application, the switching impacts on currents and voltages would have to be included. This is extremely hard to do with mathematical expressions, current ripple and other effects of transistor switching are also neglected in this report. Instead voltages and currents are considered to be average over every micro-cycle. For more information on this, refer to chapter 3 for the AFE and chapter 4 regarding the DC/DC.

6.2 AFE power losses

For calculation of losses in the AFE-stage a Matlab-script is constructed (se appendix). This script contains the conduction losses equations and switching losses equations evaluated and described in chapter 3. In this script different switching frequencies, power levels and component values can be chosen depending on application. A table is constructed to assemble calculated information relevant for this application, Table 6.1.

Table 6.1: Power-losses and efficiencies for different power-levels and switching frequencies in the AFE.

Frequency / Power	3 kHz	5 kHz	7.5 kHz	15 kHz
50 kW	1.22 kW (97.56 %)	1.87 kW (96.25 %)	2.70 kW (94.61 %)	5.16 kW (89.68 %)
100 kW	2.31 kW (97.69 %)	3.50 kW (96.54 %)	4.90 kW (95.10 %)	9.22 kW (90.78 %)
200 kW	4.85 kW (97.57 %)	7.02 kW (96.49 %)	9.73 kW (95.13 %)	17.86 kW (91.07 %)

6.3 DC/DC power losses

For calculation of losses in the DC/DC-stage a Matlab-script is constructed in the same way as for the AFE-stage (see appendix). The content is derived from chapter 4 and different parameters can be chosen. The assembled calculations and information relevant for this application can be seen in Table 6.2.

Table 6.2: Power-losses and efficiencies for different power-levels and switching frequencies in the DC/DC.

Frequency / Power	3 kHz	5 kHz	7.5 kHz	15 kHz
50 kW	0.35 kW (99.30 %)	0.54 kW (98.92 %)	0.78 kW (98.44 %)	1.49 kW (97.01 %)
100 kW	0.65 kW (99.35 %)	0.97 kW (99.03 %)	1.38 kW (98.62 %)	2.61 kW (97.39 %)
200 kW	1.33 kW (99.33%)	1.94 kW (99.03%)	2.69 kW (98.65%)	4.96 kW (97.52%)

6.4 Full system losses

In this part efficiency for the complete full system is calculated. Multiplication of the efficiency for AFE and DC/DC will manage the efficiency for the complete system presented in Table 6.3.

Table 6.3: Efficiency for different power-levels and switching frequencies in the full system.

Frequency / Power	3 kHz	5 kHz	7.5 kHz	15 kHz
50 kW	1.57 kW (96.88 %)	2.42 kW (95.21 %)	3.48 kW (93.13 %)	6.65 kW (87.00 %)
100 kW	2.96 kW (97.06 %)	4.47 kW (95.60 %)	6.28 kW (93.79 %)	11.83 kW (88.41 %)
200 kW	6.18 kW (96.92 %)	8.96 kW (95.55 %)	12.42 kW (93.85 %)	22.82 kW (88.81 %)

6.5 Reflections of results

The absolute losses for different configurations vary a lot. Since the transferred power also varies these will have a correlation, the focus will be on efficiency instead of absolute losses. When now looking at the efficiency for a full system (Table 6.3), the conclusion is that losses don't depend on the transferred power. Efficiency for both AFE- and DC/DC-stage are independent of the transferred power, which can be seen by looking at the different columns for a specific switching frequency. There is though a big difference when changing the transistor switching frequency. For example, looking at a transferred power of 100 kW for the full system in Table 6.3 the efficiency vary from 97 % to 88 %, which is a big difference. Looking at results for the different stages in Table 6.1 and Table 6.2, the most switching frequency dependent system is the DC/DC. The DC/DC efficiency is impaired with 7 % per unit in the 100 kW example, when going from 3 kHz to 15 kHz in switching frequency. Difference for the AFE is though merely 2 %. In general the switching frequency has the absolute biggest impact on efficiency for the converters in this project. Unfortunately there are high requirements on the accuracy and the switching frequency is vital to fulfill those. If the losses would have to be reduced, switching frequency in relation to accuracy should be carefully evaluated, first for the DC/DC- and then for the AFE-stage.

CHAPTER 7

7 Discussion and further work

7.1 Discussion and further work

The thesis comprises simulations and control for one grid connected capacitor charger that is a part of a new modulator topology concept. This new concept will finally consist of several capacitor chargers in parallel together with other steps in the full modulator. By verifying the functionality of the capacitor charger in a model with ideal simulations and losses calculations, a fundamental perception of the first step in the new modulator concept is given. In general are simulations within the power electronics area a good estimation of the reality, which makes it worth the effort to put some time into the simulations. Even though this argument, there is some further work proposed in order to improve and strengthen the functionality of the implementation:

- The derivation and modeling of the system is ideal, therefore are possible impacts from sensor, such as delays or disturbances not included. A simulation model should also be able to take this into account in order to be definitive, but this will require additional time on the system modeling.

- In Matlab/Simulink it is not possible to choose advanced models of specific components, such as specific dimensioning or brand of transistors, diodes, etc. A suggested improvement of this is to model the system in another software, such as SABER, and compare the results.

- The new modulator concept is based on several parallel modules. In the scope of this thesis is one capacitor charger simulated, suggested is that further investigations of a full stacked modulator should be done in order to verify the full functionality and to do a correct implementation in terms of dimensioning and control. Possible

impacts of stacked capacitor chargers will be discussed later in this chapter.

- The models for this thesis are acceptably close to the real world, but it's still ideal and mathematical, which implies that there are no guarantees that the model will give the same result as the real one. It's therefore recommended to do a real reduced-scale prototype, with the same controller principle to verify this.

- Simulation results of power losses show that the efficiency is significantly higher for a converter with lower switching frequency. A possible improvement is to lower the switching frequency in order to decrease the losses. Lower switching frequency may impact on the precision and will require additional simulations and investigations to verify the requirements on precision are fulfilled.

- It's recommended to do a study on available components on the market, transistors, diodes, etc. together with a correct dimensioning in terms of peak voltages and currents, nominal voltages and currents, switching frequency etc.

The implementation is ideal without losses since it's easier and faster to calculate them separately with mathematical expressions. Losses are calculated separately for the active components with ideal current and voltage shapes based on transistor characteristics from datasheet. This is to give more accurate efficiency calculations based on the selection of active components.

The main purpose behind stacked modulators is that it's easier to do a hypothetical expansion, standard components are also used which have higher efficiency and lower costs. Due to the lack of time in the project one module is simulated with optimized controllers and dimensioning. A single module connected to the grid will still be the worst case in terms of current harmonics, but it's better to consider the worst case than the best case. When expanding and parallel couple several modules the module signals for the different modulators are phase shifted. The low harmonic current content generated by each module will in this case be summed up and canceled. This will result in a possibility to re-dimension and lower the inductances at the grid side of the modulators and still fulfill the IEC

standards for low harmonic contents and flicker. Due to lower inductances are additional opportunities for cost reductions available.

Control of the DC/DC-converter is based upon knowledge of the exact trigger signal to the pulse, but in another application this might not be possible. Because of this advantage, maximum precision and perfect timing is achieved. The precision on the output is up to ten times higher than the specified, therefore knowledge of the exact trigger signal is not mandatory for an implementation, and imperfections from e.g. a sensor could be acceptable. Another possibility for solving this problem is to use a peak sensor to discover the maximum and minimum voltage levels at the output.

7.2 Conclusions

The main purpose of the thesis was to dimension and simulate the capacitor charger in the modulators together with the developed control for AFE and DC/DC. The conclusions from this project are:

- The strictest IEC standards, 61000-3-3 and 61000-3-2, for flicker and low harmonic currents content are applied, where the rated currents are lower than 16 A. This application sinks up to 4 MW in a pulsing pattern and has nominal sinusoidal currents up to 300 A and still fulfills these strict standards.

- The control loops in the AFE are designed in such a way that the current drawn from the grid is sinusoidal and reactive power compensation is achieved. This means that only active power is drawn from the grid and the results give a power factor of close to 1 in steady state.

- The voltage drop at the DC-link when the load starts pulsing is dependent on the choice of DC-link capacitance and grid inductances. According to the results in full system simulations, the DC-link voltage at steady state is constant with a maximum ripple less than 1 %.

- Power drawn from the grid is constant when the load is pulsing and the output voltage precision better than 0.1%.

- The full system power losses and efficiency is dependent mainly on switching frequency for the transistors. Conduction losses are

merely a fraction of the total loss and the smallest contributing part of these two. A reduction of switching frequency could be considered since the accuracy margin is significantly good.

- The full system has been dimensioned and optimized with final control parameters and works perfectly for all three different power modes evaluated; 50 kW, 100kW and 200kW. Power losses have also been determined for these power modes and states that the efficiency is power-independent.

- A complete dimensioning of all passive components has been successfully managed with help of mathematical expressions or with a simulation methodology.

- Mathematical expressions have been derived for determining the system characteristics and calculation of power losses for both the DC/DC and AFE. These expressions have successfully been arranged to calculate accurately the control parameters for the controllers.

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8 List of Figures

9 List of Tables

10 List of Acronyms

AC	Alternating Current
A	Ampere
AFE	Active Front End
BJT	Bipolar Junction Transistor
CFL	Compact Fluorescent Lamp
DC	Direct Current
DLT	Drift Tube Linac
EMC	Electromagnetic Compatibility
ESS	European Spallation Source
EUT	Equipment Under Test
eV	Electron Volt
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
HEBT	High Energy Beam Transport
Hz	Hertz
I/O	Input / Output
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
KVL	Kirchhoff Voltage Law
LEBT	Low Energy Beam Transport
LPA	Linear Particle Accelerator
MEBT	Medium Beam Transport
NI	National Instruments
PE	Power Electronic
PWM	Pulse Width Modulation
RF	Radio Frequency
RMS	Root Mean Square
RQF	Radio Frequency Quadrupole
THD	Total Harmonic distortion
V	Volt
W	Watt

List of Nomenclature

a	AFE controller parameter
C_{dc}	DC- link capacitance
C_i	Current controller transfer function
C_o	Output capacitance
C_v	Voltage controller transfer function
D	Duty-cycle
D_O	Output diode
D_{R_o}	Output pulse width
$D_{T/D}$	Duty-cycle for transistors and diodes
e	Voltage level
$e_{a,b,c}$	Grid, line-to-ground RMS voltage amplitude
$E_{off,n}$	Turn-off energy for a nominal voltage and current level
$E_{on,n}$	Turn-on energy for a nominal voltage and current level
$E_{T/D}$	Energy loss for transistors and diodes
$E_{T/D,off}$	Turn-off energy for transistors and diodes
$E_{T/D,cond}$	Conduction energy loss for transistors and diodes
$E_{T,on}$	Turn-on energy for transistors
f_c	Cut-off frequency
f_{dist}	Frequency of grid disturbances
f_{R_o}	Output pulse frequency
f_s	Transistor switching frequency
F_s	Sampling frequency discrete system
G	General transfer function
G_{c_x}	Closed loop transfer function
G_{o_x}	Open loop transfer function
i	Current
$i_{a,b,c}$	Grid, line-to-ground RMS current amplitude
$i_{d,q}$	Grid, line-to-ground peak current amplitude in dq frame
i_C	Current into capacitance
i_L	Current through inductance
I_c	DC-link, current though C_{dc}
I_{dc}	Current from the DC-link
I_f	DC-link, current through load
$I_{L_{conv}}$	Converter inductance current, line-to-ground
$\hat{I}_{L_{conv}}$	Converter inductance current, line-to-ground peak
$I_{L,n}$	A nominal current level

I_{L_o}	Current through output inductance
$I_{L_o}^{percent}$	Current ripple in DC/DC output inductance
I_N	Nominal current
$\bar{I}_0$	Average output current
I_q^*	Grid, line-to-ground RMS current reference amplitude in dq frame
I_{ripple}	Current ripple
I_s	Grid, line-to-ground RMS current amplitude
I_s^*	Grid, line-to-ground RMS current reference amplitude
K_c	Converter gain
K_i	Gain for the current control
K_p	Gain for the power control
K_v	Gain for the voltage control
L	Inductance
L_{conv}	Converter, input inductance
L_o	Output inductance
$\widehat{m}_a$	Peak value modulation wave to AFE
m_a	Modulation wave to AFE
P	Active power
P^*	Power reference
P_{AB}	Power output from DC/DC converter
P_{AB}^{est}	Power control estimation
P_{C_O}	Power from output capacitance
$P_{diode,con}$	Diode conduction power losses
P_{dc}	Power from DC-link
P_{peak}	Peak power
p_s	Power losses for switching elements
$P_{tran,con}$	Transistor conduction power losses
Q	Reactive power
R_{conv}	Converter, input resistance
R_o	Output resistance
R_{on}	Resistance when conducting
$R_{T/D}$	Forward voltage drop resistance
S	Apparent Power
S_N	Nominal power
T	Time-period
T_c	Delay for the converter
t_{cond}	Time of conduction

t_e	time early, time for when pulse reaches maximum voltage limitation in output stage
T_i	Gain for the current control
T_o	Output transistor
t_p	Time-duration of pulse
T_{pi}	Gain parameter in current controller
T_{pv}	Gain parameter in voltage controller
T_{sw}	Switching time period
T_s	Physical system sampling time
T_v	Gain for the voltage control
T_{zi}	Gain parameter in current controller
T_{zv}	Gain parameter in voltage controller
$T_{50\square z}$	Time period for 50Hz
u	Voltage
$u_{d,q}$	Grid, line-to-ground peak voltage amplitude in dq frame
$V_{a,b,c}$	Grid voltage
V_{avg}	Average voltage
V_{conv}	Converter, line-to-neutral RMS voltage amplitude
V_D	Voltage over diode
V_{dc}	DC-link, dc voltage
V_{dc}^*	DC-link, dc voltage reference
$V_{DC,n}$	A nominal voltage level
V_{dist}	Amplitude of grid disturbance
V_{drop}	Voltage drop
V_{fo}	Forward voltage drop
v_L	Voltage drop over inductor
V_N	Nominal voltage
V_o	Output voltage
V_o^{drop}	Output voltage drop
V_o^{ext}	Extrapolated output voltage
V_o^{max}	Maximum output voltage
V_o^{min}	Minimum output voltage
V_o^{wrong}	Error in output voltage
V_s	Grid, line-to-ground RMS voltage amplitude
$\hat{V}_{tri}$	Modulator, triangular peak amplitude
$V_{T/D(on)}$	Conduction voltage drop for transistors and diodes
$V_{T0/D0}$	Threshold voltage for transistors and diodes
X'	Grid filtered quantities

x_x	Transformation variable, where x is an arbitrary variable
x'_x	Transformation variable for filter, where x is an arbitrary variable
Δt	Time difference
ΔP_{AB}	Power control correction term
δ	Phase difference between converter- and grid voltage
φ	The phase difference between grid current and voltage
θ	Angular difference between alpha-coordinate and voltage
θ_C	Angular difference real and grid filtered voltage
τ	Time constant
ω	Angular frequency

Appendix A

Losses AFE

$$< I^2(t) \cdot D(t) > =$$

$$\frac{1}{T} \cdot \left[\frac{\hat{I}_{L_{conv}}^2 \cdot (3 \cdot \hat{m}_a \cdot \cos(-\delta+\varphi-\omega \cdot t) - \hat{m}_a \cdot \cos(-\delta+\varphi+3 \cdot \omega \cdot t) - 3 \cdot \sin(2 \cdot \omega \cdot t))}{24 \cdot \omega} \right]_{t_1=0}^{t_2=\frac{\pi}{\omega}} +$$

$$\left[\frac{\hat{I}_{L_{conv}}^2 \cdot (6 \cdot \hat{m}_a \cdot \cos(-\delta+\varphi+\omega \cdot t) + 6 \cdot t \cdot \omega -)}{24 \cdot \omega} \right]_{t_1=0}^{t_2=\frac{\pi}{\omega}} =$$

$$\frac{1}{T} \cdot \left(\frac{\hat{I}_{L_{conv}}^2 \cdot (3 \cdot \pi - 8 \cdot \hat{m}_a \cdot \cos(-\delta+\varphi))}{12 \cdot \omega} \right)$$

$$< I_{L_{conv}}(t) \cdot D(t) >=$$

$$\frac{1}{T} \cdot \left[\frac{\hat{I}_{L_{conv}} \cdot (\hat{m}_a \cdot \sin(-\delta+\varphi+2 \cdot \omega \cdot t) - 2 \cdot \hat{m}_a \cdot \omega \cdot t \cdot \cos(-\delta+\varphi) - 4 \cdot \cos(\omega \cdot t)}{8 \cdot \omega} \right]_{t_1=0}^{t_2=\frac{\pi}{\omega}} =$$

$$\frac{1}{T} \cdot \left(\frac{\hat{I}_{L_{conv}} \cdot (4 - \cdot \hat{m}_a \cdot \pi \cdot \cos(-\delta+\varphi))}{4 \cdot \omega} \right)$$

$$< I_{L_{conv}} > = \frac{1}{T} \cdot \int_{t_1}^{t_2} \hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t)\, dt =$$

$$\frac{1}{T} \cdot \left[-\hat{I}_{L_{conv}} \cdot \frac{\cos(\omega \cdot t)}{\omega} \right]_{t_1=0}^{t_2=\frac{\pi}{\omega}} = \frac{1}{T} \cdot \left(\frac{2 \cdot \hat{I}_{L_{conv}}}{\omega} \right)$$

$$\boldsymbol{< I_{I_{L_{conv}}}^2 > = \frac{1}{T} \cdot \int_{t_1}^{t_2} \left(\hat{I}_{L_{conv}} \cdot \sin(\omega \cdot t) \right)^2 dt =}$$

$$\frac{1}{T} \cdot \left[\hat{I}_{L_{conv}}^2 \cdot \left(\frac{t}{2} - \frac{\sin(\omega \cdot t)}{4 \cdot \omega} \right) \right]_{t_1=0}^{t_2=\frac{\pi}{\omega}} = \frac{1}{T} \cdot \left(\frac{\pi \cdot \hat{I}_{L_{conv}}^2}{2 \cdot \omega} \right)$$

Losses DC/DC

$$V_{min0} = V_o^{min} - \frac{(V_o^{max} - V_o^{min}) \cdot t_1}{t_2 - t_1}$$

Transistor losses

$$\langle I_{L_o}^2(t)\cdot D(t)\rangle =$$

$$\frac{1}{T}\cdot\left(-\frac{\Delta t\cdot {P^*}^2}{V_{dc}\cdot\Delta V_o}\cdot\left[ln\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_0}^{t_1}+\frac{L_o\cdot {P^*}^3}{3\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)^3}\right]_{t_0}^{t_1}\right)+$$

$$\frac{1}{T}\cdot\left(\frac{\Delta t\cdot {P^*}^2}{V_{dc}\cdot\Delta V_o}\cdot\left[ln\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_1}^{t_2}+\frac{L_o\cdot {P^*}^3}{3\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)^3}\right]_{t_1}^{t_2}\right)$$

$$\langle I_{L_o}(t)\cdot D(t)\rangle =$$

$$\frac{1}{T}\cdot\left(\frac{P^*}{V_{dc}}\cdot[t]_{t_0}^{t_1}+\frac{L_o\cdot {P^*}^2}{2\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)^2}\right]_{t_0}^{t_1}\right)+$$

$$\frac{1}{T}\cdot\left(\frac{P^*}{V_{dc}}\cdot[t]_{t_1}^{t_2}+\frac{L_o\cdot {P^*}^2}{2\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)^2}\right]_{t_1}^{t_2}\right)$$

Diode losses

$$\langle I_{L_o}^2(t)(1-D(t))\rangle =$$

$$\frac{1}{T}\cdot\left(\frac{{P^*}^2\cdot\Delta t}{\Delta V_o}\cdot\left[\frac{1}{V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t}\right]_{t_0}^{t_1}+\frac{\Delta t\cdot {P^*}^2}{V_{dc}\cdot\Delta V_o}\cdot\left[ln\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_0}^{t_1}-\right.$$

$$\left.\frac{L_o\cdot {P^*}^3}{3\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)^3}\right]_{t_0}^{t_1}\right)+$$

$$\frac{1}{T}\cdot\left(-\frac{\Delta t\cdot {P^*}^2}{\Delta V_o}\cdot\left[\frac{1}{\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)}\right]_{t_1}^{t_2}-\frac{\Delta t\cdot {P^*}^2}{V_{dc}\cdot\Delta V_o}\cdot\left[ln\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_1}^{t_2}-\right.$$

$$\left.\frac{L_o\cdot {P^*}^3}{3\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)^3}\right]_{t_1}^{t_2}\right)$$

$$\langle I_{L_o}(t)\big(1-D(t)\big)\rangle =$$

$$\frac{1}{T}\left(-\frac{\Delta t\cdot P^*}{\Delta V_o}\cdot\left[ln\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_0}^{t_1}-\frac{P^*}{V_{dc}}\cdot[t]_{t_0}^{t_1}-\right.$$

$$\left.\frac{L_o\cdot P^{*2}}{2\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_o^{max}-\frac{\Delta V_o}{\Delta t}\cdot t\right)^2}\right]_{t_0}^{t_1}\right)+$$

$$\frac{1}{T}\left(\frac{\Delta t\cdot P^*}{\Delta V_o}\cdot\left[ln\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)\right]_{t_1}^{t_2}-\frac{P^*}{V_{dc}}\cdot[t]_{t_1}^{t_2}-\frac{L_o\cdot P^{*2}}{2\cdot V_{dc}}\cdot\left[\frac{1}{\left(V_{min0}+\frac{\Delta V_o}{\Delta t}\cdot t\right)^2}\right]_{t_1}^{t_2}\right)$$

AFE losses calculation in Matlab

```
%% AFE analytical expression for losses

clear all;
close all;

%P1 = Ron*D*I^2 from 0 to T
%P2 = Vfo*D*I from 0 to T

%D = (1/2)*(1-ma*sin(w*t+fi-d)
%I = Ip*sin(w*t)

%Pavgloss = (1/T)*((Ron*D*I^2) + (Vfo*D*I))

%Initial paratmeters

P3 = 200e3;             % Active power three phase
P = P3/3;               % Active power one phase
Q3 = 0;                 % Reactive power three phase
Q = Q3/3;               % Reactive power one phase
L = 0.4e-3;             % Input inductor, input
resistance assumed 0 ohm
Vdc = 1100;             % DC-voltage
fs = 7.5e3;             % Sampling frequency
Vp = 325;               % Peak voltage of the grid
f = 50;                 % Grid frequency
```

```
%Calculation of useful parameters

Vs = Vp/sqrt(2);
% RMS value of the peak grid voltage
w = 2*pi*f;
% Omega
X = w*L;
% Inductance impedans
I = sqrt(2)*P3/(3*Vs);
% Input current peak value
ma = (2*sqrt(2)*P*X)/(Vdc*Vs*sin(atan(P/((Vs^2/X)-Q))));
% Modulator factor
t1 = 0;
% Integral start value
t2 = 1/(2*50);
% Integral end value
T = 1/50;
% Integrational time
d = atan(P/((Vs^2/X)-Q));
% Delta
fi = atan(Q3/P3);
% FI

%% Transistor conduction power losses calculations

Vfo = 0.9;
% Transistor forward voltage drop
Ron = 5.2e-3;
% Transistor resistance


P1t1 = Ron*((I^2)*(3*ma*cos(-d+fi-t1*w) + 6*ma*cos(-
d+fi+t1*w) - ma*cos(-d+fi+3*t1*w) + 6*t1*w -
3*sin(2*t1*w))/(24*w))/T;
P1t2 = Ron*((I^2)*(3*ma*cos(-d+fi-t2*w) + 6*ma*cos(-
d+fi+t2*w) - ma*cos(-d+fi+3*t2*w) + 6*t2*w -
3*sin(2*t2*w))/(24*w))/T;
P01 = (P1t2 - P1t1);

P2t1 = Vfo*(I*(ma*sin(2*t1*w-d+fi) - 2*ma*t1*w*cos(-d+fi)
- 4*cos(t1*w))/(8*w))/T;
P2t2 = Vfo*(I*(ma*sin(2*t2*w-d+fi) - 2*ma*t2*w*cos(-d+fi)
- 4*cos(t2*w))/(8*w))/T;
P02 = (P2t2 -P2t1);
```

```
PavgTran = (P01 + P02);
% Average conduction power losses per transistor
powerConLossTransistors = 6*PavgTran;
% Average conduction power losses for all transistors

%% Diode conduction power losses calculations

Vfo = 0.9;
% Forward voltage drop for diode
Ron = 3e-3;
% Diode resistance

P1t1 = Ron*((I^2)*(3*ma*cos(-d+fi-t1*w) + 6*ma*cos(-
d+fi+t1*w) - ma*cos(-d+fi+3*t1*w) + 6*t1*w -
3*sin(2*t1*w))/(24*w))/T;
P1t2 = Ron*((I^2)*(3*ma*cos(-d+fi-t2*w) + 6*ma*cos(-
d+fi+t2*w) - ma*cos(-d+fi+3*t2*w) + 6*t2*w -
3*sin(2*t2*w))/(24*w))/T;
P01 = (P1t2 - P1t1);

P2t1 = Vfo*(I*(ma*sin(2*t1*w-d+fi) - 2*ma*t1*w*cos(-d+fi)
- 4*cos(t1*w))/(8*w))/T;
P2t2 = Vfo*(I*(ma*sin(2*t2*w-d+fi) - 2*ma*t2*w*cos(-d+fi)
- 4*cos(t2*w))/(8*w))/T;
P02 = (P2t2 - P2t1);

P3t1 = Ron*(((I^2)/(2*T))*(t1 - (1/(2*w))*sin(2*w*t1)));
P3t2 = Ron*(((I^2)/(2*T))*(t2 - (1/(2*w))*sin(2*w*t2)));
P03 = (P3t2 - P3t1);

P4t1 = Vfo*((I/(w*T))*(-cos(w*t1)));
P4t2 = Vfo*((I/(w*T))*(-cos(w*t2)));
P04 = (P4t2 - P4t1);


PavgDiode = (P03-P01)+(P04-P02);
% Average conduction power losses per diode
powerConLossDiodes = 6*PavgDiode;
% Average conduction power losses for all diodes
```

```
%% Switching losses for the diodes and transistors

% This is over a full period per phase so that's why
multiplication by 3

Rg = 10;                                            % Gate
resistance
run('InterpolationOfCurveSwitchingLosses.m')    %
Construct curves for calculation of switching losses

I1t1 = (I/(w*T))*(-cos(w*t1));
I1t2 = (I/(w*T))*(-cos(w*t2));
Iavg = 2*(I1t2-I1t1);                               % Average
current

ETon = polyval(pETON,Iavg);                         %
Transistor turn-on energy for a specific current
EToff = polyval(pETOFF,Iavg);                       %
Transistor turn-off energy for a specific current
EDoff = polyval(pEDOFF,Iavg);                       % Diode
turn-off energy for a specific current

energySwitchLossTransistor = ETon + EToff;
energySwitchLossDiode = EDoff;

powerSwitchLossTransistors =
3*energySwitchLossTransistor*fs;   % Average switching
power losses for all transistors
powerSwitchLossDiodes = 3*energySwitchLossDiode*fs;
% Average switching power losses for all diodes

%% Calculation of efficency

powerTotalLossDiodes = powerConLossDiodes +
powerSwitchLossDiodes;
powerTotalLossTransistors = powerConLossTransistors +
powerSwitchLossTransistors;

powerTotalLoss = powerTotalLossDiodes +
powerTotalLossTransistors           % Total power losses
in the AFE
efficency = 1 - powerTotalLoss/(sqrt(P3^2+Q3^2))
```

DC/DC losses calculation in Matlab

```
%% DC/DC analytical expression for losses

close all;
clear all;

% integral of P1 = Il^2*D From t1 to t2 and from t2 to t3
% integral of P2 = Il*D From t1 to t2 and from t2 to t3

% Initial paratmeters

t1 = 0;                             % First integration time
t2 = 0.05*(1/14);                   % Second integration time
t3 = (1/14);                        % Third integration time
dt1 = t2 - t1;                      % delta t (the slope of
Vc)
dt2 = t3 - t2;                      % delta t (the slope of
Vc)
L = 1.8e-3;                         % Inductance
P = 200e3;                          % Power
Vmax = 1000;                        % Maximum voltage out
from the DC/DC
T = 1/14;                           % Integrational time
T1 = 0.05/14;                       % First Integrational
time
T2 = 0.95/14;                       % Second Integrational
time
Vdc = 1100;                         % DC-link voltage
fs = 7.5e3;                         % Switching frequency

% Calculation of useful parameters

dV = Vmax*0.15;                         % Voltage ripple/drop
Vmin0 = Vmax - dV - (dV*t2/dt2);    % Minimum voltage out
from the DC/DC @ t2 (zero time fix)
```

```
%% Transistor conduction power losses calculations

Vf0 = 0.9;                          % Transistor forward
voltage drop
Ron = 5.2e-3;                       % Transistor resistance

% Losses for falling slope
% Ron*I^2*D
E1t1 = Ron*((L*(P^3)/(3*Vdc*((Vmax-(dV*t1/dt1))^3))) -
(dt1*(P^2)*log(Vmax-(dV*t1/dt1))/(dV*Vdc)));
E1t2 = Ron*((L*(P^3)/(3*Vdc*((Vmax-(dV*t2/dt1))^3))) -
(dt1*(P^2)*log(Vmax-(dV*t2/dt1))/(dV*Vdc)));
E1 = (E1t2 - E1t1);

% Ron*I*D
E2t1 = Vf0*((P*t1/Vdc) + (L*(P^2)/(2*Vdc*((Vmax-
(dV*t1/dt1))^2))));
E2t2 = Vf0*((P*t2/Vdc) + (L*(P^2)/(2*Vdc*((Vmax-
(dV*t2/dt1))^2))));
E2 = (E2t2 - E2t1);

EConLoss1 = (E1 + E2);

% Losses for rising slope
% Ron*I^2*D
E1t2 = Ron*((L*(P^3)/(3*Vdc*((Vmin0+(dV*t2/dt2))^3))) +
(dt2*(P^2)*log(Vmin0+(dV*t2/dt2))/(dV*Vdc)));
E1t3 = Ron*((L*(P^3)/(3*Vdc*((Vmin0+(dV*t3/dt2))^3))) +
(dt2*(P^2)*log(Vmin0+(dV*t3/dt2))/(dV*Vdc)));
E1 = (E1t3 - E1t2);

% Ron*I*D
E2t2 = Vf0*((P*t2/Vdc) +
(L*(P^2)/(2*Vdc*((Vmin0+(dV*t2/dt2))^2))));
E2t3 = Vf0*((P*t3/Vdc) +
(L*(P^2)/(2*Vdc*((Vmin0+(dV*t3/dt2))^2))));
E2 = (E2t3 - E2t2);

EConLoss2 = (E1 + E2);                                  %
Energy losses per period for transistor
powerConLossTransistor = (EConLoss1 + EConLoss2)/T;     %
Average conduction power losses for transistor
```

```
%% Diode conduction power losses calculations

Vf0 = 0.9;                          % Diode forward voltage
drop
Ron = 3e-3;                         % Diode resistance

% Falling slope
% Ron*I^2*D
E1t1 = Ron*((L*(P^3)/(3*Vdc*((Vmax-(dV*t1/dt1))^3))) -
(dt1*(P^2)*log(Vmax-(dV*t1/dt1))/(dV*Vdc)));
E1t2 = Ron*((L*(P^3)/(3*Vdc*((Vmax-(dV*t2/dt1))^3))) -
(dt1*(P^2)*log(Vmax-(dV*t2/dt1))/(dV*Vdc)));
E1 = (E1t2 - E1t1);

% Vfo*I*D
E2t1 = Vf0*((P*t1/Vdc) + (L*(P^2)/(2*Vdc*((Vmax-
(dV*t1/dt1))^2))));
E2t2 = Vf0*((P*t2/Vdc) + (L*(P^2)/(2*Vdc*((Vmax-
(dV*t2/dt1))^2))));
E2 = (E2t2 - E2t1);

% Ron*I^2
E3t1 = Ron*((dt1*P^2)/(dV*(Vmax-(dV*t1/dt1))));
E3t2 = Ron*((dt1*P^2)/(dV*(Vmax-(dV*t2/dt1))));
E3 = (E3t2-E3t1);

% Vfo*I
E4t1 = Vf0*(-((dt1*P*log(Vmax-(dV*t1/dt1)))/(dV)));
E4t2 = Vf0*(-((dt1*P*log(Vmax-(dV*t2/dt1)))/(dV)));
E4 = (E4t2-E4t1);

EConLoss1 = (E3-E1)+(E4-E2);
```

```
% Rising slope
% Ron*I^2*D
E1t2 = Ron*((L*(P^3)/(3*Vdc*((Vmin0+(dV*t2/dt2))^3))) +
(dt2*(P^2)*log(Vmin0+(dV*t2/dt2))/(dV*Vdc)));
E1t3 = Ron*((L*(P^3)/(3*Vdc*((Vmin0+(dV*t3/dt2))^3))) +
(dt2*(P^2)*log(Vmin0+(dV*t3/dt2))/(dV*Vdc)));
E1 = (E1t3 - E1t2);

% Vfo*I*D
E2t2 = Vf0*((P*t2/Vdc) +
(L*(P^2)/(2*Vdc*((Vmin0+(dV*t2/dt2))^2))));
E2t3 = Vf0*((P*t3/Vdc) +
(L*(P^2)/(2*Vdc*((Vmin0+(dV*t3/dt2))^2))));
E2 = (E2t3 - E2t2);

% Ron*I^2
E3t2 = Ron*(-(dt2*P^2)/(dV*(Vmin0+(dV*t2/dt2))));
E3t3 = Ron*(-(dt2*P^2)/(dV*(Vmin0+(dV*t3/dt2))));
E3 = (E3t3-E3t2);

% Vfo*I
E4t2 = Vf0*(((dt2*P*log(Vmin0+(dV*t2/dt2)))/(dV)));
E4t3 = Vf0*(((dt2*P*log(Vmin0+(dV*t3/dt2)))/(dV)));
E4 = (E4t3-E4t2);

EConLoss2 = (E3-E1)+(E4-E2);                                    %
Energy losses per period for diode
powerConLossDiode = (EConLoss1 + EConLoss2)/T;                  %
Average conduction power losses for diode

%% Transistor and Diode switching losses

Rg = 10;                                                % Gate
resistance
run('InterpolationOfCurveSwitchingLosses.m')    %
Construct curves for calculation of switching losses

% Falling slope
I1t1 = -((dt1*P*log(Vmax-(dV*t1/dt1)))/(T1*dV));
I1t2 = -((dt1*P*log(Vmax-(dV*t2/dt1)))/(T1*dV));
Iavg1 = (I1t2-I1t1);
```

```
% Rising slope
I1t2 = ((dt2*P*log(Vmin0+(dV*t2/dt2)))/(T2*dV));
I1t3 = ((dt2*P*log(Vmin0+(dV*t3/dt2)))/(T2*dV));
Iavg2 = (I1t3-I1t2);

% Whole slope
Iavg = (Iavg1+Iavg2)/2;                          % Average
current

ETon = polyval(pETON,Iavg);                      %
Transistor turn-on energy for a specific current
EToff = polyval(pETOFF,Iavg);                    %
Transistor turn-off energy for a specific current
EDoff = polyval(pEDOFF,Iavg);                    % Diode
turn-off energy for a specific current

energyTransistor = ETon + EToff;
energyDiode = EDoff;

powerSwitchLossTransistor = energyTransistor*fs;    %
Average switching power losses for the transistor
powerSwitchLossDiode = energyDiode*fs;              %
Average switching power losses for the diode

%% Calculation of efficency

powerTotalLossTransistor = powerConLossTransistor +
powerSwitchLossTransistor;
powerTotalLossDiode = powerConLossDiode +
powerSwitchLossDiode;

powerTotalLoss = powerTotalLossDiode +
powerTotalLossTransistor         % Total power losses in
the DC/DC
efficiency = 1-(powerTotalLoss)/P
% Efficiency for the DC/CD
```

Interpolation for data sheet SKM400GB176D

```
%% Inerpolation for datasheet SKM400GB176D

figure(1);
hold on;
grid on;

% Rg and Vdc is declared by the calling script

Rg0 = 4;                                                    %
Gate resistance in datasheet
Vnom = 1200;                                                %
Voltage in datasheet

%% Diode turn off energy losses resistance

xList = [4 30];                                             %
Gate resistance
yList = (1e-3).*(Vdc/Vnom).*[80 40];                        %
Energy required to switch with modification to correct
voltage

g1 = plot(xList, yList, 'ko');

pEDOFFR = polyfit(xList, yList, 1);                         %
Interpolation
x = linspace(4,30);                                         %
Plot interval
g2 = plot(x,polyval(pEDOFFR,x), 'k');                       %
Function plot
```

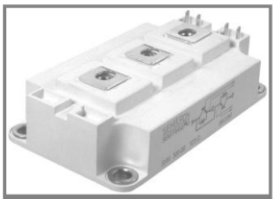
```
%% Transistor turn off energy losses resistance

xList = [4 30];                                          %
Gate resistance
yList = (1e-3).*(Vdc/Vnom).*[120 160];                   %
Energy required to switch with modification to correct
voltage

plot(xList, yList, 'ko');

pETOFFR = polyfit(xList, yList, 1);                      %
Interpolation
x = linspace(4,30);                                      %
Plot interval
g3 = plot(x,polyval(pETOFFR,x), '--k');                  %
Function plot

%% Transistor turn on energy losses resistance

xList = [4 30];                                          %
Gate resistance
yList = (1e-3).*(Vdc/Vnom).*[170 520];                   %
Energy required to switch with modification to correct
voltage

plot(xList, yList, 'ko');

pETONR = polyfit(xList, yList, 1);                       %
Interpolation
x = linspace(4,30);                                      %
Plot interval
g4 = plot(x,polyval(pETONR,x), ':k');                    %
Function plot
```

```
%% Axis, legends and labeling

axis([0 40 0 (1e-3).*600])

xlabel('Resistance R[ohm]')
ylabel('Energy E[J]')
title('Switching energy as a function of gate
resistance')
legend([g1 g2 g3 g4],{'Interpolation points','Diode turn-
off energy','Transistor turn-off energy','Transistor
turn-on energy'},'Location', 'NorthWest')

%% New plot

figure(2);
hold on;
grid on;

%% Diode turn off energy losses

xList = [50 200 300 400 500];                        %
Given values for Rg0
yList = (1e-3).*(Vdc/Vnom).*[20 60 80 90 100];       %
Energy required to switch with modification to correct
voltage

g1 = plot(xList, yList, 'ko');

pEDOFF = polyfit(xList, yList, 3);
% Interpolation
pEDOFF = pEDOFF*polyval(pEDOFFR,Rg)/polyval(pEDOFFR,Rg0);
% Modification of interpolation to correct gate
resistance
x = linspace(50,500);
g2 = plot(x,polyval(pEDOFF,x), 'k');
```

```
%% Transistor turn off energy losses

xList = [50 200 300 400 500];                          %
Given values for Rg0
yList = (1e-3).*(Vdc/Vnom).*[20 85 120 155 190];    %
Energy required to switch with modification to right
voltage

plot(xList, yList, 'ko');

pETOFF = polyfit(xList, yList, 3);
% Interpolation
pETOFF = pETOFF*polyval(pETOFFR,Rg)/polyval(pETOFFR,Rg0);
% Modification of interpolation to correct gate
resistance
x = linspace(50,500);
g3 = plot(x,polyval(pETOFF,x), '--k');

%% Transistor turn on energy losses
xList = [50 200 300 400 500];                          %
Given values for Rg0
yList = (1e-3).*(Vdc/Vnom).*[40 110 170 245 330];   %
Energy required to switch with modification to right
voltage

plot(xList, yList, 'ko');

pETON = polyfit(xList, yList, 3);
% Interpolation
pETON = pETON*polyval(pETONR,Rg)/polyval(pETONR,Rg0);
% Modification of interpolation to correct gate
resistance
x = linspace(50,500);
g4 = plot(x,polyval(pETON,x), ':k');

%% Axis, legends and labeling

axis([0 600 0 (1e-3).*450])

xlabel('Current I[A]')
ylabel('Energy E[J]')
title('Switching energy as a function of conducting
current')
legend([g1 g2 g3 g4],{'Interpolation points','Diode turn-
off energy','Transistor turn-off energy','Transistor
turn-on energy'},'Location', 'NorthWest')
```

Datasheet SKM400GB176

SKM 400GB176D



SEMITRANS® 3

Trench IGBT Modules

SKM 400GB176D

SKM 400GAL176D

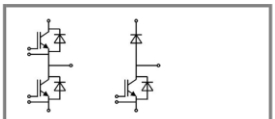
Preliminary Data

Features

- Homogeneous Si
- Trench = Trenchgate technology
- $V_{CE(sat)}$ with positive temperature coefficient
- High short circuit capability, self limiting to 6 x I_C

Typical Applications

- AC inverter drives
- mains 575 - 750 V AC
- Public transport (auxiliary syst.)
- Wind power

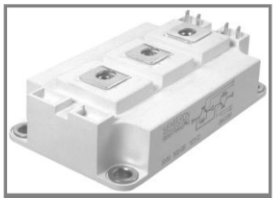


GB GAL

Absolute Maximum Ratings			T_{case} = 25°C, unless otherwise specified	
Symbol	**Conditions**		**Values**	**Units**
IGBT				
V_{CES}	T_j = 25 °C		1700	V
I_C	T_j = 150 °C	T_c = 25 °C	430	A
		T_c = 80 °C	310	A
I_{CRM}	I_{CRM}=2xI_{Cnom}		600	A
V_{GES}			± 20	V
t_{psc}	V_{CC} = 1200 V; $V_{GE} \leq$ 20 V; V_{CES} < 1700 V	T_j = 125 °C	10	µs
Inverse Diode				
I_F	T_j = 150 °C	T_c = 25 °C	440	A
		T_c = 80 °C	300	A
I_{FRM}	I_{FRM}=2xI_{Fnom}		600	A
I_{FSM}	t_p = 10 ms; sin.	T_j = 150 °C	2200	A
Freewheeling Diode				
I_F	T_j = 150 °C	T_{case} = 25 °C	440	A
		T_{case} = 80 °C	300	A
I_{FRM}	I_{FRM}=2xI_{Fnom}		600	A
I_{FSM}	t_p = 10 ms; sin.	T_j = 150 °C	2200	A
Module				
$I_{t(RMS)}$			500	A
T_{vj}			- 40 ... + 150	°C
T_{stg}			- 40 ... + 125	°C
V_{isol}	AC, 1 min.		4000	V

Characteristics			T_{case} = 25°C, unless otherwise specified			
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
IGBT						
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 12 mA		5,2	5,8	6,4	V
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}	T_j = 25 °C		0,15	0,45	mA
V_{CE0}		T_j = 25 °C		1	1,2	V
		T_j = 125 °C		0,9	1,1	V
r_{CE}	V_{GE} = 15 V	T_j = 25°C		3,3	4,2	mΩ
		T_j = 125°C		5,2	6	mΩ
$V_{CE(sat)}$	I_{Cnom} = 300 A, V_{GE} = 15 V	T_j = 25°C$_{chiplev.}$		2	2,4	V
		T_j = 125°C$_{chiplev.}$		2,45	2,9	V
C_{ies}				19,8		nF
C_{oes}	V_{CE} = 25, V_{GE} = 0 V	f = 1 MHz		1,1		nF
C_{res}				0,88		nF
Q_G	V_{GE} = -8V...+15V			2500		nC
$t_{d(on)}$	R_{Gon} = 4 Ω	V_{CC} = 1200V		330		ns
t_r		I_{Cnom} = 300A		55		ns
E_{on}		T_j = 125 °C		170		mJ
$t_{d(off)}$	R_{Goff} = 4 Ω	V_{GE} = ± 15V		880		ns
t_f				145		ns
E_{off}				118		mJ
$R_{th(j-c)}$	per IGBT				0,075	K/W

SKM 400GB176D



SEMITRANS® 3

Trench IGBT Modules

SKM 400GB176D

SKM 400GAL176D

Preliminary Data

Features

- Homogeneous Si
- Trench = Trenchgate technology
- $V_{CE(sat)}$ with positive temperature coefficient
- High short circuit capability, self limiting to 6 x I_C

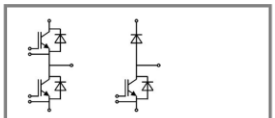
Typical Applications

- AC inverter drives
- mains 575 - 750 V AC
- Public transport (auxiliary syst.)
- Wind power

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
Inverse Diode						
$V_F = V_{EC}$	I_{Fnom} = 300 A; V_{GE} = 0 V	T_j = 25 °C$_{chiplev.}$		1,7	1,9	V
		T_j = 125 °C$_{chiplev.}$		1,8	2	V
V_{F0}		T_j = 25 °C		1,2	1,4	V
		T_j = 125 °C		0,9	1,1	V
r_F		T_j = 25 °C		1,7	1,7	mΩ
		T_j = 125 °C		3	3	mΩ
I_{RRM}	I_{Fnom} = 300 A	T_j = 125 °C		418		A
Q_{rr}	di/dt = 5800 A/µs			117		µC
E_{rr}	V_{GE} = -15 V; V_{CC} = 1200 V			78		mJ
$R_{th(j-c)D}$	per diode				0,125	K/W
FWD						
$V_F = V_{EC}$	I_{Fnom} = 300 A; V_{GE} = 0 V	T_j = 25 °C$_{chiplev.}$		1,7	1,9	V
		T_j = 125 °C$_{chiplev.}$		1,8	2	V
V_{F0}		T_j = 25 °C		1,2	1,4	V
		T_j = 125 °C		0,9	1,1	V
r_F		T_j = 25 °C		1,7	1,7	V
		T_j = 125 °C		3	3	V
I_{RRM}	I_{Fnom} = 300 A	T_j = 125 °C		418		A
Q_{rr}	di/dt = 5800 A/µs			117		µC
E_{rr}	V_{GE} = -15 V; V_{CC} = 1200 V			78		mJ
$R_{th(j-c)FD}$	per diode				0,125	K/W
Module						
L_{CE}				15	20	nH
$R_{CC'+EE'}$	res., terminal-chip	T_{case} = 25 °C		0,35		mΩ
		T_{case} = 125 °C		0,5		mΩ
$R_{th(c-s)}$	per module				0,038	K/W
M_s	to heat sink M6		3		5	Nm
M_t	to terminals M6		2,5		5	Nm
w					325	g

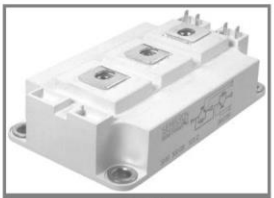
This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.



GB GAL

SKM 400GB176D



SEMITRANS® 3

Trench IGBT Modules

SKM 400GB176D

SKM 400GAL176D

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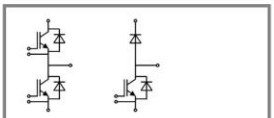


GB GAL

Z_{th} Symbol	Conditions	Values	Units
$Z_{th(j-c)I}$			
R_i	i = 1	52	mk/W
R_i	i = 2	18	mk/W
R_i	i = 3	4,6	mk/W
R_i	i = 4	0,4	mk/W
tau_i	i = 1	0,0569	s
tau_i	i = 2	0,0122	s
tau_i	i = 3	0,002	s
tau_i	i = 4	0,02	s
$Z_{th(j-c)D}$			
R_i	i = 1	85	mk/W
R_i	i = 2	28	mk/W
R_i	i = 3	10,5	mk/W
R_i	i = 4	1,5	mk/W
tau_i	i = 1	0,054	s
tau_i	i = 2	0,0075	s
tau_i	i = 3	0,0018	s
tau_i	i = 4	0,0002	s

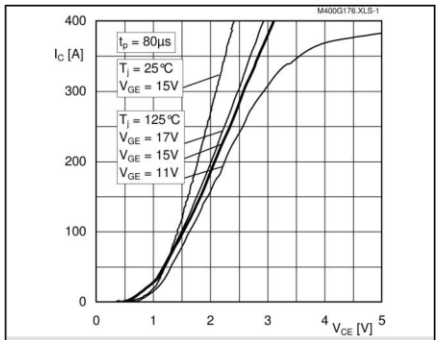


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

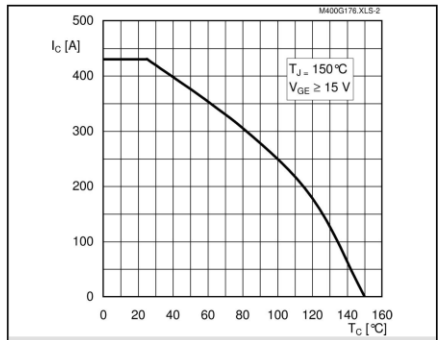


Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

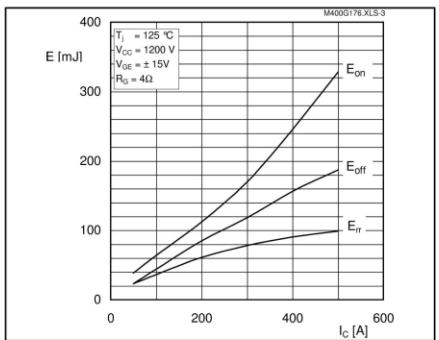


Fig. 3 Typ. turn-on /-off energy = f (I_C)

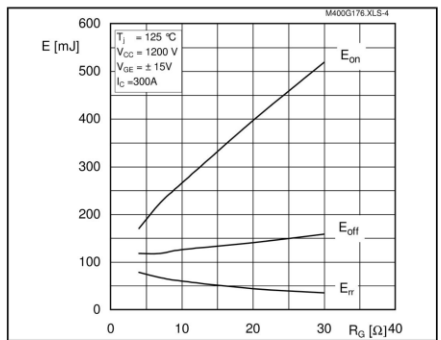


Fig. 4 Typ. turn-on /-off energy = f (R_G)

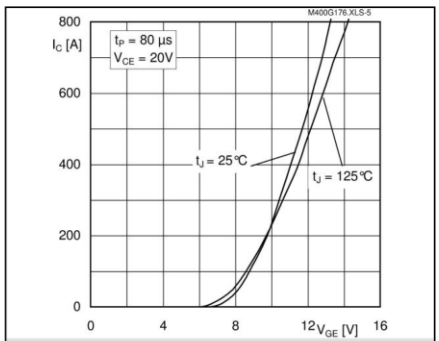


Fig. 5 Typ. transfer characteristic

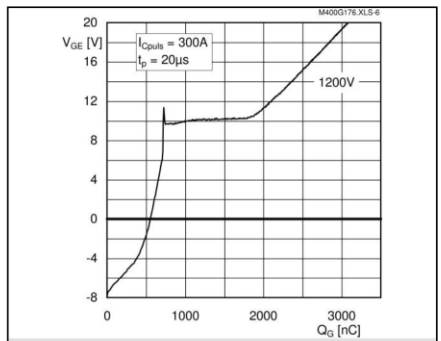


Fig. 6 Typ. gate charge characteristic

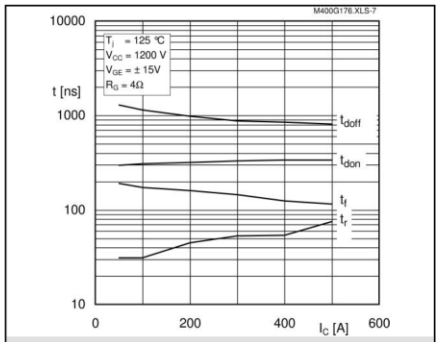


Fig. 7 Typ. switching times vs. I_C

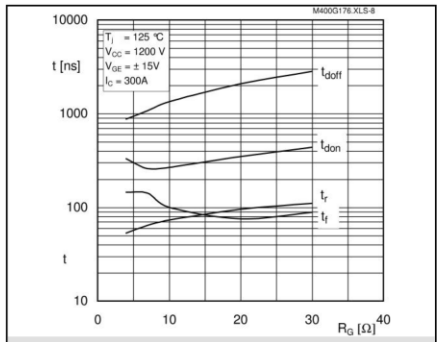


Fig. 8 Typ. switching times vs. gate resistor R_G

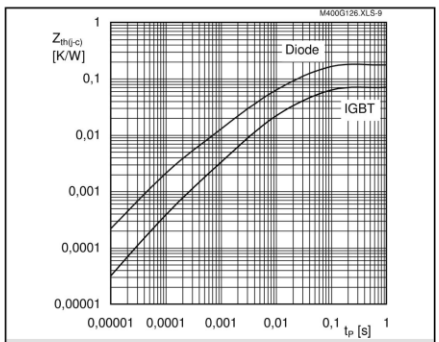


Fig. 9 Transient thermal impedance

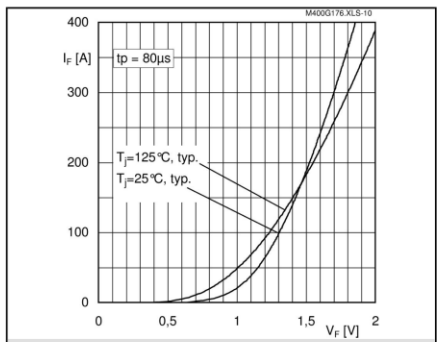


Fig. 10 CAL diode forward characteristic

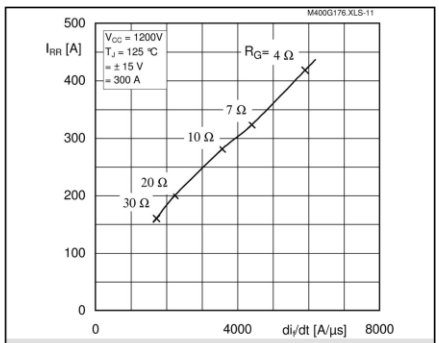


Fig. 11 Typ. CAL diode peak reverse recovery current

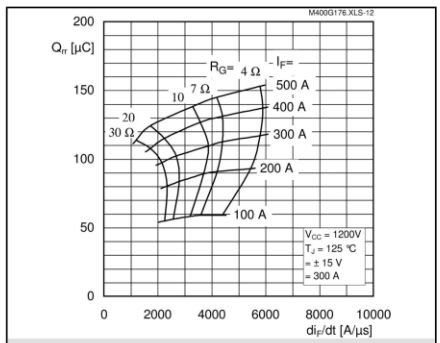
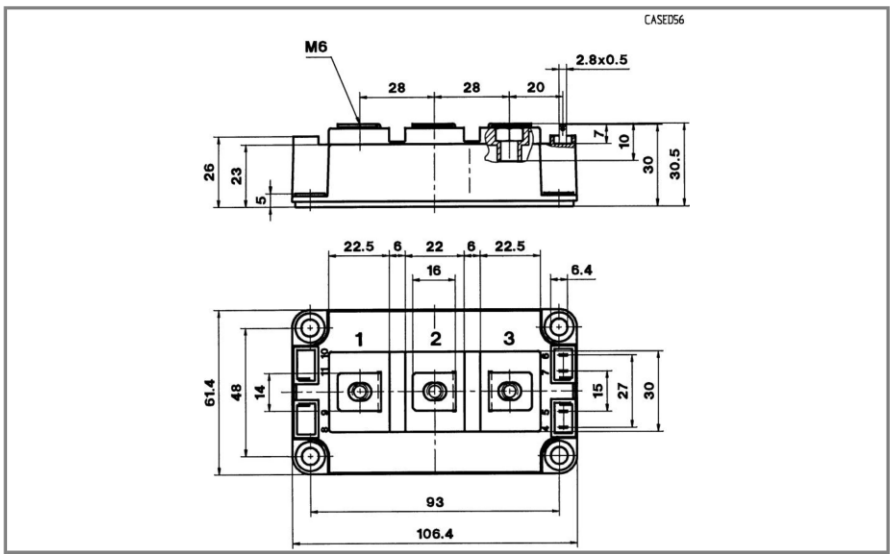
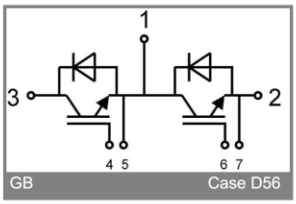


Fig. 12 Typ. CAL diode peak reverse recovery charge

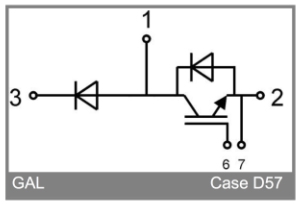
SKM 400GB176D



Case D 56



GB Case D56



GAL Case D57

Appendix B

AFE implementation figures

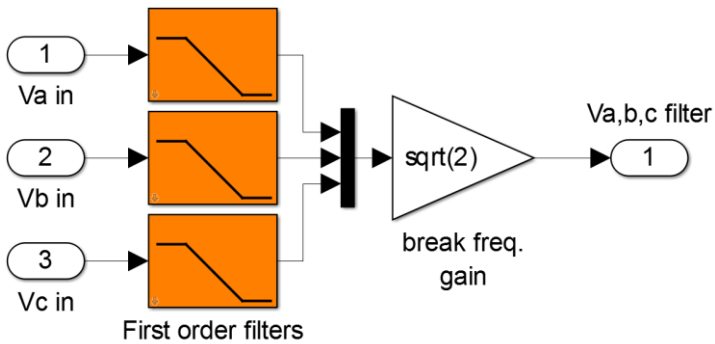


Figure B.1: First order low pass filters for grid voltage measure in AFE.

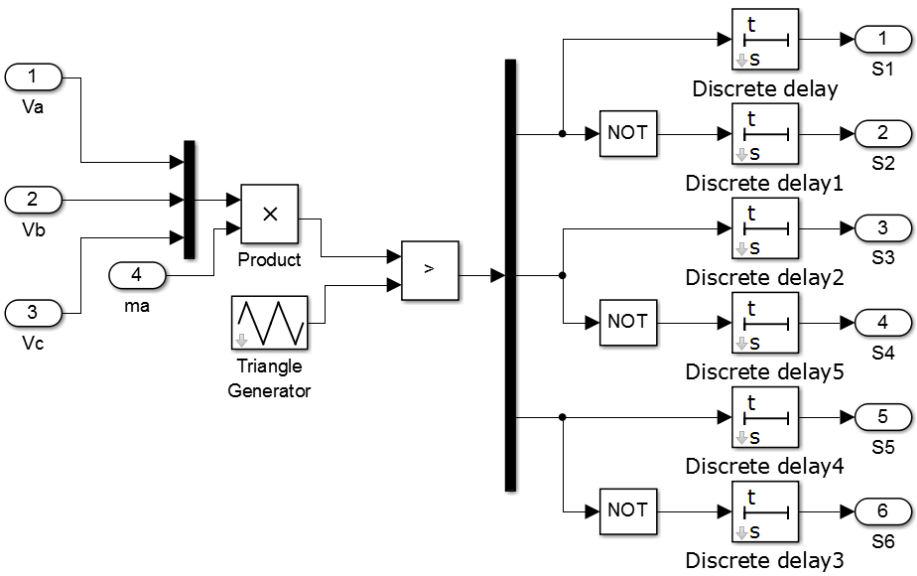


Figure B.2: PWM generator, sinusoidal input signals is compared with a triangular wave and output signals are sent to the gate on the transistor.

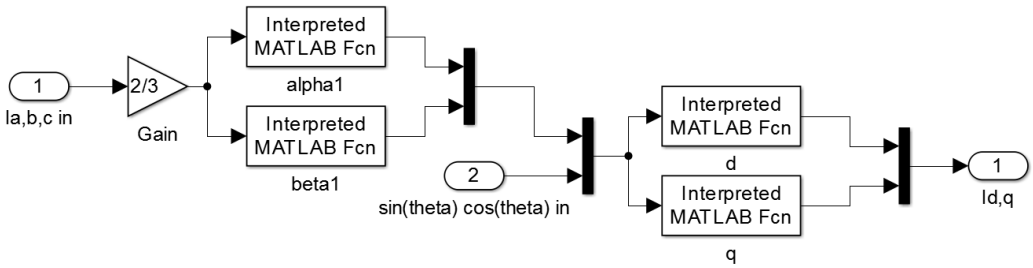


Figure B.2: The current transformation from abc to d,q.

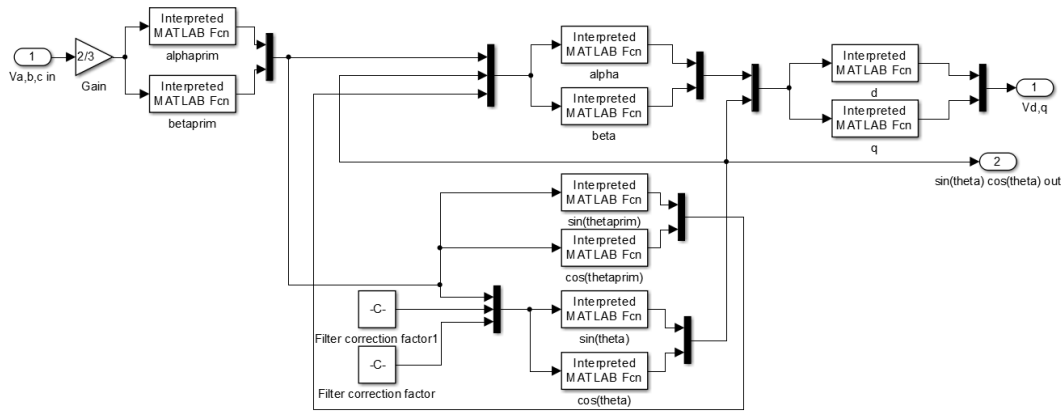


Figure B.3: The voltage transformation from abc to d,q together with filter compensation and angel generation.

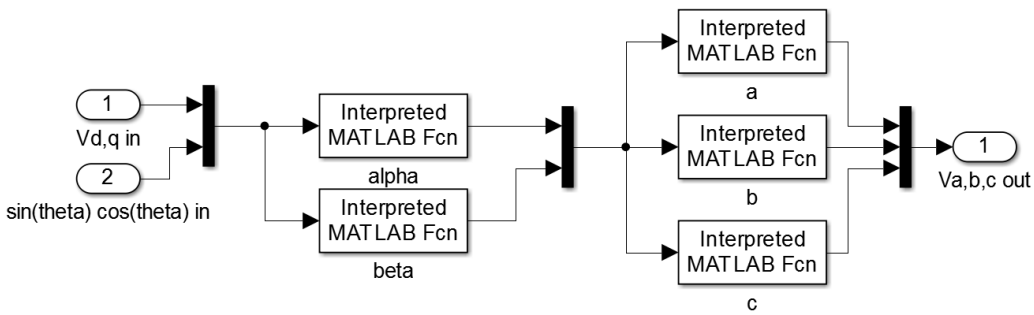


Figure B.4: The voltage transformation from d,q to a,b,c.

Appendix C

AFE simulation results

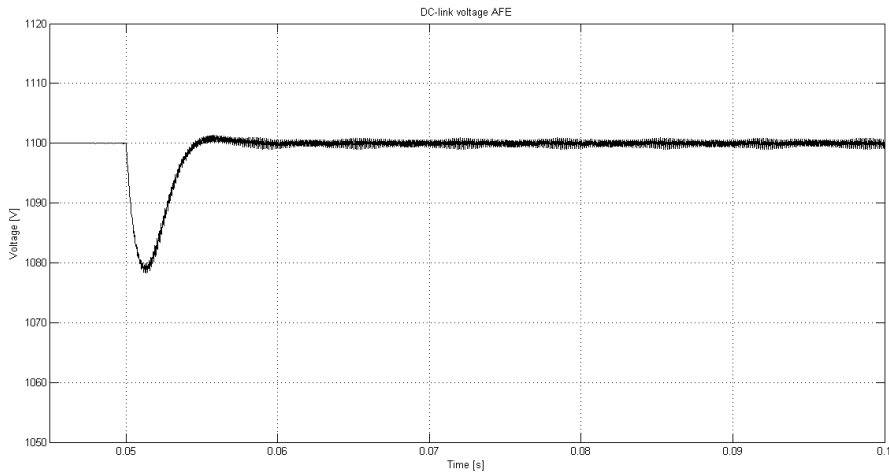


Figure C.1: Plot from simulation with output quantities; AFE DC-link voltage @ 200 kW, $L_{grid} = 0$.

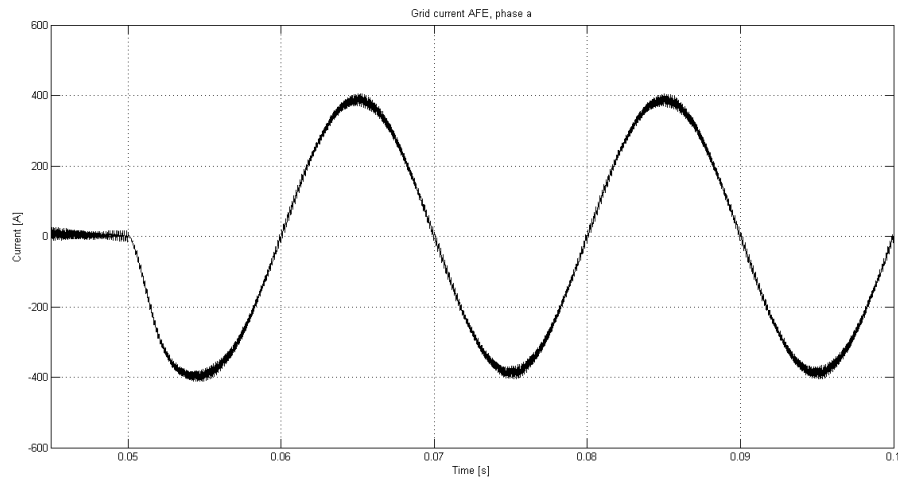


Figure C.2: Plot from simulation with output quantities; AFE grid current @ 200 kW, L_{grid} = 0.

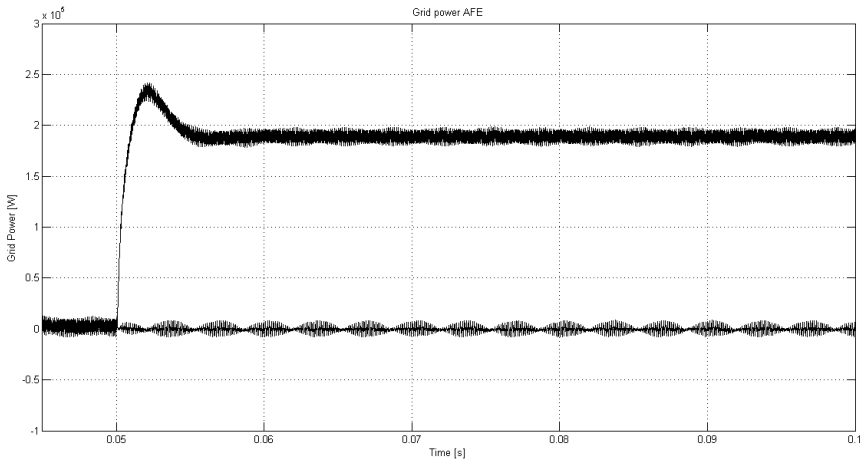


Figure C.3: Plot from simulation with output quantities; AFE grid power (Q @ ~ 0 kW, P @ ~ 200 kW, L_{grid} = 0).

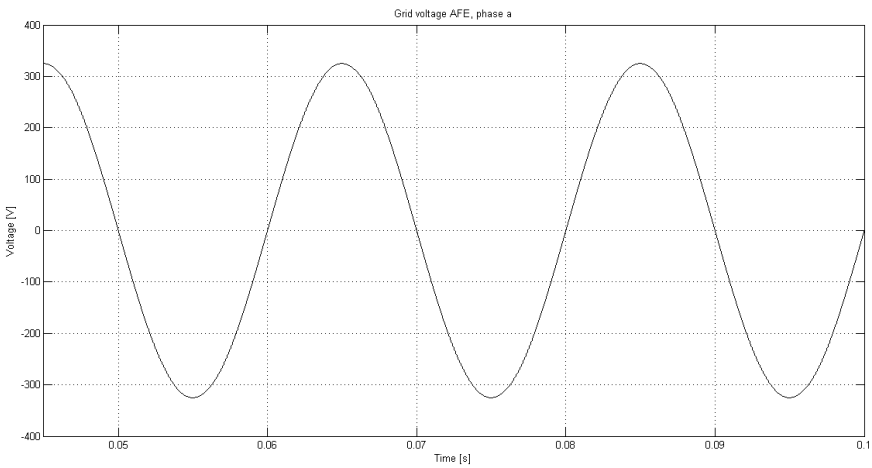


Figure C.4: Plot from simulation with output quantities; AFE grid voltage @ 200 kW, L_{grid} = 0.

DC/DC simulation results

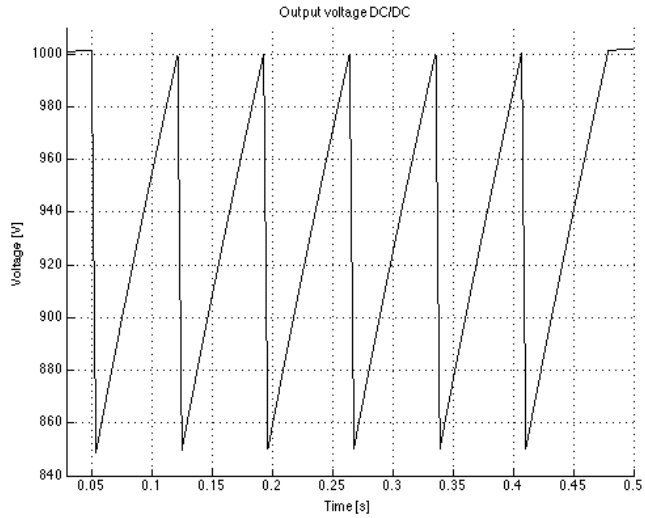


Figure C.5: Plot from DC/DC-simulation of the output voltage type 1.

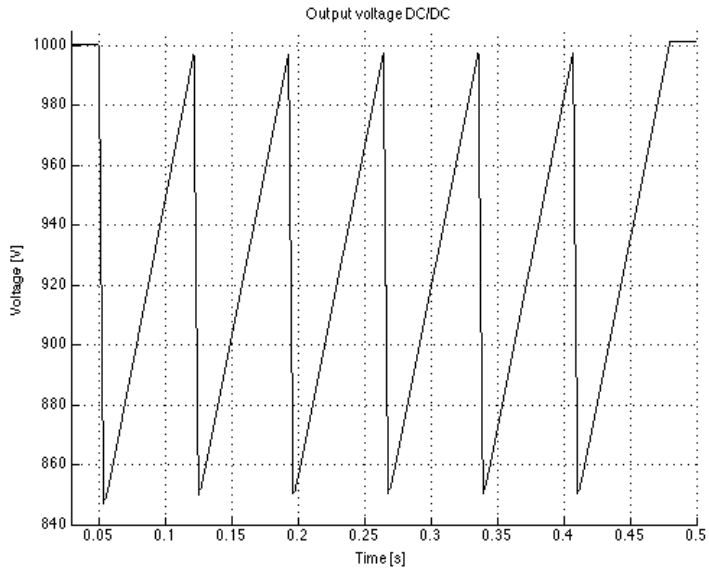


Figure C.6: Plot from DC/DC-simulation of the output voltage type 2.

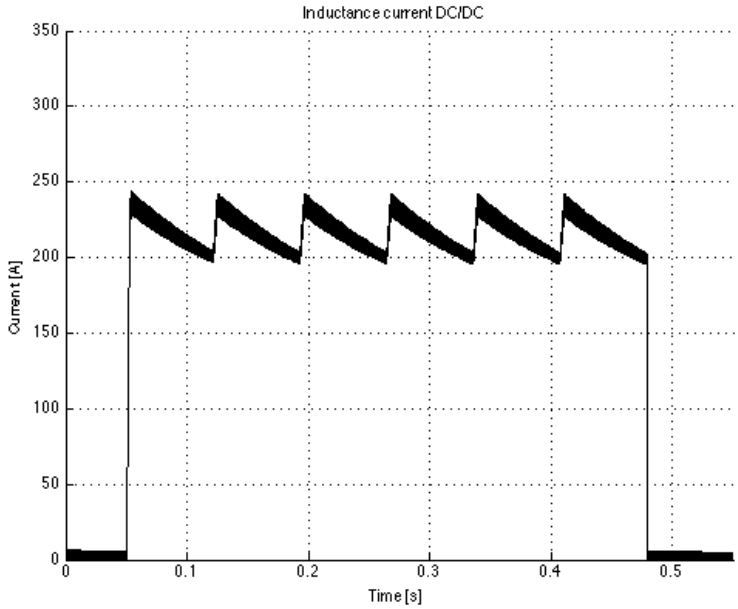


Figure C.7: Plot from DC/DC-simulation of the inductance current type 1.

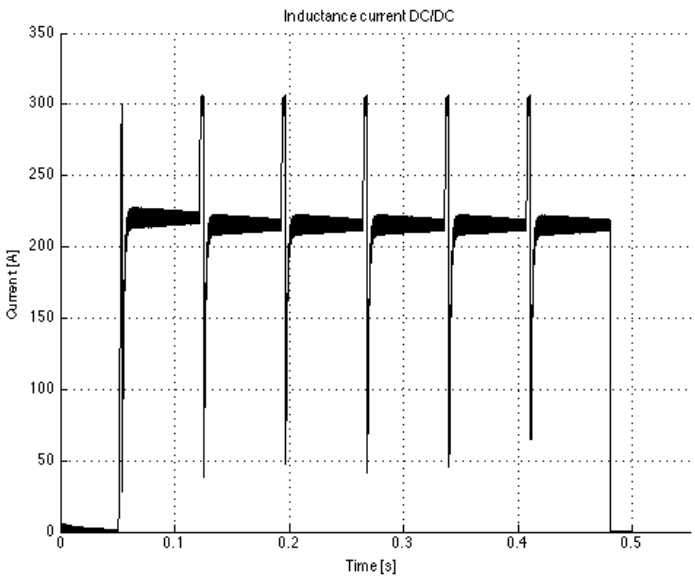


Figure C.8: Plot from DC/DC-simulation of the inductance current type 2.

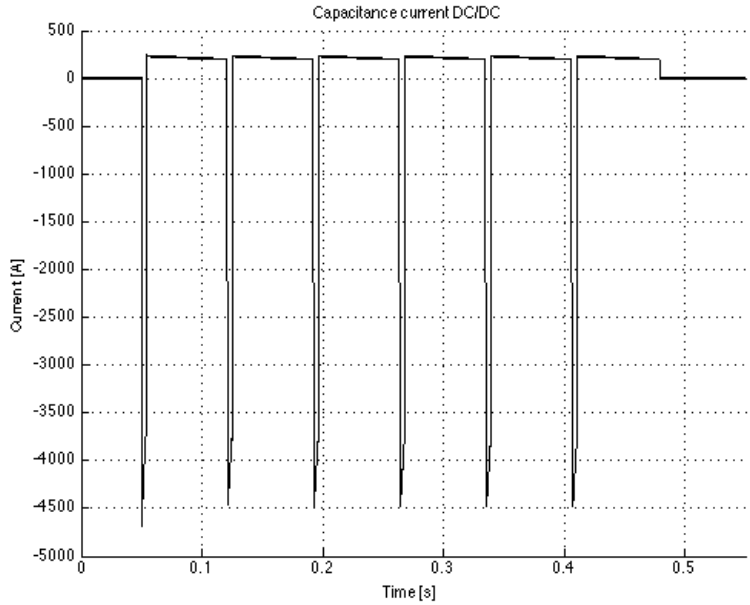


Figure C.9: Plot from DC/DC-simulation of the capacitance current type 1.

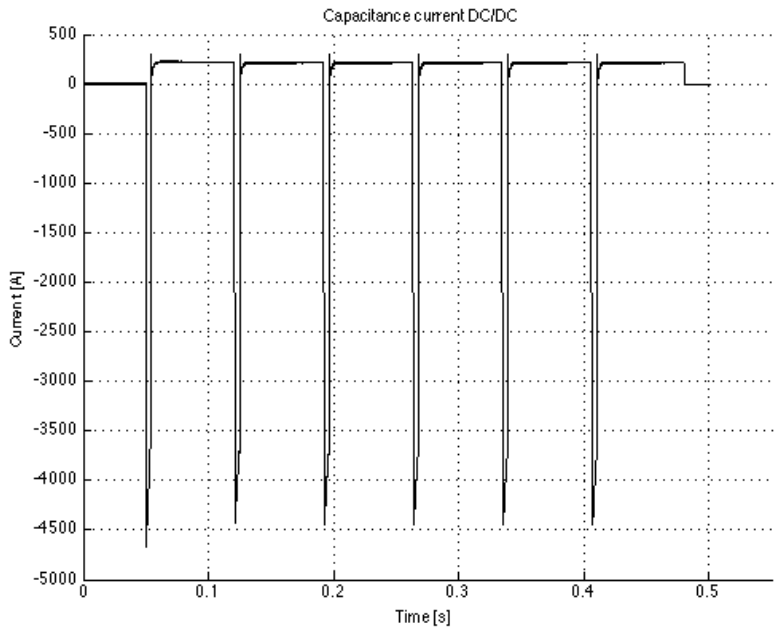


Figure C.10: Plot from DC/DC-simulation of the capacitance current type 2.

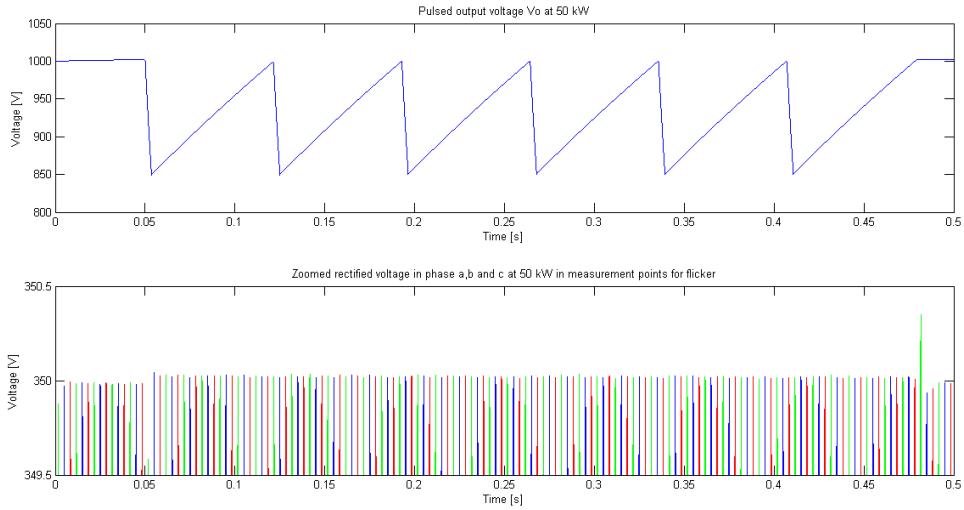


Figure C.11: Rectified voltage levels in all the three phases at 50 kW.

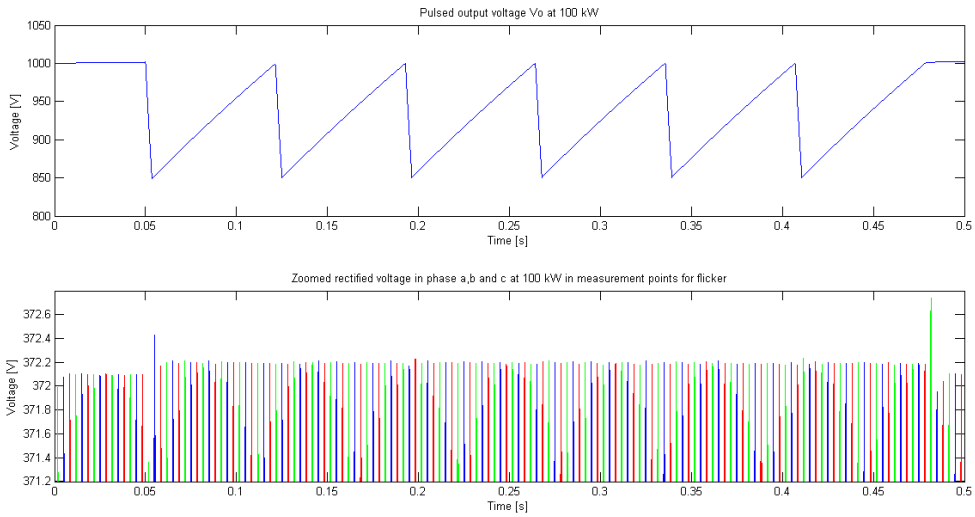


Figure C.12: Rectified voltage levels in all the three phases at 100 kW.

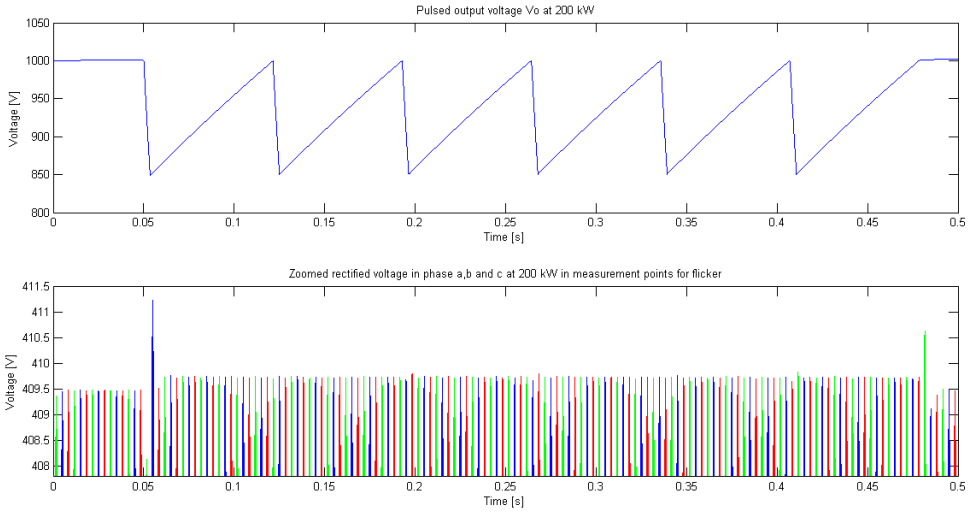


Figure C.13: Rectified voltage levels in all the three phases at 200 kW.