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Master Thesis

Low-Frequency Noise in TFETs

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"The Road goes ever on and on
Down from the door where it began.
Now far ahead the Road has gone,
And I must follow, if I can,
Pursuing it with eager feet,
Until it joins some larger way
Where many paths and errands meet.
And whither then? I cannot say."

J. R. R. Tolkien, *The Fellowship of the Ring*

LUND UNIVERSITY

Abstract

Faculty of Engineering, LTH
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Low-Frequency Noise in TFETs

by Markus Hellenbrand

Nanowire tunnel field-effect transistors (TFETs) were investigated by carrying out noise measurements and low-temperature DC measurements. The TFET tunnelling junction was realised by a GaSb/InAs heterojunction resulting in a broken band gap. TFET noise currents were measured at frequencies between 10 Hz and 1 kHz. The results imply that noise in TFETs at the current state of development is dominated by generation-recombination processes caused by traps in the gate oxide. Trap densities between 10^{20} cm^{-3} eV^{-1} and 10^{22} cm^{-3} eV^{-1} were extracted from the noise measurements. The temperature-dependent DC measurements show that the TFETs' off-current is sensitive to the temperature, with lower off-currents at lower temperatures. This indicates that it is not only the tunnelling junction which is governing the off-current. It is concluded that in the devices' off-state electrons can still tunnel into the channel area through the broken band gap but require additional thermionic excitation over the bent channel conduction band to constitute a current.

Acknowledgements

"A father's goodness is higher than the mountains, a mother's goodness is deeper than the seas." As a physicist I briefly considered extending the mountains to the stars and the seas to outer space. However, while this would get even closer to the truth, I decided to leave this presumably Japanese proverb unaltered for the sake of poetry. And in the same way as my parents' goodness reaches beyond all borders, so does my gratitude. I thank my parents for all their love, their patience and their faith in me, for their guidance and their advice, all of which I can always be sure of, no matter if I live right next door, if I move a thousand kilometres away or to the other side of the world. The same applies to my grandparents and to my siblings, Stefan and Anne, all of whom I am just as thankful to. Without you all I would not be where and who I am – thank you.

While my family has always given me the energy to reach further and beyond, there always has to be – using J. R. R. Tolkien's words – a "road [that] goes ever on and on, down from the door where it began" to direct this energy. The one who opened the door for me and showed me the road that I have travelled for the last eight months is Lars-Erik Wernersson. Always optimistic, enthusiastic about the ways of nature and inspiring the same enthusiasm in those working with him, Lars-Erik refined my general interest in solid state physics and showed me the huge world of the very small. Thank you, Lars-Erik, for opening the door for me and for letting me be part of your vision.

Pursuing the large way of this thesis I found myself on many paths and errands. On all of them I always received great support. I thank Karl-Magnus Persson for introducing me to the tuneful world of noise, its measurement and evaluation and for helping me with all my questions, Erik Lind for helping me to make sense of all the noise, Elvedin Memisevic for letting me in on the secrets of cleanroom processing and Guntrade Roll for valuable feedback on this thesis, for helping me with all kinds of measurements, from low-temperature measurements to solving setup peculiarities. Especially for the latter I also thank Göran Jönsson and Martin Nilsson who know the measurement lab better than anyone else and often provided helpful assistance. Furthermore, I thank my second supervisor and programme coordinator Dan Hessman and apart from the concrete support mentioned above I thank the whole Nanoelectronics research group for a welcoming and harmonious environment from my first work day on.

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physicists and experts from related sciences here in Lund as well as back in Heidelberg, my dear friends from Domino who are a family in their own right and of course my oldest friends from Trier. Please forgive me if I do not name all of you here – there are just so many of you whom I would like to thank. However, from this plea I have to make but two exceptions. First, I thank you, Sudha. You have been here with me the longest and will hopefully stay with me for several years to come. And second and in the end, looking back to the beginning and closing the circle, I thank my best friend Kevin. Thank you for always bringing me back in tune when I run the risk of losing the main melody among too many variations, for understanding even the most adventurous of my trains of thought and both most simply and most complex – for your friendship.

Thank you all.

Markus Hellenbrand

Contents

Acronyms

MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
TFET	**T**unnelling **F**ield-**E**ffect **T**ransistor
BTB	**B**and-**T**o-**B**and
WKB	**W**entzel-**K**ramers-**B**rillouin
MOVPE	**M**etal-**O**rganic **V**apour **P**hase **E**pitaxy
EBL	**E**lectron **B**eam **L**ithography
SEM	**S**canning **E**lectron **M**icroscope
ALD	**A**tomic **L**ayer **D**eposition
EOT	**E**ffective **O**xide **T**hickness
PSD	**P**ower **S**pectral **D**ensity
SMU	**S**ource/**M**onitor **U**nit
GPIB	**G**eneral **P**urpose **I**nterface **B**us
DUT	**D**evice **U**nder **T**est
NDR	**N**egative **D**ifferential **R**esistance
RF	**R**adio **F**requency

Physical Constants

Speed of Light	c	=	$2.997\ 924\ 58 \times 10^{8}$ m / s
Elementary Charge	q	=	$1.602 \times 10^{-19}\ C$
Boltzmann Constant	k_B	=	1.381×10^{-23} J / K
Planck Constant	h	=	6.626×10^{-34} Js
Free Electron Mass	m_0	=	9.11×10^{-31} kg
Vacuum Permittivity	ϵ_0	=	8.854×10^{-12} F / m

Symbols

E_F	Fermi Level	eV
E_V	Valence Band Energy	eV
E_C	Conduction Band Energy	eV
I	Current	A
V	Voltage	V
D	Diffusion Coefficient	m^2 / s
$n(x)$	Carrier Concentration	m^{-3}; m^{-2}
L	Length	m
T	Temperature	K
S	Subthreshold Slope	V / decade
C	Capacitance	F
k	Wave Vector	m^{-1}
m^*	Effective Mass	
T_{WKB}	WKB Tunnelling Probability	
E	Energy	eV
J_{1D}	1D Current Density	A / m
E_G	Band Gap	eV
v	Velocity	m / s
$F(E)$	Fermi Distribution	
W	Width	m
A	Area	m^2
N	Number of Carriers	
t	Time	s
$S(f)$	Power Spectral Density	A^2 / Hz; V^2 / Hz
f	Frequency	Hz

$\overline{X^2(t)}$	Noise Power	A^2; V^2
g_m	Transconductance	S
ϵ	Permittivity	F / m
Ψ	Potential	V
ξ	Maximum Junction Electric Field	V / m
τ	Time Constant	s
λ	Tunnelling Attenuation Length	m
μ	Mobility	m^2 / Vs
α_H	Hooge Parameter	

Chapter 1

Introduction

One of the most important elements of electronic devices omnipresent in our daily life is the transistor. Its most prominent realisation is the metal-oxide-semiconductor field-effect transistor (MOSFET). Over the last 50 years it has undergone continuous development, ever increasing speed and integration density. This improvement of transistors as the most basic processing unit was and is necessary to be able to cope with the ever increasing amount of information being processed on all levels of our society – be it by trivial smartphone games, life support machines or global trade.

However, the improvement of MOSFETs is facing increasing difficulties. The main developing factor has been geometrically scaling down MOSFETs and thus increasing their speed. One of the major problems of this approach is an also ever increasing energy dissipation. The energy dissipation of closely packed transistors has reached the limit of what can be dealt with. To be able to continue the improvement of transistors, their supply voltage has to be reduced to lower their energy dissipation [1]. For MOSFETs this is not possible because at a lower supply voltage the ratio between the on- and the off-current would be diminished unacceptably [2].

A quantitative measure for this problem is the subthreshold slope, which expresses the change in gate bias necessary to change the source-drain current by one order of magnitude. For MOSFETs the lower limit of the subthreshold slope is 60 mV / decade, which will be shown in the theory part. This limit comes about because the electron energies in the device contacts are governed by the Fermi-Dirac distribution. To constitute a current the electrons in a MOSFET are thermionically injected into the conducting channel. As the Fermi-Dirac distribution's high-energy tail is infinitely extended in energy and the MOSFET device design does not introduce an upper limit to the electron energies, there will always be electrons which can enter the channel – even in the device's

off-state [3]. So, to reduce transistor supply voltages and thus the energy dissipation, new device physics has to be introduced, different from that of MOSFETs.

Tunnel field-effect transistors (TFETs) are among the most promising devices to overcome the subthreshold slope limit of 60 mV / decade [2]. Instead of overcoming an energy barrier to enter the conducting channel, in a TFET the electrons tunnel through the barrier constituted by the semiconductor band gap [4]. The band structure which enables this mechanism also imposes an upper limit on the temperature-dependent electron energies in the source contact (Fig. 1.1). Thus, the subthreshold slope is not temperature-dependent anymore and can reach far below the MOSFET limit [5].

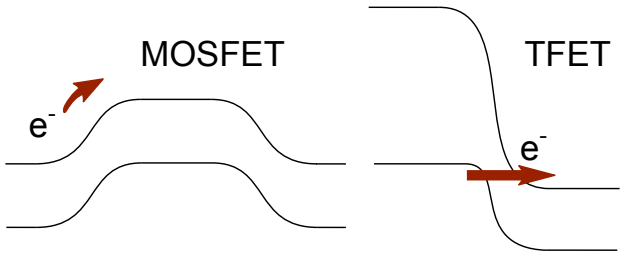

FIGURE 1.1: Schematic depictions of band structures to illustrate the different working principles of MOSFETs and TFETs.

The TFETs examined in this thesis combine the tunnelling physics with another revolutionary transistor design approach utilising nanowires instead of the conventional planar or fin-based device design. Nanowires are epitaxially grown crystals, forming rods with only a few nanometres in diameter but a few hundred nanometres length. Using nanowires as the backbone of transistors brings about two huge advantages. First, nanowires allow a gate-all-around device design which enhances the electrostatic gate control and reduces parasitic effects during device operation [6][7]. Second, nanowires allow the immediate combination of materials with different crystallographic lattice constants because of the nanowires' large surface-to-volume ratio. This ratio allows the crystal structures to relax from the strain induced at the different materials' contact area where lattices of two different lattice constants meet [8]. This possibility to combine different materials is very advantageous for the realisation of TFETs [9]. To be able to create a tunnelling junction the energy band structure at the junction has to exhibit a certain form (Fig. 1.1) which to realise is much easier by using two different materials instead of only varied doping. The TFETs examined in this thesis use an GaSb/InAs combination resulting in a broken band gap at the material junction. This broken band gap constitutes a large tunnelling window for electrons to pass through in the on-state and thus leads to large on-currents [9].

As much as MOSFETs are facing the end of their development there is still a long way to go for TFETs until they can be used industrially. In this thesis the transport and material properties of TFETs are studied by the means of low-frequency noise

measurements and temperature-dependent DC measurements. The term *noise* refers to random and spontaneous fluctuations in an otherwise well-controlled signal. Noise stems from different sources, some of which will be examined in the theory part later on. These sources can be identified from characteristic measurement results. As noise occurs in all electrical devices noise measurements on TFETs can provide information about the mechanisms diminishing device operation. These mechanisms again indicate which parts of the measured TFETs require improvement. The temperature-dependent measurements can reveal in how far TFETs are really free from the temperature effects which limit the MOSFET off-currents.

To approach the working principles of TFETs and to gain a basic understanding of noise mechanisms a brief theoretical background will be provided on both topics. To relate theory to practice an overview of the TFET fabrication process will be presented. After that, the different instruments of the measurement setup will be described, focussing on their intrinsic noise to secure the instruments' usability for noise measurements. The measurement results will be presented and analysed afterwards, completed by conclusions and and outlook on future research.

Chapter 2

Theory

2.1 Overview and Comparison with MOSFETs

First, the differences between MOSFET and TFET working principles will be elaborated on with the help of energy band structures. The main difference is shown in Fig. 2.1: In a MOSFET the current through the device is set by an energy barrier whose height determines the amount of carriers thermionically injected into the channel (Fig. 2.1(a)). In contrast to that in a TFET the carriers tunnel through a barrier to reach the channel [4] (Fig. 2.1(c)).

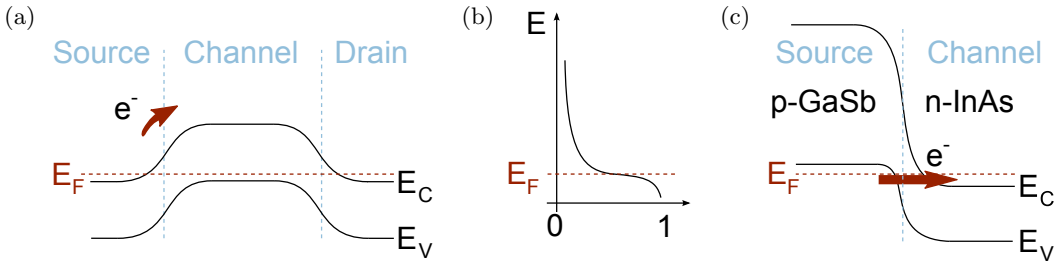

FIGURE 2.1: Figure from the introduction in more detail together with the electron energy distribution (Fermi-Dirac distribution). **(a)** For a MOSFET, electrons in the high-energy Fermi-Dirac tail **(b)** can overcome the channel energy barrier even in the transistor's off-state. **(c)** For a TFET this tail is cut off by the source valence band. E_F, E_C and E_V denote the Fermi level, the conduction and the valence band, respectively.

To switch a MOSFET between its on- and its off-state the energy barrier shown in Fig. 2.1(a) is raised or lowered so that more or less electrons can surpass it. The bands in the channel area of a TFET are raised and lowered as well but the on- and off-conditions are different from those in a MOSFET. In a TFET's on-state the channel conduction band has to be lowered below the source valence band to open a tunnelling window between source and channel. In the off-state this window is closed again when the channel conduction band is raised above the source valence band. The band structure

necessary to achieve this behaviour (Fig. 2.1(c)) can be realised by using a semiconductor heterostructure to create the tunnelling junction. III-V material combinations have been found to be very versatile in band-engineering. As mentioned in the introduction the TFETs used during this thesis are based on GaSb and InAs which results in a band structure very similar to the one shown in Fig. 2.1(c) [9][10].

Comparing Figs. 2.1(a) and 2.1(c) reveals how the tunnelling mechanism brings about a smaller off-current than the thermionic carrier injection. While in a MOSFET there are always electrons in the high-energy Fermi-Dirac tail (Fig. 2.1(b)) which can overcome the energy barrier from the source side, in a TFET this tail is cut off by the source valence band. Instead, the off-current in an ideal TFET originates in direct source-to-drain tunnelling. But as the barrier for this process is quite thick (the whole channel region) a TFET's off-current is much smaller than that of a MOSFET.

The MOSFETs' lower limit of 60 mV / decade at room temperature for the subthreshold slope originates in this fact that the Fermi-Dirac high-energy tail reaches beyond the source-to-channel energy barrier. The 60 mV / decade limit prevents MOSFETs from being operated at lower voltages as lowering the drive voltage V_{DD}, but maintaining the on-performance ($V_{DD} - V_T$), where V_T is the threshold voltage, exponentially increases the off-current and thus the power dissipation (Fig. 2.2). As in TFETs the high-energy Fermi-Dirac tail is cut off, the subthreshold slope for a TFET is not dependent on the temperature anymore and can be smaller than 60 mV / decade. This allows operation at lower V_{DD} than in MOSFETs [2] (Fig. 2.2). The downside of the tunnelling mechanism, however, is that it reduces the on-current, as the tunnelling probability exponentially depends on the barrier thickness and the band gap [11].

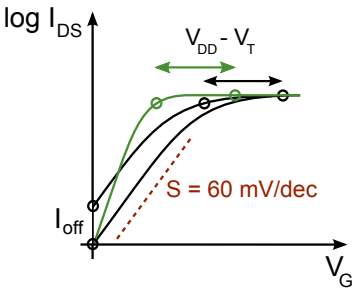

FIGURE 2.2: By keeping a MOSFET's on-state performance and thus ($V_{DD} - V_T$) constant, the off-current is increased exponentially if the gate bias range is not changed as well [2]. To overcome this, devices with a lower subthreshold slope are required.

2.2 Modelling

In the following the above-mentioned properties will be treated mathematically.

2.2.1 MOSFET Subthreshold Slope

A MOSFET's subthreshold slope's temperature dependence follows directly from the MOSFET off-current I_{off} which can be found in literature (e. g. [3]):

$$I_{off} = -qzD_n \frac{dn(x)}{dx} = -qzD_n \frac{n(0) - n(L)}{L}. \tag{2.1}$$

Here, q is the elementary charge, z the channel thickness, D_n the charge carrier diffusion coefficient, $n(x)$ the electron sheet density in the channel and L the channel length.

The electron sheet density inserted into Eq. 2.1 can be derived with the help of Fig. 2.3 [3]. For a drain bias $V_{DS} > 3k_BT/q$ this results in the off-state current

$$I_{off} = \frac{qzD_n}{L}\, n_i\, exp\left(\frac{q(\Psi_S - \Psi_B)}{k_BT}\right) \tag{2.2}$$

with the temperature T, the intrinsic carrier concentration n_i and Ψ_S and Ψ_B given in Fig. 2.3.

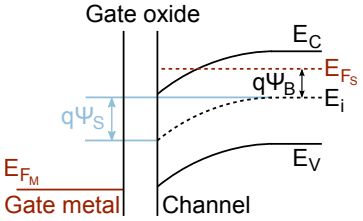

FIGURE 2.3: Energy diagram in proximity of the gate oxide [3]. Ψ_B and the surface potential Ψ_S are given as the differences between the intrinsic Fermi level E_i and the semiconductor Fermi level after doping E_{F_S} and the difference between E_i and the bent E_i close to the gate oxide, respectively. E_{F_M} is the gate metal Fermi level, E_C the semiconductor conduction band and E_V the semiconductor valence band.

As the subthreshold slope S gives the change in gate voltage V_{GS} necessary to change the off-current by one order of magnitude it is defined as [3]

$$S := \left[\frac{\partial log(I_{off})}{\partial V_{GS}}\right]^{-1} = \left[\frac{\partial log(I_{off})}{\partial \Psi_S}\frac{\partial \Psi_S}{\partial V_{GS}}\right]^{-1}. \tag{2.3}$$

This expression for S can be solved by using the relation

$$V_{GS} = \Psi_S + V_{OX} = \Psi_S + \frac{\sqrt{2\epsilon_S \Psi_S qN_D}}{C_{OX}} \tag{2.4}$$

describing the potentials in a structure like the one in Fig. 2.3. In Eq. 2.4 V_{GS} is the applied gate voltage, Ψ_S the surface potential as before, V_{OX} the part of the gate voltage dropping over the gate oxide, ϵ_S the channel semiconductor permittivity, N_D the channel doping and C_{OX} the gate oxide capacitance. Inserting Eq. 2.4 into Eq. 2.3 S becomes

$$S = ln(10)\frac{k_BT}{q}\left(1 + \frac{C_D}{C_{OX}}\right) > 60\ mV\ /\ decade \tag{2.5}$$

with the channel depletion capacitance $C_D = \sqrt{\epsilon_S q N_D/(2\Psi_S)}$.

This lower limit of 60 mV / decade at room temperature is the fundamental problem for MOSFETs' energy-efficiency and can only be overcome by changing the physical basis of the devices.

2.2.2 Wentzel-Kramers-Brillouin Approximation for Tunnelling

In band-to-band (BTB) tunnelling electrons tunnel from one energy band through the forbidden band gap into another energy band. This process of tunnelling through an energy barrier is well-known from quantum mechanics and constitutes the underlying physical principle governing the current through TFETs. To calculate this current the transmission coefficient for a tunnelling barrier is required which will be derived in the following.

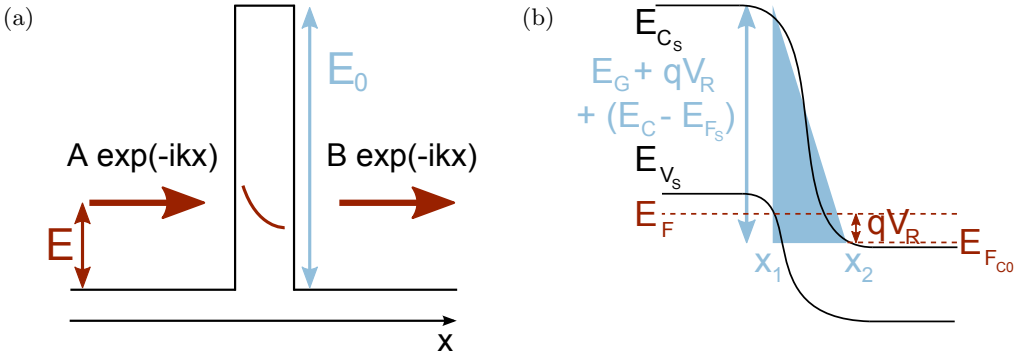

FIGURE 2.4: Quantum-mechanical tunnelling process and its application to a triangular barrier in a TFET. **(a)** Electron wave function transmitted through a rectangular barrier. The ratio of the wave amplitudes squared gives the transmission coefficient. **(b)** Triangular approximation of a TFET's tunnelling junction energy barrier with applied gate bias. E_{FC0} indicates the channel Fermi level in relation to the channel conduction band before applying a gate bias.

An electron wave function arriving at a rectangular energy barrier is partially reflected and partially transmitted depending on the wave function's energy and the energy barrier height. The transmission coefficient T can be calculated as $T = B^2/A^2$ where A and B are the amplitudes of the incoming and the transmitted wave, respectively [12] (Fig. 2.4(a)). In the Wentzel-Kramers-Brillouin (WKB) approximation it is assumed that the barrier potential which the wave function is subjected to varies slowly on the order of the de Broglie wavelength. This allows to find a solution to the Schrödinger equation as in a situation where the potential is constant [13]. For a non-rectangular barrier the WKB approximation can be applied by dividing the barrier into small rectangular sections and multiplying all transmission coefficients. This results in [11]

$$T_{WKB} = exp\left(-2\int_{x_1}^{x_2} |k_x| dx\right) \tag{2.6}$$

with the barrier boundary points x_1 and x_2 and the wave vector k_x inside the barrier. From quantum mechanics k_x inside the barrier can be calculated as

$$k_x(x) = \frac{\sqrt{2m^*(E_0(x) - E)}}{\hbar}, \tag{2.7}$$

where m^* is the effective mass, $E_0(x)$ the barrier potential and E the electron energy [12]. In a TFET structure as shown in Fig. 2.4(b) the barrier the electrons have to tunnel through can be approximated as triangular. For the barrier energy profile this results in $E_0(x) = E_G + qV_R + (E_{V_S} - E_F) - q\xi x$ with the band gap E_G, the maximum electric field $\xi = (E_G + qV_R + (E_{V_S} - E_F))/(q(x_2 - x_1))$ at the junction and $x_1 < x < x_2$. Calculating WKB transmission coefficient T_{WKB} for this structure results in

$$T_{WKB}^{1D} = exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar\xi}\right), \tag{2.8}$$

if one-dimensional (1D) transport is assumed [5]. For the calculation of the current through a nanowire TFET in the following, 1D transport will be assumed as well, although this assumption is actually ahead of the current state of development. It will be discussed later on.

2.2.3 1D Tunnelling Junction

To be able to enter the channel from the source side the source electron energy has to be higher than the highest occupied state in the channel, so there will only be a current in the energy window set by the source and channel energy levels. Compared to a junction where the charge carriers do not have to tunnel through an energy barrier the current through a tunnelling junction is diminished by the tunnelling probability. Thus, the current through a tunnelling junction can be calculated as the sum of all electrons moving from source to channel in the respective energy window multiplied by the tunnelling coefficient (e. g. [14]):

$$I = J_{1D} = 2\frac{q}{L}\sum_{k_x} v_x(F_S - F_C)\, T_{WKB}. \tag{2.9}$$

Here L is the junction length $(x_2 - x_1)$ (Fig. 2.4(b)), k_x is the wave vector in tunnelling direction, v_x the group velocity and F_S and F_C are the Fermi-Dirac distributions governing the electron energies in the source and the channel, respectively. The Fermi-Dirac distributions are denoted by a capital F to avoid confusion with the frequency f later on. The factor 2 results from spin degeneracy. Assuming that the wave vectors are

closely spaced the sum 2.9 can be converted to the integral

$$I = \frac{2q}{L}\frac{L}{2\pi}\int \frac{1}{\hbar}\frac{\partial E_x}{\partial k_x}(F_S - F_C)\ T_{WKB}\ dk_x, \tag{2.10}$$

where the group velocity $v_x = 1/\hbar\ \partial E_x/\partial k_x$ has been inserted and the pre-factor $L/(2\pi)$ results from the transformation from a sum to an integral. As the group velocity v_x contains a derivative of the energy E_x with respect to k_x the integral over k_x becomes an integral over the energy. In the case of an n-doped channel where the Fermi level in equilibrium lies above the channel conduction band the energy window in which the electrons can tunnel through the junction is directly given by the voltage V_R applied to the junction (Fig. 2.4(b)). Assuming this to be true in the given case and assuming $(F_S - F_C) = 1$ as an approximation the integral becomes

$$I = \frac{2q}{2\pi}\int_0^{qV_R}\frac{1}{\hbar}\ T_{WKB}\ dE_x = \frac{2q^2}{h}V_R\ T_{WKB}. \tag{2.11}$$

This result resembles that of the current in a 1D nanowire MOSFET in the quantum capacitance limit [14], which means that the oxide capacitance is much larger than the semiconductor capacitance. The result from Eq. 2.11 could be expected from calculating the TFET current in the same way as calculating a non-tunnelling device current and then multiplying it by an energy-independent factor accounting for the tunnelling as has been done here. Strictly, assuming $(F_S - F_C) = 1$ to arrive at the given result is only valid for a temperature T = 0 K and will be discussed in the following section.

2.2.4 Extension to Complete 1D Treatment and 3D

For a complete derivation the integral 2.10 has to be carried out over the whole energy range with $(F_S - F_C)$ remaining in the integral. With the thermal voltage $V_T = k_B T/q$ the result for this is

$$I = \frac{2q^2}{h}V_T\ ln\left(\frac{1}{2}\left(1 + cosh\frac{V_R}{V_T}\right)\right)T_{WKB}, \tag{2.12}$$

which yields a slightly reduced current as compared to Eq. 2.11 due to the smoothed out Fermi distributions at temperatures above zero. The derivation of this result can be found in [5]. At T = 0 K Eq. 2.12 simplifies to $I = (2q^2/h)\ V_R\ T_{WKB}$ again [5] which is consistent with the result above.

For a nanowire to exhibit 1D transport characteristics the separation of the energy sub-bands due to confinement in radial direction should be much larger than $k_B T$. As a simplification for an estimation the nanowire is assumed to have a square base area with the nanowire diameter as side length. For a situation like this the sub-band energy

is known from quantum mechanics to be

$$E = \frac{\hbar^2\pi^2}{2m^*}\left(\frac{p^2}{W_y^2} + \frac{q^2}{W_z^2}\right) \tag{2.13}$$

with the sub-bands p and q and the confinement widths W_y and W_z in y- and z-direction, respectively [12]. The nanowire diameters were ca. 35 nm which results in a separation of $\Delta E = 0.04$ eV $= 1.6\ k_BT$ between the first two sub-bands, so 1D transport is not really given.

If the tunnelling current is treated in 3D instead the term $exp(-E_\perp/\bar{E})$ will appear in the tunnelling coefficient to attribute for the transverse-energy-states carriers' diminishing influence on the tunnelling current. Here, $E_\perp = \hbar^2(k_y^2 + k_z^2)/(2m^*)$ is the transverse energy and $\bar{E} = (q\hbar\xi)/(2\sqrt{2m^*E_G})$ [5]. The integral used for the calculation of the current from the charge carrier flux and the tunnelling coefficient will of course also include the transverse-energy states. Here, the derivation in the 1D case has been given preference to the 3D case to show the possibility and aim of future nanowire development.

2.2.5 TFET Subthreshold Slope

From the current found in Eq. 2.11 a 1D TFET's subthreshold slope will be examined to point out one of the most important TFET advantages over MOSFETs. Summarising constants with a and b and writing the result from Eq. 2.11 as

$$I = \frac{2q^2}{h}V_R\ T_{WKB} = aV_R(V_{GS})\ T_{WKB}(V_{GS}) = aV_R(V_{GS})exp\left(-\frac{b}{\xi(V_{GS})}\right) \tag{2.14}$$

(cp. Eq. 2.8 for T_{WKB}) the subthreshold slope becomes [15]

$$S = \left[\frac{\partial log(I)}{\partial V_{GS}}\right]^{-1} = ln(10)\left[\frac{1}{V_R}\frac{\partial V_R(V_{GS})}{\partial V_{GS}} - \frac{b}{\xi^2(V_{GS})}\frac{\partial \xi(V_{GS})}{\partial V_{GS}}\right]^{-1}. \tag{2.15}$$

None of the terms in the equation above depends on the temperature which – in contrast to MOSFETs – allows TFETs to reach subthreshold slopes below 60 mV / decade.

2.2.6 TFET Transconductance

For the evaluation of the noise measurements later on the transconductance g_m will be used. It is defined as $\partial I_{DS}/\partial V_{GS}$. With I_{DS} from Eq. 2.11, this results in

$$g_m = \frac{2q^2}{h}\ T_{WKB}, \tag{2.16}$$

as $V_R = V_{GS} - V_{OX}$ (Fig. 2.4(b)), where V_{OX} is the part of the applied gate voltage V_{GS} that drops over the gate oxide.

2.3 Noise

Up to now noise in TFETs has barely been studied [16][17][18]. Therefore, not much reference can be found regarding the topic. To achieve a basic understanding of noise properties nevertheless, a brief overview over noise in MOSFET devices will be given.

The gated area of a TFET does not only consist of a tunnel junction but also of a channel adjacent to the junction. Although this channel does not limit the maximum current level it can still be assumed that the channel contributes to the devices' noise behaviour in a similiar way as in a MOSFET, so studying MOSFET channel noise properties will also reveal information about TFET channel noise behaviour.

Junction related noise properties are not covered in detail as they could not be experimentally examined so far. Furthermore, it will turn out that at room temperature the channel noise dominates the state-of-the-art TFETs' noise behaviour.

The following treatments are based on [19].

2.3.1 General Noise Properties

Electrical noise is a random and spontaneous fluctuation in an otherwise well-controlled electrical signal. For a current this can be expressed as

$$I(t) = \bar{I} + \Delta I(t), \tag{2.17}$$

where $I(t)$ is the total signal, $\bar{I}$ is the well-controlled part of the signal and $\Delta I(t)$ the fluctuation referred to as noise.

The average current through a conductor of length L can be expressed as

$$\bar{I} = q\overline{nv_d}A = q\overline{Nv_d}/L, \tag{2.18}$$

where q is the electron charge, n the free charge carrier density, v_d the drift velocity, A the conductor cross section, N the total number of free charge carriers and L the length of the conductor. For a homogeneous conductor subjected to a uniform electric field the average drift velocity is the same for all carriers. Due to noise, however, both N and v_d

for single carriers can deviate from their average value:

$$N(t) = \overline{N} + \Delta N(t) \qquad v_i(t) = \overline{v_i} + \Delta v_i(t). \tag{2.19}$$

Using 2.18 for the noise current $\Delta I(t)$ this leads to

$$\Delta I(t) = \frac{q}{L}\overline{v_d}\Delta N(t) + \frac{q}{L}\sum_{i=1}^{\overline{N}} \Delta v_i(t). \tag{2.20}$$

In this sum the first term expresses number fluctuations and the second term expresses velocity fluctuations which can be related to mobility fluctuations via $v_i = \mu_i E$ with the individual carrier mobilities μ_i and the applied electric field E.

A measure often used to describe noise is the power spectral density $S(f)$ which gives the power of a signal distributed over its frequency components. Integrated over the whole frequency range the power spectral density (PSD) gives the total signal power $\overline{X^2(t)}$:

$$\int_0^\infty S_x(f)df = \overline{X^2(t)} = \lim_{T\to\infty} \frac{1}{T}\int_0^T X^2(t)dt. \tag{2.21}$$

2.3.2 White Noise: Thermal Noise and Shot Noise

If the PSD introduced in the section above is frequency-independent (Fig. 2.5) the underlying noise is referred to as white noise. The dominant part of white noise originates in the thermic motion of charge carriers present in any material above absolute zero. Due to constant scattering of charge carriers their randomised velocities can introduce small net currents in varying directions. For a resistor with resistance R at temperature T the PSD for its thermal noise current is

$$S_I = \frac{4k_B T}{R}, \tag{2.22}$$

where k_B is the Boltzmann constant. This type of noise is also referred to as Johnson-Nyquist noise after its discoverers John Bertrand Johnson and Harry Nyquist.

Another type of white noise is the so-called shot noise, which originates in the discrete nature of an electric charge facing an energy barrier. Electric current depends on the number of carriers, which – if treated as sum of discrete particles – shows Poisson fluctuations. Thus, shot noise requires a current to flow and its noise current follows the PSD

$$S_I = 2qI \tag{2.23}$$

with the electric charge q and the current I.

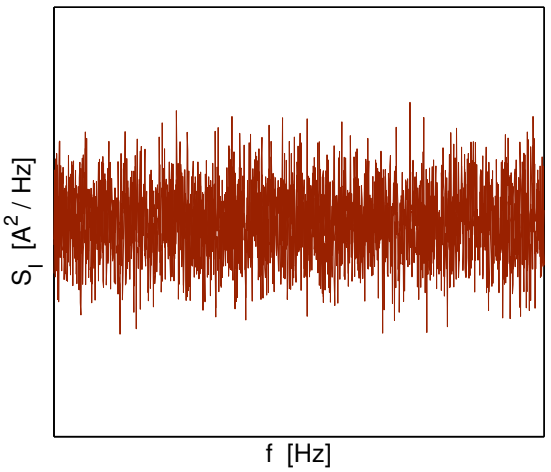

FIGURE 2.5: White noise is constant in frequency.

2.3.3 Generation-Recombination Noise and Number Fluctuations

The semiconductor and gate oxide crystal structures constituting most parts of MOS devices are not perfect but exhibit crystallographic defects ("traps") which can trap and release charge carriers (Fig. 2.6).

This trapping and the subsequent de-trapping can introduce number fluctuations in a MOS device's current. If the traps' energy levels are within a few k_BT of the Fermi level these number fluctuations will affect the device's current as noise, which is referred to as generation-recombination (g-r) noise due to the underlying physical principle. In MOS structures the devices' part which is most prone to the above-mentioned defects is the channel area where the channel semiconductor crystal is in contact with the gate oxide.

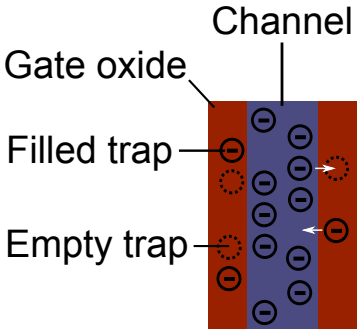

FIGURE 2.6: Schematic illustration of traps in the gate oxide. Crystallographic defects can trap and release charge carriers, which leads to number fluctuations in the current. White arrows indicate two possible tunnelling paths.

A widely accepted model explaining these trapping and de-trapping processes by tunnelling into and out of the traps was established by A. L. McWorther [20]. The corresponding theory is summarised very briefly in the following.

The g-r noise S_t generated by a single crystallographic defect trapping and releasing charge carriers can be expressed as

$$S_t = \frac{q^2}{W^2 L^2} 4\overline{\Delta N_t^2} \frac{\tau}{1 + (2\pi f \tau)^2} \tag{2.24}$$

with the elementary charge q, the channel width W, the channel length L, the variance in the number of trapped charges ΔN_t, the trapping time constant τ and the trapping frequency f. This PSD has a Lorentzian shape (Fig. 2.7).

The probability of a trap being occupied or not is given by the Fermi-Dirac distribution

$$F(E) = \frac{1}{1 + exp\left(\frac{E-E_F}{k_B T}\right)} \tag{2.25}$$

with the energy E and the Fermi energy E_F. The variance $(\Delta N_t)^2$ for the Fermi-Dirac distribution is given by

$$\overline{\Delta N_t^2} = F(E)(1 - F(E)). \tag{2.26}$$

In the next step to evaluate Eq. 2.24 a trap density $n_t(x, y, z, E)$ in the gate oxide is assumed to take into consideration contributions from more than one trap. With this it is possible to integrate over the whole channel to calculate its total noise PSD S_C:

$$S_C = 4\frac{q^2}{W^2 L^2} \int_{E_V}^{E_C} \int_0^W \int_0^L \int_0^{t_k} n_t \; F(E)(1 - F(E)) \frac{\tau}{1 + (2\pi f \tau)^2} dx dy dz dE, \tag{2.27}$$

where t_k is the high-k material thickness.

Due to the properties of the Fermi-Dirac distribution, $F(E)(1 - F(E))$ only constitutes a sharp peak around the quasi-Fermi level as $F(E)(1-F(E)) = -k_B T dF(E)/dE$. If additionally n_t is assumed to be constant in energy and in space (which will be discussed later on) the above integral simplifies to

$$S_C = 4\frac{q^2 k_B T}{WL} n_t \int_0^{t_k} \frac{\tau}{1 + (2\pi f \tau)^2} dz. \tag{2.28}$$

In Eq. 2.28 dz remains as spatial integrand as τ depends on z (cp. 2.29).

An essential part of the McWorther model is the assumption that charge carriers are trapped and released by tunneling. The time constant determining how long carriers remain trapped is given as

$$\tau = \tau_0(E) e^{z/\lambda}, \tag{2.29}$$

where z is the depth into the gate oxide measured from the interface to the channel, $\tau_0(E)$ is often taken as a constant $10^{-10} s$, and λ is the material dependent tunnelling attenuation length, which is given by the WKB theory:

$$\lambda = \left(\frac{4\pi}{h}\sqrt{2m^* \Phi_B}\right)^{-1}. \tag{2.30}$$

Here, m^* is the effective electron mass in the gate oxide and Φ_B is the barrier height towards the gate oxide. For the given material system consisting of an Al_2O_3 layer adjacent to an InAs channel (cp. Sec. 3) the values $m^* = 0.23\ m_0$ with the electron rest mass m_0 and $\Phi_B = 2.3$ eV can be taken from [21]. This results in $\lambda = 0.13$ nm.

With λ known, $\tau = 1/(2\pi f)$ and Eq. 2.29 the depth z of the traps contributing to noise at certain frequencies f can be calculated:

$$z = \lambda\ ln\left(\frac{1}{2\pi f \tau_0}\right). \tag{2.31}$$

For the frequency range of 10 Hz to 1 kHz measured later on this results in values for z between 1.9 nm and 2.5 nm. If the traps are closer to or further away from the interface than this, they respond too quickly or too slowly, respectively, to contribute to g-r noise in the given frequency range.

Inserting 2.29 and the values obtained for f, τ and λ into 2.28 the integral can be evaluated as [19]

$$S_C = \frac{q^2 kT\lambda n_t}{fWL}. \tag{2.32}$$

Earlier, the trap density n_t in the high-k material was assumed to be constant in energy and space. This is usually not the case [22] and will affect 2.32 by changing the $1/f$ behaviour to a $1/f^\gamma$ behaviour. It was discovered that γ is smaller than 1 if the trap density increases towards the channel interface and larger than 1 in the opposite case.

When using the findings derived above for evaluating measurements later on the relations

$$S_I = S_{V_{fb}} g_m^2 \qquad \text{and} \qquad S_{V_{fb}} = S_C / C_{ox}^2 \tag{2.33}$$

are helpful, where S_C is the g-r noise power that was derived above. In contrast to the gate oxide noise power S_C, S_I is the whole device's noise current power. When S_C is divided by the gate oxide capacitance C_{ox} squared, this yields the flat-band voltage noise power $S_{V_{fb}}$ which again yields the noise current power S_I if multiplied by the transconductance g_m squared:

$$S_I = \frac{q^2 k_B T\lambda n_t}{f^\gamma WLC_{ox}^2} g_m^2. \tag{2.34}$$

The possible deviation from a $1/f$ behaviour was taken into account in the last equation.

The quantity that will actually be measured in the experimental part later on is the noise current I_N. The noise current power S_I is this noise current squared. The

term *power* is used although it is not a real physical power. Conventionally, S_I is normalised with the source-drain current I_{DS} squared and S_I/I_{DS}^2 is plotted against I_{DS} to compare the measured noise to the transconductance behaviour $(g_m/I_{DS})^2$. If both follow a similar behaviour this is an indication for number fluctuations in the measured device.

Furthermore, measuring S_I and g_m allows to extract the trap density n_t from Eq. 2.34:

$$n_t = \frac{f^\gamma W L C_{ox}^2 S_I}{q^2 k_B T g_m^2}. \tag{2.35}$$

2.3.4 Random-Telegraph-Signal Noise

A special form of g-r noise is Random-Telegraph-Signal (RTS) noise. It can occur when in g-r processes only a few traps are involved. RTS noise can be observed in the time domain when the current switches between two or more discrete levels. If RTS noise is observed, this often hints to a bottleneck in a device as it is assumed that for RTS noise a single trap governs the flow of a large number of carriers rather than many carriers being involved in trapping and de-trapping.

The power spectral density for a current switching between two levels differing by ΔI was found to be

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)[(\frac{1}{\tau_l} + \frac{1}{\tau_h})^2 + (2\pi f)^2]}. \tag{2.36}$$

τ_l and τ_h are the Poisson distributed durations in the lower and the higher current state respectively.

Similar to g-r noise the RTS noise PSD has a Lorentzian shape in the frequency domain.

2.3.5 Mobility Fluctuations

At the beginning of this chapter the overall current fluctuations were separated into number fluctuations and mobility fluctuations. In contrast to the former a theory of which was treated in chapter 2.3.3 there is no widely accepted explanation for the latter. Only an empiric model by F. N. Hooge [23] which is given by

$$\frac{S_I}{I_{DS}^2} = \frac{\alpha_H}{fN} = \frac{q\alpha_H}{fWLQ_i}, \tag{2.37}$$

is often used to describe noise from mobility fluctuations. In Eq. 2.37 S_I is the noise current power, I_{DS} the source-drain current, α_H the numerical and material-dependent Hooge parameter, f the frequency, W and L channel width and length, respectively, N the total amount of charge carriers in the channel and Q_i the charge in the channel.

To obtain an equation valid for all regions of operation and again an expression that will allow to identify mobility fluctuations in the measured data later on a non-uniform charge distribution $Q_i(x)$ in the channel has to be assumed. With this and $I_{DS} = W\mu_{eff}Q_i dV/dx$, Eq. 2.37 can be expressed as

$$\frac{S_I}{I_{DS}^2} = \frac{q\alpha_H}{fWL}\frac{1}{L}\int_0^L \frac{dx}{Q_i(x)} = \frac{q\alpha_H}{fWL^2}\int_0^{V_{DS}} \frac{W\mu_{eff}}{I_{DS}}dV = \frac{q\alpha_H\mu_{eff}V_{DS}}{fL^2I_{DS}}, \tag{2.38}$$

where μ_{eff} is the effective carrier mobility in the channel and V_{DS} is the source-drain voltage. Above saturation V_{DS} has to be replaced by the saturation voltage $V_{DS,\ sat}$.

Similar to the expression for number fluctuations (Eq. 2.34) this last expression (Eq. 2.38) is often used to identify mobility fluctuations in measured data by plotting S_I/I_{DS}^2 versus the drain current I_{DS} and comparing it to a $1/I_{DS}$ graph.

2.3.6 1/f Noise

The main parts of chapter 2, 2.3.3 and 2.3.5, both served as a basis for this thesis' main topic: $1/f$ noise. This type of noise, also called flicker noise or pink noise, occurs in almost all electronic devices. A consequence of the $1/f$ PSD of this type of noise is that it is mostly visible at lower frequencies. In fact, $1/f$ noise occurs at all frequencies but the frequency dependence causes the PSD at higher frequencies to be overshadowed by white noise, its PSD being constant over all frequencies. The frequency where the $1/f$ PSD drops below the white noise PSD is called corner frequency.

In MOS devices it is assumed that 1/f noise originates in exactly the two contributions already mentioned in 2.3.1 and treated in more detail in 2.3.3 and 2.3.5: number fluctuations and mobility fluctuations. Both eqs. 2.34 and 2.38 as the main results of their respective section show the $1/f$ behaviour.

While this twofold composition of number and mobility fluctuations was shown in planar [24] as well as in nanowire MOSFETs [25] only a few noise inspections on TFETs have been carried out so far [17][18]. As mentioned before, from comparison of TFET structures to MOSFET structures, it can be assumed that the contribution of number fluctuations to $1/f$ noise will also appear in TFET measurements as there is still a channel area similar to that in a MOSFET adjacent to the tunnel junction. For mobility

fluctuations in nanowire TFETs an assumption like this is not so straight forward as there is an ungated part of the nanowire where the electric field is not well-controlled (cp. Sec. 3). This might lead to possible mobility fluctuations being balanced by an adapting electric field in this area.

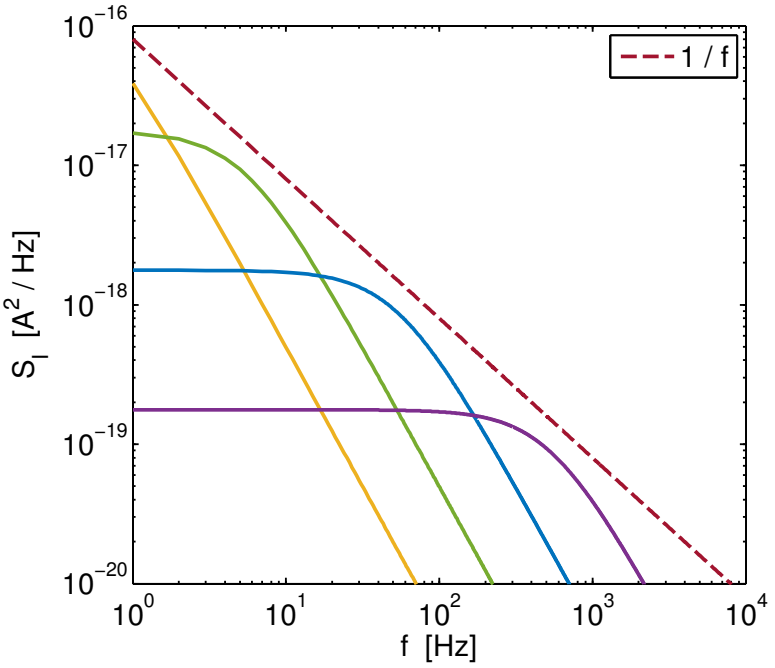

FIGURE 2.7: Lorentzian noise PSDs accordings to Eq. 2.24 with different time constants add up to $1/f$ behaviour.

2.3.7 Overview

As a brief overview the table below summarises the noise characteristics most important for the later measurement evaluations.

Noise	Characteristic Behaviour	Normalised PSD Behaviour at Fixed Frequency
White Noise	Constant in Frequency	$1/I_{DS}^2$
RTS Noise	Distinct Current Levels in Time Domain	–
G-R Noise	Adds up to 1/f Noise	$(g_m/I_{DS})^2$
Mobility Fluctuations	Adds up to 1/f Noise	$1/I_{DS}$

TABLE 2.1: Overview over different kinds of noise.

Chapter 3

TFET Fabrication

In this chapter the different steps necessary to fabricate a vertical nanowire TFET are briefly described. As this thesis does not focus on processing, the description will be mostly qualitative. The scanning electron microscope (SEM) images in this section show devices different from those actually used for noise measurements, as the latter had already been fabricated before. The fabrication process is the same, however. It was published in [26].

Nanowire Growth

A device can only be as good as the material it is made of. Therefore the growth of the nanowires making up the TFETs later on is essential. The nanowires consist of three parts: A highly n-doped ($n_D = 3 \times 10^{18}\ cm^{-3}$) InAs stem for the drain side, an intermediate intrinsic (un-doped) InAs part for the gated area and a highly p-doped ($n_A = 10^{19}\ cm^{-3}$) GaSb top part for the source side. For n-doping tetraethyltin (TESn) was used and for p-doping it was diethylzinc (DEZn). The tunnelling governing the transistor's characteristic behaviour is supposed to take place at the junction between GaSb and the intrinsic InAs part. This intrinsic part of the nanowire is required because a high doping throughout the whole nanowire would diminish gate control. Although the gated part of the nanowires is supposed to be intrinsic it was still doped to approximately $n_D = 10^{17}\ cm^{-3}$ [26] (in contrast to the intrinsic InAs carrier concentration of $n_i = 10^{15}\ cm^{-3}$) as some TESn remains inside the growth chamber after switching off the doping gas.

For the growing of InAs nanowires an InAs substrate was required. Instead of using a pure InAs substrate a Si wafer was overgrown with an InAs buffer layer by metal-organic vapour phase epitaxy (MOVPE). In this process metal-organic precursor gases are flooded over the Si substrate. They react in the gas phase as well as on the surface where they finally form a crystalline InAs layer.

Apart from the InAs buffer layer, Au seed particles are necessary to grow the nanowires. These were distributed over the InAs surface by an electron beam lithography (EBL) defined lift-off process.

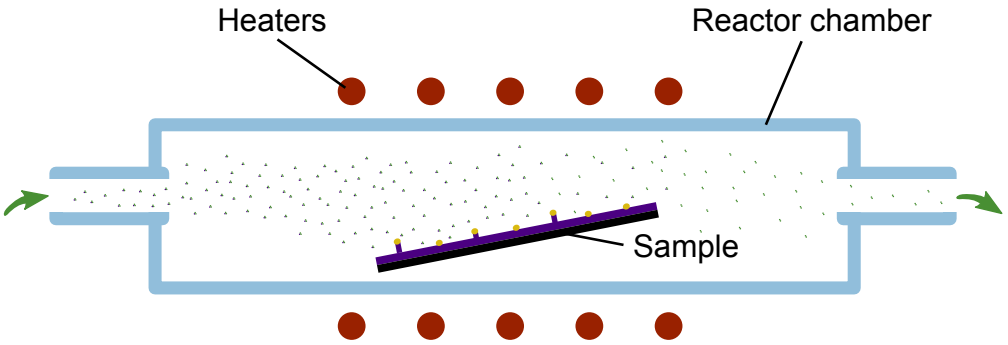

FIGURE 3.1: Schematic depiction of the growth reactor. Metal-organic precursor gases are run over the gold-particle-covered buffer layer. The nanowires grow under the Au particles pushing them upwards.

The actual nanowire growth was carried out by the same process as the buffer layer growth before, only adding another precursor gas (TESn) to add Sn as n-dopant. In and As from the precursor gases diffuse into the gold particles and crystallise below them as InAs once the gold particles are saturated. This pushes the gold particles upwards. After a certain time the doping precursor gas was switched off to obtain the un-doped InAs part in the nanowire. To obtain the p-doped (by the use of DEZn to implant Zn) GaSb part of the nanowires all gases were changed again after some time. A schematic depiction of the growth reactor is shown in Fig. 3.1. As can be seen in Fig. 3.2 the GaSb part of the nanowires has a larger diameter than the InAs part. Incorporating Sb into the Au particle increases the solubility of group III materials in gold. This changes the Au particle composition and with it the nanowire diameter [9].

Digital Etching to Remove Growth Residues

Observations have shown that during the growth of the GaSb part there is also an GaInSb shell formed around the InAs part of the nanowires. In the past this diminished the gate control over the transistors once they were completed. Since this problem was identified, the shell is removed by digital etching after the nanowire growth. Furthermore, digital etching can be used to decrease the diameter of the InAs section of the nanowires which enhances the electrostatic gate control [7].

In digital etching the sample surface is first oxidised in a plasma asher and afterwards the oxide layer is removed by an acid. This two-step process is repeated until the intended decrease in nanowire thickness is achieved.

Deposition of a High-k Material as Gate Oxide

A crucial part for every MOS transistor is the gate oxide. Its permittivity should be as

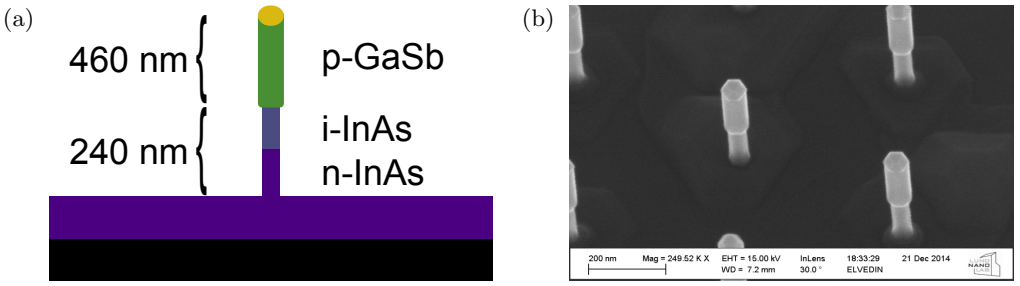

FIGURE 3.2: Nanowires grown from an InAs substrate. The GaSb top part has a larger diameter than the InAs part due to the Au particle increasing in diameter in the later growth step. At this process stage the unwanted GaInSb shell around the nanowires was already removed by digital etching. **(a)** Schematic illustration of the nanowires after growth and digital etching. **(b)** Nanowire SEM image after growth.

high as possible to achieve a gate control over the channel as far as possible. Because of their high permittivity κ the materials used are referred to as "high-k materials". Here, an Al_2O_3/HfO_2 bilayer was used. Both materials were deposited by atomic layer deposition (ALD). ALD works in a similar way as the buffer layer growth except that the precursor gases are flooded over the sample alternatingly so that the reaction only occurs at the sample and nanowire surface. This forms one closed atomic layer at a time. The thicknesses of the high-k materials were approximately 1 nm Al_2O_3 followed by 5 nm HfO_2, which corresponds to an effective oxide thickness (EOT) of ∼1.4 nm [26].

For the most recent samples an additional surface treatment right before the ALD step was introduced. This step is supposed to counteract the degradation of the surface which begins immediately after the growth of the nanowires just because they are subjected to the air in the laboratory. The success of the additional surface treatment became visible both in the TFETs' switching behaviour and in the noise measurements.

Etching of Mesa Structures to Avoid Current Diffusion

So far all the nanowires were connected through the highly n-doped InAs buffer layer. To isolate single transistors later on, mesa structures defined by UV lithography were

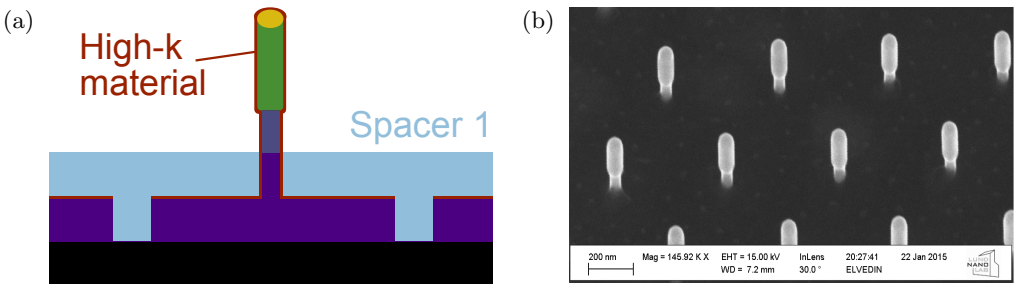

FIGURE 3.3: Both the high-k material and the spacer between drain and gate were applied. Mesa structures were etched in between these two steps. The resulting trenches were filled by the non-conductive spacer material. **(a)** Schematic illustration after applying the high-k material and the first spacer. **(b)** SEM image of nanowires sticking out of the spacer.

etched through both the high-k material and the InAs layer (Fig. 3.3). As the Si substrate is not doped it is by far less conductive than the doped InAs buffer layer, so the trenches reaching down to the Si substrate prevent the flowing of currents. DC and noise measurements can be carried out without these mesa structures but for radio frequency (RF) measurements they are indispensable.

Definition of Spacers Between Contacts

To isolate the transistors' drain contact from the gate contact a non-conductive spacer was applied on top of the drain (Fig 3.3). In contrast to the gate oxide, the material used for the spacer layer should have a permittivity as low as possible to keep parasitic capacitances as low as possible. In the current fabrication process an organic UV resist is used. It is one of the main challenges of processing to replace this material as it is not very robust. It absorbs humidity even after the processing of the transistors has been completed and it can trap charges during device operation. Both effects alter the device behaviour and thus constitute a reliability problem.

The spacer thickness was defined by simply covering the whole sample with the resist and then slowly etching back until the desired thickness was achieved. This processing step was carried out both before applying the gate metal and afterwards to isolate the drain from the gate and the gate from the source, respectively.

Deposition of the Gate Metal

After the application of the first spacer the gate metal was sputtered on. In sputtering, a target is bombarded with a sputtering gas inside a vacuum chamber. The sputtering gas physically releases atoms from the target so that these released atoms diffuse towards the sample, and cover its surface with an amorphous metal layer. Here, the whole sample surface as well as the part of the nanowires sticking out of the spacer were covered in tungsten. As it was only supposed to cover the part of the transistor that is to be gated, the tungsten had to be etched from the top of the nanowires. This was achieved in a

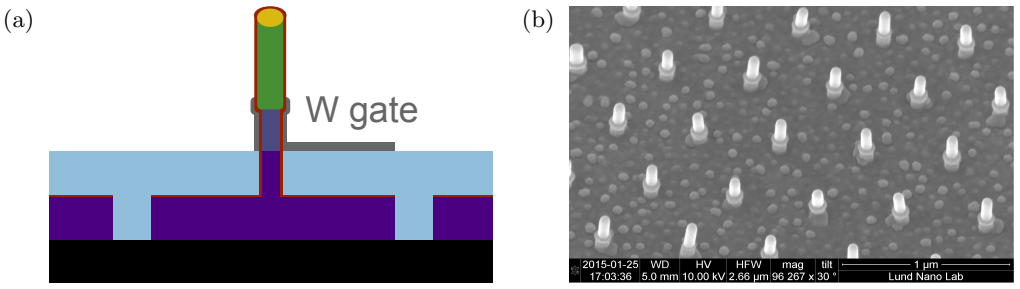

FIGURE 3.4: The gate metal W was applied on top of the first spacer. The gate length was defined by applying and then etching a resist. The gate pads were defined by UV lithography. **(a)** Schematic illustration after definition of the gate length and the pads. **(b)** SEM image after the definition of the gate length, but before the definiton of the gate pads.

similar way as the definition of the spacer thickness before. The metal-covered surface was covered by a resist which was etched back afterwards so that in the end it only covered the part of the nanowire where the tungsten was supposed to remain. The rest of the metal, now sticking out of the resist, was etched away.

Besides the gate length also the gate contact pads had to be defined, which was achieved by a UV lithography process (Fig. 3.4).

Etching Via Holes to Contact Gate and Drain

To be able to access all device contacts, via holes were etched through the spacer layers. The via holes were defined by UV lithography and etched in two similar steps (Fig. 3.5).

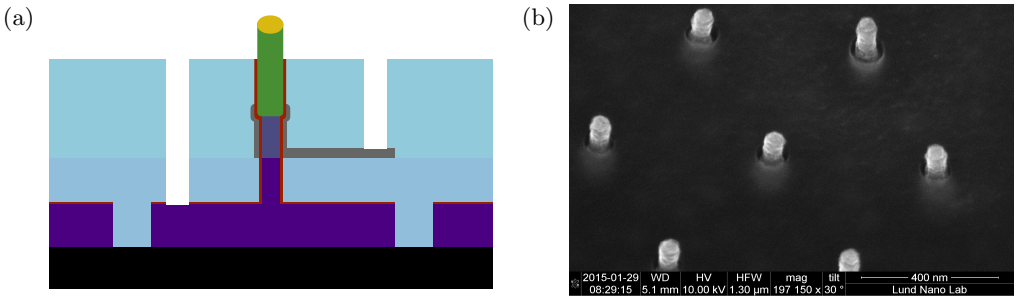

FIGURE 3.5: Via holes were etched through the spacer resists to be able to contact drain and gate. To be able to contact the source the high-k material covering the top part of the nanowires was also etched. **(a)** Schematic illustration after etching via holes to contact drain and gate and after etching the high-k material from the top of the nanowires. **(b)** SEM image after etching the high-k material from the top of the nanowires but before etching via holes.

Removal of the High-k Material From the Drain Area

After the previous steps, the top part of the nanowires and the bottom of the via holes were still covered by high-k material which had to be removed before the contacts could be applied. This was again achieved by etching (Fig. 3.5). Special care had to be taken during this step as the etchant currently used also attacks the GaSb underneath the high-k material, so the etching time was crucial.

Deposition of Contact Metals

In the second but last step all contacts were covered by metal. The contacts consist of three layers: Ni to achieve a good contact to InAs and GaSb followed by W as a diffusion barrier and finally Au to achieve a good contact in a later measurement setup. All metals were applied by sputtering. This process filled up the via holes and covered the whole sample surface.

Definition of Contact Pads

In the last step the contacts were separated by etching the metal in between the UV

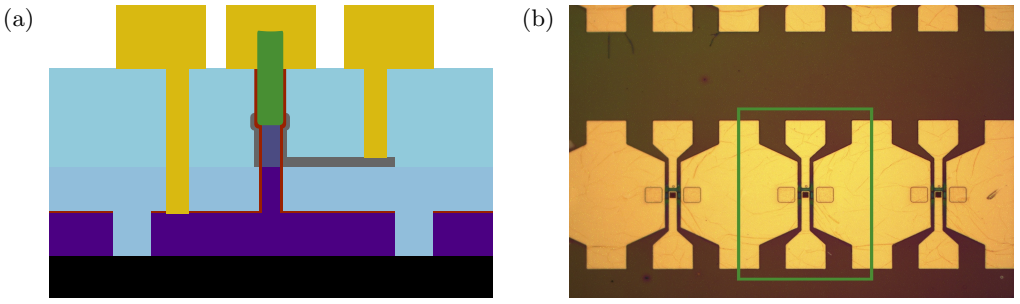

FIGURE 3.6: In the final processing step the contact metals were applied and the contact pads were defined by UV lithography. **(a)** Schematic illustration of a finished device. **(b)** Light microscope image of the contact pads after the completed processing. In this image the contact pads show some small cracks, which do not affect the measurement, however. The green rectangle indicates a single transistor. The finger reaching in from the top is the gate contact, the one reaching in from the bottom is the source contact and the large pads on both sides are the drain contacts. Close to where the contact fingers meet, the via holes and the nanowire arrays are visible as framed squares / circles and as a dark square, respectively.

lithography defined contact pads. The result can be seen in Fig. 3.6 where a green rectangle in Fig. 3.6(b) indicates a single transistor. On one sample there are approximately 200 TFETs; not all of them are working due to processing-related non-uniformities.

Sample Overview

Noise and DC measurements were carried out on three different samples. The main differences between the samples were their age which can deteriorate the behaviour of the devices and the additional surface treatment immediately before the ALD step only introduced for the third sample. Table 3.1 below summarises these differences. To make the effect of the additional surface treatment clear, typical subthreshold slopes for the different samples are added in the table. Another effect of the additional surface treatment besides the improved subthreshold slope will become obvious during the analysis of the noise measurements later on (Sec. 5.2).

Sample Number	Wires Grown on	Surface Treatment Before ALD	Subthreshold Slope [mv / decade]
1	26.01.2014	No	470 – 570
2	07.09.2014	No	470 – 570
3	27.01.2015	Yes	250

TABLE 3.1: Overview over measured samples.

Chapter 4

Experimental Setup

4.1 General Setup and Measurement Process

The aims of this thesis were measuring noise and DC properties of TFETs at different temperatures. As MOSFET noise behaviour is well investigated reference measurements on MOSFETs were carried out to verify if it is possible to use the setup for noise measurements.

Concerning the DC properties both the transfer and the output characteristics were measured. For the first one the source current was measured while the gate bias was swept at a constant drain-to-source voltage and for the second one the source current was measured while the drain-to-source voltage was swept for several fixed gate biases. For the DC measurements only the parameter analyser shown in Fig. 4.1 was required as it can act both as a voltage source as well as as a volt- and amperemeter (Fig. 4.2). The measurement data were recorded with a LabView programme controlling the parameter analyser using a General Purpose Interface Bus (GPIB).

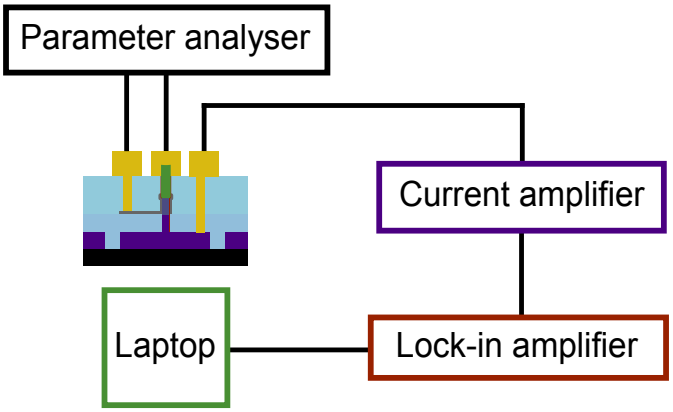

FIGURE 4.1: Schematic depiction of the measurement setup.

When examining the TFETs' noise behaviour two kinds of measurements were carried out as well. In one of them the noise current was measured while logarithmically sweeping the lock-in amplifier frequency from 10 Hz to 1 kHz. At each frequency set in this way the device's source current was measured 55 times (set by the measurement programme). The average of these 55 measurements constitutes the data point for the given frequency. This measurement process was repeated for different gate biases. In the second measurement the noise current was measured at a fixed lock-in frequency of 10 Hz to possibly identify noise behaviour following $(g_m/I_{DS})^2$ or $1/I_{DS}$ as explained in secs. 2.3.3 and 2.3.5, respectively. For these measurements at 10 Hz the 55-fold current measurement explained above was repeated ten times at each gate bias so that the average of these ten measurements constituted one data point. Both kinds of measurements were carried out for several different gate biases from considerably below to considerably above the transistors' threshold voltage. In both measurements the complete signal from the device under test (DUT) was amplified by a low-noise current amplifier. To only measure the noise current the DC part of the measured signal was removed by the lock-in amplifier, which selects a very narrow frequency range in any signal. The remaining AC signal was the noise from the device. From the lock-in amplifier the signal was forwarded to a laptop via a GPIB interface where it was recorded by a LabView programme.

For a complete measurement (at room temperature) first a transistor's transfer characteristics were measured to see if the device was working. Then the noise measurement was carried out as described above. Afterwards the transfer characteristics were measured again to capture the change in the device behaviour when stressing the transistor during the noise measurement. After this the output characteristics were measured.

In the following all measurement instruments used are briefly described including their expected intrinsic noise level to show that it is possible to conduct noise measurements with this setup. To be able to plan the measurement setup the TFETs' noise current was roughly estimated to be in the order of 1 % of the device current. This estimation takes MOSFETs' noise currents as a basis and results in approximately 1 nA for the TFETs.

4.2 Probe Station

To bias the transistors they were contacted in a probe station. A Cascade 11000B or a Cascade Microtech / New Wave Research Alessi REL-4800 Micro Probe Station was used. Both are equipped with micro-manipulators to accurately place the contact needles on the transistor pads.

Both probe stations exhibited contact and wire resistances of a few Ohm which amounts to a white noise contribution far below the expected intrinsic transistor noise level.

4.3 Parameter Analyser

The parameter analyser schematically shown in Fig. 4.1 acted as both the contacts' voltage sources and as their current monitors in DC measurements. During noise measurements the source current was not measured by the parameter analyser but by the low-noise current amplifier.

The two parameter analysers used during this thesis were a Keithley 4200 SCS and an HP4195. Both instruments provide source / monitor units (SMUs) which can be used as depicted in Fig. 4.2.

The DC accuracy for the Keithley 4200 SCS amounts to ±0.02%rdg + 300 μV for the voltage source, ±0.06%rdg + 300 fA for the amperemeter for the current range in the transistor's off-state and ±0.04%rdg + 150 nA for the current range in the transistor's on-state [28].

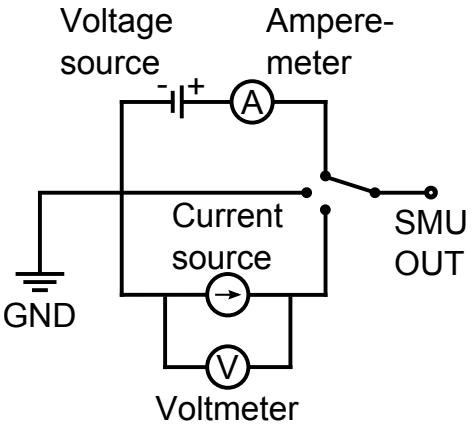

FIGURE 4.2: Simplified circuit diagram showing the different operating possibilities for the parameter analyser [27].

For the HP4195 the DC voltage accuracy V_{Nex} amounts to ±0.12% + 5 mV [29]. The current measurement accuracy was not to be found in the instrument manual so it was estimated to be ±5 in the last digit displayed. As the transistors' gate contacts are biased by the parameter analyser as DC source its voltage inaccuracy introduces an extrinsic source-drain current noise $I_{N_{ex}}$ proportional to the transistors' transconductances g_m:

$$I_{N_{ex}} = g_m V_{N_{ex}}. \tag{4.1}$$

Calculating this extrinsic noise with the given DC source inaccuracy results in an extrinsic current noise larger than the expected intrinsic transistor noise which would render the HP4195 unusable for noise measurements. However, examining the DC source with an oscilloscope showed that the DC source noise signal has a value of 1.2 mV peak-to-peak instead of the maximum inaccuracy given in the instrument manual. Further measuring only the DC source's voltage noise with the lock-in amplifier, calculating the

resulting extrinsic noise current $I_{N_{ex}}$ according to Eq. 4.1 and comparing it to the transistors' measured intrinsic noise showed that the extrinsic noise level is approximately two orders of magnitude smaller than the intrinsic noise level (Fig. 4.3). Thus, the HP4195 can be used as voltage source for noise measurements.

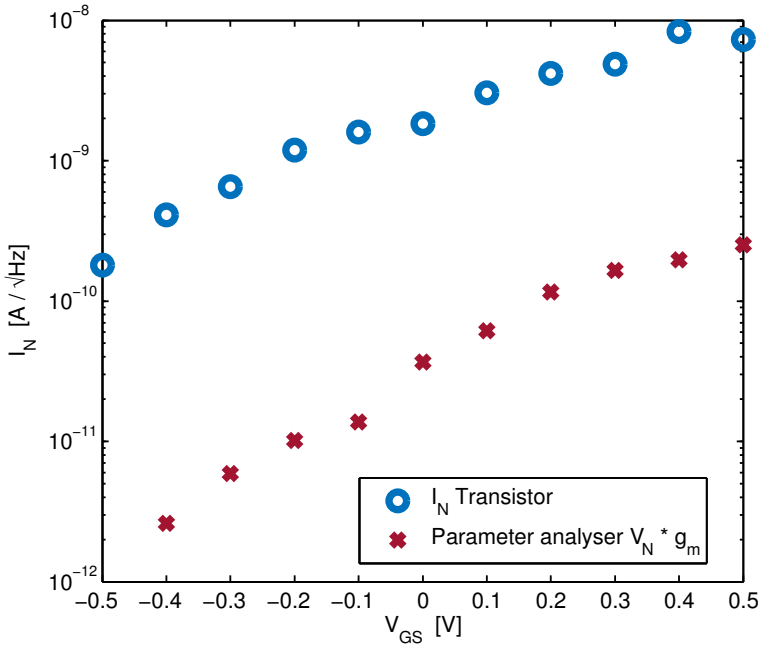

FIGURE 4.3: Comparison between intrinsic transistor noise (blue) and extrinsic noise (red) introduced by the voltage source inaccuracy affecting the transistor's gate contact for a TFET.

4.4 Low-Noise Current Amplifier

As the currents measured could be very small (∼10 pA – ∼1 μA) a current amplifier was used to facilitate measuring the even smaller noise signal. In this setup an SR570 low-noise current amplifier was used. It can be operated on a battery instead of line voltage which is advantageous for any kind of frequency-dependent measurements as it suppresses voltage spikes at the line voltage frequency and its multiples. Furthermore the amplifier worked as a transimpedance amplifier converting the input current into an output voltage which was then forwarded to the lock-in amplifier.

The amplifier's internal noise depends on the sensitivity setting. For the lowest sensitivity (meaning the lowest amplification) that was used (10^{-6} V/A) the noise level is given as 600 fA for a frequency-independent contribution but can reach up to 800 fA if the intrinsic 1/f-noise is considered [30]. The upper (meaning the highest amplification) limit for the amplifier's sensitivity was not the highest instrument setting but the available bandwidth as it decreases with increasing amplifier sensitivity. In the case of the

measurements being carried out at a fixed frequency of 10 Hz sometimes also the signal's DC component set a lower limit to the sensitivity as the amplified DC signal could overload the current amplifier's output. Even the highest instrument noise of 800 fA does not reach into the expected intrinsic noise range of the measured devices.

4.5 Lock-In Amplifier

In a lock-in amplifier a very narrow band-pass filter is applied to the incoming signal, only measuring the passed AC amplitude. In this way the measured signal's DC component was removed so that only the noise current was measured.

The lock-in amplifier used was an SR830 whose internal noise is given as 6 nV / $\sqrt{Hz}$ [31]. Compared to the measured noise voltage amplitude of usually at least 10 mV after amplification the lock-in amplifier's internal noise is negligible.

4.6 Cooling System

For the low-temperature DC measurements the TFET samples were contacted in a dedicated cryo probe station. The voltages and currents were controlled and measured by the HP4195 parameter analyser described above. The cryo probe station used was a LakeShore CRX-6.5K model with a standard temperature range between $<$ 10 K and 350 K and a vacuum pressure of 10^{-6} Torr at base temperature. Liquid Helium is used to cool down the system and the probe station is equipped with a sample holder and a radiation shield around the sample holder.

The only noise sources from the cryo probe station were the wire and tip resistances which added up to a few Ohm.

4.7 Setup Issues

Changing the probe station and the parameter analyser in the course of the measurements involved changing the laboratory. This constituted a major setup challenge for the continuation of the measurements. First, almost all devices on one sample broke in one single incident and later on almost all DUTs individually broke randomly and without apparent reason, usually showing a gate-oxide-breakthrough. For the first issue, where almost a whole sample was destroyed at once it became obvious that switching the probe station's microscope light causes a voltage spike in the sample large enough to

destroy its devices. This was solved by interrupting the light path instead of switching the light. For the later incidents, where almost during every measurement the DUT was destroyed after some time the problem at least partly originated in the laboratory's grounding: The breaking of devices seemed to be correlated to other laboratory users switching instruments or the light in the laboratory. However, not every switching event in the laboratory causes a voltage spike in the measurement setup as could be observed by examining the lines connecting the voltage source and the probe station with an oscilloscope. A solution which at least reduced the problem was to decouple all instruments involved in the measurements from the laboratory earth with the help of a transformer and to connect their grounds to another earth than that used for the rest of the laboratory. This improved the situation but did not eliminate it completely.

As this measure did not completely solve the problem and devices continued to break during measurements – though less often – the connexions between the parameter analyser and the probe station were examined more closely to possibly identify voltage spikes originating from either one of the measurement instruments or from the changed grounding. Spikes large enough to destroy the measured transistors could not be detected despite monitoring the signal for several hours and randomly switching the light and other instruments in the laboratory. However, not being able to identify any spikes during this observation could have been bad luck as it is possible that just during this time none of the events which could have destroyed a transistor occurred. This issue definitely has to be solved before continuing noise measurements with this setup.

4.8 Setup Overview

The table below summarises which instruments and which samples were used for which kind of measurement.

Measurement	Instruments Used	Samples Used (cp. Table 3.1)
DC at room temperature	Probe Station, Parameter Analyser, Low-Noise Current Amplifier	1, 2, 3
Noise	Probe Station, Parameter Analyser, Low-Noise Current Amplifier, Lock-In Amplifier	1, 2, 3
Temperature-dependent DC	Cryo Probe Station, Parameter Analyser	1

Table 4.1: Measurement Setup Summary.

Chapter 5

Results and Analysis

5.1 Reference Measurements on MOSFETs

In publication [25] low-frequency noise in nanowire MOSFETs was studied in detail. There, both number and mobility fluctuations were identified as described in 2.3.3 and 2.3.5, respectively. Mobility fluctuations occur below the threshold voltage as the gate electric field confines the conducting electrons to the nanowire core. Above the threshold voltage the gate electric field pulls the electrons close to the nanowire surface instead so that g-r noise becomes dominant due to the high-k material interface and border defects. With the help of the reference measurements it was intended to find out if the results found in [25] can be reproduced with the given setup. If so, this proves that the measurement setup can be used for noise measurements. For the reference measurements MOSFETs fabricated according to the same processing scheme as the MOSFETs examined in [25] were used.

The results of the reference measurements showed a behaviour similar to that reported in [25] as can be seen in Fig. 5.1. On first sight, the normalised noise values $(I_N/I_{DS})^2$ are much higher for the reference measurements carried out here than they are in [25]. The noise currents without normalisation, however, show the same order of magnitude for both measurement series. The difference in the normalised values is caused by the fact that the MOSFETs used here exhibit lower currents than in [25], mostly due to a smaller diameter (ca. 34 nm as compared to ca. 45 nm). Here, however, this difference in the normalised values is of minor interest as it results from the processing of the devices which is not subject of this thesis. More importantly both measurements showed the same noise behaviour. The g_m used for the $(g_m/I_{DS})^2$ curves was calculated from DC measurements carried out together with the noise measurements.

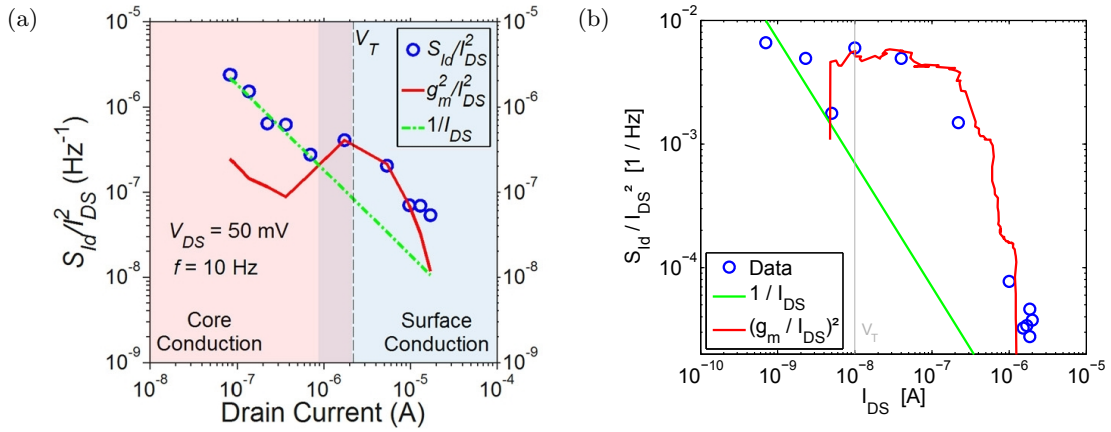

FIGURE 5.1: Comparison between MOSFET noise data measured with a spectrum analyser at KTH and published in [25] and measurements carried out with the setup described in chapter 4. The vertical lines in the graphs labelled with V_T indicate the threshold voltages determined from DC measurements. **(a)** Reference from [25]. Reprinted with the permission of the authors. **(b)** Measurements carried out to verify the setup. The measurement errors of 20 – 50% in **(b)** were left out to increase the comparability with **(a)** where the measurement errors were not given.

Decreasing nanowire diameters also lead to g-r noise becoming the dominating noise process in a device's off-state. This can be seen in Fig. 5.2(a) where the normalised noise current follows $(g_m/I_{DS})^2$ also below the threshold voltage.

In addition to the characteristic noise behaviour at a fixed frequency (Fig. 5.1) the MOSFET frequency dependence was measured. The results showed a $1/f^\gamma$ frequency dependence (Fig. 5.2(b)) as described in 2.3.6 with γ between 1 and 1.3. $\gamma > 1$ indicates that the trap density in the gate oxide decreases towards the interface to the channel. In [25] a $1/f$ dependence ($\gamma = 1$) was observed. The small difference can be attributed to processing variations.

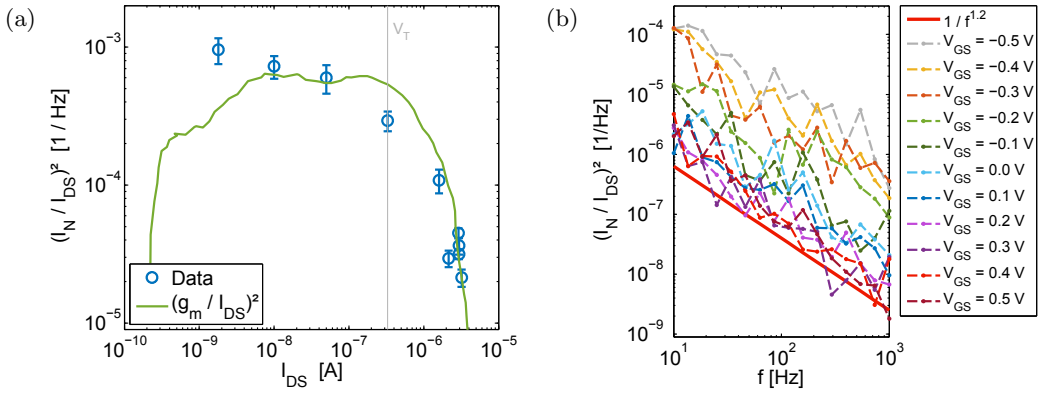

FIGURE 5.2: Results from the reference measurements carried out to verify the setup. **(a)** For low nanowire diameters the data points following $(g_m/I_{DS})^2$ indicate that g-r noise at the nanowire / high-k material interface becomes dominant also below V_T. **(b)** Noise adding up to a $1/f^{1.2}$ behaviour. The red line is a guide to the eye.

5.2 TFET DC Characteristics

The first measurements performed on any transistor were DC measurements to find out if the transistor was working. In the following a brief overview over TFET DC characteristics will be given pointing out the differences from MOSFETs.

TFETs on three different samples have been measured. The main difference between the samples was an additional surface treatment immediately before the application of the gate oxide only introduced for the third sample (Table 3.1). All measurement processes are described in section 4.1.

As the characteristic working principle TFET transfer curves look very similar to those of MOSFETs. Below the threshold voltage there is only a minimum off-current. In a MOSFET this corresponds to the energy bands of the channel constituting an energy barrier which the vast majority of the electrons in the source cannot overcome. In a TFET the bands align in a way that the channel conduction band lies above the source valence band so that there is no energy window the electrons can tunnel through. The resulting current for TFETs can be seen in Fig. 5.3.

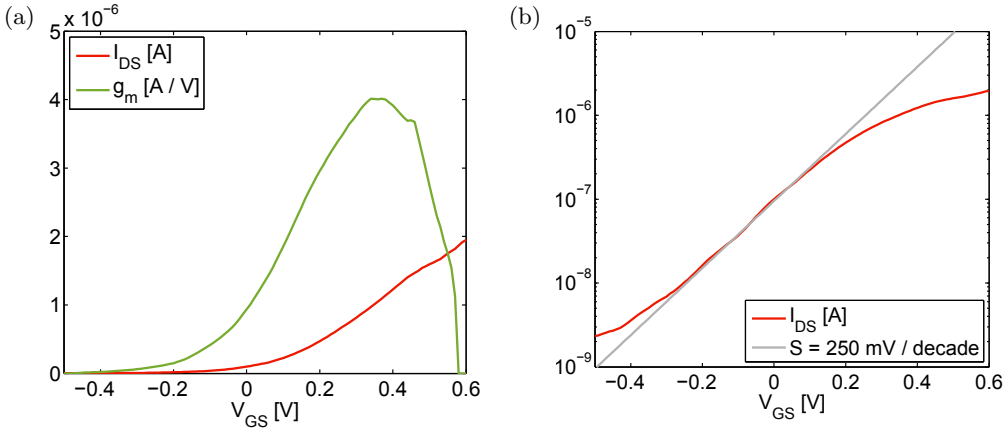

FIGURE 5.3: Transfer characteristics of a TFET consisting of four nanowires measured at a source voltage of 0 V and a drain voltage of 0.05 V. The subthreshold slope of 250 mV / decade is still far away from the aim of $<$ 60 mV / decade. **(a)** TFET transfer characteristics in linear representation. Linear plots like this allow to roughly determine the threshold voltage V_T. **(b)** TFET transfer characteristics in logarithmic representation. The grey line indicating the subthreshold slope is not a fit but an estimation.

From Fig. 5.3 it becomes obvious that the TFETs measured during this thesis are still under development. The subthreshold slope is quite far away from below 60 mV / decade and the current levels are rather low. TFETs with channels consisting of eight nanowires reached current and transconductance levels that were reached by MOSFETs with only a single nanowire as channel.

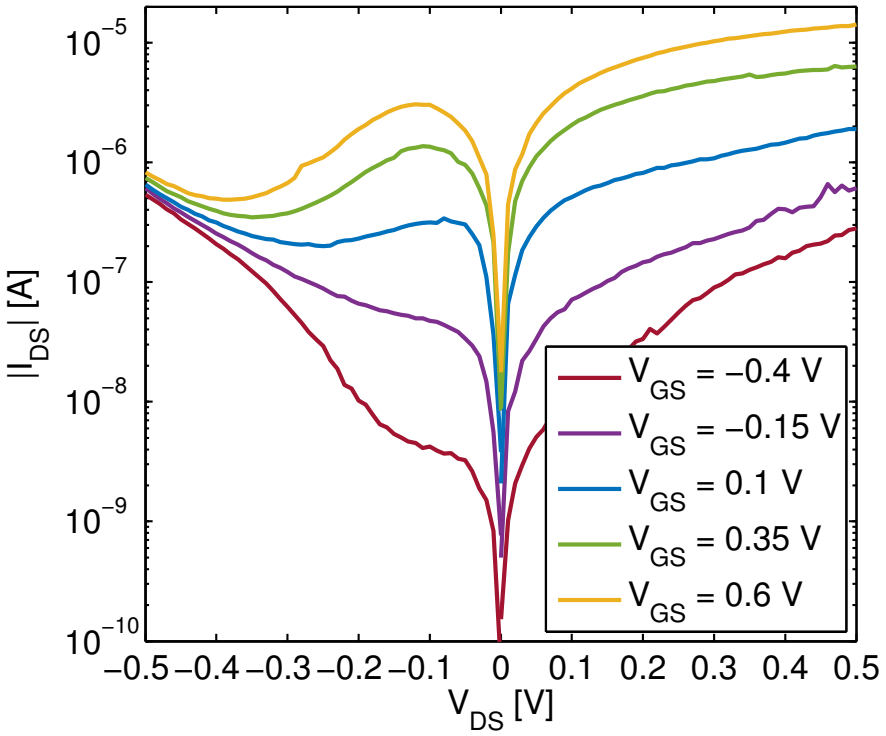

FIGURE 5.4: Output characteristics for a TFET. For a positive V_{DS} the source potential was kept constant at 0 V and the drain bias was varied. For a negative V_{DS} the bias direction was switched: The drain potential was kept constant and a positive bias was applied to the source.

While the transfer characteristics for TFETs and MOSFETs mostly differ in the magnitude of the current, TFET output characteristics show a unique feature only observable if a device shows BTB tunnelling. In the forward bias direction ($V_{DS} > 0$), TFETs show the same behaviour as MOSFETs. However, while MOSFETs show symmetrical behaviour in the forward and the reverse bias direction ($V_{DS} < 0$) for TFETs in the reverse bias direction negative differential resistance (NDR) is observed as known from Esaki diodes [32]: The voltage increases but the current decreases. This follows from the TFET band structure as shown in Fig. 5.5. To bias a TFET in reverse direction the drain voltage was kept at 0 V and a positive source voltage was applied. When the source bias in the transistor's on-state is varied this affects the tunnelling junction. By applying a positive bias to the source side, at some point the source energy bands are lowered far enough to close the tunnelling junction opened by the gate bias before. At this point the channel conduction band aligns with the source valence band, tunnelling is not possible anymore and the current decreases. Increasing the source bias further lowers the source energy bands far enough so that electrons from the channel can thermionically enter the source and the current increases again. The same effect can be reached by keeping the source voltage constant and biasing the drain with a negative voltage until the drain conduction band is raised over the source valence band.

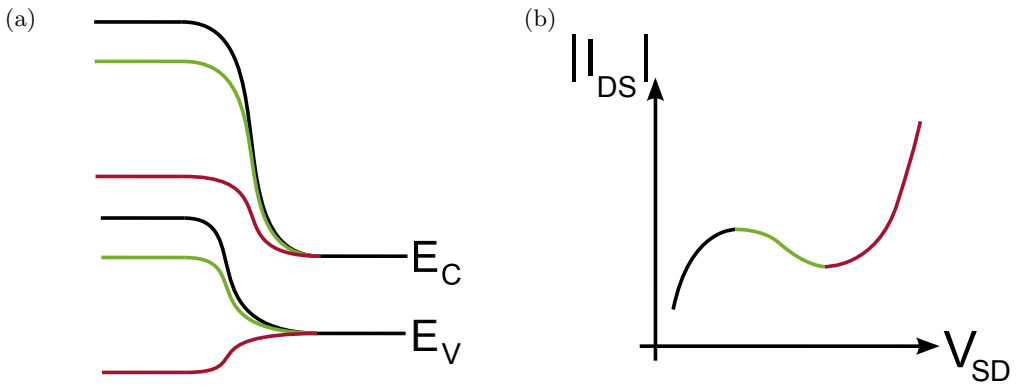

FIGURE 5.5: Schematic explanation for TFETs' NDR behaviour. First the bands on the source side align in a way that closes the tunnelling junction opened by the gate. Later the electrons can enter the source thermionically over the conduction band energy barrier. **(a)** Schematic illustration of the source energy bands closing the tunnelling junction under positive source bias. A positive source bias pushes the energy bands down. **(b)** TFET current resulting from the change in the band structure as shown in **(a)**. The changed index at the x-axis indicates that the source is biased instead of the drain.

For quite some time during the development of nanowire TFETs, NDR behaviour could only be observed for devices consisting of a few nanowires due to the difficulty to apply a fabrication process uniformly affecting all nanowires. Recently, NDR in nanowire TFETs consisting of a few hundred nanowires could be observed. The TFETs were fabricated by the research group where this thesis was carried out.

5.3 TFET Noise Measurements

With the measurement setup verified and an overview over TFET DC characteristics, in the following the main results of this thesis will be analysed. The data from the frequency sweeps are plotted as the normalised noise power versus the frequency to check for the devices' low-frequency dependency. The 10 Hz measurement results are plotted as explained in sections 2.3.3 and 2.3.5, looking for accordance between the data points and $(g_m/I_{DS})^2$ or $1/I_{DS}$, respectively. In all the 10 Hz measurement plots the threshold voltage V_T is indicated by a vertical grey line. Both V_T and the g_m used to show the $(g_m/I_{DS})^2$ curves are taken from the DC measurements carried out together with the noise measurements.

5.3.1 Frequency Sweeps

At room temperature all of the measured devices showed low-frequency characteristics following dependencies between $1/f$ and $1/f^{1.3}$ as explained for MOSFETs in section 2.3.6 (Fig. 5.6). $1/f^{\gamma}$ dependencies with $\gamma > 1$ indicate that the trap density in the gate oxide decreases towards the interface to the channel. Comparing the noise levels of the frequency-dependent measurements with those from InAs MOSFET measurements [25] both are in a similar order of magnitude. The TFET normalised noise power, however, on average reaches one order of magnitude lower as well as one order of magnitude higher values. This is probably mostly due to the TFETs' larger range in drain current. TFETs usually covered drain currents between 1 nA and a few μA, whereas the MOSFETs from [25] covered drain currents between 100 nA and 20 μA. Comparing the InAs/GaSb TFETs with Si TFETs [17] the Si TFETs' noise level is generally two orders of magnitude lower. This originates most likely in the interface between the channel and the gate oxide. For Si TFETs the natural SiO_2 separating the semiconductor channel from the gate stack forms a very clean interface whereas the

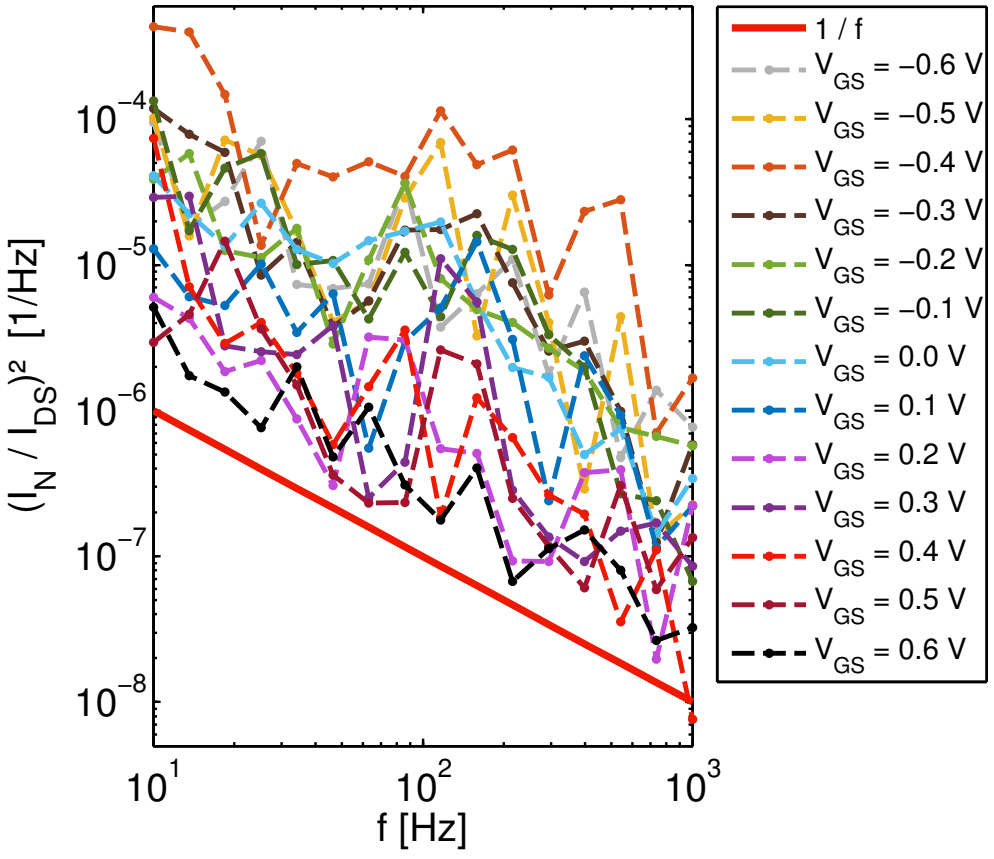

FIGURE 5.6: Frequency-dependent TFET measurement at room temperature. Dependencies between $1/f$ and $1/f^{1.3}$ were measured for different devices. The red line is a guide to the eye.

interface between the InAs/GaSb channel and the gate stack possesses a considerably worse quality.

The observed $1/f^{\gamma}$ frequency-dependence of TFETs indicates that, in spite of their different channel injection physics, TFETs in the current state of development do not exhibit low-frequency noise which is different from conventional electronic devices. This shows that either the tunnelling junction governing the TFET current does not introduce a noise mechanism dominating the ones assumed to contribute to the characteristic $1/f$ behaviour in non-tunnelling devices, or it shows that the junction exhibits the same noise behaviour as the mentioned contributions. For further analyses the measurements carried out at a fixed frequency of 10 Hz will be analysed.

5.3.2 Frequency Sweep Error Considerations

The fluctuations in the frequency sweeps in Fig. 5.6 are believed to be both inherent in a noise signal as a fluctuating measure and to the properties of nanowires. These fluctuations were also observed when MOSFETs were measured with the lock-in amplifier setup earlier [33] so the effect is neither inherent to TFET noise measurements nor an error in the measurement setup. The conductivity of nanowires is known to vary with time (Fig. 5.10) which, as the noise current is related to the DC current, also causes fluctuations in the noise current. Although the noise current is normalised by the DC current this does not smooth the fluctuations in the noise current induced by the DC current as only the averages of both currents are used for the normalisation instead of normalising every single measured noise current point by its respective DC current point. If the assumptions from above are correct, averaging over more measurement points at each frequency or applying a faster measurement technique (e. g. by using a spectrum analyser) should smooth the frequency curves. For the measurements carried out until now, the measurement programme did not allow changing the number of sample points or extracting the statistical error of the averaged data points. For future measurements this should be changed so that the number of sample points can be varied. To avoid masking the uncertainty of the measurements the data points in Fig. 5.6 were not smoothed and plotted with error bars but plotted as raw data instead. Still, the low-frequency behaviour is distinct.

5.3.3 10 Hz Measurements

The results of the 10 Hz measurements on the first two samples scattered a lot and were thus difficult to interpret. Tendencies similar to the MOSFET noise behaviour described in chapter 2.3 were recognisable but the results were not sufficiently distinct to make a

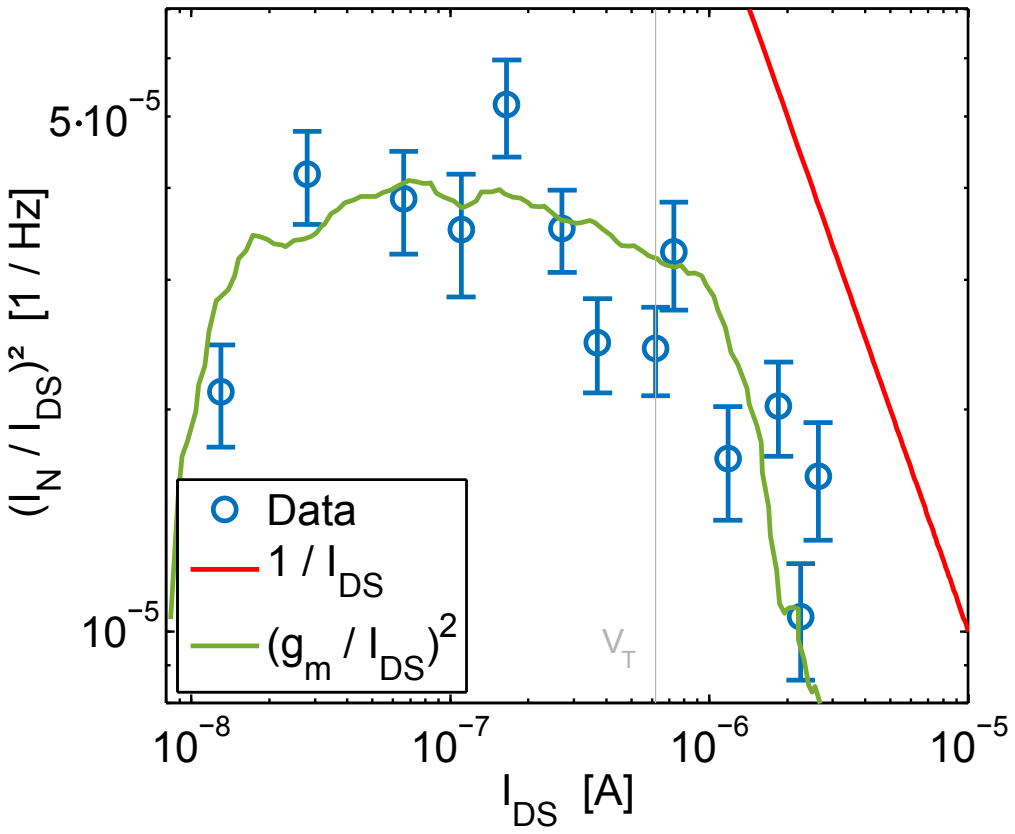

FIGURE 5.7: Measurement results from the third sample. Accordance is clearly visible between the normalised noise power and $(g_m/I_{DS})^2$ which indicates number fluctuations as dominant noise mechanism. There could be an accordance between the data points and $1/I_{DS}$ around the threshold voltage but it is not safe to say so. The $1/I_{DS}$ graph is included as a reference. The behaviour shown in this figure could be seen on all the devices measured on the third sample.

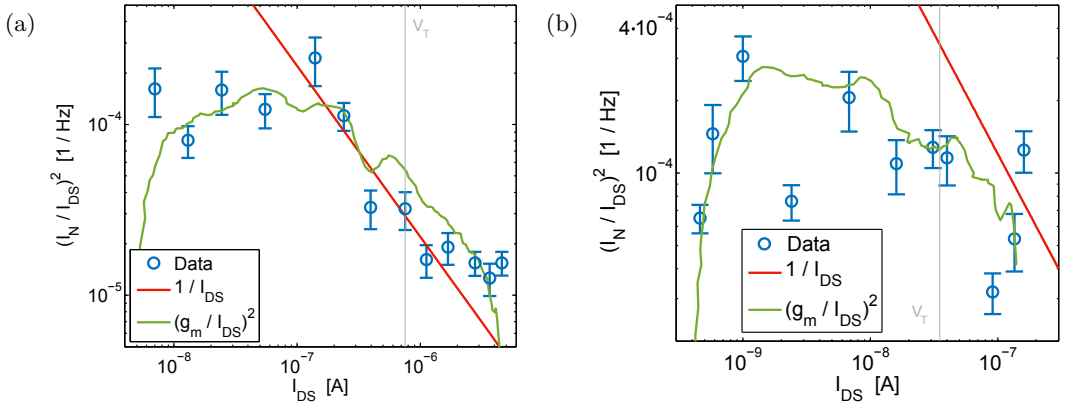

FIGURE 5.8: Two more results form the third sample to give an impression of the device to device variation. Both figures **(a)** and **(b)** show clear accordance between the measured data and $(g_m/I_{DS})^2$, indicating number fluctuations as the dominant noise mechanism. The $1/I_{DS}$ curves are included for reference. The deviating measurement point in **(b)** was a measurement error.

clear statement. For the processing of the third sample, however, treating the nanowire surface before applying the high-k material was introduced as a new processing step. This improved the noise measurement results dramatically as now the results consistently showed a distinct noise behaviour (Figs. 5.7, 5.8).

Before introducing the additional surface treatment the devices' noise behaviour did not show any systematic, neither agreeing with the noise behaviour known from MOSFETs nor indicating a different dependency. This implies that without this surface treatment the channel-oxide interface almost always exhibited defects to a degree that strongly randomised the devices' electrical noise behaviour either by forming additional interface traps or by statically affecting the gate electric field. The latter assumption is also supported by the generally higher DC currents and better gating measured for the devices on the third sample. Introducing the additional surface treatment decreased the subthreshold slope values by 50 % (cp. Table 3.1).

Without the contaminations on the nanowire surfaces the low-frequency noise of the third sample's devices clearly follows $(g_m/I_{DS})^2$ as can be seen in Figs. 5.7 and 5.8. For several devices on the third sample the data points around the threshold voltage V_T also seem to follow $1/I_{DS}$. However, it is not completely safe to assume this behaviour from only a few data points and it has to be analysed further. Showing a $(g_m/I_{DS})^2$ noise behaviour in the devices' on-state is well-known from nanowire MOSFETs and hints to g-r noise being the dominant noise mechanism and thus the gate oxide's interface traps being the dominant noise source instead of the tunnelling junction. In the off-state, however, MOSFETs rather show a $1/I_{DS}$ behaviour. The TFETs showing a $(g_m/I_{DS})^2$ behaviour in the off-state as well can be explained with the help of Fig. 5.9 which shows a more realistic approach to the TFET band structure than the simplified structure used in the theory part [9]. Although the tunnelling junction is effectively closed in the off-state as the channel potential blocks the path from the source to the drain, electrons can still tunnel into the channel area due to the broken band gap which results from the GaSb/InAs material combination [9]. From the potential well into which the electrons can tunnel they can be thermionically excited and then overcome the channel potential barrier. Once the electrons really enter the channel and are transported towards the drain they are subject to g-r processes dominant in nanowires with small diameters, which explains the observed noise behaviour

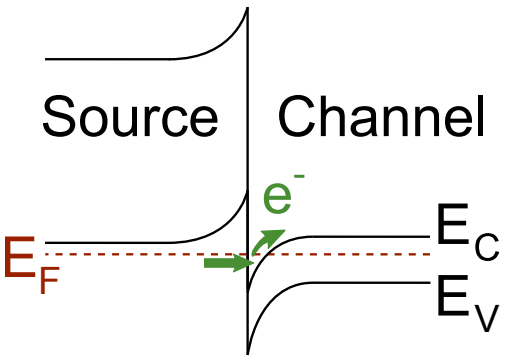

FIGURE 5.9: More realistic approach to the TFET band structure [9]. In the off-state electrons can still tunnel into the channel area but have to be thermionically excited to be able to establish a current.

following $(g_m/I_{DS})^2$. This mechanism for the off-current as explained by Fig. 5.9 will be supported by the temperature-dependent DC measurements later on.

There are also other effects known to contribute to the off-current such as direct or defect-assisted source-to-drain tunnelling, tunnelling through the gate-oxide or Shockley-Read-Hall (SRH) generation. Source-to-drain tunnelling was shown to play a role for channel lengths below 20 nm [5]. For the given devices the channel length is much larger so this contribution should play a minor role. The tunnelling attenuation length for the given gate stack is only 0.15 nm so tunnelling through the gate oxide should only play a minor role, too. SRH generation could give a contribution to the off-current but for the given device structure the effect explained above is believed to dominate as it is supported by the low-temperature DC measurements later on.

Comparing the TFET normalised noise level for the 10 Hz measurements with that of InAs MOSFETs [25] the TFET noise level is several orders of magnitude higher. As both the TFET and the MOSFET low-frequency noise seems to originate in g-r processes this difference in the normalised noise level probably results from the higher drain currents in MOSFETs. In fact, comparing the noise levels without normalisation, the TFETs exhibit lower noise than the MOSFETs. Just as for the frequency sweeps a comparison with Si TFET noise measurements [17] reveals lower noise levels for the Si TFETs. The assumed origin (gate-channel interface) of this was explained above. However, while showing higher noise than Si TFETs, III-V also show higher on-currents, which results from the band structure as discussed earlier.

So far the interpretation of the measurement results has not taken into account the tunnelling junction itself possibly featuring a noise behaviour following $(g_m/I_{DS})^2$. Two reasons make this possibility seem unlikely. The first one is the known difficulty to achieve a high-quality high-k film forming the gate oxide. Apart from the different nanowire material structure the TFETs' processing follows the same scheme as the nanowire MOSFETs' processing. Both TFETs and MOSFETs suffer from the same known processing difficulties and both show similar noise behaviour. This suggests that the noise in both stems from the same source as well. Concerning the second reason, the tunnelling junction constitutes a barrier for electrons to pass through, so, if a noise contribution is assumed to be truly originating in the altered device physics (i. e. tunnelling) shot noise should be expected first, as explained in section 2.3.2. Shot noise, however, is constant in frequency which the observed noise behaviour is not. The assumption that the dominant noise sources at room temperature are the gate oxide's interface traps is thus justified. Depending on the distribution of these traps around the Fermi level a noise contribution from the tunnelling junction itself can possibly be observed at low temperatures where the g-r noise contribution should be reduced.

5.3.4 10 Hz Measurement Error Considerations

The accordance between the noise data and the $(g_m/I_{DS})^2$ curve is very good (Fig. 5.7). The error bars shown in the results above are the standard error of the mean value. For a comparison of the measurement results with the models given by the $(g_m/I_{DS})^2$ and the $1/I_{DS}$ dependencies this error is more meaningful than the standard deviation as the standard deviation only shows the spread of the measurements and not their accuracy. For the calculation of the errors, the statistical error from averaging the ten measurement points and the fluctuation of the DC current used for normalisation were taken into account. These two errors were much larger than the instrument errors – at least one order of magnitude in case of the DC current fluctuation and around three orders of magnitude in case of the noise current's statistical error. Of these two the fluctuation of the noise was much larger than the fluctuation of the DC current. Still, both were taken into account as the plotted measure directly contains both the noise current and the DC current. The origin of the large fluctuations of the noise current is assumed to be the same as for the fluctuations of the frequency-dependent measurements, which was explained above. Despite the standard deviation being as large as the measured value in some cases the measurement accuracy reached in this thesis can still be considered as good, as spreads up to several orders of magnitude are not uncommon for noise measurements on scaled transistors [34].

One of the reasons for deviations of the data points from the model is that the nanowires' conductivity changes over time. The transfer characteristics measurements resulting in the $(g_m/I_{DS})^2$ curves were carried out before and after the noise measurements. However, it takes around one and a half hours to complete noise measurements at all gate biases and the device behaviour is known to change during this time (Fig. 5.10).

This reliability problem is believed to mostly originate in the organic resist used as spacer layer between the device contacts and has already been mentioned in section 3. Measuring several transfer curves during the noise measurement and using one of those recorded at around half of the time or even averaging the transfer curves would not further increase the accordance between the data points and the $(g_m/I_{DS})^2$ curve. In any case only very few of the noise data points would have been measured at exactly the same device condition as one of the transfer curves. Furthermore, referring to the problem of devices breaking during measurements, it could be that one of the measurement instruments creates a spike when starting a transfer measurement. For this reason transfer measurements in between noise measurements were discarded. With increasing device reliability the accordance between the measured data and the model should increase even further.

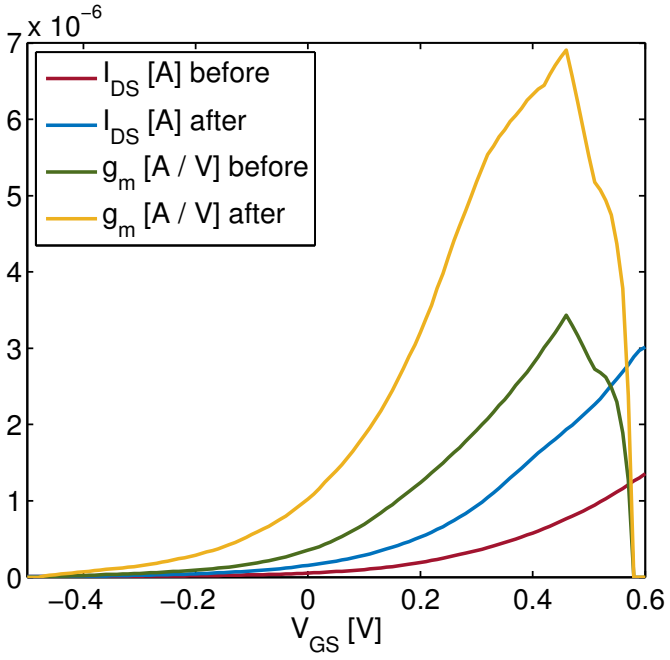

FIGURE 5.10: Comparison of the transfer characteristics before and after a noise measurement. The sharp edges are measurement artefacts.

5.3.5 Extraction of Gate Oxide Trap Densities

With the measured values for the noise current power and the transconductance according to Eq. 2.35 the trap density in the gate oxide can be estimated. For convenience Eq. 2.35 is repeated here:

$$n_t = \frac{f^\gamma W L C_{ox}^2 S_I}{q^2 k_B T g_m^2}. \tag{5.1}$$

W is the gate width – in the case of gate-all-around nanowire transistors this is the nanowire circumference –, L is the gate length, C_{ox} the gate oxide capacitance per unit area, S_I the measured noise current power, q and k_B the elementary charge and the Boltzmann constant, respectively, T the temperature and g_m the measured transconductance. From processing the gate length L is estimated to be approximately 150 nm and the gate capacitance C_{ox} is calculated according to standard electrostatics for a cylindrical capacitor with inner radius r_1, outer radius r_2 and length L:

$$C = 2\pi\epsilon_0\epsilon_r \frac{L}{ln\left(\frac{r_2}{r_1}\right)}. \tag{5.2}$$

C_{ox} is normalised with the gate area $W \times L$. All inserted values are taken from the processing specifications in chapter 3. For III-V material devices the semiconductor capacitance C_S has to be taken into account as well [35]. As the semiconductor capacitance and the gate oxide capacitance are in series, the gate capacitance is diminished. Several studies on nanowire capacitances [35][36] imply that the semiconductor capacitance is in

the order of the gate oxide capacitance. Thus, as the semiconductor capacitance was not measured during this work, the calculated value of the gate oxide capacitance is divided by two to account for the semiconductor capacitance. The values found for the trap densities range from 10^{20} cm^{-3} eV^{-1} to 10^{22} cm^{-3} eV^{-1} 5.11. This is comparable to values that were found for MOSFETs with the same oxide-channel material combination [25].

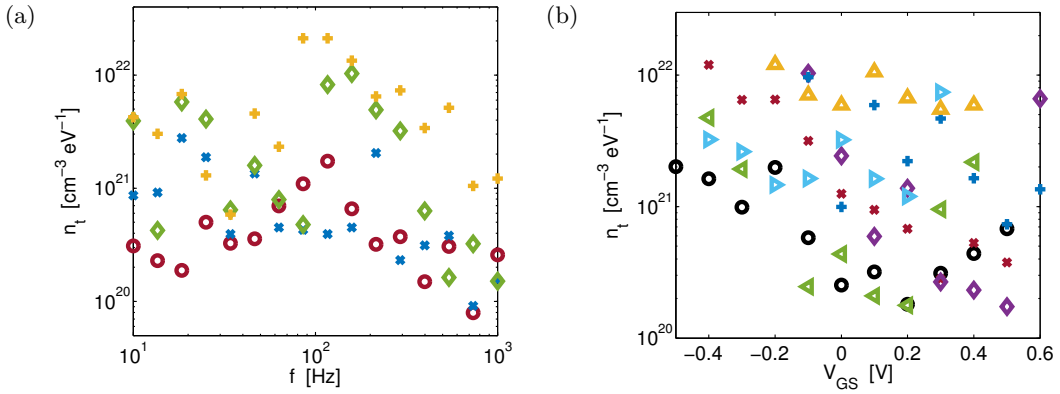

FIGURE 5.11: Gate oxide trap densities for different samples plotted with different dependencies. The additional surface treatment only affects the immediate interface between channel and oxide so there is no difference between the samples deeper in the high-k crystal **(b)**. **(a)** A clear frequency dependence is not visible. **(b)** The triangle markers are for a sample without additional surface treatment, the other markers are for a sample where the surface treatment was included.

In the theory part it was shown that different trap depths result in different frequency contributions (cp. Eq. 2.31). To investigate this spatial distribution in the gate oxide the calculated trap densities were plotted against the frequency. Fig. 5.11(a) shows that there is no considerable frequency dependence which implies that the trap density is mostly uniform in the probed depth between 1.9 and 2.5 nm into the gate oxide. For some of the samples there might be a small peak at ca. 150 Hz, which corresponds to a depth into the oxide of ca. 2.1 nm.

Fig. 5.11(b) shows that the additional surface treatment immediately before the application of the gate oxide has no effect on the high-k crystal quality away from the interface. There is no difference in the trap densities between the samples with or without special surface treatment. Generally, the extracted trap densities are quite scattered but especially for the devices from the sample with additional surface treatment the trap densities increase towards negative gate voltages. Comparing this observation with C-V measurements for similar material systems [22][37] suggests that in energy the trap density in the gate oxide increases into the conduction band.

5.4 Temperature-Dependent DC Measurements

Temperature-dependent DC measurements on TFETs were carried out at five different temperatures: 10 K, 70 K, 140 K, 210 K and at room temperature. As in the DC measurements before, the source was biased at 0 V and the drain at 50 mV. The measurements were carried out on one of the older samples so the additional surface treatment introduced for the newest sample was missing. Still, the results give insight into the temperature-dependence of TFETs. Fig. 5.12 shows the transfer characteristics of all measured temperatures for one of the measured devices.

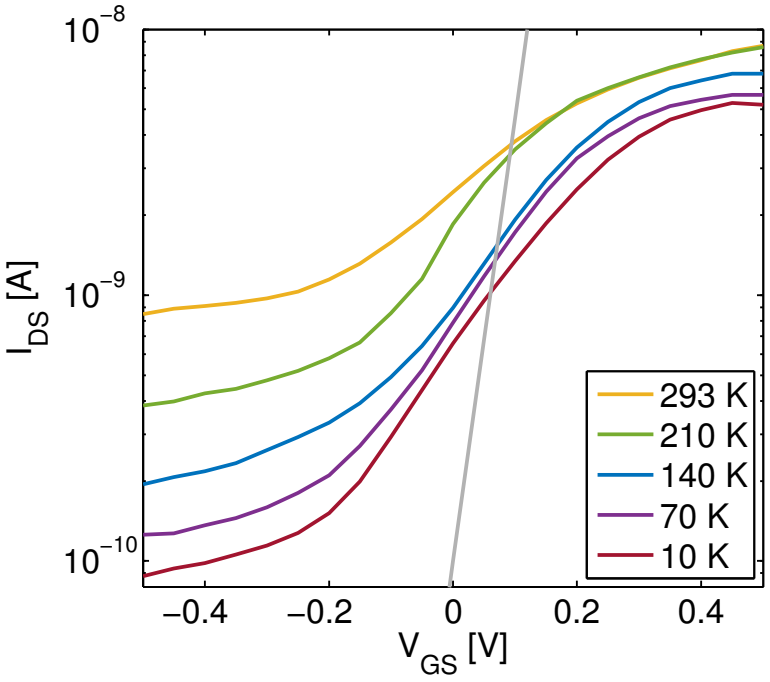

FIGURE 5.12: Transfer characteristics at different temperatures. The measurement errors were found to be negligible for this measurement so the differences in the off-currents are really a temperature-dependency. The grey line indicates a subthreshold slope of 60 mV / decade.

The only instrument contributing to measurement errors was the parameter analyser. Here again, the largest influence was the inaccuracy of the voltage source (cp. 4.3) and thus the fluctuation in the source-drain current proportional to the transconductance. The errors were calculated for all measurement values according to $\Delta I_{DS} = g_m \Delta V_{GS}$ with g_m calculated from the transfer characteristics measurements and ΔV_{GS} taken from the instrument manual. All errors calculated in this way were at least two orders of magnitude smaller than the respective measurement values and were thus neglected in Fig. 5.12 (cp. also Fig. 4.3 for the intrinsic noise of the parameter analyser).

Because the errors are so small the clear separation of the off-current curves in

Fig. 5.12 indeed has to originate in a temperature-dependency. The fact that the off-current increases with the temperature supports the assumption about the off-current made in section 5.3.3 and explained by the band structure in Fig. 5.9. It was assumed that after tunnelling through the broken band gap in the transistors' off-state the electrons are thermionically excited into the channel area before they contribute to a current. With decreasing temperature the thermionic excitation decreases and thus also the current. This of course undermines the initial idea of a temperature-independent subthreshold slope as it re-introduces a temperature dependency in switching off the TFETs. Fig. 5.12 shows that the measured devices' subthreshold slope is far from 60 mV / decade. However, in this case it is assumed that the poor switching does not result from temperature effects but from a poor gate control over the junction. The measured sample was one of the first TFET samples working at all so the devices are far from being ideal TFETs. Furthermore, Fig. 5.12 shows that the subthreshold slope barely varies with the temperature (Table 5.1) which supports the assumption that the poor switching behaviour at this state of development is not a temperature effect.

Temperature	Subthreshold Slope
10 K	300 – 420 mV / decade
70 K	390 mV / decade
140 K	300 mV / decade
210 K	300 mV / decade
293 K	420 – 660 mV / decade

TABLE 5.1: The variations in the subthreshold slopes are attributed to device-to-device fluctuations rather than to a temperature-dependency.

There are different possible explanations for the degradation of the subthreshold slope in TFETs. Examples are band-tails, phonon or trap assisted tunnelling or interface defects [26]. Because of the subthreshold slope's weak temperature dependence and the known difficulties to achieve a good oxide-to-channel interface here interface defects are assumed to be the dominant source for the subthreshold degradation. According to standard MOS electrostatics the energy bands E_g in the gated transistor area follow the applied gate voltage V_{GS} as

$$\delta E_g = \frac{q\, C_{OX}}{C_S + C_{OX} + q^2 D_{it}}\, \delta V_{GS}, \tag{5.3}$$

where C_{OX} is the gate oxide capacitance, C_S the semiconductor capacitance and D_{it} is the interface defect density [26]. A high D_{it} reduces the energy bands' sensitivity to the gate voltage and thus diminishes the subthreshold slope. Assuming these interface defects to be the dominant degradation source is further supported by the considerably improved subthreshold slope on the sample with a specially treated interface.

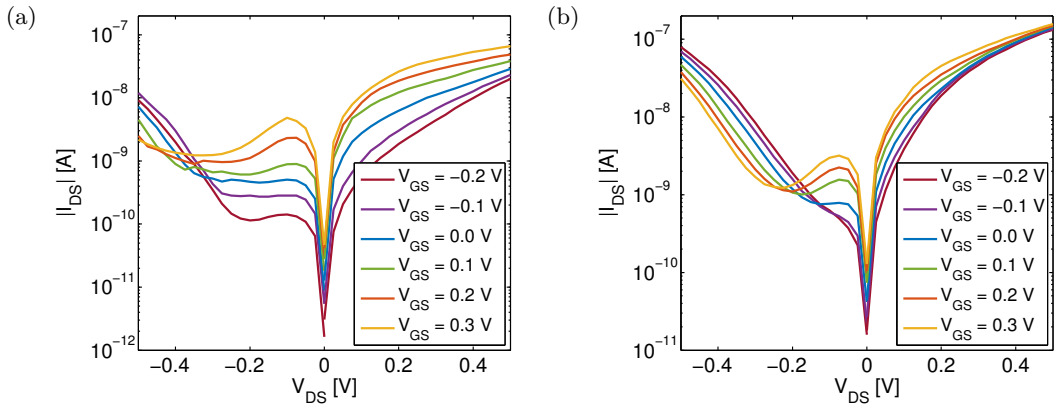

FIGURE 5.13: TFET output characteristics for the same device at **(a)** 10 K and at **(b)** 293 K. A temperature effect is mostly visible in the reverse bias direction.

In the TFET output characteristics a temperature-dependency is not only visible in the off-current but also in the reverse bias direction (Fig. 5.13). At 10 K the NDR region in the reverse bias direction is broader and more separated than at room temperature and at room temperature the current level is generally higher. These observations support the assumptions made about NDR behaviour in section 5.2. At 10 K the electrons have less thermal energy than at higher temperatures so a higher reverse bias at the source contact is required to lower the energy barrier from channel to source far enough for the electrons to be able to overcome the barrier. Thus, the NDR region is broader. The fact that the curves lie closer together at 293 K, are less distinct and generally at a higher level than at 10 K is probably the result of an unwanted influence of thermal electron energy which cannot be suppressed by the imperfect gate control of the TFETs at the current state of development.

Chapter 6

Conclusion and Outlook

In this work low-frequency measurements and temperature-dependent DC measurements have been carried out on InAs/GaSb TFETs with an Al_2O_3/HfO_2 bilayer gate oxide. It has been found that the noise behaviour of these TFETs at room temperature very much resembles that of MOSFETs. All devices showed $1/f$ behaviour as expected for conventional electronic elements. For TFETs with a thoroughly treated interface between the channel area and the surrounding high-k material g-r noise is dominant at all gate voltages. This can be inferred from the normalised noise power following $(g_m/I_{DS})^2$. For the further development of TFETs this implies that reducing the trap density in the high-k material and at its interface to the channel is the most critical aspect for reducing noise in the devices. Improving the high-k material in this way will also improve the gate control over the junction and thus the switching behaviour of the devices. Comparing the measured InAs/GaSb TFETs with Si TFETs [17] revealed that the Si TFETs exhibit lower noise levels. As the interface between Si and the gate stack (SiO_2 as interface layer) is of much higher quality than for InAs/GaSb this emphasises the importance of the gate oxide for the device behaviour. The trap densities in the Al_2O_3/HfO_2 gate oxide were found to range between 10^{20} cm^{-3} eV^{-1} and 10^{22} cm^{-3} eV^{-1}. This is comparable to MOSFETs consisting of the same materials. Low-frequency noise measurements are a valuable tool for this kind of material analysis as it is difficult to evaluate traps in this range with standard probing techniques [19].

Complementing the noise measurement results with the low-temperature DC measurement results suggests that in the TFETs' off-state the electrons can still tunnel through the junction into the channel area but to contribute to the off-current they have to be thermionically excited to overcome the barrier resulting from the band bending in the channel. The fact that electrons are still able to tunnel into the channel is a consequence of the broken bandgap between the materials of the source (GaSb)

and the channel (InAs). As this exact material combination was introduced to achieve high on-currents for the time being it is not an option to change the materials. As the second-most critical aspect regarding the off-current, it is probably most sensitive to the alignment of the gate to the junction, so special care has to be taken during this processing step. As the subthreshold slope is related to the off-current this processing step is just as crucial for a low subthreshold slope. The subthreshold slope did not show a strong temperature dependence. Thus, it is assumed that the dominant sources causing a degradation of the subthreshold slope in the TFETs examined here are not thermal effects but interface traps between the gate oxide and the channel.

For future research it would be very interesting to carry out noise measurements at low temperatures as well. These might reveal whether the tunnelling junction itself constitutes a significant noise source which might become dominant once the gate oxide trap density is sufficiently reduced. It would also be worthwhile to repeat the temperature-dependent DC measurements on samples with a specially treated channel-to-gate-oxide interface. Furthermore, it would be interesting to carry out noise measurements at different source-drain voltages to see whether the TFETs' noise behaviour changes at higher operating voltages or in the reverse operating direction. Especially for the latter measurements, which would require single devices to be measured over a long time, the measurement setup has to be fixed so that it does not damage the devices under test anymore. This might be achieved by adding a high-pass filter to the setup in case external voltage spikes are the cause for breaking devices or operating the whole setup with batteries as power sources. In case one of the measurement instruments is identified as responsible for breaking devices the instrument has to be changed. A general first idea would be using the cryo probe station for room temperature measurements as well as it possesses a generally better shielding against external influences.

A further improvement for noise measurements would be the use of a spectrum analyser instead of a lock-in amplifier. This would increase measurement speed and thus reduce errors as described in the chapter before. Furthermore, it would allow to accumulate more data (more different devices as well as more data points) and thus further facilitate the evaluation of the results. However, it could be shown that noise measurements using a lock-in amplifier are possible and render meaningful results.

Apart from improving the high-k material and its interface to the channel the next great steps will be to further reduce the TFETs' nanowire diameter to improve the electrostatic gate control and to approach 1D conduction. On a larger scale the integration of TFETs into circuits will be very interesting. Towards the end of this thesis the first RF measurements on TFETs could be carried out, which provide more insight into the device properties and open promising opportunities for circuit integration.

Looking at TFETs based on nanowires on a larger scale the most critical challenge is probably the alignment of the gate. Without this processing step being implemented in an efficient and reliable way nanowire TFETs will probably not become interesting for large scale production. This challenge applies to vertical devices in particular. On the other hand, impressive progress has been made during the last years and the urgent need for low-power electronics definitely requires novel devices. As stated in the introduction to this thesis TFETs are among the most promising candidates for low-power electronics. May TFETs be realised in nanowire or in a different architecture, in any case, with vertical nanowire TFETs it is possible to gain much more insight into the device physics which will bring forward future developments. Future developments are still necessary for TFETs but as Edward Teller once put it: “The science of today is the technology of tomorrow.”

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