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Master Thesis Project

Implementation of a 200 MSps 12-bit SAR ADC

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Abstract

Analog-to-digital converters (ADCs) with high conversion frequency, often based on pipelined architectures, are used for measuring instruments, wireless communication and video applications. Successive approximation register (SAR) converters offer a compact and power efficient alternative but the conversion speed is typically designed for lower frequencies. In this thesis a low-power 12-bit 200 MSps SAR ADC based on charge redistribution was designed for a 28 nm CMOS technology.

The proposed design uses an efficient SAR algorithm (merged capacitor switching procedure) to reduce power consumption due to capacitor charging by 88 % compared to a conventional design, as well as reducing the total capacitor area by half. Sampling switches were bootstrapped for increased linearity compared to simple transmission gates. Another feature of the low power design is a fully-dynamic comparator which does not require a pre-amplifier.

Pre-layout simulations of the SAR ADC with 800 MHz input frequency shows an SNDR of 64.8 dB, corresponding to an ENOB of 10.5, and an SFDR of 75.3 dB. The total power consumption is 1.77 mW with an estimated value of 500 μW for the unimplemented digital logic. Calculation of the Schreier figure-of-merit was done with an input signal at the Nyquist frequency. The simulated SNDR, SFDR and power equals 69.5 dB, 77.3 dB and 1.9 mW respectively, corresponding to a figure-of merit of 176.6 dB.

Acknowledgements

We would like to thank our supervisors Mattias Palm and Roland Strandberg at Ericsson for the warm welcome and invaluable guidance throughout the project. We would also like to thank our supervisor at LTH, Pietro Andreani, for rewarding discussions concerning the design work and for providing interesting scientific articles on the subject. Finally, we would like to thank our examiner Peter Nilsson at LTH for the feedback on our work.

Victor Gylling and Robert Olsson

Preface

This thesis work was carried out at the Faculty of Engineering, Lund University in collaboration with Ericsson Research in Lund, over the period from January 2015 to June 2015. In this thesis work the two authors has been working together towards the same goal - designing a functional SAR ADC that fulfills the requirements. Both authors have taken part in all steps of the process, from literature study to design of the individual components and verification of the converter. It is hard to separate who have done exactly what, but the main responsibilities in writing the report were chapters 1, 4 and 6 for Victor while Robert focused on chapters 2, 3 and 5.

Table of Contents

Introduction 1

1 Theory 3
- 1.1 Fundamental concepts of analog-to-digital converters . . . 3
  - 1.1.1 Noise 3
  - 1.1.2 Dynamic specifications 5
  - 1.1.3 Figure of merit 6
- 1.2 Successive approximation converters . . . 7
  - 1.2.1 Sub-blocks of a SAR ADC 8
  - 1.2.2 Charge redistribution circuit implementation 9
  - 1.2.3 Differential architecture 10
- 1.3 Switching procedures . . . 11
  - 1.3.1 Energy dissipation due to capacitor charging 12
  - 1.3.2 Conventional switching 12
  - 1.3.3 Merged capacitor switching 14
- 1.4 Effects of capacitor mismatch . . . 16
- 1.5 Comparator . . . 17

2 The design process 19
- 2.1 Available resources . . . 19
  - 2.1.1 Simulation tools 19
  - 2.1.2 Process design kit 19
- 2.2 Specifications . . . 20
- 2.3 Design requirements . . . 21
  - 2.3.1 Effective resolution 21
  - 2.3.2 Power consumption 21
  - 2.3.3 Unit capacitance matching 22
  - 2.3.4 Requirement on kT/C noise 22
  - 2.3.5 Clock generator 23

3 High-level model 25
3.1 Capacitive DAC 27
3.1.1 Switching power 27
3.1.2 Requirements on unit capacitance mismatch 28
3.1.3 Switch scaling 30
3.2 Comparator 30
3.3 SAR register 30

4 Implementation in 28 nm SOI 33
4.1 Capacitive DAC 33
4.1.1 MOM capacitors 33
4.1.2 Switches 35
4.1.3 Switch buffers 39
4.1.4 Down-sizing of switches 39
4.2 Comparator 40
4.2.1 Single-stage latch 41
4.2.2 Two-stage latch 42
4.3 Full ADC implementation 44

5 Verification of the design 45
5.1 Resolution 45
5.2 Monte Carlo simulation 46
5.3 Power consumption 46
5.4 Robustness 47
5.4.1 Temperature 47
5.4.2 Supply voltage 48
5.4.3 Common-mode voltage 48
5.4.4 Reference voltage 50
5.4.5 Source impedance 50
5.4.6 Sampling frequency 50
5.4.7 Process corners 51
5.5 Input signal variations 51
5.5.1 Amplitude 51
5.5.2 Frequency 52
5.6 Circuit area 52
5.7 Comparison with state-of-the-art ADCs 53

6 Discussion 55

7 Conclusion 57

References 59

A List of acronyms **61**

B Source code **63**
B.1 Verilog-A model of capacitor with mismatch 63
B.2 Spectre model file for the capacitor model 64
B.3 Verilog-A model of comparator 64
B.4 Verilog-A model of successive approximation register for MCS procedure 66

Introduction

Analog-to-digital converters (ADCs) with high sampling rate and medium resolution are important building blocks in instrumentation (oscilloscopes, spectrum analyzers, medical imaging), video applications and wireless communication where pipelined ADCs often are used [1]. One major disadvantage of the pipelined architecture is the static power consumption from amplifiers between the converter stages. Successive approximation register (SAR) ADC architectures offer a compact and power efficient alternative but are generally designed for lower frequencies, as shown in figure 0.1.

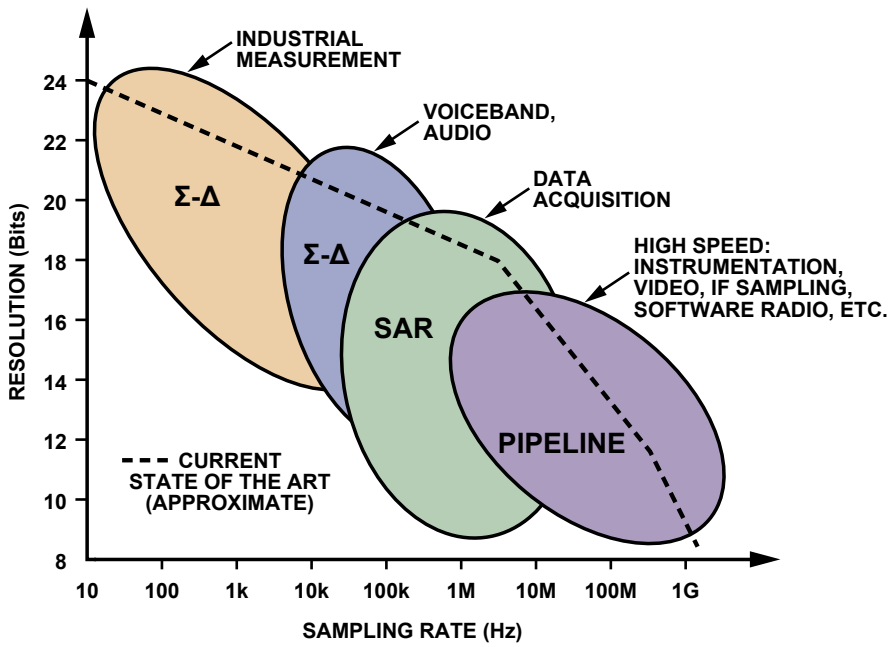


Figure 0.1: Overview of common ADC types [1].

In this master thesis project a 12-bit SAR ADC based on switched capacitor technology is proposed. It is designed using a 28 nm CMOS technology provided by STMicroelectronics. The SAR ADC is to operate at a conversion speed up to 200 MSps while maintaining a low power consumption. To achieve this an alternative switching procedure is used in which the power dissipation due to the repeated charging and discharging of capacitors is reduced by an order of magnitude.

The chapters are organized in the following way:

- ADC theory relevant for the design is discussed.
- Available tools and design requirements are presented.
- A high-level model of a 12-bit SAR ADC is implemented using ideal sub-blocks. This model is then used to confirm the requirements on the different sub-blocks.
- The SAR ADC is implemented using the process design kit (PDK) supplied by STM. To be able to fulfill the performance requirements the SAR ADC is further improved by altering the design.
- The functionality and performance of the final design are verified. Simulations are made to test the ADC robustness to PVT (process, voltage and temperature) variations.
- Discussion regarding the impact of design choices are made followed by a brief review of future work.
- Finally the thesis is concluded based on the discussions and measurements presented throughout the report.

Chapter 1
Theory

1.1 Fundamental concepts of analog-to-digital converters

This chapter introduces theory of fundamental data converter concepts. Different sources of noise are discussed and central performance metrics are defined. In the second part of the chapter, essential theory related to SAR ADCs is described. The conversion algorithm and sub-blocks of a SAR ADC are introduced. Different switching methods and the relationship between capacitor mismatch and resolution are also described.

1.1.1 Noise

Random deviations from an ideal signal are characterized as *noise*. If the noise contribution relative to the signal is too large, logical errors might occur which in turn could lead to performance degradation or even device malfunction. In most real devices this is unacceptable, making noise analysis an important aspect designing an ADC. There are several types of noise with different origins. A few examples of relevant ADC noise sources are described below.

Quantization noise

Analog-to-digital conversion is based on the concepts of sampling and quantization. Sampling is the process of capturing values, or samples, of the input signal at discrete points in time while quantization is the approximation of these values with discrete levels. The two processes are illustrated in figure 1.1 where the analog signal, which is continuous in both time and amplitude, is converted into a digital signal which is discrete in both time and amplitude.

The accuracy of the quantization depends on the resolution, i.e. how many quantization levels there are. The resolution is normally expressed in number of bits n, which relates to the number of quantization levels R as $2^n = R$. The quantization errors can often be seen as white noise with the power calculated

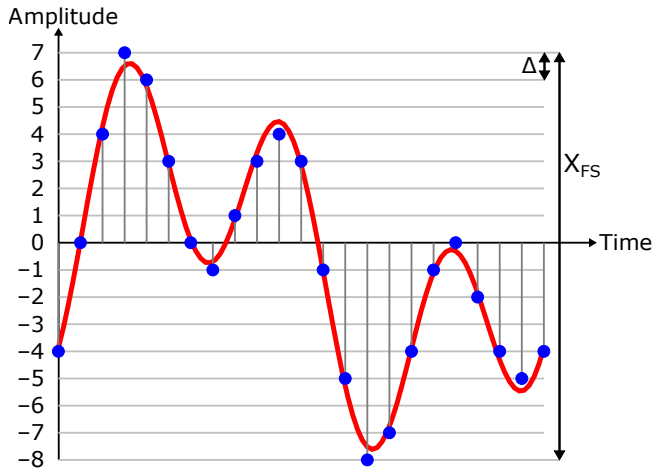


Figure 1.1: Illustration of sampling and quantization - basic concepts of analog-to-digital conversion.

as in equation (1.1), where Δ is the step size between available quantization levels and X_{FS} is the full scale-swing [2, p. 19].

$$P_Q = \frac{\Delta^2}{12} = \frac{(X_{FS}/2^n)^2}{12} \quad [\mathrm{V}^2] \tag{1.1}$$

The quantization noise represents the error due to quantization, and it is a fundamental lower limit for the total noise of an ADC. The equation above states that quantization noise cannot be completely removed as it would require infinite R.

Jitter noise

Ideally, sampling of an ADC signal is performed with a fixed period. If there is a deviation, so called *jitter*, in the time between two samples an error occurs. The size of the error depends on how fast the signal changes and how large the time deviation is. Jitter noise becomes more dominant for high-frequency devices since it has a strong dependency on input frequency f_{in} as seen in equation (1.2), where $\langle \delta_{ji} \rangle$ denotes the jitter constant [2, p. 20].

$$P_{ji} = \frac{A_{in}^2 \cdot (2\pi \cdot f_{in})^2}{2} \cdot \langle \delta_{ji}(t)^2 \rangle \qquad [\mathrm{V}^2] \tag{1.2}$$

Thermal noise

Another fundamental limitation on the minimum noise level is given by the thermal agitation of electrons in the electrical conductors. This noise is lin-

early dependent on temperature T and inversely proportional to the load capacitance C as seen in equation (1.3) where k is the Boltzmann constant [2, p. 23]. It is therefore sometimes called kT/C noise.

$$P_{kT/C} = \frac{kT}{C} \qquad [\mathrm{V}^2] \tag{1.3}$$

Equation (1.3) shows that the thermal noise can be suppressed by increasing the capacitance C. However, a larger capacitance comes at the expense of increasing area on chip and a higher power consumption when the capacitor is being charged.

1.1.2 Dynamic specifications

The Signal-to-Noise Ratio (SNR) is an important performance metric to describe the signal quality. SNR is defined as the ratio between the power levels of the input signal and the noise. There are several definitions of noise ratio differing in which signal disturbances that are included. In this work the Signal-to-Noise-and-Distortion Ratio (SNDR or SINAD), which includes distortion as well as noise, is used. Distortion is defined as signal dependent nonlinear effects resulting in a degradation of the signal quality. Equation (1.4) presents an equation for calculating SNDR for the most dominant contributions in noise and distortion [2, p. 62]. The input signal power P_{signal} depends on the waveform; for a full-scale sine wave it is equal to $X_{FS}^2/8$ [2, p. 19].

$$\mathrm{SNDR} = 10 \cdot \log_{10}\left(\frac{P_{signal}}{P_Q + P_{ji} + P_{kT/C} + P_{distortion}}\right) \qquad [\mathrm{dB}] \tag{1.4}$$

As previously mentioned it is impossible to completely remove noise from the system. It is therefore not possible to reach the resolution of an ideal ADC circuit. One way to measure the dynamic performance is to define the effective number of bits (ENOB), which describes the equivalent resolution corresponding to a certain SNDR value. In an ideal converter where the only noise is due to quantization, equations 1.1 and 1.4 can be transformed into equation (1.5).

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{1.5}$$

In ADC design it is usually a good compromise to allow some degradation due to noise and distortion. Otherwise these effects have to be extremely small which would require components with very high power consumption. For a typical ADC it is normal that between one and two bits are assigned to degradation when implementing the system.

1.1.3 Figure of merit

One method of comparing the energy efficiency of ADCs is by using a figure of merit (FOM). There are different FOM definitions with slightly different approaches on how to represent the performance in the best way. FOM is applicable on all converter architectures and is used to illustrate the position of present research as well as showing ongoing trends in ADC development.

A well-used definition is the Schreier figure of merit ($\mathrm{FOM_S}$) as defined in equation (1.6). In this equation BW is the bandwidth of the signal and P is the total power consumption of the converter.

$$\mathrm{FOM_S} = \mathrm{SNDR} + 10 \cdot \log_{10}\left(\frac{BW}{P}\right) \qquad [\mathrm{dB}] \tag{1.6}$$

The plot in figure 1.2 is the result of a survey of numerous ADCs presented in scientific papers [3]. It displays $\mathrm{FOM_S}$ versus the Nyquist sampling frequency which is defined as twice the signal bandwidth.

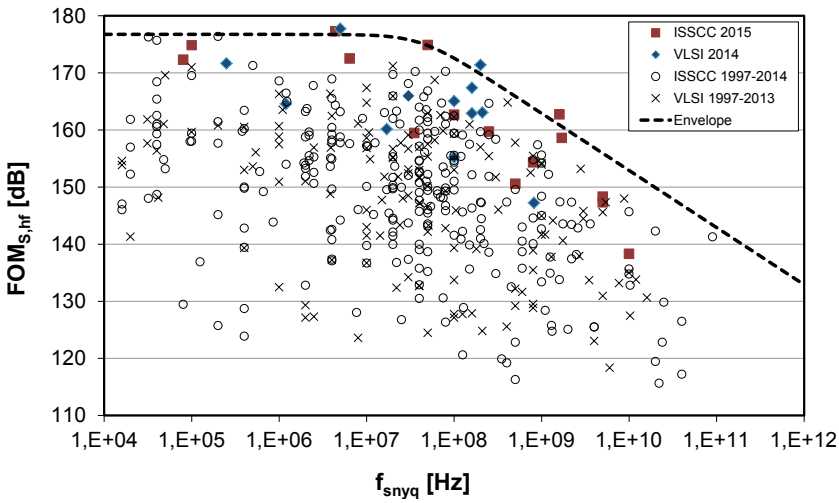


Figure 1.2: Schreier figure of merit vs Nyquist sampling frequency

Another well-used definition is the Walden figure of merit ($\mathrm{FOM_W}$) which describes the energy required for each conversion-step. $\mathrm{FOM_W}$ is defined in equation (1.7).

$$\mathrm{FOM_W} = \frac{P}{2^{\mathrm{ENOB}} \cdot f_s} \qquad [\mathrm{J/conv\text{-}step}] \tag{1.7}$$

High-resolution ADCs are often limited by thermal noise which means that the power must be increased four times to gain one bit of resolution. In this regime the $\mathrm{FOM_S}$ is a more suitable description of how SNDR relates

to the power dissipation, compared to FOM_W which scales the power with a factor two for each bit. Figure 1.3 shows how state of the art ADCs with high resolution follow the constant FOM_S line while the FOM_W may be more suitable for low resolution designs. The Schreier FOM is therefore used when comparing our design to other ADCs.

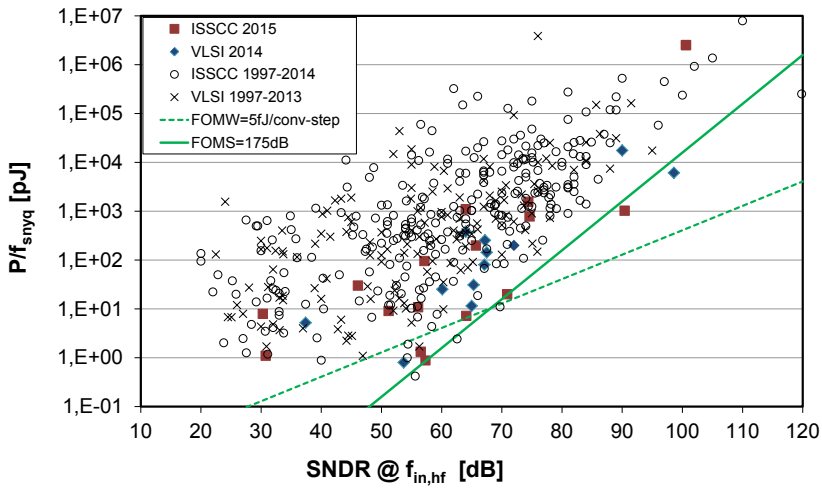


Figure 1.3: Comparison of Schreier and Walden figures of merit.

1.2 Successive approximation converters

The SAR ADC uses a binary search algorithm similar to that shown in figure 1.4 to perform an A/D conversion [2, p. 178]. Since only one bit is converted at a time the complexity and power consumption of the device can be reduced at the expense of reduced conversion rate. The time required for an n-bit conversion is (n+1) clock cycles, assuming only one clock cycle is needed for sampling the input signal before the actual conversion takes place.

The first step of the successive approximation algorithm is determining the most significant bit (MSB). This is done by comparing the sampled input voltage $V_{S\&H}$ to the voltage $V_{DAC} = {}^1\!/_2 V_{FS}$ corresponding to the digital code 10...00. If the input voltage exceeds this level the MSB value is set to 1 and vice versa. This procedure is repeated for determining the next bit with a V_{DAC} of either ${}^3\!/_4 V_{FS}$ or ${}^1\!/_4 V_{FS}$, corresponding to 11...00 and 01...0 respectively, depending on the value of the MSB. When all bits are determined at the end of the conversion cycle the digital output of the ADC is updated and a new conversion cycle begins.

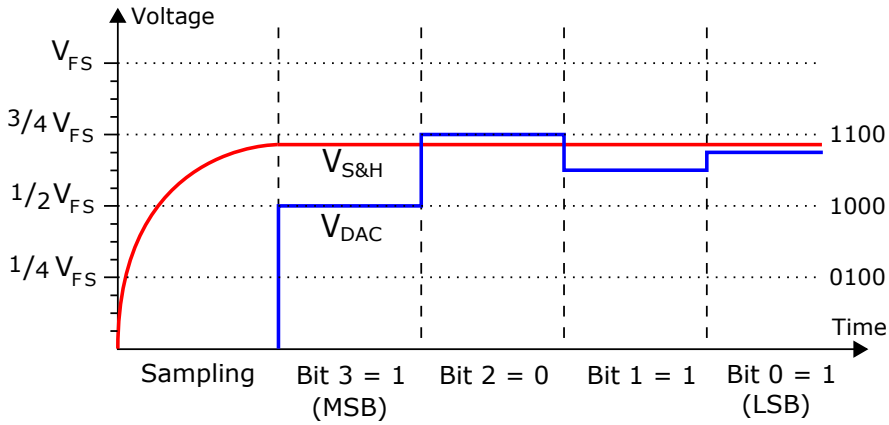


Figure 1.4: Binary search algorithm of a 4-bit SAR ADC.

1.2.1 Sub-blocks of a SAR ADC

Figure 1.5 shows the main building blocks of a SAR ADC. The sample and hold (S&H) block samples the input signal during the first clock cycle and holds it during the rest of the conversion cycle. The successive approximation register (SAR) is a logic block which stores the values of each bit and provides the digital input to the digital-to-analog converter (DAC) which converts it into the voltage V_{DAC}. The two voltages $V_{S\&H}$ and V_{DAC} are compared and the output of the comparator is fed into the SAR which is then updated for the conversion of the next bit.

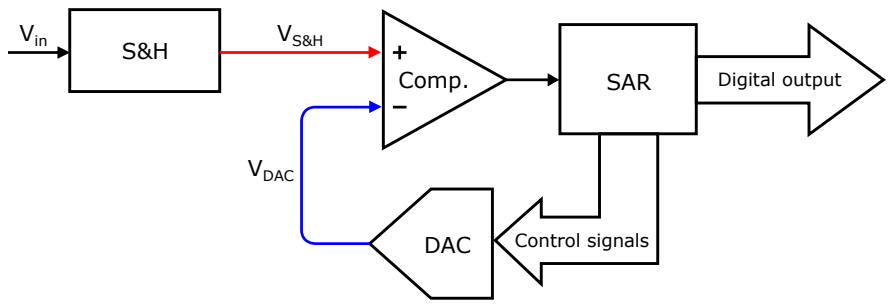


Figure 1.5: Block diagram of a SAR ADC.

An advantage of SAR ADCs compared to other architectures is the compact design. Another common ADC type, the flash converter, performs simultaneous comparisons of the input voltage with $(2^n - 1)$ reference voltage levels, each requiring its own comparator. In contrast, the SAR ADC only needs a single comparator, trading increased conversion time for lower power consumption and chip area.

1.2.2 Charge redistribution circuit implementation

A common circuit implementation for SAR ADCs is based on charge redistribution in a network of capacitors which acts as both S&H, DAC and subtractor. Figure 1.6 shows an example of such a circuit.

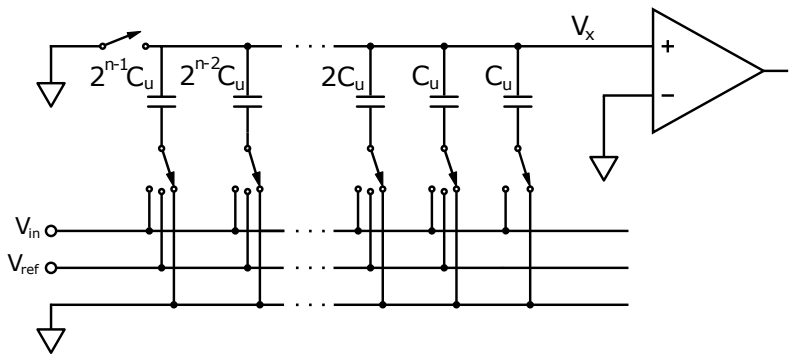


Figure 1.6: Charge redistribution SAR ADC.

An advantage of this implementation is that the DAC only consumes power during charging and discharging of the capacitive network. The SAR is a digital block which can be implemented in CMOS with good power efficiency resulting in low power consumption determined mainly by capacitor charging and power dissipated in the comparator [2, p. 184].

The capacitors in the network are binary weighted and range from C_u (unit capacitance) for the LSB to $2^{n-1}C_u$ for the MSB. An additional C_u (dummy) in parallel to the LSB capacitor gives a total capacitance of 2^nC_u. During the sampling phase the top plates of the capacitors are discharged through a switch to ground and the bottom plates are charged with the input voltage. Given the definition of capacitance ($C = Q/V$) the total charge on the top plates of the network is calculated using equation (1.8) [2, p.183]:

$$Q_{tot} = 2^nC_u(0 - V_{in}) = -2^nC_uV_{in} \tag{1.8}$$

In the next clock cycle the top-plate switch is opened before the SAR sets the MSB value to 1 which in turn connects the bottom plate of the MSB capacitor to V_{ref}. The remaining capacitors are switched to ground. Since the top plate is only connected to the high input impedance of the comparator, the total charge remains the same. However, switching causes the charge to redistribute resulting in a change in top plate potential V_x. As seen in equation (1.9), this voltage is defined as the difference between the DAC and input voltages.

$$
\begin{aligned}
Q_{tot} &= Q_{\text{MSB}} + \ldots + Q_{\text{LSB}} + Q_{\text{dummy}} \\
-2^n C_u V_{in} &= 2^{n-1} C_u (V_x - V_{ref}) + 2^{n-1} C_u V_x \\
V_x &= \frac{V_{ref}}{2} - V_{in}
\end{aligned} \tag{1.9}
$$

If V_x is negative it means that $V_{in} > \frac{V_{ref}}{2}$ and the MSB value of 1 is retained; otherwise it is reset to zero. In the next step the second most significant bit is set to 1, generating a reference level of either $^3/_4 V_{ref}$ or $^1/_4 V_{ref}$ depending on the value of the MSB. Since the DAC voltage approaches the sampled input voltage, as seen in figure 1.4, the output voltage V_x of the capacitive DAC converges step by step towards zero until the LSB is determined. Equation (1.10) describes the general case where x unit capacitors are connected to V_{ref}. Each bit value b_i determines if capacitor i is connected to V_{ref} or ground.

$$
\begin{aligned}
Q_{tot} &= Q_{ref} + Q_{\text{ground}} \\
-2^n C_u V_{in} &= x C_u (V_x - V_{ref}) + (2^n - x) C_u V_x \\
V_x &= \frac{x}{2^n} V_{ref} - V_{in} = \sum_{i=0}^{n} \frac{V_{ref}}{2^{n-i}} b_i - V_{in} = \\
&= \frac{V_{ref}}{2} b_{n-1} + \frac{V_{ref}}{4} b_{n-2} + \ldots + \frac{V_{ref}}{2^{n-1}} b_1 + \frac{V_{ref}}{2^n} b_0 - V_{in}
\end{aligned} \tag{1.10}
$$

1.2.3 Differential architecture

The previously described SAR ADC was single-ended with only one input and one output. Differential architectures, in which two identical halves convert the difference between the two inputs into a differential output, require more chip area and power but offer some advantages to their single-ended counterparts:

- Twice the input range
- Common-mode rejection
- Suppression of even-order harmonics

In the single-ended case, input voltages between ground and V_{ref} can be converted. In a differential implementation the input range is increased to $[-V_{ref}, V_{ref}]$. This is done by using an additional pair of reference voltages

which are created simply by swapping the two original references V_{ref} and ground. The advantage of a larger input range is the increase in maximum signal power which makes the influence of noise less critical.

Common-mode rejection means that the influence of signals that are common to both inputs (e.g. a DC offset) can be suppressed. Even if the common-mode input causes changes in the outputs the changes are nearly identical which keeps the difference between the output voltages unaffected.

The third advantage has to do with the linearity of the circuit. An ideal converter has a linear relationship between input and output but in reality there are always non-linear effects introducing distortion. The transfer function of such a system may be described as in equation (1.11).

$$V_{out}(t) = a_1 V_{in}(t) + a_2 V_{in}(t)^2 + a_3 V_{in}(t)^3 + a_4 V_{in}(t)^4 + ... \tag{1.11}$$

In the differential architecture both the input and output signal are defined as voltage differences. Assume that the single-ended input V_{in} in equation (1.11) is converted into a pseudo-differential signal consisting of $+V_{in}$ and $-V_{in}$. The two voltages are converted separately to generate two output voltages V_{out+} and V_{out-}. Equation (1.12) shows how the even-order terms in the differential output cancel each other. The resulting reduction of the total harmonic distortion improves the ADC performance.

$$\begin{aligned} V_{out+}(t) &= a_1[+V_{in}(t)] + a_2[+V_{in}(t)]^2 + a_3[+V_{in}(t)]^3 + ... \\ V_{out-}(t) &= a_1[-V_{in}(t)] + a_2[-V_{in}(t)]^2 + a_3[-V_{in}(t)]^3 + ... \\ V_{out}(t) &= V_{out+}(t) - V_{out-}(t) = 2a_1 V_{in}(t) + 2a_3 V_{in}(t)^3 + ... \end{aligned} \tag{1.12}$$

1.3 Switching procedures

In the conventional capacitive DAC a majority of the total energy dissipation is due to repeated charging and discharging of the large capacitor array. Several new techniques using alternative switching algorithms have been proposed which dramatically decrease this power consumption. The split-capacitor- [4] and energy-saving [5] techniques propose reduction in switching energy of 37% and 56% respectively, while the monotonic switching technique [6] offer savings of up to 81%. In the following section the conventional switching procedure is described in depth and compared to one promising alternative, merged capacitor switching (MCS) [7, 8], suggesting energy savings of 87.5%.

1.3.1 Energy dissipation due to capacitor charging

The energy dissipated in each switching step can be calculated by studying the changes in voltage across each capacitor. Switching the bottom plate of a capacitor from ground to V_{ref} causes the voltage V_x on the top plate to change as described in section 1.2.2. In the general case the voltage at the bottom plate of a capacitor C_i is changed by ΔV_b causing a change ΔV_x at the top plate. The energy drawn from the reference voltage source V_{ref} connected to C_i, which is determined by the change in charge stored on the capacitor, is described in equation (1.13) [4].

$$\begin{aligned} E &= \int_{t_1}^{t_2} V_{ref} \cdot i_{ref}(t)dt = V_{ref} \int_{t_1}^{t_2} \frac{-dQ(t)}{dt}dt = -V_{ref}\Big(Q(t_2) - Q(t_1)\Big) = \\ &= -C_i V_{ref}\Big((V_x(t_2) - V_b(t_2)) - (V_x(t_1) - V_b(t_1))\Big) = \\ &= C_i V_{ref}(\Delta V_b - \Delta V_x) \end{aligned} \tag{1.13}$$

To determine the average energy per conversion step the contribution of each capacitor in the array must be taken into consideration.

1.3.2 Conventional switching

For the conventional switching procedure the differential input voltage is sampled on the bottom plates of the capacitors. During sampling all capacitors on the positive side of the DAC are connected between the common-mode voltage $V_{cm} = 1/2 V_{ref}$ and $V_{in,p}$. In the next clock cycle the bottom plate of the MSB capacitor is switched to V_{ref} and those of the remaining capacitors to ground while the opposite procedure is done for the negative side. Figure 1.7 shows the switching procedure for a 3-bit capacitive DAC.

In the first switching step the top plate voltage changes from V_{cm} to $V_{cm} - V_{in,p} + 1/2 V_{ref}$. For the MSB capacitor this means that $\Delta V_b - \Delta V_x = (V_{ref} - V_{in,p}) - (1/2 V_{ref} - V_{in,p}) = 1/2 V_{ref}$. The remaining capacitors on the positive side do not contribute to the power consumption since they are connected to ground. On the negative side all but the MSB capacitor are switched to V_{ref}. A similar analysis as for the positive side gives the same difference between ΔV_b and ΔV_x. The total energy dissipated in this stage is therefore calculated as in equation (1.14).

$$E = E_p + E_n = 2 \cdot \Big(2^{n-1} C_u V_{ref}(1/2 V_{ref})\Big) = 2^{n-1} C_u V_{ref}^2 \tag{1.14}$$

Depending on the result of the comparison the top plate on the positive side is switched towards either a higher or lower voltage as shown in figure 1.7.

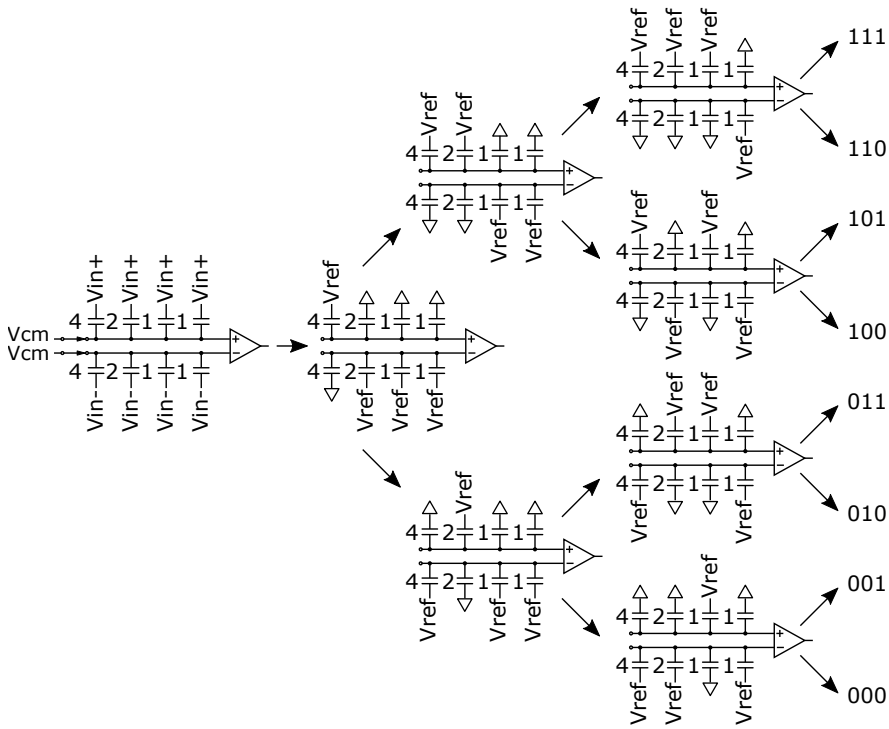


Figure 1.7: Conventional switching method for a 3-bit capacitive DAC. The numbers by each capacitor indicate the number of unit capacitors. An upward transition corresponds to a bit determined to be 1.

The upward transition, which is performed by switching the next capacitor from ground to V_{ref}, requires the energy equal to that of equation (1.15).

$$\begin{aligned} E_{up} &= E_p + E_n = \\ &= \left(2^{n-1} C_u V_{ref}(0 - 1/4 V_{ref}) + 2^{n-2} C_u V_{ref}(V_{ref} - 1/4 V_{ref})\right) + \\ &+ 2^{n-2} C_u V_{ref}(0 + 1/4 V_{ref}) = \\ &= 2^{n-3} C_u V_{ref}^2 \end{aligned} \tag{1.15}$$

Switching towards a lower value is more inefficient since it also requires resetting the capacitor previously switched to V_{ref}, requiring the corresponding capacitor on the negative side to be switched to V_{ref}. The energy drawn from the reference voltage, given by equation (1.16), is five times larger than for the upward transition.

$$\begin{aligned} E_{down} &= E_p + E_n = \\ &= 2^{n-2} C_u V_{ref}(V_{ref} + 1/4 V_{ref}) + \\ &+ \left(2^{n-1} C_u V_{ref}(V_{ref} - 1/4 V_{ref}) + 2^{n-2} C_u V_{ref}(0 - 1/4 V_{ref})\right) = \\ &= 5 \cdot 2^{n-3} C_u V_{ref}^2 \end{aligned} \tag{1.16}$$

Further investigation of the switching energy results in the average energy per conversion step seen in equation (1.17) [6, p. 733]. The average energy is directly proportional to the size of the unit capacitance which motivates the use of a C_u as small as possible without being limited by kT/C noise.

$$E_{avg,conv.} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1) C_u V_{ref}^2 \tag{1.17}$$

1.3.3 Merged capacitor switching

The MCS procedure takes advantage of the differential architecture by making each comparison before the capacitive network is switched. In this way the unnecessary steps used in the trial-and-error approach of a conventional ADC are eliminated. The input voltage is sampled on the top plate which means that no switching energy is required before the first comparison. The MCS procedure is illustrated in figure 1.8.

The MCS switching scheme utilizes the common-mode reference that is already present in a differential SAR ADC. The tri-level DAC gains an additional bit in resolution compared to one with only two reference voltages,

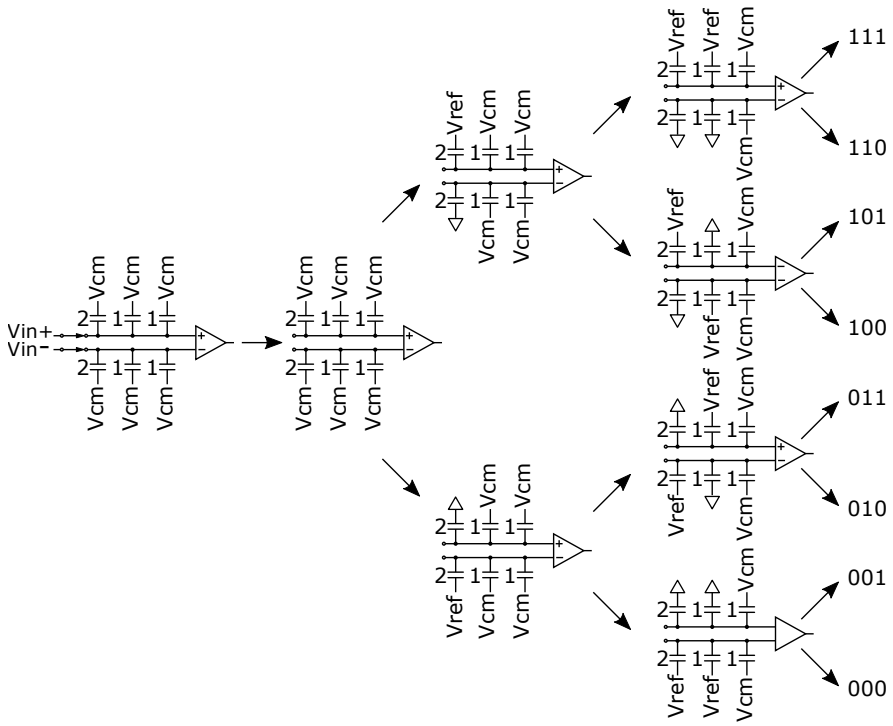


Figure 1.8: MCS procedure for a 3-bit capacitive DAC. The numbers by each capacitor indicate the number of unit capacitors. An upward transition corresponds to a bit determined to be 1.

which means that one capacitor on each side can be removed. The effect of removing the largest capacitor in a binary scaled array is that C_{tot} is reduced by half, decreasing power consumption and area cost. If limited by kT/C noise the total capacitance cannot be reduced but there is still the advantage of fewer capacitors. The larger C_u required to keep C_{tot} constant has the advantage of a smaller perimeter-to-area relationship resulting in less relative parasitics.

By charging the bottom plates to V_{cm} during sampling, "up" and "down" transitions become symmetrical regarding power dissipation. Because of the complementary nature of a differential architecture the charge required from the V_{cm} node on one side is supplied by the other. This charge-recovery reduces the total switching power since the only energy drawn from the V_{cm} reference is that used to charge the bottom-plate parasitics during sampling.

The reduction of C_{tot} reduces power consumption by 50 %. Compared to the previously mentioned monotonic method [8], which also has a reduced C_{tot}, the MCS technique has been shown to save an additional 33% in switching energy. This corresponds to a 87.5 % power reduction compared to a conventional SAR ADC. The additional improvement is because of the charge-recovery in the V_{cm} node as well as the precharging of the capacitive array to V_{cm} instead of V_{ref}.

1.4 Effects of capacitor mismatch

When electronic components are fabricated some variation in their properties, such as device dimensions and layer thickness, is inevitable. Systematic errors such as a slightly higher or lower unit capacitance, typically related to "global" variations during chip production, are usually not a problem. Relative errors, e.g. mismatch between unit capacitors due to differences within a chip, can on the other hand cause deviation from the ideal transfer curve of the DAC resulting in a distorted output. This makes matching of unit capacitors critical for the accuracy and resolution of the entire ADC.

As shown in equation (1.10) the output voltage of a capacitive DAC is determined by the fraction of the total capacitance C_{tot} connected to the reference voltage. With x unit capacitors connected to V_{ref} the top plate voltage becomes:

$$V_x = \frac{C_{ref}}{C_{tot}} V_{ref} \approx \frac{x}{2^n} V_{ref} \tag{1.18}$$

Assuming the distribution of unit capacitance C_u is Gaussian with mean C_0 and standard deviation σ_0 and that the values of unit capacitors are uncorrelated the distributions of C_{ref} and C_{tot} are also Gaussian with the mean

and variance shown in equation (1.19).

$$C_u \sim \mathcal{N}(C_0, \sigma_0^2) \Longrightarrow C_{ref} \sim \mathcal{N}(xC_0, x\sigma_0^2),\ C_{tot} \sim \mathcal{N}(2^nC_0, 2^n\sigma_0^2) \tag{1.19}$$

Since C_{tot} contains the capacitance values of C_{ref} the two are correlated. This means that the ratio C_{ref}/C_{tot} can be approximated by a normal distribution by using a Taylor series expansion [9, p. 304]. The mean and standard deviation of this ratio is shown in equation (1.20).

$$V_x \sim \mathcal{N}(\mu_x, \sigma_x^2), \quad \mu_x \approx \frac{x}{2^n}V_{ref}, \quad \sigma_x \approx \frac{\sqrt{x - x^2/2^n}}{2^n} \cdot \frac{\sigma_0}{C_0}V_{ref} \tag{1.20}$$

Statistically, V_x lies within $3\sigma_x$ from its mean value μ_x with a probability of 99.7 %. To ensure that DAC has no missing codes the deviation (integral non-linearity or INL) from the ideal value μ_x must be smaller than $1/2$ LSB. By finding the maximum value from the expression for σ_x above one can conclude that the worst case INL is at midscale ($x = 2^{n-1}$). The standard deviation at this point is given by equation (1.21).

$$\max(\sigma_x) = \frac{1}{\sqrt{2^{n+2}}} \cdot \frac{\sigma_0}{C_0}V_{ref} \tag{1.21}$$

In a differential architecture the output voltage is the difference between two voltages. As the variance of a sum of two independent variables is the sum of the individual variances, the standard deviation σ_x in the differential case is $\sqrt{2}$ times larger than in the single ended one. However, the full-scale voltage swing V_{FS} of the differential DAC is twice as large as the reference V_{ref}. With these modifications a requirement on the standard deviation of the unit capacitance can be found. For a differential n-bit SAR ADC to achieve m-bit resolution the requirement is given by equation (1.22).

$$\begin{aligned} &3 \cdot \sqrt{2} \cdot \max(\sigma_x) < 1/2 \text{ LSB} \quad \Longrightarrow 3 \cdot \sqrt{2} \cdot \frac{1}{\sqrt{2^{n+2}}} \cdot \frac{\sigma_0}{C_0}V_{ref} < \frac{2V_{ref}}{2^{m+1}} \\ &\Longrightarrow \frac{\sigma_0}{C_0} < \frac{\sqrt{2^{n+1}}}{3 \cdot 2^m} \end{aligned} \tag{1.22}$$

1.5 Comparator

Comparators used in data converters are typically implemented using a single or multiple pre-amplifiers followed by a track-and-latch stage [10, p. 317]. The pre-amplifiers are used to amplify the input signal before reaching the latch

which reduces the input referred noise and enables detection of smaller signals which may be necessary in high-resolution converters. Another advantage of pre-amplifiers is the reduction of kick-back effects. When the comparator takes a decision a full swing output is generated, which capacitively couples back to the comparator input affecting the charge stored on the capacitor bank. The disadvantage of pre-amplifiers is their static (continuous) power consumption.

The regenerative latch uses positive feedback between two back-to-back inverters to quickly compare two input voltages. The output of the latch can be followed by an set-reset-latch (SR-latch or flip-flop) consisting of two NAND gates to hold the determined value until a new decision has been made. A simplified block diagram of a typical comparator architecture is shown in figure 1.9.

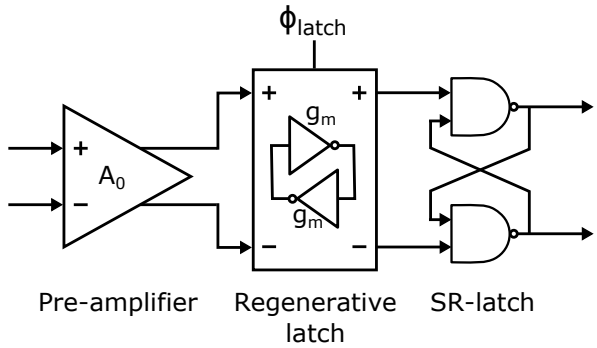


Figure 1.9: Block-diagram of a typical comparator

If the comparator decision time is short and the input voltage small the regenerative latch can stay in a so called metastable state in which the output voltage is not equal to either of the logical levels (1 or 0). If the comparator output is undefined at the end of the latch phase no decision has been made resulting in an error in the output code.

Chapter 2
The design process

2.1 Available resources

In this section the tools used for designing and testing the SAR ADC are presented. Functional circuit models with different degrees of complexity were used, ranging from ideal representations of building blocks to more accurate component models.

2.1.1 Simulation tools

Cadence Virtuoso

The design environment used in this project was Cadence Virtuoso which contains a complete set of tools for integrated circuit design, e.g., schematic editor, simulator engine (Spectre) and layout editor. It is a powerful tool when simulating analog as well as digital circuits. The design environment includes libraries containing ideal components and circuitry which can be used. These libraries are complemented with a design kit provided by STmicroelectronics describing the CMOS technology.

Verilog-A

Verilog-A is a hardware description language for analog circuits designed for the Spectre simulator. In this project it was used to implement models of SAR ADC sub-blocks. These models make it is possible to simulate the functionality of sub-blocks without having to implement them on component level.

2.1.2 Process design kit

The process design kit (PDK) includes process specific libraries of both analog (transistors, passive components etc.) and digital (gates, functional blocks etc.) components. For each device there is a model attached which describes

e.g. the nominal behavior and corners. The provided PDK from STMicroelectronics describes a 28 nm fully-depleted silicon-on-insulator (FDSOI) transistor technology, see figure 2.1.

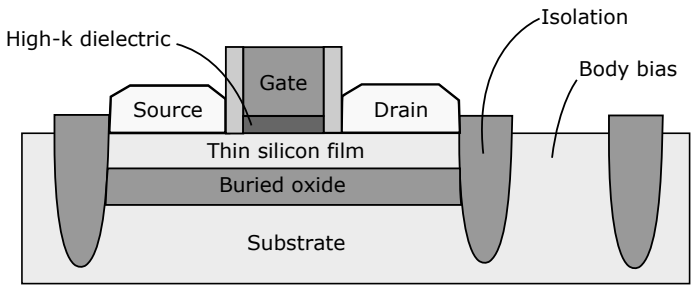


Figure 2.1: Fully-depleted silicon-on-insulator transistor technology.

The use of a depleted transistor improves the electrostatic control as well as device scalability. In modern CMOS processes, low-threshold voltage devices are utilized to provide high switching speed. By varying the bulk voltage, the transistor threshold voltage V_th is altered. For the provided technology low V_th is achieved by connecting the NMOS bulk contacts to V_{DD} and the PMOS bulk contacts to ground. The technology primarily targets low power as to serve wireless and battery operated applications [11].

As shown in section 1.3 the unit capacitance value is of great importance when it comes to power consumption. The minimum capacitance value that can be chosen for the standard MOM capacitor component in the PDK is 1.73 fF. Smaller capacitors could be designed by custom layout, but this was not included in the project. The models for such custom designed capacitors would lack some data, e.g. process variation and random mismatch, that is provided for the standard components in the PDK.

2.2 Specifications

The first step of the design process is to set up a specification on properties which reflect the desired ADC performance for this project. The 12-bit SAR ADC that is to be designed should:

- operate at conversion speeds up to 200 MSps.
- achieve an ENOB greater than 10.
- handle input frequencies up to 800 MHz (for the possibility of using it as a sub-ADC in a time-interleaved architecture).
- be as power efficient as possible.

- use a supply voltage of 1 V.

2.3 Design requirements

The specifications in the previous section were used to set up requirements on the system. The following sections treats aspects such as resolution, power consumption, capacitor matching as well as kT/C and jitter noise.

2.3.1 Effective resolution

From the specification it is possible to calculate the amount of noise and distortion that can be tolerated in the circuit. For an ideal ADC with 12-bit resolution, SNDR is calculated to 74.0 dB using equation (1.5).The specification allows two bits of implementation loss for the whole ADC which can be translated into a minimum requirement on SNDR. In order to achieve an ENOB of 10, SNDR can not be lower than 62 dB.

As previously discussed in section 1.2.3 the effects of noise and distortion can be reduced using a differential SAR ADC architecture. The improvements in noise performance are considered worth the increase in power consumption in order to reach the requirement on the resolution. From here on the SAR ADC will refer to a differential architecture if nothing else is stated.

2.3.2 Power consumption

The Nyquist sampling criterion states that the maximum signal bandwidth that can be captured by a sampling system is theoretically equal to half the sampling frequency [2, p. 5]. This limit, often called the Nyquist frequency, is equal to 100 MHz for a 200 MHz sampling frequency. Figure 1.2 displays the performance of state-of-the-art ADCs achieving FOM_S up to around 170 dB at $f_{s,nyq} = 2 \cdot BW = 200$ MHz. With these values and the assumption of an SNDR at the minimum requirement of 62 dB, equation (1.6) was used to estimate the magnitude of power. Calculations suggest that in order to achieve $\text{FOM}_\text{S} \geq 170$ dB the required power must be less than 1.6 mW. Note that it is not a definite number, but serve to give a hint on what magnitude of power to aim for.

Using equation (1.17) with the minimum unit capacitance of 1.73 fF and a reference voltage of 1 V results in an average switching energy of 9.44 pJ/conversion. By multiplying this value with the 200 MSps sampling frequency an estimated 1.89 mW of the capacitive DAC power can be found which means that the switching energy alone would consume the entire power budget. The MCS procedure described in section 1.3.3 has been shown to save 87.5 % which

gives a switching power of 236 μW. In the power budget there is now room for other components such as the comparator, switches and register.

The differential input voltage to the comparator needs to be sufficiently large for a correct decision to be made fast enough. By adding one or more pre-amplifier stages the signal can be amplified, making it easier for the comparator to take a decision when the input difference is small. However, a pre-amplifier consumes a lot of power due to its static operation. If the comparator is able to resolve its differential input without the pre-amplifier stage there is much to gain in terms of power. Eliminating it altogether might result in problems with *kick-back charge* causing distortion [10, p. 318]. However, a differential ADC architecture and large DAC capacitance counteract the effect of kick-back charges. It is also possible to reduce kick-back by altering the comparator design. It is assumed no pre-amplifier is needed as long the comparator operates correctly.

2.3.3 Unit capacitance matching

The mismatch discussion in section 1.4 can be applied on the ADC that is to be designed. A SAR ADC based on the MCS procedure has only half the number of capacitors compared to a conventional architecture. A 12-bit MCS DAC therefore corresponds to that of an 11-bit conventional SAR ADC ($n = 11$). To fulfill the specified requirement of 10-bit resolution ($m = 10$), equation (1.22) suggest a matching requirement of $\frac{\sigma_0}{C_0} < 2$ % for the unit capacitance. While this may seem like a large value, the binary weighted capacitors consist of several unit capacitors in parallel which causes their relative standard deviation ($\frac{\sigma}{C}$) to decrease as shown in section 1.4.

2.3.4 Requirement on kT/C noise

Using the equations for noise power in section 1.1.1, the impact of kT/C noise can be calculated.

- Calculating the quantization noise power with $X_{FS} = 2$ V and n=12 gives $P_Q = 2.0 \cdot 10^{-8}$ V^2.
- To calculate the thermal noise power, $C_u = 1.73$ fF is assumed resulting in a total capacitance of $2^{11}C_u = 3.54$ pF on each side of the differential DAC. At room temperature ($T = 300$ K) the noise is $P_{kT/C} = 2.3 \cdot 10^{-9}$ V^2.

Because of the large number of unit capacitors in the 12-bit cap-DAC, the kT/C noise is an order of magnitude smaller than the quantization noise even with the smallest available unit capacitance in the PDK. The thermal noise

contribution can therefore be neglected when summarizing the total noise power which simplifies the calculations in upcoming sections.

2.3.5 Clock generator

In this work the clock signals are produced by an ideal clock generator. To verify that the generation of necessary clock signals is realistic in terms of jitter noise some calculations are performed. Equation (2.1) combines equations (1.1), (1.2) and (1.4) to calculate the requirement on clock jitter $\langle \delta_{ji}(t) \rangle$.

$$\mathrm{SNDR} = 10 \cdot \log_{10} \left(\frac{X_{FS}^2/8}{\frac{(X_{FS}/2^n)^2}{12} + \frac{A_i^2 \cdot (2\pi \cdot f_{in})^2}{2} \cdot \langle \delta_{ji}(t)^2 \rangle} \right) \tag{2.1}$$

For a sine input with $f_{in} = 800$ MHz and $A_{in} = 1$ V the jitter constant $\langle \delta_{ji}(t) \rangle$ must be smaller than 0.15 ps for the 62 dB SNDR requirement to be fulfilled. Thermal noise does not need to be included in the calculations as discussed in section 2.3.4.

The requirements on the clock generator are tough as it should have low noise and at the same time be able to generate frequencies up to 2.6 GHz. The implementation of a clock generator is not included in this project but many ADCs with the ability to convert GHz input signals have previously been presented [3].

Chapter 3

High-level model

The requirements discussed in the previous chapter served as a guideline throughout the SAR ADC design process. However, before implementing the circuit with the provided PDK a *high-level model* was created. The high-level model consists of ideal sub-block models which are either described in Verilog-A code or implemented using ideal components from the analogLib library in the Cadence design environment. Although the sub-blocks do not take all non-idealities into account, limiting the accuracy of simulations, the overall functionality can be analyzed with great benefit using these models. One advantage of using a high-level model instead of directly going for a fully implemented design is that the simulation time can be reduced drastically by using simplified models during early stages of development. Moreover, the models enable a systematic investigation of how each sub-block affects the performance of the ADC, since each sub-block can be changed from a high-level model to a transistor level implementation.

The circuit was simulated using the test bench shown in figure 3.2 where input signal, reference voltage, clock signal and power supply all were generated by ideal voltage sources. The measurements were made with a sine wave as input signal and the ADC operating at a conversion speed of 200 MSps as stated in the specification. In order to analyze the digital ADC output an ideal DAC was put in series converting it to an analog signal. The *fast Fourier transform* (FFT) of this analog version of the output generates a spectrum in the frequency domain. From this spectrum metrics such as SNDR and *spurious-free dynamic range* (SFDR), which is the ratio between the signal and the largest tone in the FFT, could be extracted by using the built-in spectrum-analysis tools in the Cadence environment. To provide an integer number of signal periods (coherent sampling) for the 256-point FFT a signal frequency of $\frac{1021}{256} \cdot 200$ MHz ≈ 800 MHz was used.

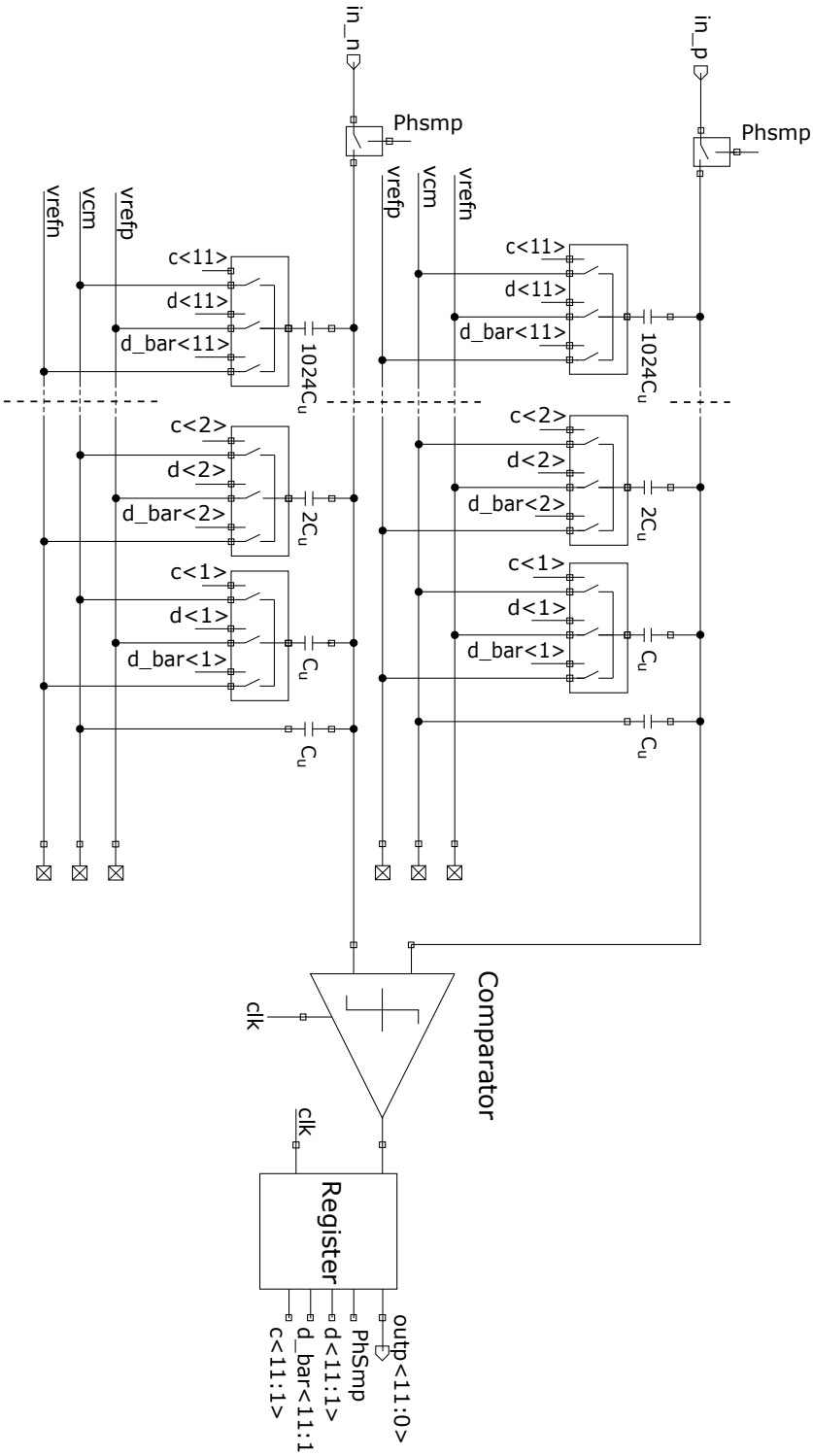


Figure 3.1: Simplified schematic view of the 12-bit SAR ADC.

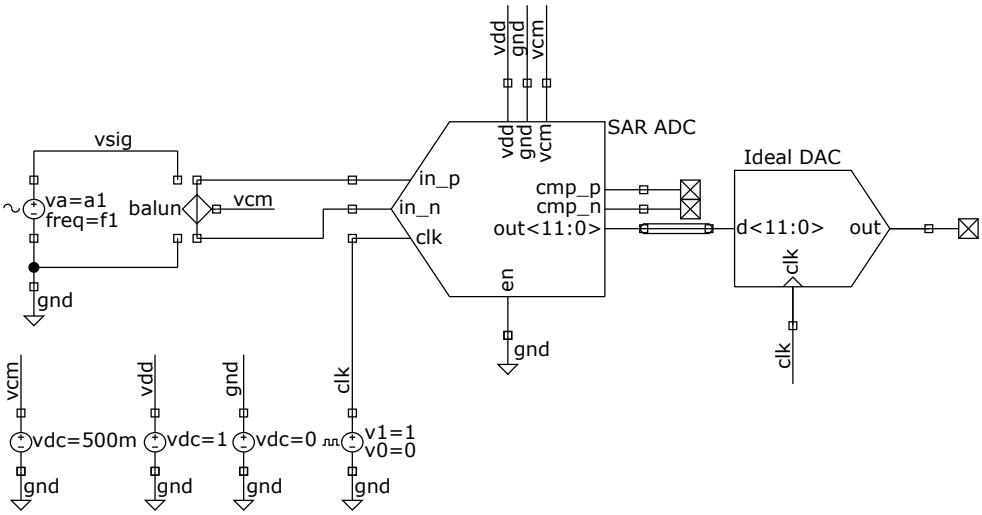


Figure 3.2: Test bench used to verify the SAR ADC performance.

3.1 Capacitive DAC

A differential 12-bit SAR ADC with a switched capacitor DAC, based on the MCS architecture, was implemented using ideal capacitors and switches. The schematic is shown in figure 3.1. This high-level model was used for evaluation of general functionality, measure switching power and to verify the matching requirements of unit capacitors. A corresponding model for the conventional switching method was also created for comparison.

3.1.1 Switching power

Simulations with ideal high-level models of both the MCS based SAR ADC and the conventional one were performed to investigate the power drawn from the reference voltage source. The power was calculated by measuring the current from the voltage source, multiplying this with V_{ref} and taking the average value over a number of signal periods. Both simulations were done with a minimum size unit capacitor of 1.73 fF and a V_{ref} of 1 V. The results are shown in table 5.3a together with the theoretical values from section 2.3.2.

	Calculated [μW]	Simulated [μW]
Conventional	1889	1955
MCS	236	235

Table 3.1: Comparison of theoretical and simulated power consumption due to capacitor charging.

The results in table 3.1 confirm the conclusions made in the the theoretical investigation of the switching methods - the power consumption can be drastically reduced simply by changing the switching procedure.

3.1.2 Requirements on unit capacitance mismatch

The unit capacitance C_u in the DAC is of high importance as it greatly affects the overall ADC performance. To confirm the mismatch requirements calculated in section 2.3.3 the effects on SNDR and ENOB were analyzed by simulations of the high-level model.

Modelling capacitor mismatch in Verilog-A

To study the effects of mismatch, a Verilog-A model of a capacitor with a distribution in capacitance value was created. The spread is modeled as Gaussian function with a specified mean and standard deviation. The Verilog-A source code and Spectre model file can be found in sections B.1 and B.2 respectively. The performance degradation for different levels of unit capacitor mismatch (σ_0/C_0) was investigated; the results of the sweep are shown in figure 3.3.

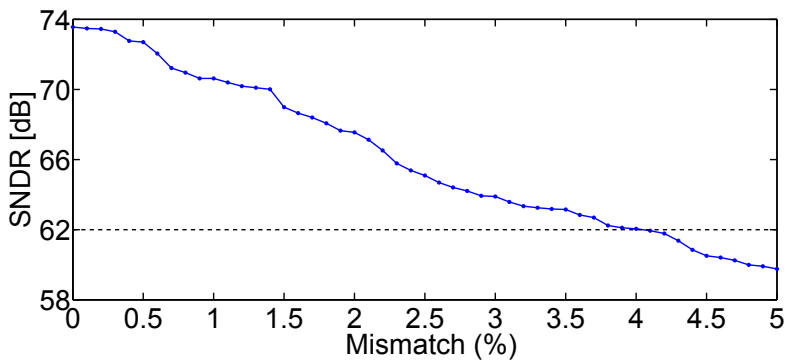


Figure 3.3: Effects of unit capacitor mismatch (σ_0/C_0). The dotted line corresponds to an ENOB equal to 10.

With ideal capacitors SNDR is close to the ideal 74 dB and as the capacitor mismatch increases SNDR starts degrading. The previously calculated SNDR limit of 62 dB, corresponding to an effective resolution of 10 bits, is illustrated as a dotted line in the figure. The plot suggests that a mismatch of 4 % is acceptable, but since the values shown in this figure depend on the random numbers used to generate the capacitor mismatch the resulting SNDR values will vary. A more thorough investigation of the behavior is required to ensure that the previously calculated 2 % limit holds.

Monte Carlo simulation

The effects of mismatch variations can be simulated using the Monte Carlo method. Monte Carlo simulations use pseudo-randomly generated numbers to solve complex numerical problems by repetitive sampling. The parameters for each sample are unique which causes a spread in the results. Figure 3.4 shows the SNDR distribution for a mismatch of 2 %.

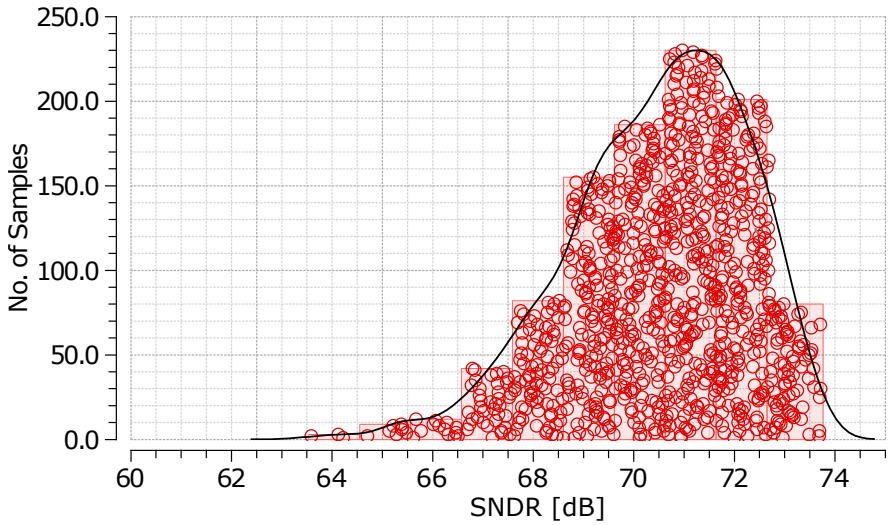


Figure 3.4: SNDR distribution from Monte-Carlo simulation with 1000 samples. The unit capacitor matching was set to 2 %.

The SNDR distribution starts close to the ideal 74 dB, has a peak around 71 dB (11.5 bits) and tail towards lower values. Out of the 1000 samples taken not a single one falls below 62 dB which suggests that the previously calculated capacitor matching requirement is a realistic estimate.

3.1.3 Switch scaling

The switches in the capacitive DAC present a resistance in series with each binary weighted capacitor. The charging time of this RC-network depends on the time constant $\tau_{eq} = R_i C_i$, which should be small compared with the clock period. The switch scaling can be done so that the time constants are equal for each individual branch which allows increasingly larger resistances going from MSB towards LSB. Since a switch with a larger resistance can be made physically smaller, the binary switch scaling results in a reduction of area compared to a design using only low resistance switches. A smaller area is valuable from an economical perspective as the device area is directly associated to the costs of chip fabrication.

The binary-weighted switches help to improve the linearity of the circuit since the settling time is equal for all bits, thereby maintaining a binary weighted ratio between the unit elements. The nonlinear effect of unequal settling is more pronounced in a high speed design, such as the one described here, than in a low speed design where the DAC has more time to settle to the final value. Another benefit of minimizing switch size is that the switch drivers see a smaller capacitive load, which leads to a lower power consumption.

3.2 Comparator

The Verilog-A model presented in appendix B.3 describes the basic functionality of the comparator. The comparison of the two input voltages is done at the specified clock edge and the differential output is either +1 V or -1 V. In this project the parameter *trigger_ edge* is set to -1 in the schematic which makes the comparator trigger on falling clock edges. The model also includes the possibility to add contributions from non-idealities such as noise, offset and a limited regeneration time constant.

3.3 SAR register

The successive approximation algorithm, previously described in section 1.3.3, was implemented in an ideal register sub-block using Verilog-A. The algorithm is sequentially executed in (n+1) states , one state for each of the n bits and an additional state dedicated for sampling. Each state describes the events at a certain clock cycle in the conversion. In contrast to the comparator, the register triggers on rising clock edges. The Verilog-A code of the register can be found in appendix B.4.

At the start of the conversion cycle the bottom plates of all capacitors are connected to the common-mode voltage V_{cm}. The first clock cycle is dedicated to sampling input voltage which is done directly onto the capacitor top plates by closing the sampling switches. The bottom plate and sampling switches are controlled by signals $c\langle i\rangle$ and smp respectively.

In the beginning of each of the following clock cycles the register switches a capacitor from V_{cm} to V_{ref} or ground depending on the output of the comparator.This is controlled by signals $d\langle i\rangle$ and $d\_bar\langle i\rangle$. The rise time of $c\langle i\rangle$, $d\langle i\rangle$ and $d\_bar\langle i\rangle$ is slightly longer than the fall time as a simple method of generating non-overlapping control signals. This is done to prevent two bottom-plate switches being opened at the same time which would cause a short circuit current between V_{ref} and ground.

The timing diagram in figure 3.5 displays an example of the clock- and sampling signal as well as the bit specific control signals in the register. The comparator output was simulated with a 1 V DC source which resulted in all capacitors on one side of the differential DAC being switched from V_{cm} to V_{ref} and all on the other side to ground. One capacitor at a time is reconnected as $c\langle i\rangle$ falls and $d\langle i\rangle$ rises. Figure 3.5 also shows that the control signals are non-overlapping.

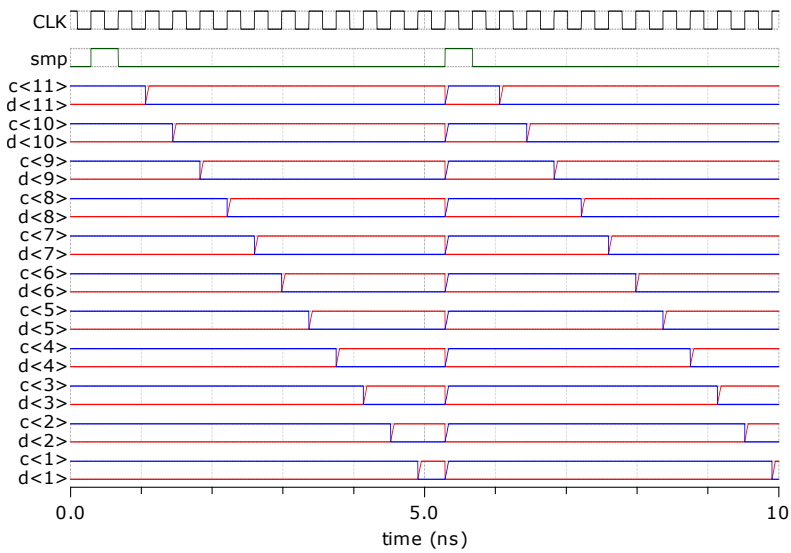


Figure 3.5: Clock-, sampling- and bit specific control signals for a successive approximation register. Inverse control signals $d\_bar\langle i\rangle$ are excluded for simplicity.

The two top-plate voltages gradually converge as shown in figure 3.6 as the binary output word is built in steps going from MSB to LSB. When the LSB has been determined, the output binary word is updated to conclude the conversion cycle. Simultaneously, the register memory is reset and the capacitor bottom plates are once again connected to V_{cm} to prepare for next conversion cycle.

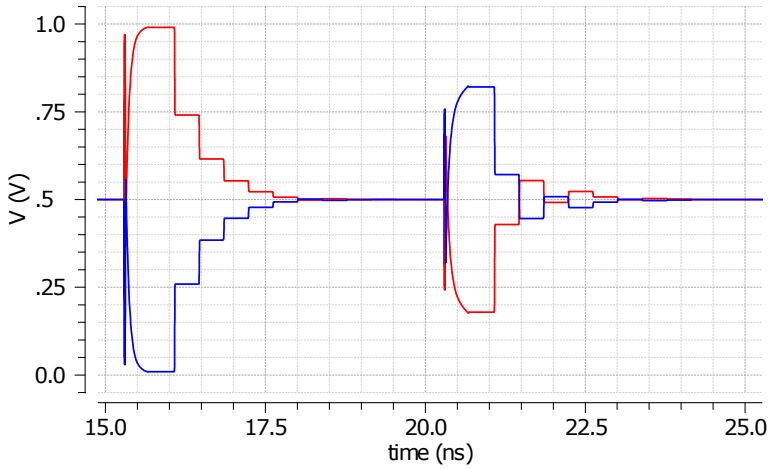


Figure 3.6: A transient simulation of MCS-based high-level model shows how the top-plate voltages gradually converge towards V_{cm} during each conversion cycle.

Chapter 4
Implementation in 28 nm SOI

After the functional high-level model had been created, the different components were implemented using more accurate models. Properties of the unit capacitor were investigated followed by the design of switches and comparator on transistor level. Finally, buffers to drive the switches were included in the design.

4.1 Capacitive DAC

The unit capacitor is important as it affects both the accuracy and power consumption of the DAC. In this section the choice of unit capacitor structure and size is motivated from a mismatch perspective followed by a description of the switches in the DAC.

4.1.1 MOM capacitors

The available PDK contains different types of capacitors. The capacitors models provide the option of simulating with or without mismatch and process variation effects.

In this work the capacitor structure of choice for the DAC is a metal-oxide-metal (MOM) configuration. As the name suggests, the capacitor consists of parallel metal plates separated by oxide. The supplied MOM capacitors are based on a woven structure as seen in figure 4.1.

The advantage of such a layout is the high capacitance density compared to a simple plate capacitor. The woven structure introduces lateral flux between fingers in addition to the vertical flux between layers which contributes to the high capacitor density. The fingers in adjacent metal layers are oriented in different directions to reduce parasitic inductance [12, p. 129].

An alternative to MOM is the metal-insulator-metal (MIM) structure. It is similar in structure with the difference being MIM capacitors having a thinner high-k dielectric separating the metal plates. This makes the MIM capacitors

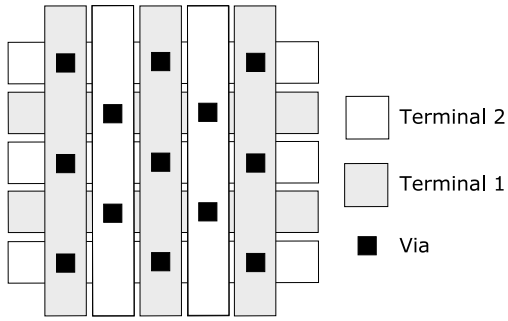


Figure 4.1: Woven capacitor.

more dense in terms of capacitance-per-area. The downside of MIM is the requirement of more advanced fabrication steps. Furthermore, the capacitance can be made smaller using MOM which will prove to be the deciding factor regarding the unit capacitance in this work. The MIM structure can be utilized in places where the capacitors are not to be minimum size in order to save some area.

Effect on using different metal layers in the capacitor

MOM capacitors can easily be realized through the metal interconnections on the chip. Depending on which metal layers being used for top- and bottom-plates the properties of the capacitor vary. An investigation of the effect on mismatch when changing metal layers was performed using Monte Carlo simulations. The finger width and the distance between the fingers were held constant at 100 nm for all simulations. To be able to relate the standard deviations to each other, the mean unit capacitance was held as constant as possible (around 10 fF) by adjusting the number of capacitor fingers. The mismatch σ/C_u for different combinations of capacitor metal layers is presented in table 4.1 along with the corresponding number of fingers in the array.

Bot. \ Top	2	3	4	5
1	0.345%	0.380%	0.412%	0.434%
2		0.345%	0.379%	0.392%
3			0.345%	0.364%
4				0.359%

Table 4.1: Mismatch σ/C_u for different combinations of top and bottom metal layers.

Lower mismatch is achieved using metal layers close to each other. The difference in mismatch is small for the scenarios with metal 1-to-2 and metal

4-to-5, while capacitors made with several metal layers show a larger mismatch per unit capacitance. However, the use of low level metal layers increases the parasitic capacitance due to cross-coupling with the substrate [13, sec 3.2.2]. To minimize the effect of parasitics the top- and bottom-plate are selected as metal 5 and metal 4 respectively.

Selection of unit capacitor size

In general the unit capacitance is selected as small as possible to decrease power dissipation and save chip area. Normally there are restrictions of how small it can be whether it is due to mismatch or limitations in the PDK. As shown in section 2.3.4 the kT/C noise is negligible even for a minimum size unit capacitor. However, the 2 % capacitor matching requirement as calculated in section 2.3.3 must be fulfilled to ensure 10-bit resolution. The unit capacitor mismatch was investigated for different values on C_u and the results are presented in figure 4.2.

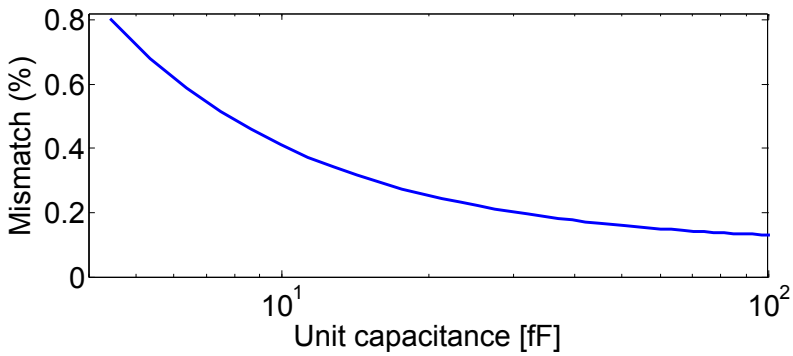


Figure 4.2: Effects of unit capacitor size on the mismatch.

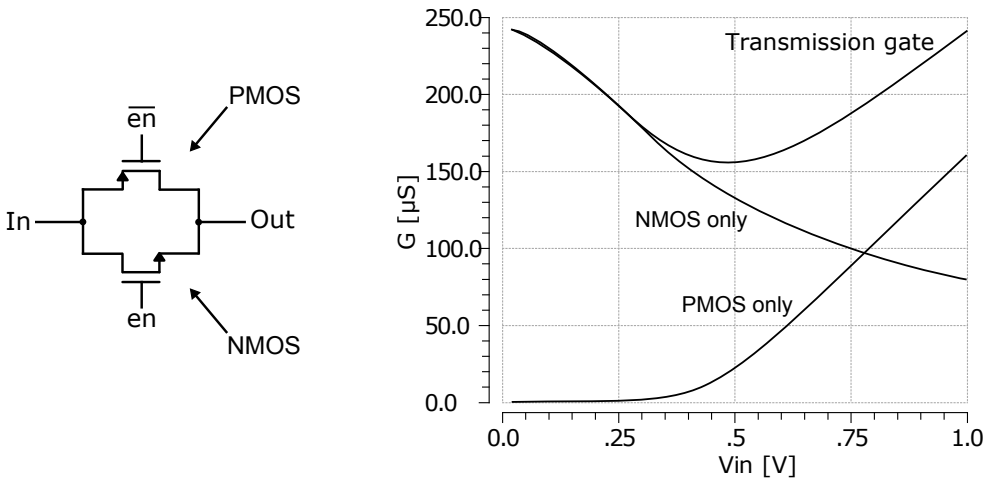
Increasing the size of the unit capacitor seem to have little effect on the mismatch. Even for the smallest capacitor provided by the PDK mismatch does not exceed 2%. C_u was therefore selected as a 1.73 fF MOM capacitor.

4.1.2 Switches

In addition to capacitors, the DAC implements switches for sampling the input and switching the bottom plates between V_{cm}, V_{ref} and ground. This section includes a description of the functionality and design related to the different types of implemented switches.

Transmission gate switches

Transmission gates are used as switches that either conduct or blocks a signal depending on a control signal. They are implemented with one n- and one p-type MOSFET that are connected in parallel, see figure 4.3a. The control signals en and $\overline{en}$ biases the gates in a complementary manner so that both transistors are turned either on or off at the same time.



(a) Schematic **(b)** Conductance versus input voltage

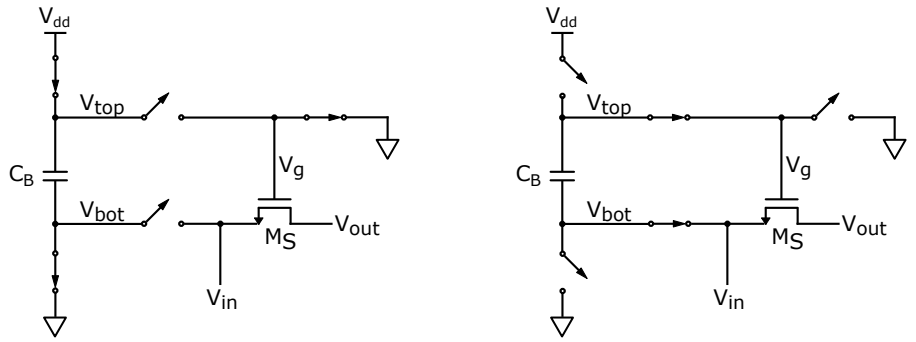
Figure 4.3: Simple transmission gate implementation.

This transmission gate implementation is simple and useful but unfortunately not without issues. The gate overdrive voltage for the transistors depends on input voltage, resulting in a signal dependent conductance [2, p. 236]. This kind of signal-dependent behavior introduces distortion in the sampled voltage which might limit SNDR and the effective number of bits. Figure 4.3b shows an example of transmission gate conductance versus input voltage as well as the contributions from each transistor.

Simulation of the ADC with all switches implemented as transmission gates and with everything else ideal (comparator, capacitors, register etc.) results in an SNDR of 35.2 dB, corresponding to an effective resolution of 5.6 bits. In order to avoid clipping, a lowered signal amplitude of 0.95 V was used for the simulation. As the presented performance is far below the requirements a more linear switch is needed.

Bootstrapped sampling switches

The main source of non-linearity was found to be the input sampling switches. The limited linearity of transmission gates can be overcome by using a bootstrapped switch which holds the gate-to-source voltage of the main switch transistor at a constant level during the on-phase. This improves linearity by providing a constant on-resistance independent of the input signal. There are many variations of bootstrapping implementations and most of them are based on charging a capacitor to V_{dd} during the off-phase and connecting it between gate and source during the on-phase. This bootstrapping concept is illustrated in figure 4.4.



(a) Off-phase **(b)** On-phase

Figure 4.4: Simplified illustration a bootstrapped switch.

Figure 4.5 shows the circuit implementation used in this work. The switch is controlled by the sampling signal *smp* from the SAR register and the two phases of the bootstrapping mechanism can be described as follows:

1. *Off-phase:* when *smp* is low ($\overline{smp}$ high) transistor M_2 is turned on, connecting the bottom plate of the capacitor C_B to ground. The node V_g is grounded through M_5 and M_6 which enables charging of C_B to V_{dd} through transistor M_1. The switch transistor M_S is turned off and separated from the capacitor by the turned-off transistors M_3 and M_4.

2. *On-phase:* when *smp* is high both M_2 and M_6 are turned off by the low voltage $\overline{smp}$ signal. The gate of M_3 is connected to the bottom of C_B causing a gate-to-source voltage close to $-V_{dd}$ turning the PMOS transistor on and thereby connecting the gate node V_g to the top plate of C_B. The voltage stored on the capacitor during the off-phase is therefore applied between the gate and source nodes of the switch transistor.

Figure 4.6 shows the node voltages of one of the bootstrapped sampling switches. During the sampling phase the gate voltage is fixed at a level ap-

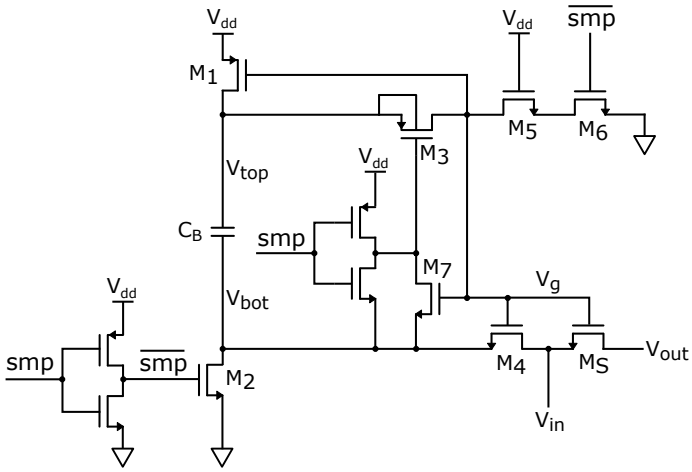


Figure 4.5: Bootstrapped switch implementation.

proximately $V_{dd} = 1\text{V}$ higher than the input which provides good linearity and low resistance. The ability to generate gate voltages V_g exceeding the supply voltage is required for a full-scale input range from ground to V_{dd}. Since the output node of the switch is connected to the top plates of the capacitive network the input voltage is sampled when the switch turns off.

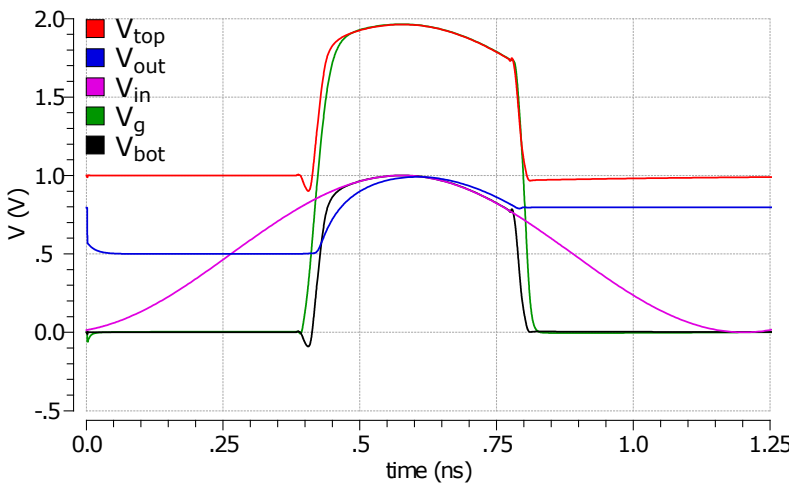


Figure 4.6: Node voltages in a bootstrapped sampling switch during sampling.

When designing the bootstrapped switch the most critical transistor is the main switch M_S which has to be large enough to ensure low resistance but not too large considering power dissipation and charge-injection effects. The width

of M_S was chosen to 50 μm after tests with an ideal switch model similar to that shown in figure 4.4. The remaining transistors were then scaled for a low enough resistance but as small as possible to reduce the parasitic capacitance on the gate node V_g. The bootstrapping capacitor C_B must be large enough to provide charge for M_S as well as M_1, M_4 and M_7 and also to allow some leakage before M_1 is fully turned off. In this work C_B was chosen to be 2 pF.

Replacing the transmission gates at the top plate with bootstrapped switches gives an SNDR of 65.05 (10.51 bits) which is a clear improvement from 35.2 dB, but there is still a loss of around one and a half bits in resolution compared to an ideal 12-bit ADC.

The remaining distortion from the switches may be due to non-linear bulk effects. The threshold voltage of the transistors depend on the bulk-to-source voltage which is signal dependent since the substrate is at a fixed voltage. More complex methods for bulk-effect compensation are available but for this project the more basic implementation was sufficient.

4.1.3 Switch buffers

Simulations up to this point have been done with the ideal Verilog-A register directly driving the switches. In a real circuit buffers are often placed between the digital logic and the switches. The buffers can be implemented by two inverters in series, where the SAR is connected to the first one and the second drives the switches. Buffers were included in the transmission gate cells to generate the required gate voltages. The inverted control signal $\overline{en}$ driving the PMOS transistor was extracted from the node between the two inverters. Early simulations with a buffered, fully binary-scaled switch network showed a power of almost 3 mW to drive the transmission gate switches in the DAC. To reduce this value the switch scaling had to be adjusted.

4.1.4 Down-sizing of switches

In the original design each unit capacitor had a corresponding bottom-plate switch, each consisting of three transmission gates to V_{cm}, V_{ref} and ground. The down-sizing was done by increasing the number of capacitors with a single switch. At the same time the number of switches for the largest capacitor was reduced from 1024 to 128, leaving the switches of the largest capacitors binary scaled. Figure 4.7 shows the number of switches for each capacitor. The switch reduction reduced the total power consumption of switches and buffers to around 500 μW without degrading performance.

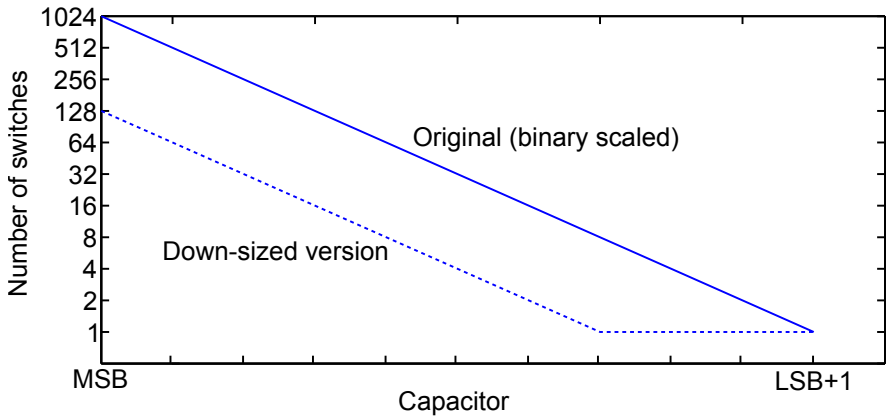


Figure 4.7: Switch scaling for binary and down-sized array.

4.2 Comparator

As mentioned in section 1.5 the latched comparator is a popular approach in ADCs. The latched comparator provides dynamic operation which means that it only draws a current when making the decision making it very power efficient. In a design where kick-back is a true problem, an isolating linear stage is needed between the comparator and the capacitive DAC. Figure 4.8 shows a block diagram of the entire comparator. The clock signal is inverted before reaching the latch to make the latch trigger on falling clock edges. This allows the capacitive DAC to settle for half a clock cycle before the comparison is made. The output nodes are separated from the SR-latch using two buffers.

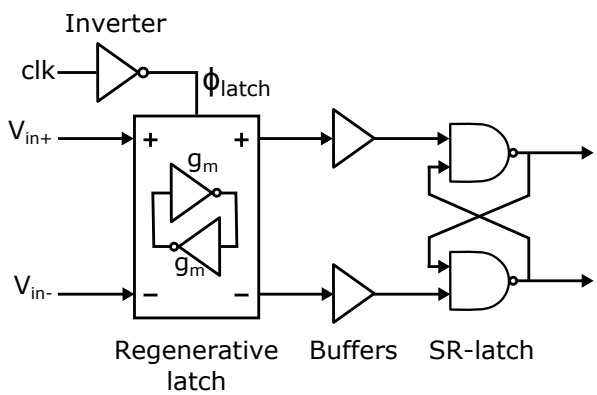


Figure 4.8: Block diagram of the comparator used in this project.

4.2.1 Single-stage latch

Figure 4.9 shows the schematic of a single-stage regenerative latch used in this project. The signal ϕ_{latch} controls both the reset transistors connected to V_{ref} and the current source in the bottom of the schematic. The reset transistors connect the output nodes and as well as other internal nodes to V_{dd} between comparisons to prevent hysteresis, which is when the result of a comparison depends on the previous one. Since both sides of the differential comparator are pre-charged equally the circuit is not biased in either way, i.e. any memory from previous clock cycles stored on the capacitance on those nodes is reset before a new comparison is being made.

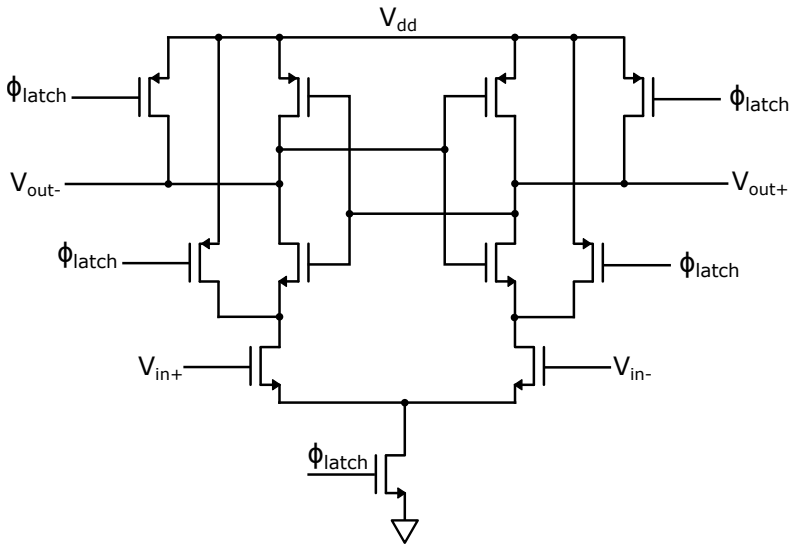


Figure 4.9: Single-stage latch implementation.

Figure 4.10 shows the mechanism of the single-stage latch. At the rising edge of ϕ_{latch} the reset transistors are turned off and the current source transistor is turned on. Current starts flowing through the latch and the differential input voltage determines which output voltage falls the fastest. The cross-coupled inverters create a positive feedback loop making the circuit unstable which eventually causes one of the output nodes to lock to V_{dd} and the other to ground. When the decision has been made no more current flows through the device. The output voltages are buffered before reaching the SR-latch which in turn holds the value for an entire clock cycle.

A transient simulation without noise was done for an ADC with the latched comparator and all other components ideal results in a SNDR of 68.2 dB. The loss of almost one bit in resolution suggests there is a significant amount of non-linear effects in the comparator. The main reason for the performance

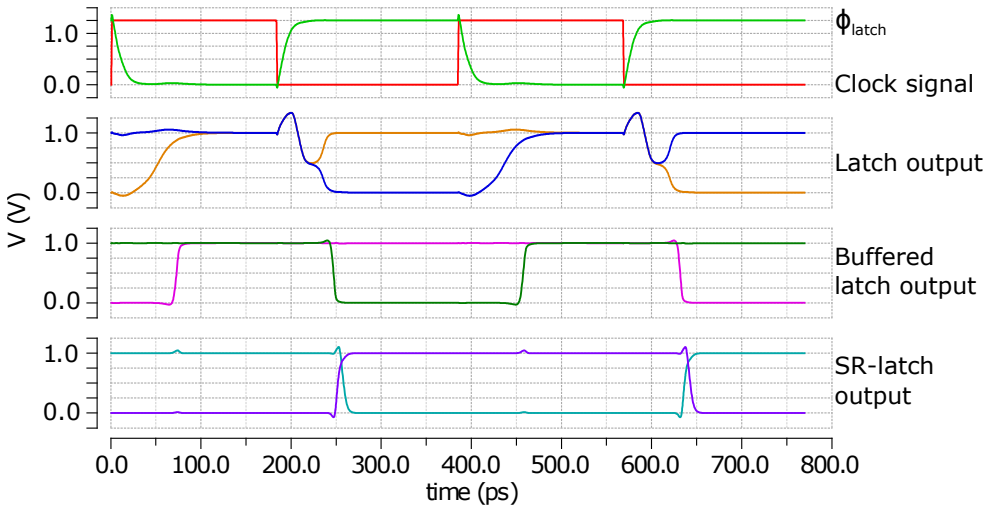


Figure 4.10: Transient analysis of the single-stage latched comparator for an alternating input signal of $\pm 100\,\mu$V.

degradation is most likely the kickback, which causes large voltage variations at the input of the comparator. By using equation (1.4) and neglecting kT/C and jitter noise since both switches and clock generator are ideal the distortion power was calculated to $P_{distortion} = 5.58 \cdot 10^{-8}$ V^2. Adding noise to the transient simulation decreases the SNDR to 64.0 dB, corresponding to an addition of noise with power $1.23 \cdot 10^{-7}$ V^2. The maximum noise frequency in the simulation was chosen as 130 GHz, corresponding to 50 times the maximum frequency f_{clk}. The lowest noise frequency was 5 MHz to fit a few periods within the simulation time of 1.34 μs. The power consumption of the entire comparator was 230 μW. From the results shown above, it is clear that a more linear and less noisy comparator is needed.

4.2.2 Two-stage latch

To reduce kick-back effects a two-stage latch similar to that in [14] and [15] was implemented. The circuit, which is presented in figure 4.11, separates the input pair from the output nodes by a couple of inverters. In this way there is no longer direct coupling between the gates of the input transistor pair and the output nodes which significantly reduces signal dependent disturbances of the top-plate voltages. The first stage can be seen as a dynamic pre-amplifier which only consumes power around the transitions of ϕ_{latch}.

A simulation without noise results in an SNDR of 71.1 dB which shows that the two-stage latch reduces signal distortion at the expense of increased power consumption (377 μW). The calculated distortion power was reduced

to $P_{distortion} = 1.89 \cdot 10^{-8}$ V^2. Adding noise resulted in a SNDR of 68.5 dB, corresponding to a noise power of $3.12 \cdot 10^{-8}$ V^2.

The real advantage with an improved latch is for higher resolution architectures where the noise must be reduced further. Since noise is inversely proportional to the size of the transistors and the current through them one way to reduce the noise is to scale up the input stage of the latch. With the previously shown single-stage latch without a pre-amp a larger input pair increases the effects of kick-back charges. However, the two-stage latch design can be enlarged to reduce noise without severely affecting distortion. Simulations show that a larger version of the two-stage latch show that SNDR>70 dB is possible at the cost of increasing the power consumption to around 1 mW. From a power efficiency perspective a reduction of noise is not worth the increase in power, since the SNDR is limited by the linearity of the switches.

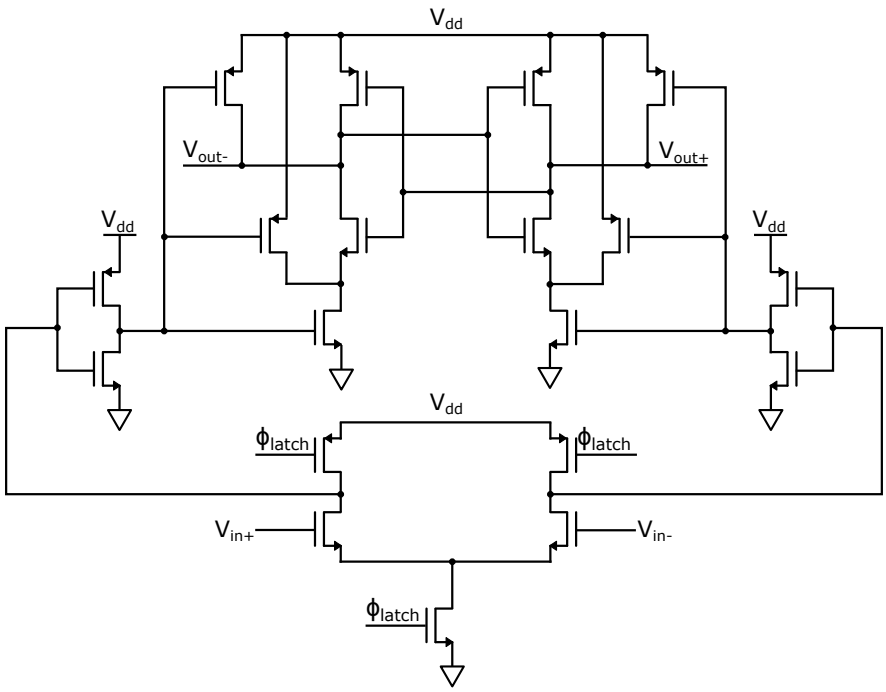


Figure 4.11: Two-stage latch implementation.

4.3 Full ADC implementation

In this report the design process of a 12-bit SAR ADC have been presented. The design choices and sub-blocks of the final implementation are summarized below:

- A fully differential architecture is implemented bringing benefits such as common-mode rejection, larger input range and suppressed distortion at the expense of higher power consumption.
- The MCS technique reduces the DAC power dissipation by using a more efficient switching procedure.
- An unit capacitance of 1.73 fF is used for low power.
- The DAC switches are implemented as CMOS transmission gates in all places, with the exception of the sampling switches which are boot-strapped in order to minimize signal-dependent behavior. Power related to the DAC is reduced by down-sizing the binary scaling of the switches.
- Functionality of the register is described using a Verilog-A block and further implementation of the digital logic is not included in this project.
- A power-efficient dynamic comparator without a pre-amplifier stage is used. The comparator implements a two-stage architecture in order to reject kick-back .

Chapter 5

Verification of the design

In this chapter the performance and robustness of the ADC implementation are examined. The ADC was simulated with the same input signal (800 MHz sine wave) and test bench as in previous chapters. The simulated performance is related to the specification and compared to state-of-the-art ADCs. An estimation of the area distribution is also performed.

5.1 Resolution

The resulting FFT spectrum of the SAR ADC output signal can be seen in figure 5.1. The calculated dynamic performance metrics at f_{in}=800 MHz are SNDR=64.8 dB, equivalent to ENOB=10.5, and SFDR=75.3 dB.

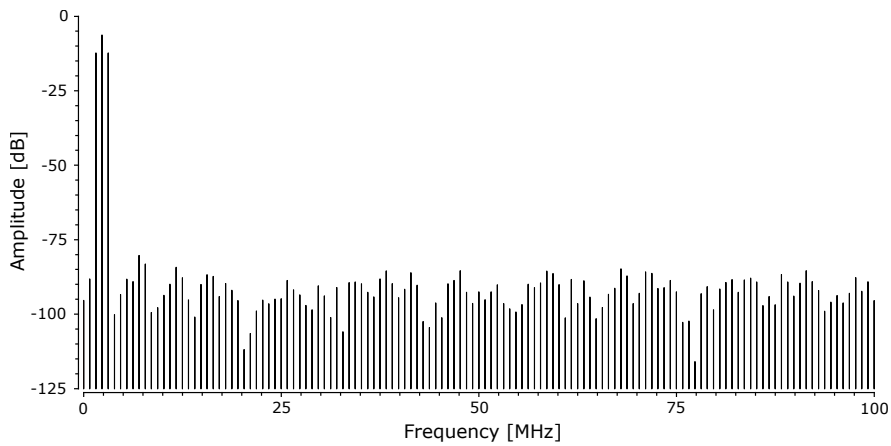


Figure 5.1: Simulated spectrum data at 200 MSps with 800 MHz input sine wave.

5.2 Monte Carlo simulation

A Monte Carlo analysis with 500 samples was performed to investigate the effects of component mismatch due to local variations. The resulting SNDR distribution is shown in figure 5.2. In order to reduce simulation time, the simulations did not include transient noise. It is expected that the amount of noise added in a transient noise analysis is more or less constant which means that the effects of noise simply can be "added" to the results if desired.

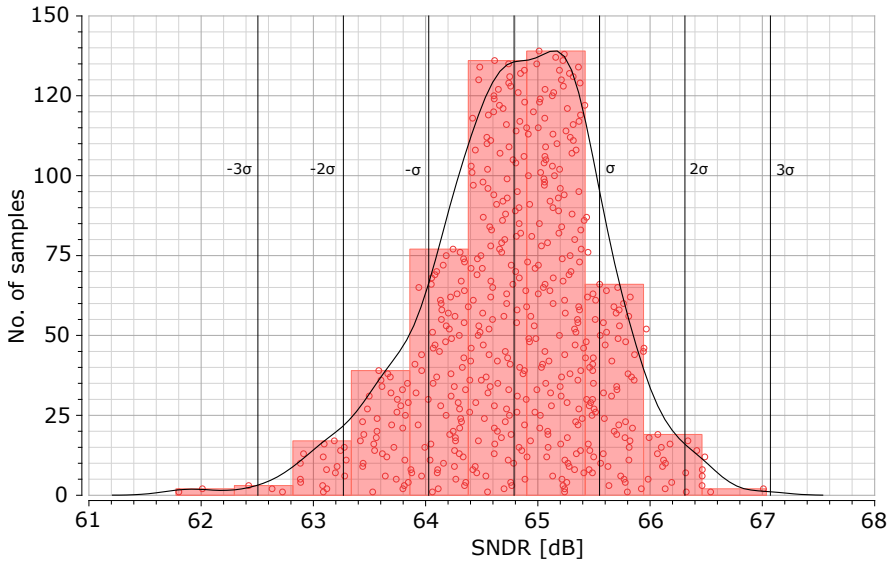


Figure 5.2: Monte Carlo simulations of SNDR with 500 samples.

According to equation (1.4) an SNDR equal to 62 dB corresponds to a total noise and distortion power of $3.15 \cdot 10^{-7}$ V^2, assuming a full-scale input signal. As shown in previous chapters the dominant noise source is the comparator. Allocating $3.12 \cdot 10^{-8}$ V^2 to comparator noise (see section 4.2.2) results in a distortion budget of $2.84 \cdot 10^{-7}$ V^2, corresponding to SNDR = 62.5 dB. Since 3 of the 500 samples from the Monte Carlo analysis are below this value, the yield with added noise was estimated to 99.4 %. Additional effects such as jitter noise would further reduce the yield, but in this project these effects were not investigated further.

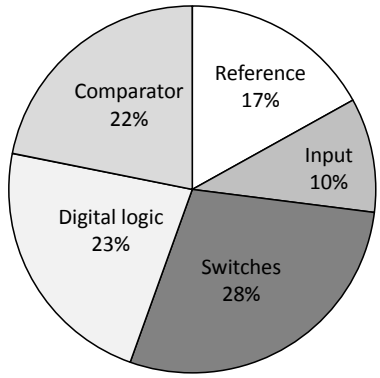
5.3 Power consumption

The power consumption of the design was estimated by measuring the currents from respective voltage source during normal operation. The calculated average power P_{AVG} for different blocks is presented in figure 5.3a.

	P_{AVG} [μW]
Switches	503
Digital logic	400 *
Comparator	386
Reference	299
Input	178
Total	**1766**

*Estimated

(a) Average power.



(b) Distribution of power.

Figure 5.3: Power dissipation in the SAR ADC.

Since the digital logic was not implemented in this project its power contribution had to be estimated. [8] reports a digital power of 1.7 mW for a MCS-based 10-bit 100 MSps SAR ADC fabricated in 90 nm CMOS technology. The digital power associated with the repeated charging of transistor gates is proportional to both the capacitance, which relates to transistor area, and the frequency [16]. The digital power for a 28 nm process was estimated to 400 μW by compensating for the differences in resolution, sampling frequency and technology node as shown in equation (5.1). This value is in line with similar work done at the department, and is therefore assumed to be a realistic estimate.

$$P_{\text{digital}} \approx 1.7 \text{ mW} \cdot \left(\frac{12}{10}\right)\left(\frac{200 \text{ MSps}}{100 \text{ MSps}}\right)\left(\frac{28 \text{ nm}}{90 \text{ nm}}\right)^2 \approx 400\,\mu\text{W} \tag{5.1}$$

With the digital logic included the total power of the design equals 1.77 mW. Figure 5.3b displays the distribution of power in the design.

5.4 Robustness

In previous sections the performance has been verified for the operating point the ADC was designed for. Real data converters need to be robust, meaning that they are able to withstand some variations in the operating conditions. This section describes this additional testing of the design.

5.4.1 Temperature

The effect of extreme temperatures on the SAR ADC performance was investigated. Simulated SNDR for -20°C, room temperature and 100°C are listed

in table 5.1. The performance is degraded as the temperature increases, partly because of the increase in kT/C noise and partly because of increased switch resistance.

Temperature [°C]	SNDR [dB]
-20	66
27	64.8
100	62.9

Table 5.1: SNDR for low and high temperatures.

5.4.2 Supply voltage

The sensitivity to variations in supply voltage was also investigated, see table 5.2. As the conductance of transistors depends on the voltage driving them the performance is degraded as V_{dd} is reduced. Similarly, the performance is improved for an increased supply voltage.

V_{dd} [V]	SNDR [dB]
0.9	60.9
1.0	64.8
1.1	66.5

Table 5.2: Effects of V_{dd} variations on performance.

5.4.3 Common-mode voltage

V_{cm} was changed from its ideal value of $1/2 V_{ref} = 0.5$ V. This makes "up" and "down" transitions unequal causing the two top-plate voltages to converge toward a another value than 0.5 V. In an ideal SAR ADC this is not an issue since the differential architecture rejects the V_{cm} change, leaving the differential output voltage unaffected. However, converging toward another voltage can affect the performance of the comparator. A V_{cm} closer to V_{ref} makes "up" transitions smaller than "down" transitions in the DAC, causing both top-plate voltages to move towards a lower value. Since these voltages directly drive the input pair of the comparator the decision time increases, potentially causing an incorrect decision. Figure 5.4 shows how the reduction of the top-plate voltages causes a comparison error. The resulting performance for different values of V_{cm} is presented in table 5.3.

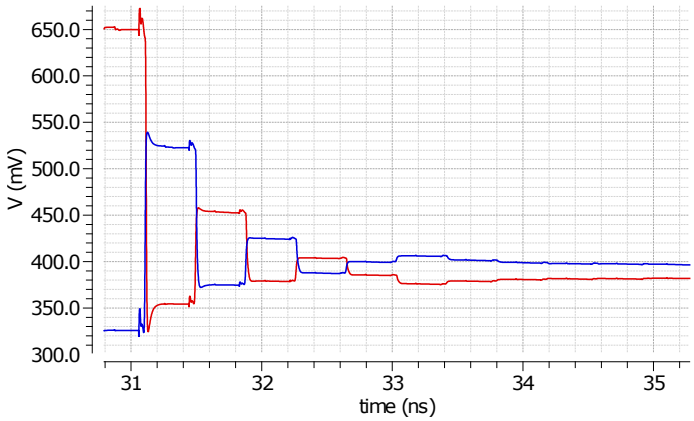


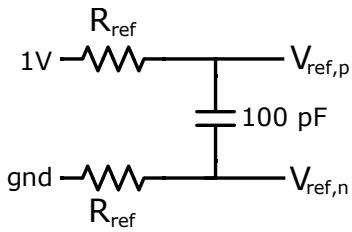
Figure 5.4: A transient simulation with $V_{cm} = 0.6$ V shows how the top-plate voltages converge towards 0.4 V instead of the 0.5 V. The comparator makes an error for one of the intermediate bits causing the voltages to separate in the next clock cycle.

V_{cm} [V]	SNDR [dB]
0.40	65.1
0.50	64.8
0.55	66.3
0.60	38.8

Table 5.3: Effects of V_{cm} variations on performance.

5.4.4 Reference voltage

The effect of including non-ideal reference voltages $V_{ref,p}$ and $V_{ref,n}$ was examined. Figure 5.5a show the circuit which serve to limit the amount of current that can be drawn from the ideal voltage sources. Simulations with different values on the reference resistance R_{ref} are displayed in figure 5.5b. Already for low R_{ref} values a degradation in SNDR can be observed.



(a) Circuit for simulating a non-ideal reference voltage.

$R_{ref}[\Omega]$	SNDR [dB]
1	65.1
5	62.1
10	58.1

(b) SNDR for different values on the reference resistance.

Figure 5.5: Simulating a non-ideal reference voltage.

5.4.5 Source impedance

To test the requirements on the source impedance, resistors were put in series with the input pins. Increasing the resistance caused some signal attenuation, decreasing SNDR slightly.

$R_{in}[\Omega]$	SNDR [dB]
0	64.8
10	64.7
100	62.5

Table 5.4: Effects of source impedance on performance.

5.4.6 Sampling frequency

The presented SAR ADC was designed to operate at a sampling frequency f_s of 200 MSps which corresponds to the internal clock working at 2.6 GHz. This high frequency gives a very short time for the DAC to settle and comparator to make a decision. A good measure of design robustness is the ability to operate at higher frequencies. The performance for different values on f_s is presented in figure 5.6.

SNDR is relatively constant for low frequencies and does not fall off until around 300 MHz where the time for the comparator to make a decision starts

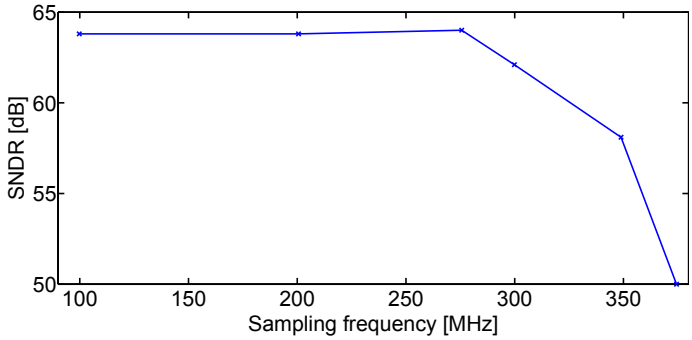


Figure 5.6: SNDR versus sampling frequency.

becoming to short. For even higher sampling rates more and more incorrect decisions are made and the performance continues to drop.

5.4.7 Process corners

Circuits implementing MOS transistors may run faster or slower depending on variations in the fabrication process. Process corners represent the extremes of these variations. A commonly used convention for naming process corners is to denote the mobility of NMOS and PMOS transistors respectively. The mobility can be either higher (fast corner) or lower (slow corner) than the nominal case (typical corner). The results of simulating the fast-fast and slow-slow corners can be seen in table 5.5 representing the scenarios where both NMOS and PMOS are fast or slow. The presented data does not show any significant variations in performance.

Process corner	SNDR [dB]
fast-fast	64.7
typical-typical	64.8
slow-slow	65.1

Table 5.5: Simulated SNDR for different process corners.

5.5 Input signal variations

5.5.1 Amplitude

The response to variation of the input signal amplitude is presented in figure 5.7. The amplitude sweep ranges from 1 mV to 1.1 V with SNDR peaking close to full-scale. For amplitudes above full-scale, SNDR can be seen to drop

drastically. This is due to clipping distortion in internal node(s). It is also seen that the SNDR increases by 1 dB/dB of input amplitude as expected, since the noise level is roughly constant as the signal varies.

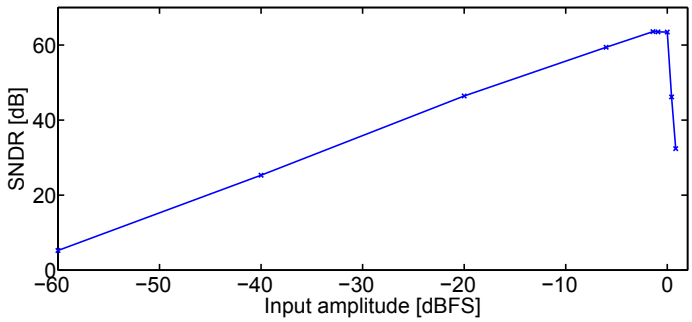


Figure 5.7: SNDR versus the input amplitude expressed in decibels relative to full-scale.

5.5.2 Frequency

The performance for input frequencies other than the operating point were simulated as seen in figure 5.8. To avoid clipping of the output signal, the input amplitude was decreased slightly from full-scale (1 V) to 0.95 V. The simulation shows that SNDR is degraded with increasing input frequency. As the frequency increases, it gets more difficult for the top-plate voltages to follow the quickly changing input signal during the sampling phase.

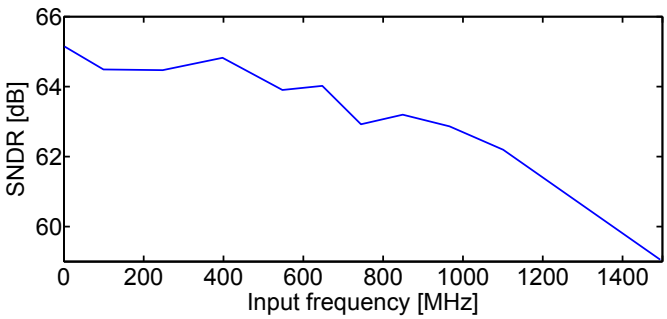


Figure 5.8: SNDR versus input frequency.

5.6 Circuit area

After a circuit has been implemented and the performance is tested, the next step in the design process is to make a layout of the design. In a layout the

components are represented by two-dimensional geometric shapes which correspond to the metal, oxide and semiconductor layers that make a real circuit. The creation of a layout is a crucial step in the design process as it introduces new limitations related to the fabrication. As the scope of this project reaches as far as verification of pre-layout performance this step was not included in the design work. However, a rough estimation of the different blocks was made to illustrate the area distribution by generating a simple layout from the schematics using the standard cells for transistors and capacitors provided by the PDK. The resulting total area was 0.03 mm^2 with the distribution as seen in figure 5.9.

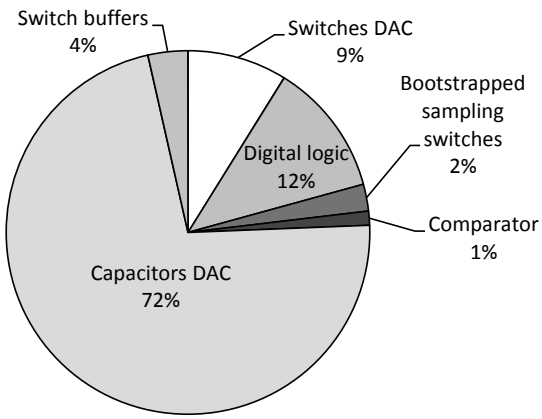


Figure 5.9: Estimated area distribution of the SAR ADC.

The biggest contributor is the capacitors in the DAC which takes 72 % of the total area. One straightforward way of reducing this area is to decrease the size of unit capacitors by creating a custom layout. The switches occupy 13 % of the total area. Estimation of the digital logic area was made from a literature study of similar work. The SAR ADC in [17] presents a comparable digital block which therefore can serve as an rough estimate on the logic area in this work. The presented data suggest that the digital logic would take up 12 % of the area.

5.7 Comparison with state-of-the-art ADCs

To evaluate how well the design compares to state-of-the-art ADCs, it was simulated with an input signal at the Nyquist frequency f_{ny}=100 MHz which is the standard for calculating FOMs in the previously mentioned survey [3]. The resulting SNDR equals 69.5 dB and the total power consumption was

1.9 mW. FOM_S was calculated to 176.6 dB at $f_{s,ny}$=200 MHz, see figure 5.10.

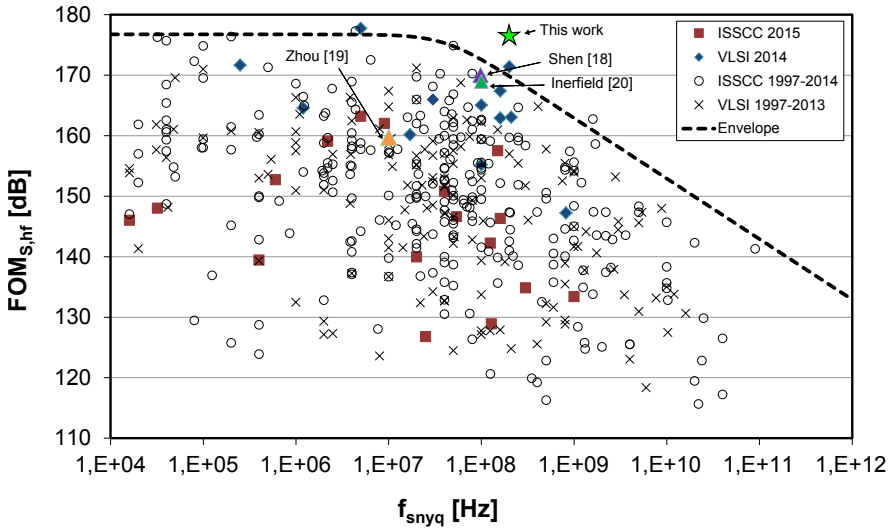


Figure 5.10: Simulated data for the designed SAR ADC in comparison with state-of-the-art ADCs.

The simulated performance of the designed ADC is summarized and compared to other similar SAR ADCs in table 5.6. I should be noted that the converters used for comparison present measured data while this work present simulated data.

	Shen [18]	Zhou [19]	Inerfield [20]	This work
Architecture	Pipelined SAR	Pipelined SAR	SAR	SAR
Technology	65 nm bulk	40 nm bulk	28 nm bulk	28 nm FDSOI
Resolution (bits)	12	12	15	12
Sample rate (MS/s)	100	160	100	200
Input freq. (MHz)	49.1	5	50	100
SNDR (dB)	69.4	66.7	67.1	69.5
Power (mW)	8.6	5.0	8.0	1.9
FOM_S (dB)	170.0	159.7	169.0	176.6
Area (mm^2)	N/A	0.04	0.10	0.03 *

Table 5.6: Performance summary and comparison. (* Estimated)

Chapter 6
Discussion

The **simulation** time could be reduced from a couple of hours to a few minutes by replacing all but the component of interest by ideal high-level models. The final design included a majority of effects present in a real circuit. Some details not included in the models were jitter noise and additional parasitics extracted from a layout.

In order to increase the yield and have a larger margin for additional effects degrading performance the **matching** could be improved by using a slightly larger C_u. The mismatch $\frac{\sigma_0}{C_0}$ is reduced to approximately 1 % by increasing the width and spacing of capacitor fingers, resulting in a C_u of 2 fF. Another approach for reducing the effects of capacitor mismatch is using some form of calibration or digital error correction.

Simulations with implemented switches and ideal comparator gave an SNDR equal around 65 dB and with the latched comparator and ideal switches the SNDR exceeded 68 dB. **The limiting factor** in the final design is therefore the switch linearity. Since the distortion introduced by switches dominates not much can be gained from improving other components, e.g. reducing comparator noise. This would only increase the total power without significantly improving performance.

In contrast to the sources of noise and distortion, the **power consumption** within the ADC (switches, comparator, digital logic, capacitor switching) is approximately evenly distributed. This means that a large reduction of power is difficult since several parts of the design have to be improved. The switches are already limiting dynamic performance and can therefore not be scaled down further. The switching power depends on the size of C_u which cannot be decreased since capacitor matching must be maintained. Disregarding the digital logic not implemented the best strategy for reducing power is by altering the comparator design. As switches are the limiting factor it is possible to trade a slight noise increase for a reduction in power without a large effect on performance.

The **MCS technique** proved to be a good alternative to conventional SAR

technology. The main advantages are the reductions in both switching power and area. Another benefit is that the input voltage is sampled directly onto the two top-plate nodes, requiring only two bootstrapped switches instead of one for each capacitor. There are many alternative methods for decreasing power. Articles about other switching procedures found in literature claim reduction of switching power with more than 90 % compared to the conventional method. However, many of them require more complicated logic or an increased number of switches, making them less practical to implement compared to the relatively simple method used in this project. Another common way to reduce power is to split the capacitive array into two or more binary-scaled sections separated by attenuation capacitor in series [2, p.184]. This decreases the total number of unit capacitors but the matching requirement of the attenuation capacitors is highly critical for DAC linearity.

The requirements on the **reference voltage** are strict because of the large capacitance that has to be charged. The resistance of the reference net is most critical for the largest capacitors as a larger amount of current has to be supplied. The MCS-based architecture is less demanding compared to a conventional SAR ADC due to the more efficient switching method. Another advantage is that the largest capacitance in the binary-scaled array is only half as large, assuming kT/C noise is not a limiting factor. The reduced current from V_{ref} leads to less voltage ripple on the reference voltage. Thus, MCS can tolerate a higher resistance on V_{ref} than the conventional SAR ADC.

Simulations show that the **sampling frequency** could be increased to around 300 MSps, which is a sign of a reliable design. For the ADC to work the DAC has to be fast enough to settle before the comparator makes the decision. The comparator must also be fast enough to make a decision before the register is updated. Since the time allocated for each of them depends on the sampling frequency the preserved functionality at 50 % higher sampling frequency suggests that there is a sufficient margin at normal operating conditions.

The implementation of the register did not fit in the scope of this project as the work was focused on core aspects (DAC, comparator) of the ADC. **Future work** includes designing this digital block. Additional non-idealities such as wire parasitics can be included in the simulations by creating a layout of the design.

Future work could also include improved versions of the switches and comparator. A large performance improvement could be gained by using a more sophisticated bootstrap implementation, for example with compensation of bulk effects. Improving the comparator design to reduce V_{cm} sensitivity is also of interest.

Chapter 7
Conclusion

A 12-bit 200 MSps successive approximation register analog-to-digital converter was successfully implemented. Pre-layout simulations show that the design dissipates 1.8 mW achieving an SNDR of 64.8 dB for a 800 MHz input signal, fulfilling the requirements on an effective resolution of 10 bits. With an input signal at the Nyquist frequency the design achieves an SNDR of 69.5 dB while dissipating 1.9 mW. Schreiers figure of merit is calculated to 176.6 dB at the Nyquist frequency, which is comparable with state-of-the-art ADC considering the presented data are simulated values.

The merged capacitor switching procedure used proved to be a power-efficient alternative to the conventional method. MCS reduces the number of unit capacitors by half and simulations show that the switching power is drastically reduced. This motivates MCS as a promising alternative for future ADC implementations.

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Appendix A

List of acronyms

ADC Analog-to-digital converter

BW Bandwidth

CMOS Complementary metal-oxide-semiconductor

DAC Digital-to-analog converter

ENOB Effective number of bits

FOM Figure-of-merit

FFT Fast Fourier transform

INL Integral non-linearity

LSB Least significant bit

MCS Merged capacitor switching

MIM Metal-insulator-metal

MOM Metal-oxide-metal

MOSFET Metal-oxide-semiconductor field-effect transistor

MSB Most significant bit

MSps Megasamples per second

NMOS N-type metal-oxide-semiconductor

PMOS P-type metal-oxide-semiconductor

PDK Process design kit

PVT Process, Voltage, Temperature

S&H Sample-and-hold

SAR Successive approximation register

SFDR Spurious-free dynamic range

SINAD Signal-to-noise and distortion ratio. See also **SNDR**

SNDR Signal-to-noise and distortion ratio. See also **SINAD**

SNR Signal-to-noise ratio

SR Set-reset

Appendix B
Source code

B.1 Verilog-A model of capacitor with mismatch

```
// VerilogA for xjob_models, cap_spread, veriloga
// Normally distributed capacitance with specified standard
    deviation 'sigma'

`include "constants.vams"
`include "disciplines.vams"

module cap_Gauss(p,n);
  parameter real Cu = 0;
  parameter integer multiplier = 1;
  parameter real mismatch = 0; // Relative unit cap mismatch [%]
  (*cds_inherited_parameter*)parameter real random = 0;
  real sigma, C;
  inout p, n;
  electrical p, n;

  analog begin

    @(initial_step) begin
      sigma = sqrt(multiplier)*Cu*mismatch;
      C = multiplier*Cu + sigma*random; // Gaussian distribution
      $strobe("Cu = %g, multiplier = %g, mismatch = %g, random = %
    g, sigma = %g, C = %g",Cu, multiplier ,mismatch ,random ,sigma ,C);
    end

    I(p,n) <+ C*ddt(V(p,n));

  end

endmodule
```

B.2 Spectre model file for the capacitor model

```
simulator lang=spectre
parameters random=0
statistics {
  mismatch {
    vary random dist=gauss std=1
  }
}
```

B.3 Verilog-A model of comparator

```
// Comparator
// Models gaussian noise and comparator offset.
//
// Note:
// Latch regeneration time becomes a signal dependent delay if
    parameter latch_tau is specified, otherwise td is used as a
    constant latch delay.


`include "constants.vams"
`include "disciplines.vams"

`define clk_per 4e-9    // Clock period. Used to display warning
    error of regeneration time becomes too large.

module comparator(din_p, din_m, dout_p, dout_m, clk, vdd, vss,
    nbulk, pbulk);
input din_p, din_m, clk;
output dout_p, dout_m;
inout vdd, vss, nbulk, pbulk;
electrical din_p, din_m, dout_p, dout_m, clk, vdd, vss, nbulk,
    pbulk;

parameter real td = 25p;
parameter real tt = 50p;
parameter real vth = 0.5;
parameter real vhigh = 1.0;
parameter integer trigger_edge = 1; // +1=rising edge, -1=falling
    edge
parameter real vos = 0;          // Offset voltage [V]
parameter real noise_rms = 0;    // Input noise voltage rms (std
    dev) [V]
parameter real latch_tau = 0;      // Time constant for
    regenerative latch [s] (~gm/Cload). Disabled if zero.
parameter real latch_v = 10e-3;   // Desired latch output voltage
    [V]. Required to calculate latch time.
// Assume that 10mV output from latch is sufficient for preceding
    circuits to amplify into rail-to-rail and detect a 0/1.
```

```
real xp, xn, vnoise, vsig, rtime;
// xp, xn internal variables for output state.
// vnoise internal variable for output Gaussian noise.
// vsig internal variable for differential input signal + noise +
    offset.
// rtime regeneration time of latch.

integer seed;

analog begin

  @(initial_step) begin
     xp=0;
     xn=0;

  end // initial

  @(cross(V(clk)-vth, trigger_edge)) begin
   vnoise = noise_rms*$rdist_normal(1, 0, 1); // Gaussian noise
   vsig = V(din_p,din_m) + vnoise + vos; // Add noise and offset
   xp=0;
   xn=0;
   if(vsig > 0) begin
     xp=1;
     xn=0;
   end else begin
     xp=0;
     xn=1;
   end

   if(latch_tau > 0) begin
     rtime = latch_tau * ln(latch_v/abs(vsig));
   end else begin
     rtime = td; // Disable regeneration time calculation and have
     a fixed comparator delay specified by td.
   end
     if(rtime <= 0)  // Negative delays not realistic. Occurs when
     vsig>latch_v.
       rtime = 0;

     if(rtime > `clk_per) //Regeneration longer than clock period
         $strobe("Warning! Regeneration time: %g\n", rtime);
   end //end cross

  V(dout_p) <+ transition(xp * vhigh, rtime, tt, tt );
  V(dout_m) <+ transition(xn * vhigh, rtime, tt, tt );

end // analog

endmodule
```

B.4 Verilog-A model of successive approximation register for MCS procedure

```
// Successive approximation register for n-bits
// n+1 states: LSB+sampling+output, MSB, MSB-1,..., LSB+1
//
//  The word from (previous) n-bit conversion is outputed at
    sampling phase.
//
// Operation of comparator in SAR: Vin>Vref/x? : cmp_value=1/0


`include "constants.vams"
`include "disciplines.vams"

`define BITS 12   // Number of ADC bits

module sar_MCSreg12(clk, cmp_value, d, smp, b, d_bar, c);

input clk, cmp_value;
output [`BITS-1:1] d;    //DAC control
output [`BITS-1:1] d_bar; //Inverse of d (except during sampling)
output [`BITS-1:1] c;    //Extra DAC control (connect to Vcm)
output [`BITS-1:0] b;    //Word output
output smp;


electrical clk, cmp_value, smp;
electrical [`BITS-1:1] d;
electrical [`BITS-1:1] d_bar;
electrical [`BITS-1:1] c;
electrical [`BITS-1:0] b;

parameter real vth = 0.5;
parameter real vhigh = 1.0;
parameter integer trigger_edge =1; //+1 rising edge || -1 falling
    edge
parameter real tr = 50p;

integer i_d[`BITS-1:1];
integer i_b[`BITS-1:0];
integer i_c[`BITS-1:1];

integer state, value, i_smp;
genvar i;

analog begin

  @(initial_step) begin //Setup
    state=0;
```

```
    i_smp=0;
    for (i = 'BITS-1; i>=0; i = i-1) begin
      i_b[i] = 0;
    end
    for (i='BITS-1; i>=1; i = i-1) begin
      i_c[i] = 1;
      i_d[i] = 0;
    end
  end

  // Sequential process. Rising clock edge.
  //Comparator output from previous clock period determines DAC
    value.
  @ (cross(V(clk) - vth, trigger_edge)) begin

    if(state==0) begin // Do final comparison and write output
    data, Reset, Sample

      if(V(cmp_value)>vth) begin  // Determine LSB
        i_b[0] = 1;
      end else begin
        i_b[0] = 0;
      end

      for (i = 'BITS-1; i>=1; i = i-1) begin //Update output b
    from d
        i_b[i] = i_d[i];
      end

      for (i = 'BITS-1; i>=1; i = i-1) begin //Reset  d and
    connect bottom plates to vcm
        i_d[i] = 0;
        i_c[i]=1;
      end

      i_smp = 1; //sample

    end else if(state==1) begin
      i_smp = 0;

    end else if((state>1) && (state<='BITS)) begin
      if(V(cmp_value)>vth) begin // Determine MSB to second last
    bit from prev. DAC word.
        i_d['BITS-state+1] = 1;
      end else begin
        i_d['BITS-state+1] = 0;
      end
      i_c['BITS-state+1]=0;
    end

        state = state+1;
```

```
    if(state>`BITS) begin
      state = 0;
    end
  end

  //Write signals (continuously)

  for (i = `BITS-1; i>=1; i = i-1) begin
      V(c[i]) <+ transition(i_c[i], 0, tr, 1p);  // Longer rise
    time for non-overlapping clock cycles
      V(d[i])   <+ transition((i_d[i]&&!i_c[i]), 0, tr, 1p);
      V(d_bar[i]) <+ transition((!i_d[i]&&!i_c[i]), 0, tr, 1p);
  end

  for (i = `BITS-1; i>=0; i = i-1) begin
      V(b[i])   <+ transition(i_b[i], 0, 10p);
  end

  V(smp) <+ transition(i_smp, 0, 1p, 1p);
end


endmodule
```