Optimizing the RF-parameters of an III-V FinFET

Hugo Sjöberg
Supervisor: Erik Lind, Cezar Zota
The Faculty of Engineering Lund University

July 7, 2015

ABSTRACT

Using the 3D finite element tool COMSOL a III-V FinFET was modeled based on Cezar Zota, Erik Lind and Lars-Erik Wernerssons work. Using this model, the gate-source parasitic capacitance, the gate-drain parasitic capacitance, the source and drain resistances were simulated. Changing the geometry of the FinFET was done in order to optimize the transistor in regard for the transition frequency and the maximum oscillation frequency and improving the frequencies with over 350%.

"A ship in the harbor is very safe, but this is not what ships are for."
-William G.T. Shedd

ACKNOWLEDGEMENTS

Thank you Erik Lind for all your guidance and your patience, without you this wouldn't be possible.

CONTENTS

ACRONYMS

FinFET Fin-Field effect transistor

MOSFET Metal-oxide-semiconductor Field effect transistor

FET Field effect transistor

CMOS Complementary Metal Oxide Semiconductor

FE Finite Element

FEM Finite Element Method

RF Radio Frequency

1

INTRODUCTION

One of the most important building blocks in modern electronics is the transistor. The areas of usage are many, spanning from analog electronics making wireless communications to digital electronics. Simplified, a transistor consist of a gate, source and a drain. The source and drain are not in direct contact with each other and a current cannot be conducted between the two without applying an gate voltage. When a voltage is applied on the gate a channel between the source and the drain forms that can conduct current between source and drain.

1.1 HISTORY

The transistor history starts in the 1920's with papers that propose the idea of an amplifying device using a field-effect, however due to lack of semiconductor material or rather knowledge of it the device could not be made. Scientists at Bell Laboratory began studying the semiconductor material silicon to use in an crystal-detector and found the neat property of silicon conducting a positive current flow and a negative current flow, the so called PN-junction[1].

Later in 1947 also at Bell laboratory, William Shockley, John Bardeen and Walter Brattain created a device that would have a greater output then input this creating the first working transistor[2]. In 1956 Shockley, Bardeen and Brattain were awarded the Nobel Prize in physics "for their researches on semiconductors and their discovery of the transistor effect".[3]

An big industry started to grow around the transistor and our electronic began to rely heavily on these transistors and the industry's attempts to make them smaller and more efficient. In 1965 the Co founder of Intel, Gordon E.Moore made a statement that the number

transistors on a dense integrated circuit would double every two year and that statement seems to have been proven right, see figure 1.[4]

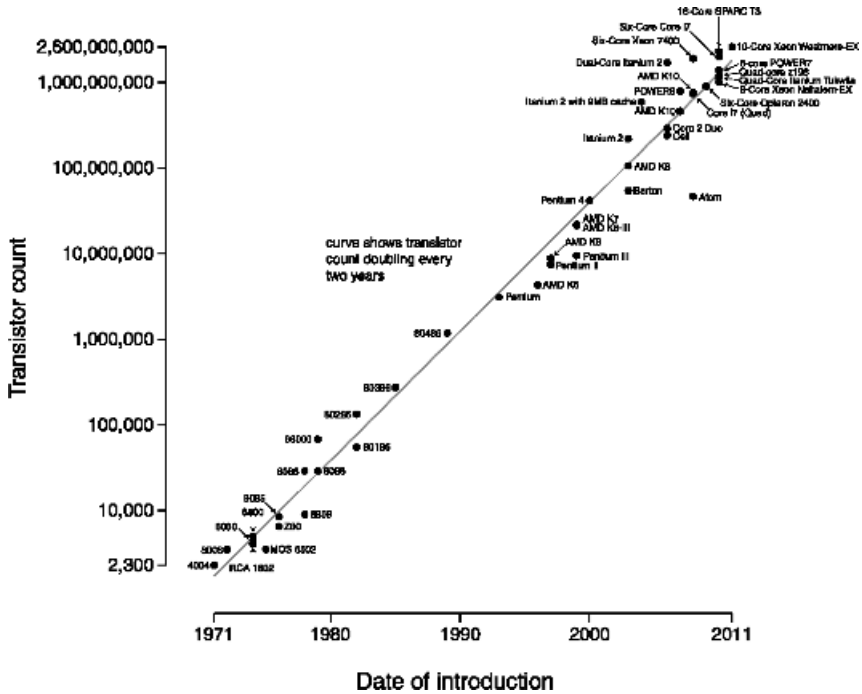

Figure 1: Shows how the transistor count doubles every two year with different kind of microprocessors, from 1971 to 2011, according to Moore's law.

1.2 FUTURE

Until now the industry have kept up with Moore's law by making transistors smaller and reducing the distance between them. The problem that arise with reducing size is that the transistor will conduct even when turned off and thus consume power. To make the chips even denser new architecture have to be used since old techniques can not be reduced further in size. One new promising architecture is the FinFET that have the gate surrounding the channel which gives a better control and therefore reduces current leaking[5].

One way of creating a FinFET is to use a nanowire as a channel and build a gate on top of it. This kind of transistor has been built at

Lunds University by Cezar Zota, Erik Lind and Lars-Erik Wernersson. The transistor built shows record breaking result in terms of f_t and f_{max}[6]. To making this transistor excel even further one must change parameters such as materials, or geometry design. To reduce time spent in the lab guessing what geometry to use simulations can be used to find optimum values for the geometry.

2

LIMITATIONS

Limitations in this thesis are based on the limitations of simulating the FinFET in Comsol. In the models used in Comsol only the parasitic capacitance and the drain, source resistance can be simulated. All the other parameters used for benchmarking etc. are taken from Cezar Zota, Erik Lind and Lars-Erik Wernerssons article $In_{0.53}Ga_{0.47}As$ *multiple-gate field-effect transistors with selectively regrown channels*[7]. The simulations will be limited to simulate a nanowire FinFET described in the article.

3

THEORY

3.1 BASIC MOSFET

One of the most important devices in modern electronics is the metal-oxide-semiconductor field-effect transistor(MOSFET). The MOS part of MOSFET describes the layout of the device, a semiconductor with an oxide-layer between the semiconductor and an metal-layer see figure 2. The FET part of MOSFET describes how it operates, by introducing an electric field between the metal and semiconductor an channel is introduced in the semiconductor material.[8]

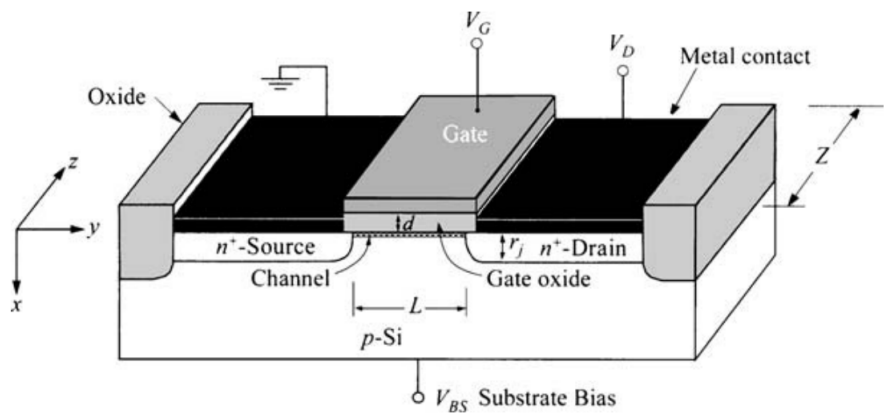

Figure 2: Schematic of an basic n-type MOSFET[9]

A MOSFET got four-terminals, source, drain, gate and an substrate contact which is almost always connected to ground together with source. When ground is applied to the gate the channel between source and drain is turned off, when the voltage is increased above a certain threshold voltage a channel is formed[9]. The source and drain side of the MOSFET is doped, either n doped (extra electrons)

or p doped (extra holes), the substrate is also doped but with the opposite of the source and drain.

The oxide layer of the gate makes the gate metal contact and the semiconductor material of the substrate work like an parallel plate-condenser. If an positive voltage is applied to the gate contact and an negative voltage is applied to the p-type substrate, electrons from the substrate will be attracted and the force holes away from the surface of the substrate and the charge of the the area will be negative. If the voltage is increased enough a bigger area will be negative charged and the p-material turns n-type, the minimum voltage needed for the channel to be formed is called threshold voltage,V_T. This area is called an inversion-layer and when the layer is big enough it connects with the source and the drain see figure 3. When the inversion layer is connected between source and drain it can conduct a current with the help of an voltage applied between source and drain[8].

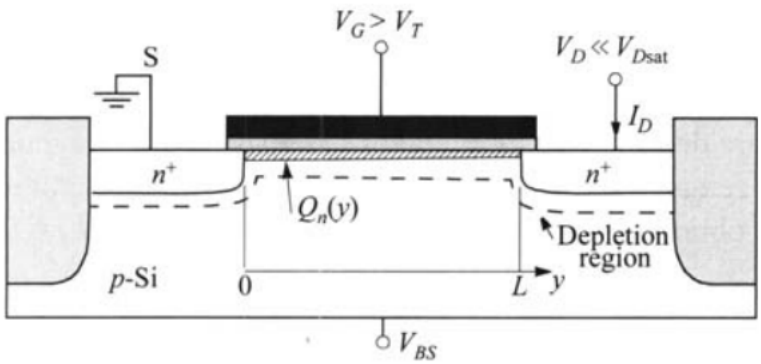

Figure 3: Shows the channel formed between source and drain when the gate voltage is above V_T[9].

3.2 III-V FINFET

Another kind of transistor is the FinFET. A FinFET works by the same principle as an MOSFET but instead of the planar structure of the MOSFET a FinFET has a 3D-structure, allowing more complex geometry. With the complex structure as can be seen in figure 4 allows for better electrostatics gate control. The better electrostatic gate control is gained because the gate is wrapped around the gate and get contact

with the gate on three sides instead of a contact with the channel on one side only as in MOSFET. [10]

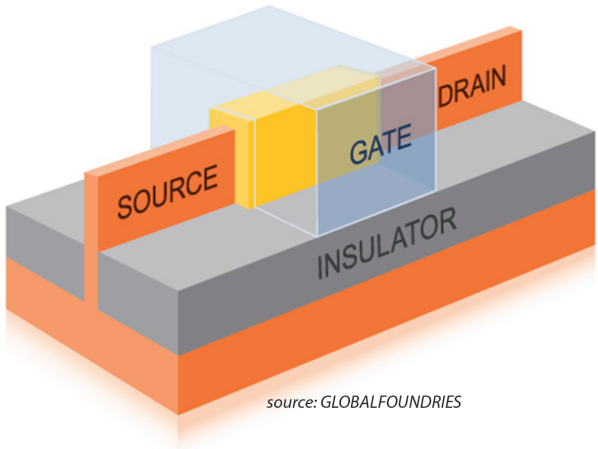

Figure 4: Schematic of an basic FinFET, with the yellow being the gate oxide.

Changing the transistor models is just not enough to push Moore's law further but a change of material is also needed. The electron mobility is good in silicon but is even better in III-V materials. If it was possible to make the same silicon transistor with InAs that as an mobility ten times that of silicon would result in a transistor with a frequency ten times higher then the silicon transistor[8]. However there are limiting factors such as velocity saturation that occurs when a very strong electric field is applied that can no longer make the current travel faster due to electrons interacts with the material[9].

3.3 RESISTANCE

To calculate the resistance for a simple geometry, such as a cylinder equation (3.1) can be used.

$$R = \frac{l}{\sigma A} \tag{3.1}$$

Where l is the length of the cylinder, A is the cross-sectional-area and σ is the electrical conductivity of the material. Calculation of the resistance is more complicated if the geometry is complex, for this equation (3.2) is used. The equation describes the voltage between two

points in an arbitrary structure and the current that flows between the same points. In the simulations the two voltages, v_a and v_b, are set to ground, $0V$ and to terminal, $1V$. Since v_a and v_b are known the problems lies in finding i_{ab}.

$$R = \frac{v_a - v_b}{i_{ab}} \tag{3.2}$$

The resistance is important in a transistor since a high resistance will result in a high effect as can be seen in equation (3.3). A high power will result in an unwanted high temperature and will also restrict the flow of electrons, resulting in a low current between the source and drain.

$$P = R \cdot I^2 \tag{3.3}$$

3.4 CAPACITANCE

Capacitance is the ability for an body to store and return energy, it is defined by two metal bodies with a charge q and $-q$ and with voltages v_a and v_b. The capacitance is defined by equation (3.4).

$$C = \frac{q}{v_a - v_b} \tag{3.4}$$

Where q is the charge, v_b and v_b are two voltages. As can be seen in (3.4) if the two voltages v_a and v_b are known only the charge q has to be calculated to get the capacitance. Since the charges in the bodies can't move to the other metal body there will be an electrical field that attracts the two metal bodies. If there is an contact between the bodies can discharge and return energy charged between the bodies.

An easy example that illustrates how capacitance can be calculated in simple geometries is the parallel plate capacitor approximation. Between two metal plates with the area A with an distance d between the two plates an approximation of the capacitance can be calculated using equation (3.5).

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{3.5}$$

Where ε_0 is the permittivity in vacuum, ε_r is the material constant relative permittivity. Using this approximation to get lower capacitance the material can be changed to lower ε_r or the geometry to lower

A or the space d between the two metal plates can be increased.[11] Capacitance is important in a transistor since it is has many small capacitance's through it's structure and it takes time to charge and discharge the capacitance, and with higher charge and discharge times of a transistor the worse will the performance of it be.

3.5 FINITE ELEMENT

Physical phenomena can be described using differential equations. These equations can be complicated to solve and even harder to solve if a big complex model is to be calculated. Finite element allows for numerical approach solving these equations approximately. The area or volume over the equations are applied are divided up in smaller areas or volumes called finite elements. Depending on what information is needed different equations will be used. To calculate for example the resistance in a body, one solves the equation in one finite element and then solves the next finite element using boundary information for the element next to it[12]. FEM can be used to simulate the resistance in an structure by solving equation (3.7)

$$\nabla \cdot J = \nabla \cdot [-\sigma(r)\nabla v] = 0 \tag{3.6}$$

Equation (3.6) can be used to describe thermal conduction, the flow of liquid etc. and is in this case used for calculating the flow of electrons. Boundary conditions are needed to limit the simulation to just be calculated on the represented structure, this is done by setting equation (3.6) equal to zero outside of the model, this is equal to saying that there are no flow electrons in or out of the model so that the only flow of electrons occurs inside the structure. The current can then be calculated using equation (3.7), and from that the resistance can be calculated, using equation (3.2).[8]

$$i_{ab} = \int_{S_a} J \cdot e_n dS = \int_{S_a} [-\sigma(r)\nabla v] \cdot e_n dS \tag{3.7}$$

The capacitance can be simulated in an similar way as the resistance is, however it is a little bit trickier since electrical field propagates infinitely through space and makes it impossible to calculate with a computer. Limitations to the simulations have to be made in order to make the simulation solvable for a computer, this is done by running the simulation of the structure inside an box which sides

have an applied voltage that makes it impossible for charges to propagate outside the box. The size of the box determines the accuracy of the simulation, the bigger box the more accurate the simulation. The electric field can be calculated using equation (3.8).[11]

$$\nabla \cdot (\varepsilon_0 \varepsilon_r E) = 0 \tag{3.8}$$

3.6 RF-PARAMETERS

Benchmarking is done in order to determine the performance of the transistor. The parasitic capacitance's $C_{gs,p}$, $C_{gd,p}$, the resistances R_S and R_D are studied. The RF-benchmark values f_t and f_{max} are evaluated.

$$C_{gd,t} = C_{gd} + C_{gd,p} \tag{3.9}$$

$$C_{gs,t} = C_{gs} + C_{gs,p} \tag{3.10}$$

$$C_{gg,t} = C_{gs,t} + C_{gd,t} \tag{3.11}$$

As can be seen in equation (3.9),(3.10) and (3.11) $C_{gs,p}$ and $C_{gd,p}$ is together with the intrinsic capacitance used to calculate the total gate, source and drain capacitance which is later used in equation (3.12),(3.14) and (3.13). See figure 5 so see what the capacitance's in equation (3.9)-(3.11) corresponds to in the transistor.[13]

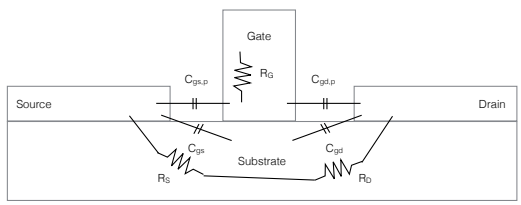

Figure 5: Schematic of an transistor that shows the different resistances and capacitance's.

The RF-parameter cutoff-frequency, f_T, describes the switching speed and is the frequency at which the current-gain is equal to 1. A high cutoff-frequency is more crucial in digital applications. Equation (3.12), describes how to calculate f_T.[13]

$$\frac{1}{2\pi f_T} = \frac{C_{gg,t}}{g_m} + \frac{C_{gg,t}}{g_m}(R_S + R_D) + (R_S + R_D)C_{gd,t} \tag{3.12}$$

The maximum oscillation frequency, f_{max}, is defined as the frequency at which the power-gain is equal to 1. The maximum oscillation frequency is of more interest in RF-applications. Equation (3.13), describes how to calculate f_{max}.[13]

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{gd,t}[1 + (\frac{2\pi f_T}{C_{gd,t}})\psi]}} \tag{3.13}$$

$$\psi = (R_D + R_S)\frac{C_{gg,2}^2 g_d^2}{g_m^2} + (R_D + R_S)\frac{C_{gg,t}C_{gd,t}g_d}{g_m} + \frac{C_{gg,t}^2 g_d}{g_m^2} \tag{3.14}$$

In order to get an transistor with high f_t and high f_max it is crucial to have an device with low resistance, low capacitance, high transconductance g_m, and low output conductance g_d.

4

METHOD

4.1 COMSOL

First a working 2D-model that represented the FinFET described in Zotas article was made. This was accomplished by doing a model of half a FinFET, only modelling the source half of the transistor, as can be seen in figure 6. The reason that only half of the transistor is simulated is because it is symmetrical and simulating the whole transistor would only be time consuming and would not contribute to any additional information.

When a working 2D-model was accomplished, the 2D-model was easily extruded to an 3D-model. The problem with this was to have good representation of the nanowire. The nanowire was later added to the final model as can be seen in figure 7. As can be seen in figure 2 the nanowire is rotated 56°. This is due to the nanowire is grown in this angle in Zotas article. The nanowire is represented by an square, this is because it is a structure that is easy to simulate and because the exact known geometry of the nanowire is unknown.

Simulation was done using modules electrostatics and electric currents. These two models are used to simulate capacitance and resistance. As described in the theory part under capacitance and resistance, the two parameters are contingent with material parameters and geometry. For simulating the capacitance relative permittivity and for resistance the conductivity is used. See table 1 to see what materials and material parameters that are used.

Several different geometries was simulated, however there was one main geometry that was modeled and the others are a variation of

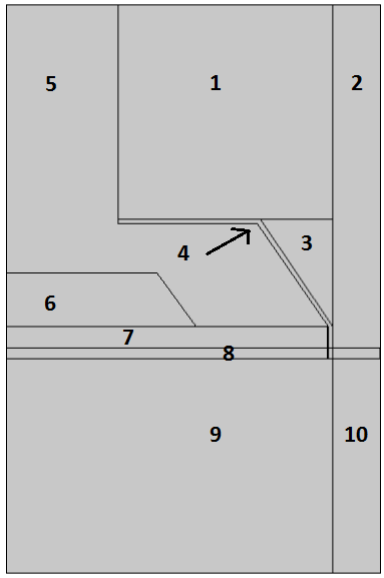

Figure 6: Shows the 2D representation of the FinFET. Number 1-3 is the gate, 4 is the gate oxide, 5 is air, 6 is the source contact, 7 is the source, 8 is the nanowire, 9 and 10 is the base

that one. The main model of how the spacing, w_{source}, between the source and the gate oxide affects the transistor parasitic resistance and capacitance, see figure 8. This was executed by doing a parametric sweep using the distance 1 to 40 nm change in spacing and one separate simulation using the distance 0 nm. The reason for doing this in two steps is because when a difference between the source and gate-oxide new surfaces are also introduced that are of interest. These surfaces cannot be marked for simulation if they are not first introduced in the model. Variation of that simulation can be seen in the list below.

- Different materials in the spacing. The materials used was, air using ε_r = 1, silicon using ε_r = 11.7 and an generic oxide with ε_r = 3.9.
- Using different angle on the nanowire from 5 $^\circ$ to 35 $^\circ$
- Using different conductivity in the nanowire from 8000 $1/\Omega$ to 400 $1/\Omega$

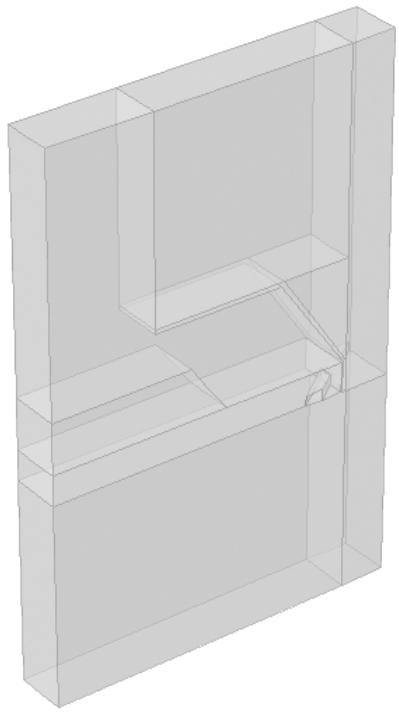

Figure 7: Shows the 3D representation of the FinFET.

- Parametric sweep of the gate height, h_{gate} from 60 nm to 300 nm, see figure 8
- Sweeping the gate width, w_{gate}, from 100 nm to 260 nm, see figure 8
- Parametric sweep of the nanowire width and height, from 5 nm to 30 nm
- Sweeping the nanowire spacing from 30 nm to 70 nm, with the original spacing being 50 nm
- Using a straight gate instead of the original, see picture 9

Part of transistor	Material	Relative permittivity [1]	Electrical conductivity [S/m]
Gate	Copper	1	$5.98 \cdot 10^7$
Gate oxide	Oxide	20	10^{-13}
Source Contact	Copper	1	$5.98 \cdot 10^7$
Source	InGaAs	14	$8 \cdot 10^3$
Base	InP	12.6	10^{-7}
Nanowire	InGaAs	14	$8 \cdot 10^3$

Table 1: Material Parameters of the simulated FinFET

4.2 POST DATA PROCESSING

The capacitance and resistance simulated in Comsol only are parasitic and cannot be used soley to calculate f_t and f_{max}. $C_{gs,t}$, $C_{gd,t}$, g_m and g_d are completely taken from Zotas article [7], see table 2, R_G is set to 11 Ω this is because it gives more realistic values to f_t and f_{max} then the R_G of 7 Ω used in the article. One other difference between the simulation and Zotas article [7] are the number of nanowires used. In the simulation only nanowire is used and in the article the FinFET has 200 nanowires.

The first step was to add the first values that was simulated when the spacing between the source and gate-oxide was zero, then the results was calibrated with the FinFET from the article by dividing the resistance with 200 and multiply the capacitance with 200. This is because the simulated values are achieved using only one nanowire and the values taken from the article has 200 nanowires. The resistances R_S and R_D are ready to be used.

To calculate the new $C_{gs,t}$, $C_{gd,t}$ and $C_{gg,t}$ for different geometries, equations (3.9)-(3.11) are used. $C_{gs,p}$ and $C_{gd,p}$ were simulated when the spacing between the source and the gate oxide is 0, these values are then removed from $C_{gs,t}$, $C_{gd,t}$ and new parasitic capacitance is added when the spacing is increased, see appendix for the code used.

To calculate f_t and f_{max} equations (3.12) and (3.13) was used. The results were then plotted.

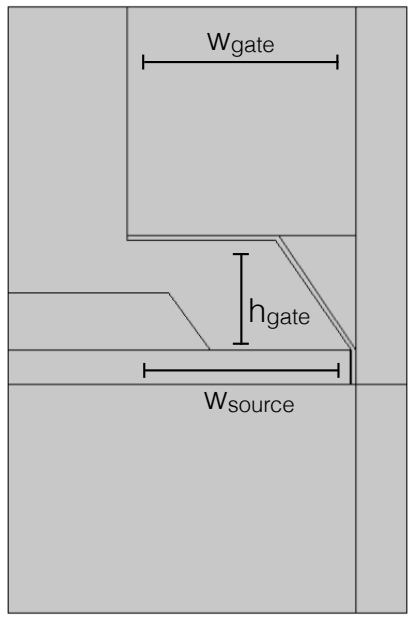

Figure 8: Shows the gate width, gate height and source spacing

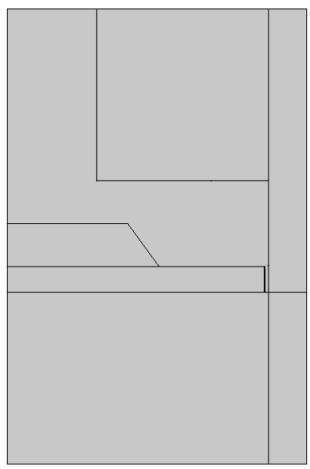

Figure 9: Shows the FinFET with an straight gate instead on the shape of the gate that can be seen in figure 6

g_m	$22 \cdot 10^{-3} S$
g_d	$5.3 \cdot 10^{-3} S$
$C_{gs,t}$	$8.5 \cdot 10^{-15} F$
$C_{gd,t}$	$5 \cdot 10^{-15} F$
$C_{gg,t}$	$13.5 \cdot 10^{-15} F$

Table 2: Values used to calculate f_t and f_max

5

RESULT

In this section the results from post data processing will be presented in forms of plots of the data.

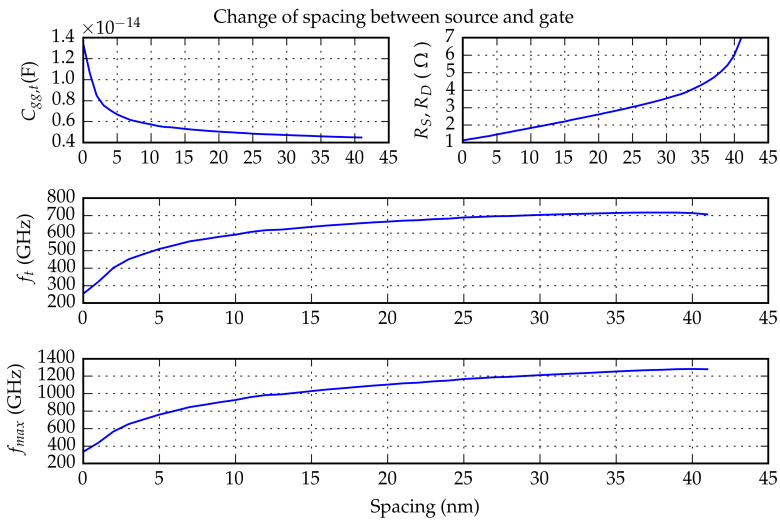

Figure 10: Shows the characteristics $C_{gg,t}, R_S, R_D, f_t$, and f_{max} with increasing spacing between the source and the gate oxide

In figure 10, the results of simulating the original FinFET with increasing spacing between the source and the gate is shown. Both $C_{gg,t}, R_S, R_D, f_t$ and f_{max} is plotted. The reason for plotting $C_{gg,t}$ and not the simulated capacitance is because $C_{gg,t}$ contains more information then just the parasitic and also because $C_{gs,t}$ and $C_{gd,t}$ are also included in $C_{gg,t}$. R_S and R_D are plotted together since they are equal. As can be seen in the plots an optimal value for f_t and f_{max} can be found at around 30-40 nm. f_t starts to decrease after 40 nm.

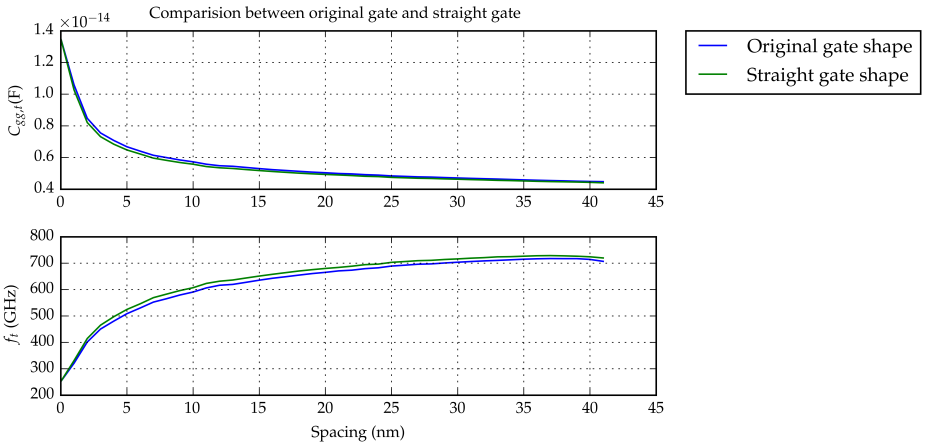

Figure 11: Shows the characteristics $C_{gg,t}$ and f_t both for the original FinFET and an FinFET with an straight gate instead of an pyramid type gate.

Figure 11 shows what happens if the gate geometry is changed. Since the resistance is not effected by the change of gate geometry it is not plotted. The oscillation frequency is not plotted since it is heavily dependent on f_t it will have the same shape and dependence as f_t. As can be seen in the plot, the geometric shape of the gate have little effect on the performance of the device.

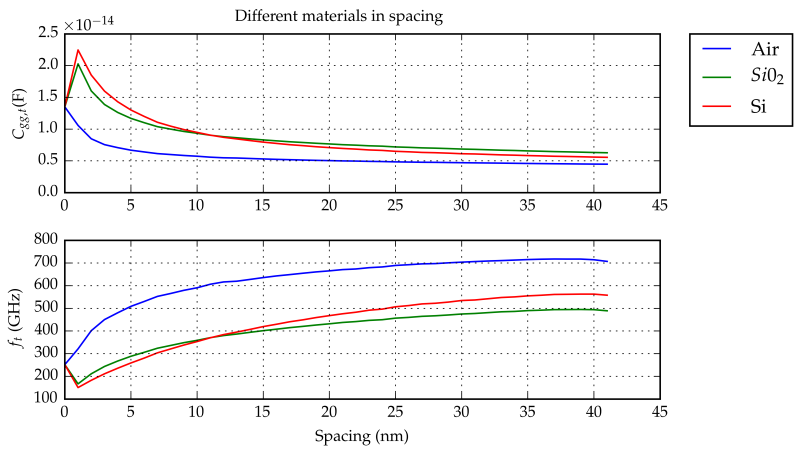

Figure 12: Shows the characteristics $C_{gg,t}$, R_S, R_D, and f_t with different oxide and with increasing spacing

The plots in figure 12 shows the result of simulating the transistor with an oxide surrounding the FinFET. $C_{gg,t}$ and f_t are the only values that are plotted since adding an oxide to the structure will only affect the capacitance and therefore the resistances will be the same as in figure 10, the oscillation frequency as is shown in equation (3.13) is heavily dependent on f_t and will behave like the results in figure 10. The odd shape in the beginning of the plot showing $C_{gg,t}$ is due to an drawback of the post data processing script. The reason for the frequencies for silicon oxide to surpass the $Si0_2$ oxide is unknown. The conclusion from the result is that a material with an lower relative permittivity is more favourable then a material with an higher relative permittivity.

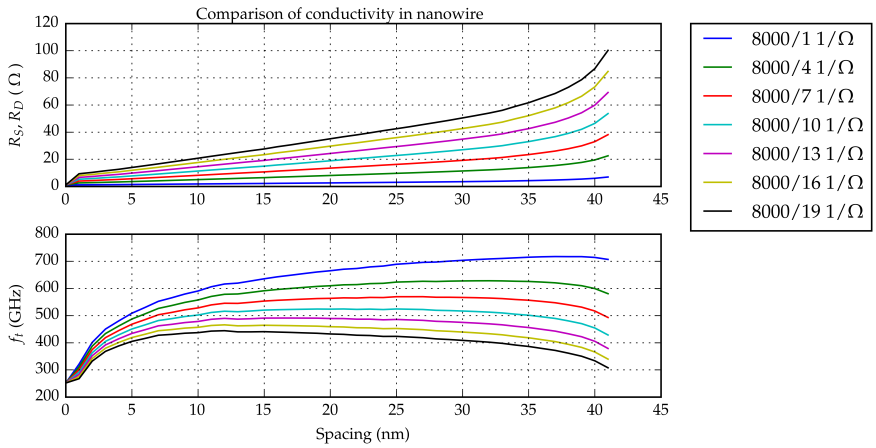

Figure 13: Shows the characteristics R_S, R_D, and f_t with different electrical conductivity for the nanowire and with increasing spacing

In figure 13 the result of simulating with different electrical conductivity in the nanowire is shown. The capacitance is not plotted since it is not effected by different electrical conductivity, the oscillation frequency is not plotted using the same argument as previously. The results suggests that an nanowire with higher conductivity is more favourable then an nanowire with lower conductivity due the lower R_S and R_D that will result in better frequencies.

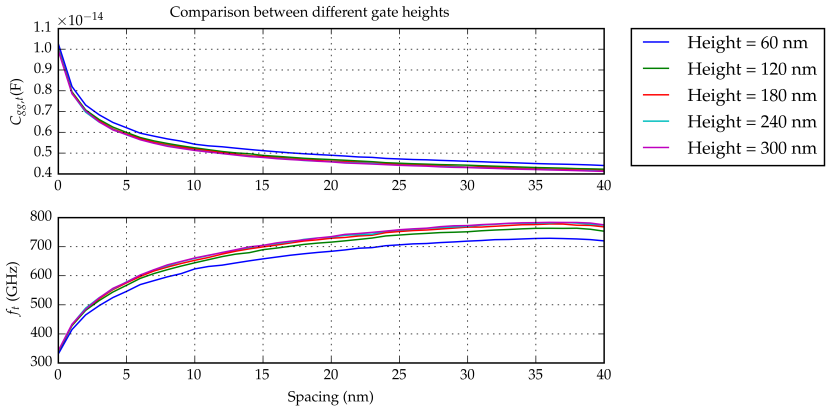

Figure 14: Shows the characteristics $C_{gg,t}$ and f_t with increasing gate height and spacing

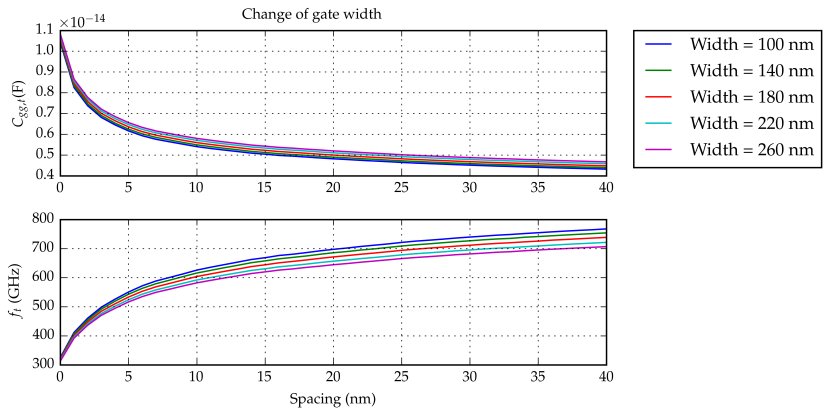

Figure 15: Shows the characteristics $C_{gg,t}$ and f_t with increasing gate width and spacing

In figure 14 and 15 simulations have been done with different gate height and width. The change in geometry only effects the capacitance and the oscillation frequency is not plotted with the same argument used above. The height of the gate have little effect on the device performance but the gate width have an effect where an smaller gate width is more favourable then an higher gate width due to an lower $C_{gg,t}$.

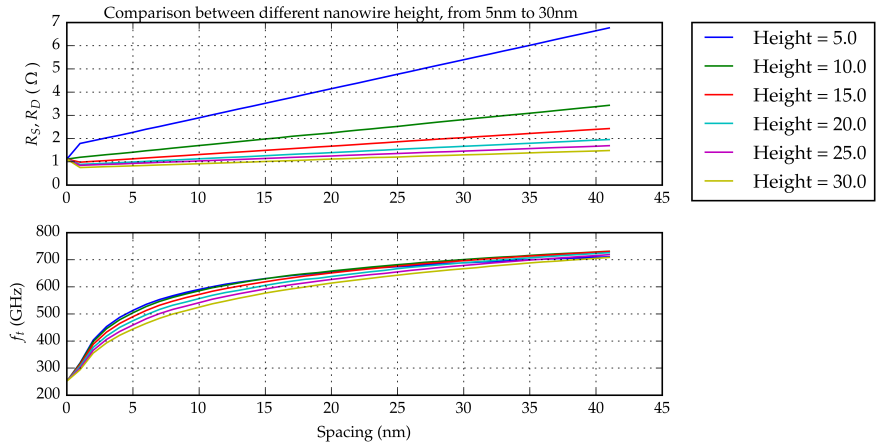

Figure 16: Shows the characteristics R_S, R_D, and f_t with different nanowire height and with increasing spacing

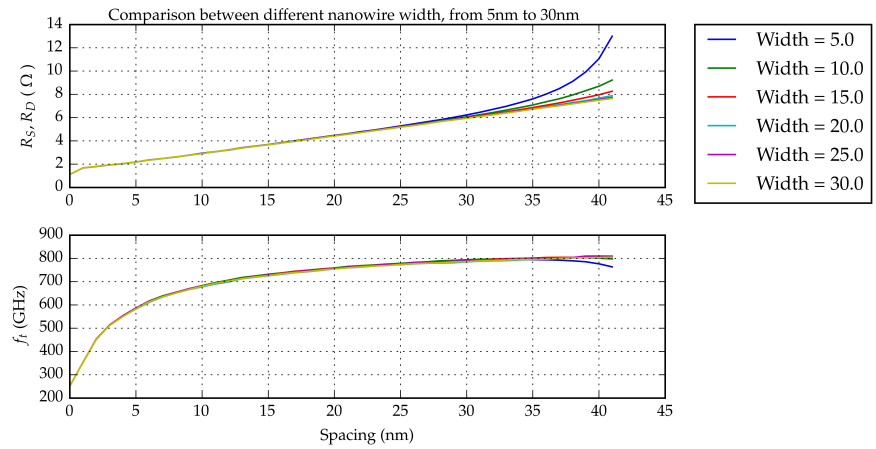

Figure 17: Shows the characteristics R_S, R_D, and f_t with different nanowire width and with increasing spacing

In figure 17 and 16 simulations have been done with different width and height of the nanowire. The change in geometry does not have an effect on the capacitance and is therefore not plotted. The two plots shows that an smaller nanowire will result in an higher R_S and R_D that will have an small impact on the device performance.

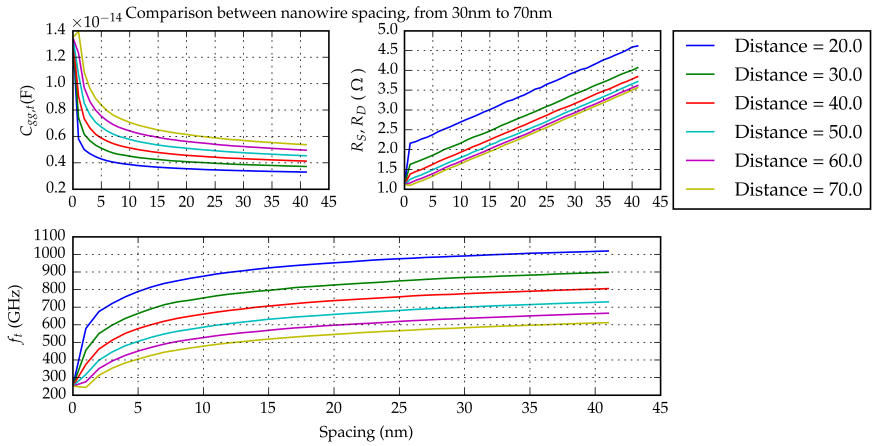

Figure 18: Shows the characteristics $C_{gg,t}, R_S, R_D, f_t$, and f_{max} with different nanowire spacing and with increasing spacing

Figure 18 shows the result of simulating with different space between the nanowires. $C_{gg,t}, R_S, R_D$, and f_t is plotted. As can be seen in the plot an smaller distance between the nanowires will increase R_S and R_D but will however decrease $C_{gg,t}$. The decrease of $C_{gg,t}$ boosts the device performance to above 1THz at an 20 nm distance between the nanowires.

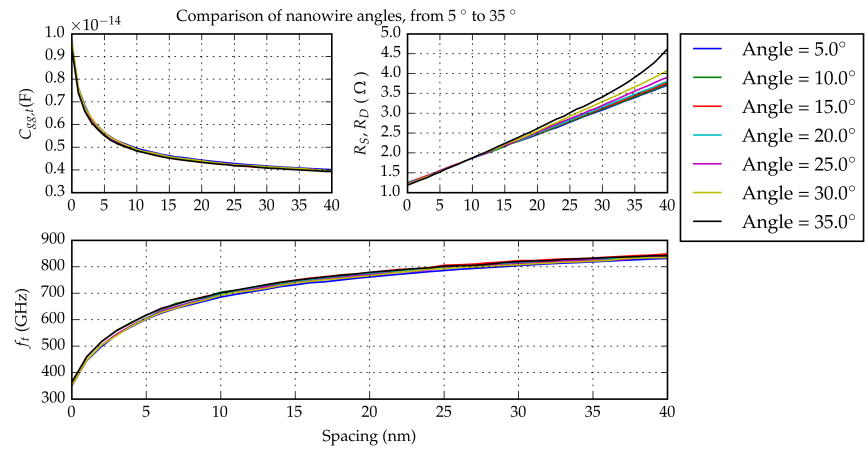

Figure 19: Shows the characteristics $C_{gg,t}, R_S, R_D, f_t$, and f_{max} with different nanowire angle and with increasing spacing

Figure 19 shows the result of simulating with different angle of the nanowire. As can be seen in the plot, the angle of the nanowire have almost no effect on the result. The small change of resistance is because with an angle the wire make the wire longer and therefore have a slightly higher resistance.

6

DISCUSSION

The results in figure 10 is as expected from the theory that with increasing spacing the capacitance $C_{gg,t}$ goes down and the resistance R_S, R_D increases with more spacing. When the spacing is 0 nm the capacitance is at a peak value of $1.4x10^{-14}F$ and goes down to about $0.5x10^{-14}F$, that is a decrease of 35 %. The resistance start with 1 Ω at 0 nm spacing and increases to 7 Ω at 40 nm spacing, the increase is 700%. The sudden peak in the resistance plot is because when the spacing is increased the nanowire start to loose more and more contact with the source and when then when the spacing is big enough the two will loose physical contact with another and as a result the resistance is greatly increased. The benchmark values f_t increases from about 280 GHz to around 700 GHz, an increase of 250% and f_{max} has increased with 364%. Considering a rather low decrease of $C_{gg,t}$ and a big increase of R_S, R_D the results seems unexpected. By studying equations (3.12) and (3.13) it can be noticed that the resistance does not play a huge part instead the different capacitance are what mostly determines f_t and f_{max}.

In figure 11 the geometry if the gate is changed and as a result the straight gate performs slightly better then the original gate. The change in performance is so small so it is safe to say that the geometry change of the gate have almost none effect of the performance of the transistor.

The oxides in the spacing as can be seen in 12 actually makes the transistor preform worse. The results are in line with the theory which clearly states that using an material with an higher relative permittivity increases the capacitance. The decrease in frequency in figure 12 can be explained by the capacitance has an start value stated in the

method section. The reason for silicon dioxide to have better performance then silicon in the when low spacing is used and for silicon to have better performance then silicon dioxide with increased spacing is unknown.

With lower conductivity in the nanowire the resistance increases as can be seen in figure 13. The result is highly expected however it can be used in further research as a guidance to what conductivity the nanowire has.

In figure 14 and figure 15 is is shown that with an increase in gate height and an decrease in gate width the performance is pushed even further to a better result.

A change in the nanowire geometry does not have an big impact on the device performanceas can be seen in figure 16 and 17. With an decreasing size of the nanowire the resistance is increased an causes f_t to decrease slightly, the size currently used for the nanowire width and height can be recommended since an increase does not seem to make the transistor preform better however the nanowire size can be reduced to make the transistor smaller.
Decreasing the space between the nanowires increases the performance according to figure 18. With a lower nanowire spacing a lower capacitance is gained but also an higher resistance. The transition frequency shows great results showing an f_t over 1 THz.

To make the device preform better then 1 THz a lower nanowire spacing is needed, in this model the spacing could not be reduced further because of the size of the nanowire but as can be seen in figure 16 and 17 a reduced size of the nanowire does not have an big impact on the device performance. Using a smaller gate width and a nanowire with as high electrical conductivity as possible would make the performance of the FinFET very good.

6.1 FURTHER WORK

To further investigate this FinFET another module in COMSOL should be used to simulate the transistor in order to get more information about it performance. A module named "Semiconductor" can be used

for this specific assignment and to check the transistors performance in other areas. It would also be good to make some changes to the transistor in similar fashion with the changes done in this thesis, to check if it has some effect on the performance to make sure that the simulations shows a true result so this method can be used in future work with other transistors.

7

REFERENCE

[1] *Invention of the first transistor*, http://www.aps.org/publications/apsnews/200011/history.cfm, Mar. 2015.

[2] K. Dawon, "A historical perspective on the development of mos transistors and related devices," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 23, no. 7, pp. 655–657, 1976.

[3] *The nobel prize in physics 1956*, http://www.nobelprize.org/nobel_prizes/physics/laureates/1956/, Mar. 2015.

[4] E. Gordon, "Cramming more components onto integrated circuits," *LIFE FELLOW, IEEE*, no. 7, 1965.

[5] *Transistor wars*, http://spectrum.ieee.org/semiconductors/devices/transistor-wars, Mar. 2015.

[6] C. B. Zota, G. Roll, L.-e. Wernersson, and E. Lind, "Radio-frequency characterization of selectively regrown ingaas lateral nanowire mosfets," vol. 61, no. 12, pp. 4078–4083, 2014.

[7] C. B. Zota, L. E. Wernersson, and E. Lind, "Ino.53ga0.47as multiple-gate field-effect transistors with selectively regrown channels," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 342–344, 2014, ISSN: 07413106.

[8] A. Gustafsson, *Komponentfysik - En introduktion*. 2001.

[9] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*. 2006, ISBN: 9780470068328.

[10] H. Riel, L.-E. Wernersson, M. Hong, and J. a. del Alamo, "Iii–v compound semiconductor transistors—from planar to nanowire structures," *MRS Bulletin*, vol. 39, no. August, pp. 668–677, 2014, ISSN: 0883-7694. DOI: 10.1557/mrs.2014.137.

[11] M. G. Daniel Sjöberg, *Kretsteori, ellära och elektronik*. 2011.

[12] N. Ottosen and H. Petersson, *Finite Element Method*. 1992, ISBN: 9780134738772.

[13] W. Liu, *Fundamentals of III-V Devices HBTs, MESFETS, and HFETs/HEMTs*, ser. A Wiley-Interscience publication. 1999, ISBN: 9780471297000.

8

APPENDIX

```
def cap(capacitance):
    """Makes an capacitance list"""
    Nw=200
    Co=2.78e-17*Nw
    Cgdp=[Co]
    for x in capacitance:
        z=x*Nw
        Cgdp.append(z)

    Cgsp=Cgdp
    Cggt=[]
    Cgst=[]
    Cgdt=[]
    for x in range(0,len(Cgdp)):
        Cggt.append(13.5*10**(-15)+Cgsp[x]+Cgdp[x]-
            Co-Co)
        Cgst.append(8.5*10**(-15)-Co+Cgsp[x])
        Cgdt.append(5*10**(-15)-Co+Cgdp[x])
    return Cggt, Cgdt, Cgst

def res(res):
    """Makes an resistance list"""
    resistance=[]
    Nw=200
    Ro=223.2/Nw;

    for x in res:
        z=x/Nw
        resistance.append(z)
```

```
    resistance.insert(0,Ro)
    return resistance

def calculate(Cggt,Cgst,Cgdt,Rs,Rd):
    """Use to calculate ft,fmax"""
    gd=5.3*10**-3
    gm=22*10**-3
    Rg=11
    d=len(Cggt)
    ft=[]
    for k in range(0,d):
        ft.append(1/(2*pi*(Cggt[k]/gm+(((gd*Cggt[k
            ])*(Rs[k]+Rd[k]))/gm)+(Rs[k]+Rd[k])*Cgdt
            [k]))))
    psi=[]
    for k in range(0,d):
        psi.append((Rd[k]+Rs[k])*((Cggt[k]**2*gd
            **2)/gm**2)+(Rd[k]+Rs[k])*((Cggt[k]*Cgdt
            [k]*gd)/gm)+((Cggt[k]**2*gd)/gm**2))
    fmax=[]
    for k in range(0,d):
        fmax.append(sqrt(ft[k]/(8*pi*Rg*Cgdt[k
            ]*(1+((2*pi*ft[k]/Cgdt[k]*psi[k]))))))

    return ft,fmax
```