Optimizing the RF-parameters of an III-V FinFET

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By using the 3D finite element tool COMSOL an existing III-V FinFET to optimize the parameters and the performance. Changing the geometry of the FinFET done in order to optimize the transistor in regard for the transition frequency and the maximum oscillation frequency and improving the frequencies with over 350%

One of the most important component in building blocks in modern electronics is the transistor. The areas of usage are many, spanning from analog electronics making wireless communications to digital electronics. Simplified, a transistor consist of a gate, source and a drain. The source and drain are not in direct contact with each other and a current cannot be conducted between the two without applying gate voltage. When a voltage is applied on the gate a channel between the source and the drain forms that can conduct current between source and drain. The transistor history starts in the 1920's with papers that propose the idea of an amplifying device using a field-effect, due to lack of semiconductor material or rather knowledge of it the device could not be made. Scientists at Bell Laboratory began to study the semiconductor material silicon to use in an crystal-detector and found the neat property of silicon conducting a positive current flow and a negative current flow, the so called PN-junction.[1] An big industry started to grow around the transistor and our electronic began to rely heavily on these transistors and the industry's attempts to make them smaller and more efficient.

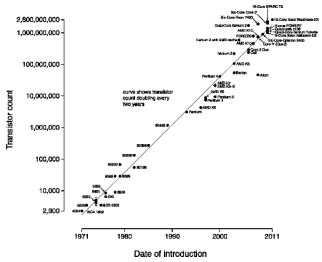

Figure 1: Shows how the transistor count doubles every two year with different kind of microprocessors, from 1971 to 2011, according to Moore's law.

In 1965 the Co-founder of Intel, Gordon Moore made a statement that the number transistors on a dense integrated circuit would double every two year and that statement seems to have been proven right, see figure 1.[2] Until now the industry have kept up with Moore's law by making transistors smaller and reducing the distance between them. The problem with reducing size is that the transistor will conduct current even when turned off and thus consume power. To make the chips even denser new architecture has to be used since old techniques cannot be reduced further in size. One new promising architecture is the FinFET that have the gate surrounding the channel which gives a better control and therefore reduces current.[3]

A new FinFET design used by researchers at Lund University uses a nanowires as a channel and build a gate on top of them. This design shows record frequencies.[4] To make this transistor excel even further one must change parameters such as materials, or geometry design. Instead of spending a lot of time in the lab guessing what geometry to use, one can spend little time in front of the computer doing 3D-simulations using finite element method. Using finite element method when simulating allows for solving equations in complex 3D-structures, doing this by hand is almost impossible but by using a computer program, for example COMSOL, this is fairly easy. By changing the geometry of the FinFET the simulations suggests that the performance of the transistor can be increased up to 350% by just changing the distance between the source and the gate, and decreasing the distance between the nanowires.

[1] **invTrans**.
[2] **moore**.
[3] **transWar**.
[4] **zota2014a**.