Lund University

Master Thesis

Hall Measurements on Regrown Nanowires

Author:
Sudhakar Sivakumar

Supervisors:
Dr. Erik Lind
Dr. Dan Hessman

A thesis submitted in fulfilment of the requirements for the degree of Master of Science

in the

Nanoelectronics Group
Electronis and Information Techonology

October 2015

Lunds universitet
Naturvetenskapliga fakulteten

"An expert is a man who has made all the mistakes, which can be made, in a very narrow field"

Neils Henrik David Bohr

LUND UNIVERSITY

Abstract

Faculty of Science
Electronis and Information Techonology

Master of Science

Hall Measurements on Regrown Nanowires

by Sudhakar Sivakumar

Ternary semiconductor alloys like $In_xGa_{1-x}As$ have lured competing attention in connection to sub-50 nm high performance, low power, planar Complementary Metal Oxide Semiconductor technology. This compound semiconductor owes its popularity to excellent bulk carrier mobility, minority carrier diffusion constant, small bandgap, high electron injection velocity and its capability to take Moore's law beyond silicon platform. Though they exhibit exceptional properties in their bulk, their properties in confined architectures like a nanowire (NW) still remains relatively less explored. In this work, the transport properties of $In_xGa_{1-x}As$ is explored in a planar confined device architecture, by performing **Hall Measurements** on $In_xGa_{1-x}As$ NWs, in a home built measurement setup. The device of interest is fabricated with the help of Electron Beam Lithography (EBL) and a novel method of **selective area regrowth**. The pattern is made with the help of Hydrogen Silesquixone (HSQ) negative tone E-beam resist on a semi-insulating InP substrate. The device geometry allows placement of probe electrodes exactly opposite to each other, which is very important to extract Hall voltage and hence the mobility of the NW. Ti/Pd and Au bilayer is used to make the contact pads which are again defined by EBL with PMMA positive E-beam resist. The samples were mounted on an insulating ceramic holder and each device was manually wire bonded to the contact pins using a 0.25 µm gauge aluminium wire. And Hall measurements were performed on the successful devices at room temperature. For the proposed geometry, the devices exhibited electron mobility values $\approx (5000 \pm 800)$ cm^2/Vs.

Acknowledgements

No long journey can be successful without help along its path. Like all long journeys, I had a lot of help during mine. A simple thanks won't be enough, but its a start.

I would like to thank my parents for supporting me economically and emotionally. Without them, my dreams of pursuing higher education or the trip to Lund university would be impossible. And in my country, sending your son/daughter to another country for eduction, is not an easy decision. I extend my gratitude and love to them for making that tough decision and standing by it.

First and foremost, I would like to thank Dr.Erik Lind, my mentor, who allowed me to take part in his research. He is a kind optimist and an excellent teacher. The way he tutored in his lectures created interest in me to work with him. I thank him for all his advice and kindness. I would like to thank Mr.Cezar Zota for teaching me all the fabrication techniques and helping me with my doubts and questions. He played a pivotal role as a good practical teacher for the past one year. And I thank Mr.Olof Hultin for teaching me how to use the measurement setup and Mr.Fredrik Lindelöw for helping me during the measurements. And Dr.Dan Hessman, my programme co-ordinator and second supervisor, for all his valuable contributions in the past two years. And I would like to thank everyone at Nanoelectronics research group for the positive support they provided.

Friends become an important part in your life when you start living in a different country far away from home. Lund is my home away from home because of my friends here. I thank Markus for cheering me up all the time and just being there whenever I needed him. I hope our friendship will continue for times to come. Finally, I thank my mentors at Solid state physics and staff at Lund Nano Lab for their help.

I Thank you all.

Sudhakar Sivakumar

Contents

List of Figures

List of Tables

Abbreviations

LNL	**L**und **N**ano **L**ab
FTF	**F**asta **T**illståndets **F**ysik
RF	**R**adio **F**requency
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NWFET	**N**ano **W**ire **F**ield **E**ffect **T**ransistor
HEMT	**H**igh **E**lectron **M**obility **T**ransistor
SEM	**S**canning **E**lectron **M**icroscope
UVL	**U**ltra **V**iolet **L**ithography
XRL	**X** **R**ay **L**ithography
SMU	**S**ource **M**easure **U**nit
HSQ	**H**ydrogen **S**iles**q**uioxane
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductor
VLS	**V**apour **L**iquid **S**olid
EUV	**E**xtreme **U**ltra**v**iolet
MIBK	**M**ethyl **I**so**b**utyl **K**etone
TMAH	**T**etra**m**ethyl**a**mmonium **H**ydroxide
BOE	**B**uffered **O**xide **E**tch
PMMA	**Poly** **M**ethyl**m**eth**a**crylate

Symbols

$a_\circ$	Lattice constant	(Å)
E_g	Bandgap	(eV)
I	Current	(A)
V	Voltage	(V)
W	Width	(m)
L/l	Length	(m)
Q	Charge	(C)
E	Electric Field	(J/C)
B	Magnetic Field	(T)
F	Force	(N)
V_H	Hall Voltage	(V)
R_s	Sheet resistance	(Ω)
t	Thickness	(m)
J	Current density	(Am^{-2})

μ_e	Electron mobility	($\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$)
μ_h	Hole mobility	($\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$)
μ	Mobility	($\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$)
τ	Time	(s)
υ	Velocity	(m/s)
σ	Conductivity	(S)
ρ	Resistivity	(Ω)
η_s	Sheet carrier density	(cm^{-2})
η	Carrier concentration	(cm^{-3})

Dedicated to my loving parents...

Chapter 1

Introduction

Traditional Semiconductor scaling is destined to end at some point in time. Even according to Gordon Moore, Moore's law was supposed to be a mere observation. But it mutated into a vital force that drove the semiconductor industry over several obstacles in the last three decades. Major players of the industry construct the ITRS[1] roadmap every year to identify the technologies and innovations that would be needed to sustain the industry in the future. ITRS deems that it takes more than geometrical scaling to steer the industry in its current path. The current research scenario in both academic and industrial sectors is to understand the complex problems associated with scaling. But, one simple question lies at the heart of all these complexities, which is "How to tackle the crippling socio-economic problems that might arise when physical scaling in Si-CMOS technology reaches its limit and how to circumvent such problems?[2]" It goes without saying that Moore's law is not about shrinking transistor size but rather reducing the transistor cost. Utilizing III-V compound semiconductors as channel material is a viable alternative which will carry the industry into the future without degrading the economic benefits involved in scaling[3]. Though other family of materials are being extensively researched, none of them have traits on par with the III-V family[1].

1.1 Ballistic Channel

The future of semiconductor industry relies on scalable solid state devices, realized on silicon platforms that are operating in the *ballistic regime*, at relatively low power and at room temperature[4]. A semiconductor device is said to operate in the ballistic regime, if the charge carriers pass through the bulk of the device without encountering any scattering from lattice phonons or intrinsic impurities. A CMOS transistor operating

[1] International Technological Roadmap for Semiconductors

in the ballistic regime can have electrons traversing the channel scattering only at the device boundaries as shown in Fig. 1.1. Then the transistor channel can be called a

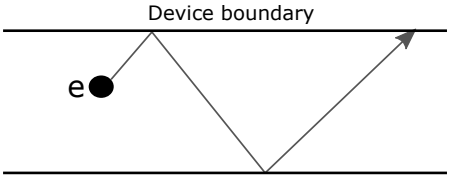


FIGURE 1.1: Schematic representation of ballistic transport. An electron being scattered only at the device boundaries.

ballistic channel. Ballistic conduction is not feasible in devices that are commercially available now because, the device dimensions are much larger than the electron mean free path. **Phonon Scattering** is one such temperature dependent scattering mechanism that deteriorates device performance. But such scattering events are less common in a ballistic device; this avoids performance degradation in such ballistic device architecture that arises due to temperature dependent effects[4]. So, ballistic devices pave way to ultra fast devices operating at **room temperature**[5]. And the III-V family has an answer to this too. *InGaAs*, a ternary alloy, exhibits relatively high electron mobility at room temperature as shown in Figure. 1.2[1], which under proper conditions might be a viable candidate for room temperature ballistic transport.

1.2 Electrical Characterization of nanowires

Mesoscopic devices that utilize *nanowire* architecture have the potential to operate in the ballistic regime at room temperature, as their dimensions are comparable to the electron mean free path[5]. Very few reports exist till date that elucidate the carrier transport properties in such nanowire architectures. Extraction of Hall Voltage from a nanowire enables us to perform precise calculation of carrier mobility and carrier concentration[6]. Proper extraction of the Hall voltage relies on placing metal electrodes precisely opposite to each other. This is difficult to achieve in a nanowire device geometry. Utilizing vertical nanowires poses additional practical difficulties. Lateral nanowires fabricated from thin films might be suitable. But, **top-down** fabrication approach of III-V semiconductor materials is found to degrade the transport properties of the materials[7]. In order perform carrier transport characterization on III-V nanowire structures, one has to develop an approach that compensates for its prohibitive architecture and replace the top-down fabrication approach. In this work, a novel and stable approach is developed to overcome both of the above mentioned obstacles.

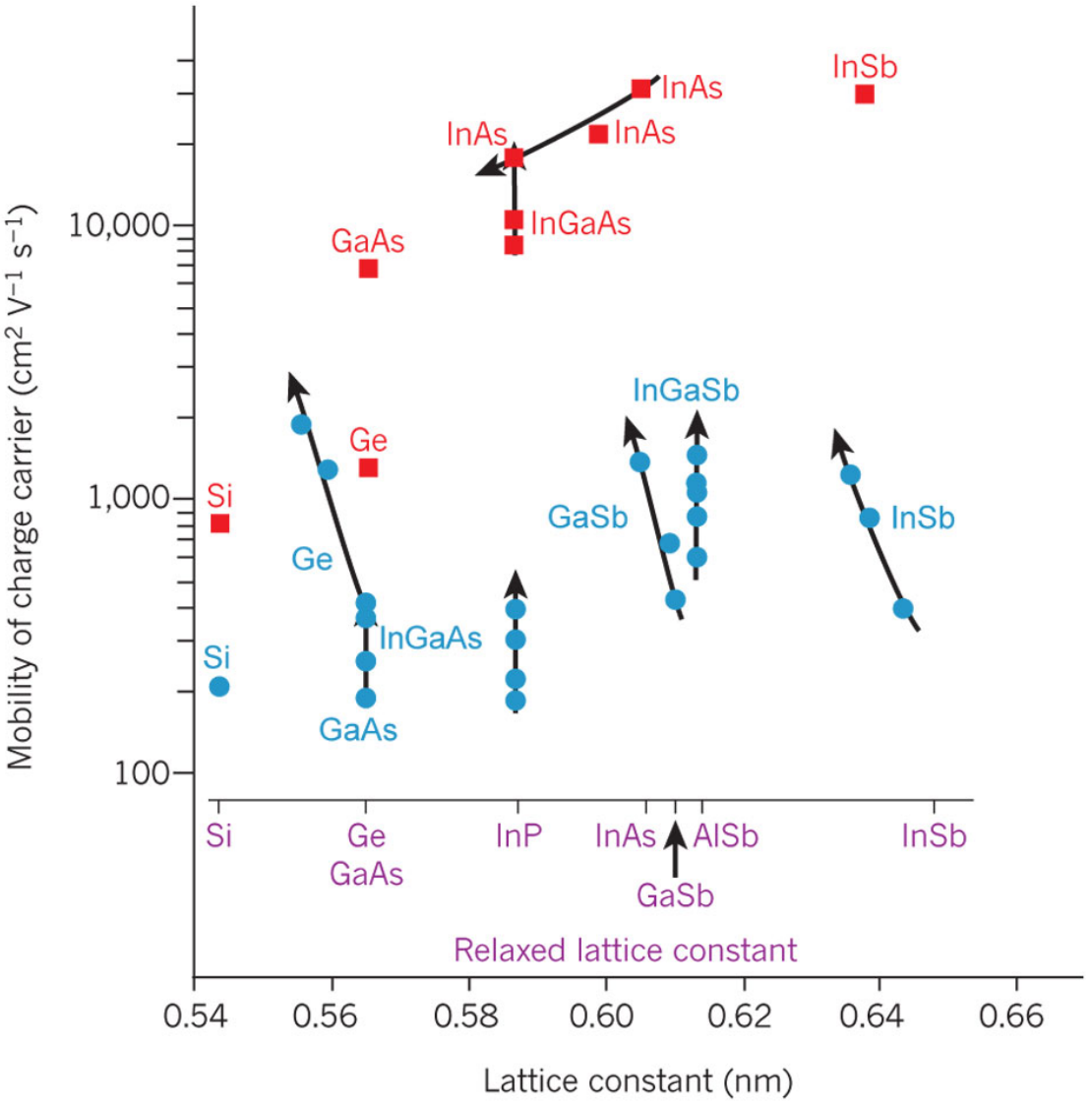


FIGURE 1.2: Electron and hole mobility in III-V compound semiconductors, electron mobility is represented by red dots and hole mobility by blue dots (adapted plot)[1].

Hall measurements were performed on single and multiple lateral *InGaAs* nanowires. Multiple nanowires in parallel provided a better signal-to-noise ratio. The nanowires were grown in a Hall Bar geometry which simplifies placing Hall probes that are precisely opposite to each other. And the novel **Selective Area Regrowth** is employed as a pattern transfer mechanism, since it has been proved to avoid scattering due to side wall roughness[7][8]. All the measurements were performed at room temperature and under similar experimental conditions. Apart from the noise in measurements, leakage current between the contact pads was dominant in Hall measurements on single nanowires. Hence substantial changes, both in device design and fabrication process were needed in order to reduce pad to pad leakage.

All steps of the fabrication process is performed at **LNL** and the Hall Measurement setup is custom built by Dr. Kristain Strom at FTF, Lund University.

Reader's Guide

The remaining chapters of this thesis is structured as follows.

Chapter:2-Background Theory and Motivation outlines the basic theory behind this thesis, like the Hall Effect and provides rationale for this work.

Chapter:3-Device Fabrication outlines the device fabrication techniques employed in both Generation-one and Generation-two.

Chapter:4-Experimental Setup is a brief account of the setup used for device characterization.

Chapter:5-Results and Analysis discusses in detail about the results obtained from the various measurements.

Chapter:6-Conclusion and Outlook states the conclusion drawn from the results and lays ground for future research.

Chapter 2

Background Theory and Motivation

In the past two decades, nanowire devices have procured indisputable research interest, both in academics and in the semiconductor industry. Nanowire device fabrication techniques have also been optimized and made reliable in recent times. Mesoscopic dimensions make nanowire devices the ideal candidate for investigating nanoscale physics. Thus, in a material science perspective, for investigating novel materials and novel properties of materials that are well established in the industry, nanowire device architecture is indispensable[9]. This chapter provides a brief introduction to III-V Semiconductor devices, bottom-up fabrication techniques and side wall scattering. It proceeds with a detailed account on selective area regrowth, rationale for material selection and the device geometry utilized. It concludes with a theoretical account on carrier transport, semiconductor Hall Effect and Hall Mobility.

2.1 III-V Compound Semiconductors

2.1.1 Power Constrained Scaling

Relentless scaling for more than three decades, pushed **Si-CMOS** technology into a state where it is now difficult to achieve an overall efficient scaling. Various operational characteristics like the sub-threshold slope and minimum voltage swing do not scale properly beyond a certain node[10]. As dimensions shrink, diverse tunnelling effects come into play and increase the static power leakage. Static power dissipation is more application specific and is tolerated to various extents depending on the application.

Applying the basic definitions of electric power, the static power dissipation in CMOS can be defined mathematically as follows,

$$P_{static} = I_{staticlkg} \times V_{supply} \tag{2.1}$$

Where $I_{staticlkg}$ is the leakage current and V_{supply} is the supply voltage of the transistor. In one way or the other, power dissipation constraints will bring an end to CMOS scaling. Roughly a decade ago, static power dissipation reached 100 W/cm^2 and as a result, important performance metrics have to be compromised in order to avoid device overheating[10]. Reducing the supply voltage to counteract the power dissipation lowers the drive current and hence, the performance[7]. The power is mostly dissipated in the form of heat, unless ultra efficient cooling systems are invented, power dissipation limits should be regarded seriously and alternative ways to sustain scaling must be considered.

2.1.2 III-V Alloys

"III-V Semiconductors" is a relatively popular name for the binary, ternary and quaternary alloys of elements from *group 13* and *group 15* in the **Periodic Table**. The alloys from this group have attracted a lot of interest since the birth of the Semiconductor Industry. Band-structure engineering in such alloys gives them very unique optical properties and hence, are used in lasers and optical communication systems[11]. Also, outstanding carrier transport properties of these materials help in improving the RF performance and are widely used in hand-held wireless communication devices, for example, the High Electron Mobility Transistors (**HEMT**) are used in various wireless communication devices. These semiconductor alloys when incorporated in **MOSFETs**, provide higher drive currents and improved electrostatic gate control at lower supply voltages in comparison to Silicon[12], thus making this group of semiconductors an interesting alternative.

2.1.3 Rationale for Material selection

Though III-V semiconductors have an edge over Silicon, selecting one among them is a question of balancing their physical properties and one that best serves the task at hand. The goal of this thesis is to quantify the carrier transport properties of III-V semiconductors, in a 1-Dimensional nanowire architecture. The material selected should be able to satisfy that goal. And the bigger picture behind all such academic exploration is to find a way to integrate novel materials to the well established Si-Platform. Silicon being an indirect band-gap semiconductor, suffers from transmission

loss within the Integrated Circuit. Integration of direct band-gap semiconductors like Indium Phosphide on silicon is proved to be an viable alternative[13]. The choice of InP as substrate material, is very well motivated even in a future perspective, where integration on Silicon platform is commercialized.

TABLE 2.1: Physical parameters of selected III-V binary and pseudo binary semiconductor alloys(μ_e is electron mobility, μ_h is hole mobility, $a_\circ$ is lattice constant and E_g is bandgap)

Material	$\mu_e(cm^2V^{-1}s^{-1})$	$\mu_h(cm^2V^{-1}s^{-1})$	$a_\circ(\mathring{A})$	$E_g(eV)$
GaAs	8500	400	5.65	1.42
$In_xGa_{1-x}As$	12000	300	5.87	0.74
InP	5400	200	5.87	1.34
InAs	40000	500	6.06	0.35

Electron and hole mobilities are important transport properties to be considered while characterizing a semiconductor material. In table. 2.1 if we consider electron mobility as a key parameter for material selection, Indium Arsenide stands out with the highest electron mobility. But, $InAs$ and InP are lattice mismatched semiconductors with a $\approx 3\%$ mismatch. Such a mismatch can be elastically tolerated in a vertical nanowire architecture[14]. But, high surface quality is crucial for fundamental physics research as explained in 2.2.1. So, it is better to avoid such lattice mismatches. The carbon allotrope *Graphene* has relatively high mobility, but lacking a band gap, it is considered incompatible to gated NW architectures.

Indium gallium arsenide, is the next material in the table to have high electron mobility. And the chosen substrate InP and $In_xGa_{1-x}As$ are lattice matched semiconductors; this helps in growing high quality epitaxial layers. Thattachary et al[7], employ Indium rich $In_{0.7}Ga_{0.3}As$ as channel material in a long channel gated Nanowire Field Effect transistor **(NWFET)** architecture with integrated Hall probes, and explains a quantitative technique for carrier mobility estimation. It also demonstrates ballistic transport of carriers over short channel lengths, though the channels have endured etch damage from the fabrication process. Carrier transport is predominantly ballistic over channels shorter or equal to electron mean free path and the gate length is no longer in control of the transistor `ON` current. $InGaAs$ **HEMTs** have also demonstrated a carrier injection velocity v_{inj}[1] about $2.3\times10^7(\mathrm{cm^2s^{-1}})$ at a supply voltage of 0.5 V. The `ON` current in a ballistic transistor depends on v_{inj}. So, the transistor can still produce high enough drive currents at low supply voltage without compromising switching speed. Hence the static power dissipation as given by Eq: 2.1 is reduced. This makes $In_xGa_{1-x}As$ an obvious choice for digital electronics and our cause.

[1]Carrier velocity at the highest energy in the conduction band

2.2 Semiconductor Nanowire Devices

More research funding and personnel is being dedicated to optimize the production method of nanowires. Interesting carrier transport phenomena that are not seen in the bulk, can be found at nanowire dimensions[9]. More and more devices are found to be incorporating nanowires as the channel material due to their unique transport properties. Apart from transport properties, NWFET's pave way for new device architectures like *Gate all around* structure for better electrostatic control over the transistor channel[15]. There are several optimal ways to grow a perfect nanowire structure, but all of them fall into one of the two genres of **Growth Techniques**, either *Bottom-up* or *Top-down* processing. Both of the growth techniques have their own advantages.

The **Top-Down** growth technique is more suitable for lateral and relatively bigger nano-structures, as the process relies mostly on optical lithography and wet etching. Optical lithography has been the backbone of device integration since its invention. The resolution of the process greatly depends on the wavelength of the light source used for exposure. Advanced techniques like **UVL** (*using UV light*) or **XRL** (*using X-rays*) can be used when a resolution of around 1 nm is required. But, as wet etching is used to define the device structures at some point during the processing, the surface quality of these nano-structures tends to be poor. Surface roughness or surface states are induced either during the growth or in post processing[16]. Sub-50 nm structures are prone to surface roughness induced states and carrier scattering arising from such states. In terms of Fundamental Physics research, such scattering plays a dominant role and masks the advantageous electrical properties like carrier mobility[7].

The **Bottom-up** fabrication technique follows nature's way of building, integrating many small units into a bigger structure. Bottom-up fabrication relies on device definition by various types of epitaxial growth techniques. The most common production process used is the VLS[2] process, in which vapour phase precursors are used as growth materials. Surface roughness/damage can be avoided by either protecting the device during wet etching or not using etching during device processing. Consequently, bottom-up approach is preferable when surface quality is of utmost importance as in our case.

2.2.1 Selective Area Regrowth

Both the genres of nanowire growth seem to have their own set of advantages. Top-down processes have been the primal cog in the production line of the semiconductor

[2]Vapour-Liquid-Solid systems

industry for a long time. But due to aggressive scaling off late, in the near future, top-down industrial standards have to join hands with the bottom-up processes to avoid stagnation. An alliance between these two genres is not a novel idea, **DSA**[3] of co-polymer masks combined with epitaxial growth is capable of producing high density, high throughput nano-structures with high resolution[17]. Though **DSA** has already proved to be fruitful, it is still far away from being put to commercial use.

Selective Area Regrowth is such a synergy between the two approaches. High surface quality is ensured by using *bottom-up* epitaxial growth[8]. So the scattering mechanisms and the consequent reduced carrier mobility can be counteracted.

The following is an simple outline of the *selective area regrowth* process. A clean semiconducting substrate is spin-coated[4] with a high resolution E-Beam resist[5], for example HSQ[6]. The desired pattern is defined on the resist with the help of EBL as shown in Fig. 2.1.

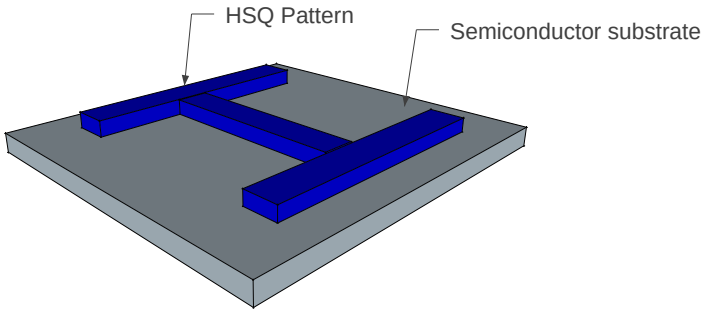


FIGURE 2.1: Schematic illustration of Selective Area Regrowth (semiconducting substrate with HSQ lines on top of it).

The resist is developed with a suitable developer and will serve as the *regrowth mask*. The substrate is then subjected to epitaxial growth, as in our case a typical metalo-organic vapour phase epitaxy chamber (**MOVPE**) with suitable precursors. The key is to select an E-Beam resist that can withstand the high temperature environment of **MOVPE** reactor. HSQ can handle high temperatures because once cured, it turns in to stable silicon di-oxide. Growth takes place on the substrate in between the HSQ mask

[3]Directed Self Assembly
[4]Spin coating is a process in which a liquid is spread over a flat uniform surface through centrifugal force.
[5]a special polymer mixture used for pattern transfer in lithography
[6]Hydrogen silesquixone

as shown in Fig. 2.2. The HSQ is then etched away using a buffered oxide etch and the transferred device pattern is revealed as shown in Fig. 2.3.

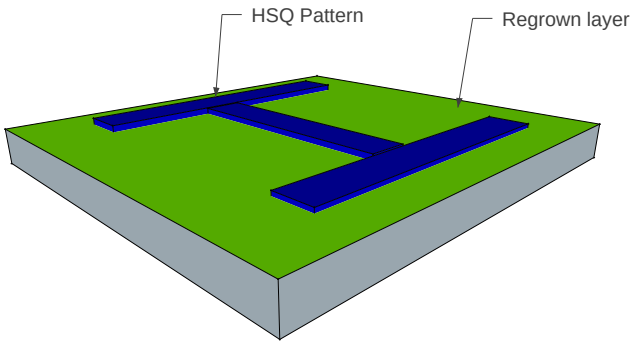


FIGURE 2.2: Schematic illustration of Selective Area Regrowth (semiconducting substrate with a regrown epitaxial layer).

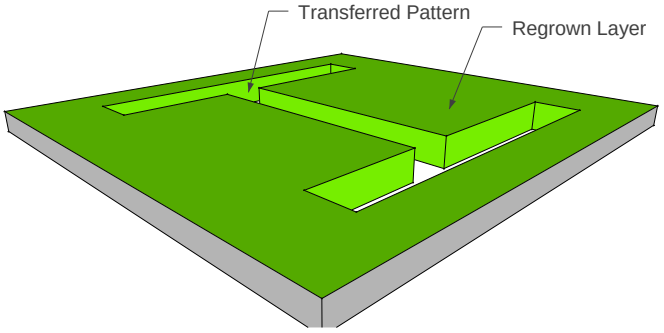


FIGURE 2.3: Schematic illustration of Selective Area Regrowth (HSQ etched away to reveal pattern).

This regrowth process can be repeated or the substrate can be subjected to further device processing as required[8]. A detailed description of the Selective area regrowth process specific to this thesis will be discussed in the *Device Fabrication* section.

2.3 Device Design

Accurate carrier transport studies rely on quantitative measurement of charge carriers, which can only be obtained from Hall Measurements. Device design plays a pivotal role in obtaining accurate Hall Voltage; the Hall probes must be placed perfectly opposing each other. Lithographically placing such probes and trying to make proper contacts is not impossible but a tedious task. Such probe electrodes have already been realized on single *InP* core-shell nanowires to perform spatially resolved Hall measurements[6]. As the device design is defined by EBL, it was easy to alter the design and it evolved with time and feedback from the measurements.

2.3.1 Generation-one - Single *InGaAs* NW with 50 nm isolation between probes

Generation-one devices are enclosed inside a 500×500 μm^2 square. This boundary also serve as electrical isolation between the source and drain contact pads. Fig. 2.4a shows a zoomed SEM image of a NW with Hall probes after regrowth. The integrated Hall probes are isolated from each other and from the source and drain pads by a 50 nm wide semi-insulating *InP* valley. This valley was defined by a HSQ mask before regrowth, represented by the red polygons in Fig. 2.4b. As there is a compositional symmetry between source and drain pads, they can be used interchangeably. There are two pairs of Hall probes opposing each other meeting the nanowire at a lateral angle of 45°. This is done so that the growth facets align as intended and there is no overgrowth on the HSQ mask[8].

2.3.2 Generation-two - Multiple *InGaAs* NW with 1.5 µm isolation between probes

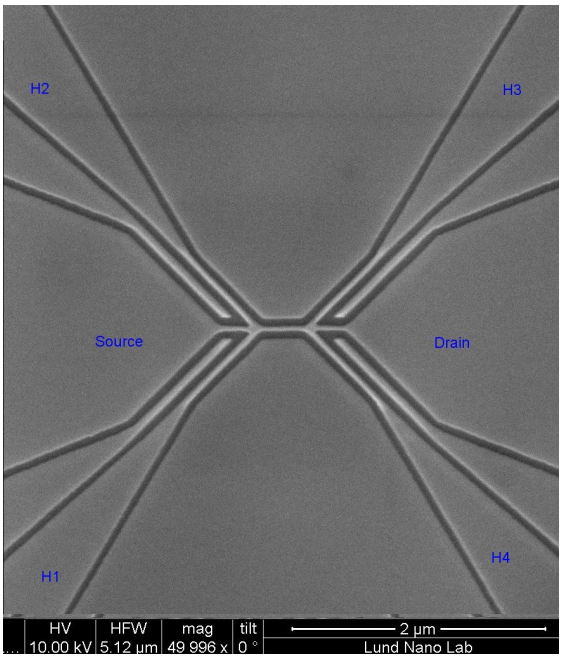
Generation-two devices are not enclosed inside a border, instead the residual *InGaAs* film after regrowth is etched away by a mesa wet etch. Fig. 2.5 shows a zoomed in image of the NW with integrated Hall probes after contact metal deposition. The spaces in between the nanowire and contacts consists of semi insulating *InP* substrate that serves as isolation between the contacts.

2.4 Electrical Properties of Semiconductors

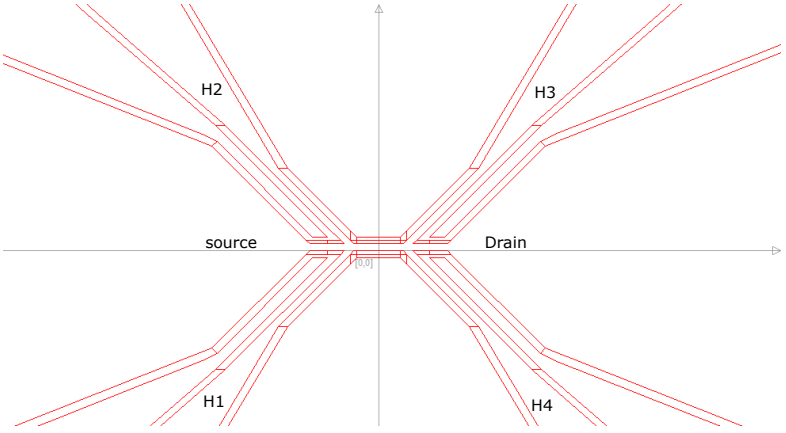
The basic electrical properties of the semiconductors like carrier transport, resistivity, conductivity, sheet resistance and Semiconductor Hall Effect (**SHE**) will be treated mathematically in this section.

2.4.1 Transport of Charge Carriers

In a semiconductor two types of carrier transport phenomena occurs, the motion of carriers due to an external electric field is called **carrier drift** and the current due to such motion as **drift current**. The carrier transport due to thermal difference is called **carrier diffusion** and the respective current as **diffusion current**. Both transport phenomena contribute to the total current in a semiconductor[18]. Since there is no



(A) Scanning Electron Microscopy image of a Generation-one device showing the nanowire and the Hall probes after regrowth.



(B) Generation-one mask design, the red polygons represent the HSQ lines. H1, H2, H3 and H4 represents the Hall probes

FIGURE 2.4: Generation-one device design.

intentional temperature gradient involved in our analysis, carrier drift is assumed to be dominant.

Let us consider an uniform semiconductor of length l, width W and thickness t, carrying a current I, under the influence of an applied electric field strength $\mathbf{E}$ as shown in Fig. 2.6.

Assuming that there is no difference in mass between the different types of charge carriers, all of them shall travel with the same average drift velocity $\boldsymbol{\upsilon}$ under equilibrium. Then the current flowing through the semiconductor can be given as follows[19],

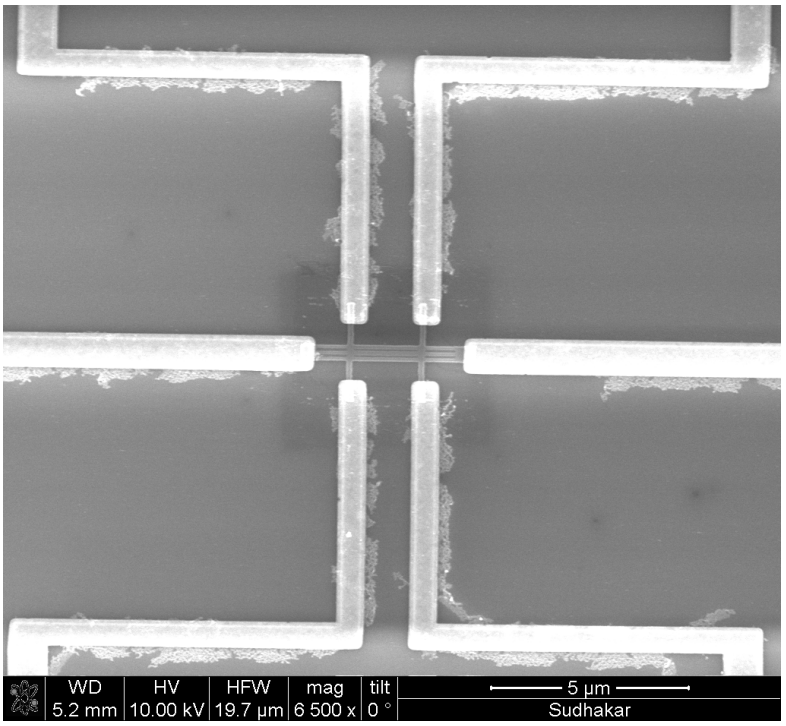


FIGURE 2.5: SEM image of a Generation-two device after contact metal deposition, showing the NW and Hall probes).

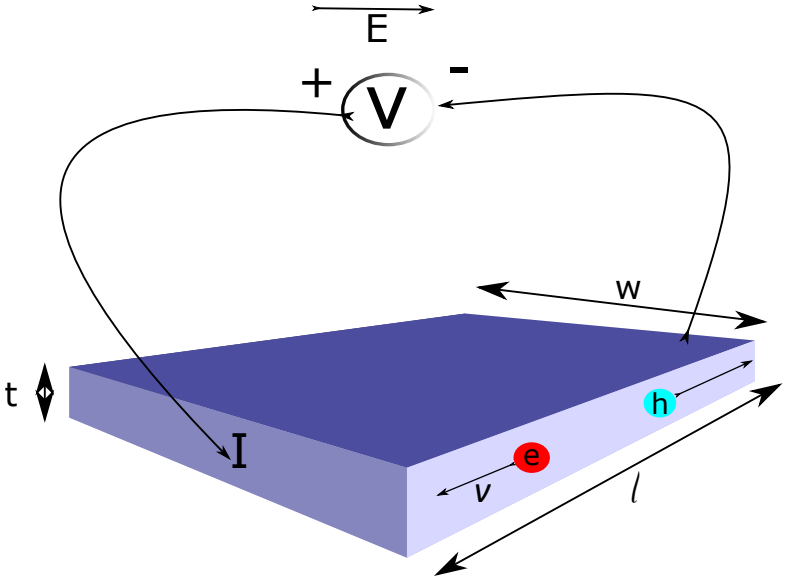


FIGURE 2.6: Schematic illustration of carrier drift in a semiconductor under the influence of an applied field.

$$I = \frac{Q}{\tau} \tag{2.2}$$

where Q is the total charge in the semiconductor and τ is the time needed for a charge

carrier to travel from one electrode to the other. The transit time in terms of length and average velocity is,

$$\tau = \frac{l}{\boldsymbol{\upsilon}} \tag{2.3}$$

Combining eq: 2.2 and 2.3

$$I = \frac{Q\boldsymbol{\upsilon}}{l} \tag{2.4}$$

The current density **J** is defined as the amount of current flowing per unit cross-sectional area of the semiconductor[20].

$$\mathbf{J} = \frac{I}{tW} \tag{2.5}$$

Substituting eq: 2.4 in eq: 2.5,

$$\mathbf{J} = \frac{Q\boldsymbol{\upsilon}}{ltW} \tag{2.6}$$

The total charge divided by the volume of the semiconductor can also be written as elementary charge q times the carrier concentration η[18].

$$\mathbf{J} = q\boldsymbol{\upsilon}\eta \tag{2.7}$$

The mobility μ of charge carriers is technically defined as the average drift velocity of the carriers per unit applied electric field[21].

$$\mu = \frac{\boldsymbol{\upsilon}}{\mathbf{E}} \tag{2.8}$$

Substituting $\boldsymbol{\upsilon}$ in terms of carrier mobility in eq: 2.7,

$$\mathbf{J} = q\eta\mu\mathbf{E} \tag{2.9}$$

A more basic definition states that the conductivity σ of a semiconductor material is the current density per unit applied electric field[22]. By that definition,

$$\sigma = q\eta\mu \tag{2.10}$$

The resistivity ρ of the material is the inverse of its conductivity by definition,

$$\rho = \frac{1}{q\eta\mu} \tag{2.11}$$

Hence the mobility of the semiconductor material can be derived from the above equations as,

$$\mu = \frac{1}{q\eta\rho} \tag{2.12}$$

Substituting sheet the carrier density $\eta_s = \eta t$ instead of bulk carrier density in eq: 2.12, the carrier mobility becomes,

$$\mu = \frac{t}{q\eta_s\rho} \tag{2.13}$$

The sheet resistance R_s of the semiconductor material is defined as the ratio between resistivity and the thickness of the material[23], then eq:2.13 becomes

$$\mu = \frac{1}{q\eta_s R_s} \tag{2.14}$$

2.4.2 Semiconductor Hall Effect (SHE)

The semiconductor Hall Effect was discovered by E.Hall in the year 1879. His experimental results were published in a crude form in the American Journal of Mathematics[24]. However its popularity shot up in the later half of the 19^{th} century when commercial integrated circuits started using Hall effect sensors and transducers[25]. Hall measurement is an indispensable tool to characterize semiconductors.

When a point charge q is travelling with an average velocity $\boldsymbol{\upsilon}$ perpendicular to the direction of an applied magnetic field $\mathbf{B}$ and in the direction of applied electric field $\mathbf{E}$, the point charge will experience a **Lorentz Force F**, acting perpendicular to the current direction. Its magnitude is as follows,

$$\mathbf{F} = q(\mathbf{E} + \boldsymbol{\upsilon} \times \mathbf{B}) \tag{2.15}$$

The Lorentz force **F** deflects the point charge from its path and creates an imbalance in charge distribution. The Hall effect is a result of Lorentz force; in a semiconductor of finite dimensions, the deflected charges should accumulate at one of the boundaries. Such accumulation gives rise to a potential build-up called the **Hall Voltage** V_H inside the semiconductor[26].

Let us assume that a current I is flowing through a semiconductor slab of length L, thickness t and width w as shown in Fig. 2.7.

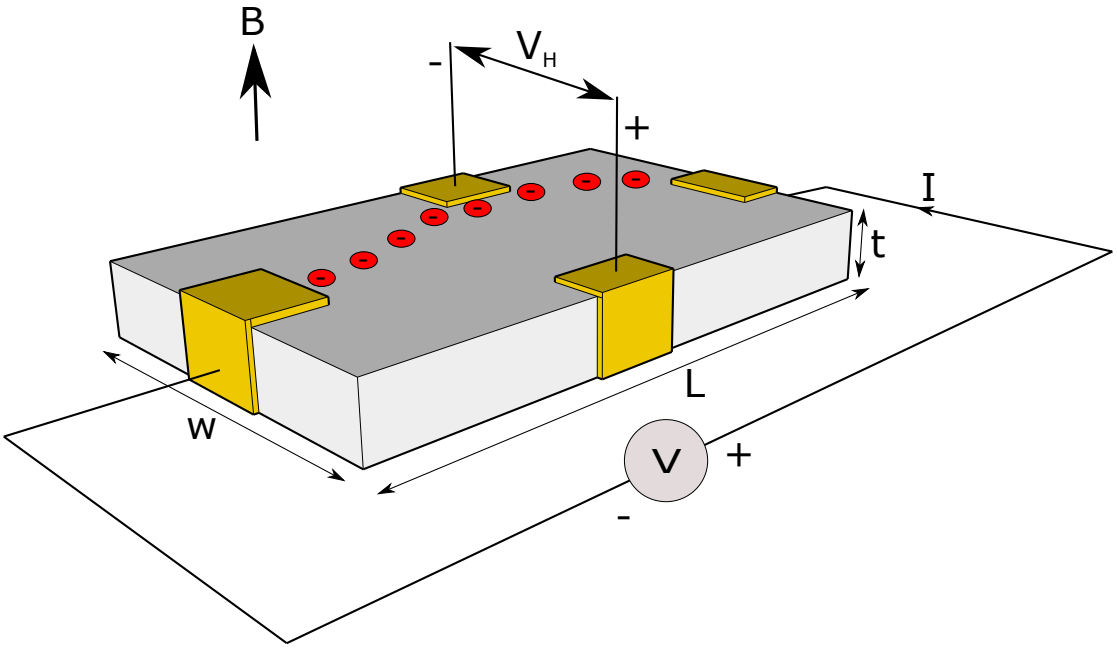


FIGURE 2.7: Schematic illustration of Hall Effect. The electrons are experiencing a Lorentz force under the influence of an applied magnetic field. Charge depletion and accumulation creates a Hall voltage V_H.)

The magnetic field **B** is acting perpendicular to the semiconductor plane, the charge carriers(in our case electrons) are experiencing a Lorentz force perpendicular to both the applied electric field **E** and the magnetic field. With two opposing electrodes placed in a line perpendicular to the direction of current, on the semiconductor slab as shown in Fig. 2.7, asymmetry in charge distribution gives rise to a Hall voltage V_H whose magnitude is given as follows[23],

$$V_H = \frac{I\mathbf{B}}{q\eta_s} \tag{2.16}$$

where η_s is the sheet carrier density, whose relation with the carrier concentration can be deduced from eq. 2.13. Besides the sheet carrier density is often used owing to the fact that it is independent of any physical dimensions. So, the sheet carrier density in

terms of Hall voltage is given as follows,

$$\eta_s = \frac{I\mathbf{B}}{qV_H} \tag{2.17}$$

Once the η_s value is calculated from the above equation, the charge carrier mobility can be deduced from eq: 2.14.

2.5 Contact Material

From an electrical characterization perspective, selecting a suitable contact material is very important. At nanoscale device dimensions, current density increase tremendously and poor contacts lead to an increased circuit *time constant*. An ideal contact material should be ohmic with minimal contact resistance and shouldn't add a DC voltage drop to the measurement circuitry. Fortunately, extensive research has already achieved fruitful results in this regard for an n-type $InGaAs$. Contact resistivity as low as 0.004 Ω/mm has been reported for n-type $InGaAs$ with Ti/Pd/Au (Titanium, Palladium and Gold) after special surface treatment[27]. Such low resistivity involves subjecting the material to special surface treatment. But in general, Ti(Pd)/Au top contacts is proven to give both low contact resistance and form ohmic contacts[28]. So, Ti and Au were selected to be the contact materials and were used for all the samples.

2.6 Summary

1. Power constrained CMOS scaling is the main motivator behind most of the innovative research in the semiconductor industry.
2. $In_xGa_{1-x}As$ has excellent transport properties and when used as transistor channels, it can produce high drive currents at low supply voltages, thereby reducing, static power leakage.
3. Selective Area Regrowth is a novel method that combines both top-down and bottom-up fabrication techniques.
4. Performing Hall measurement on semiconductors is an indispensable material characterization technique.

Chapter 3

Device Fabrication

This chapter explains the device fabrication process of both *Generation-one and two* Hall devices, as developing a reliable fabrication process was a primary motivation for this work. In total, 24 different batches were fabricated each with different number of samples varying from 1 to 3. Out of these 24 batches, 20 batches belong to Generation-one and the remaining 4 batches belong to Generation-two. The differences between the fabrication process were discussed briefly in Chapter.2. So, only the very important processes like E-beam lithography and thin film growth are explained in this chapter.

3.1 Fabrication process - Generation-One

The processing for the most part is common for both the generations, only varying at some process steps.

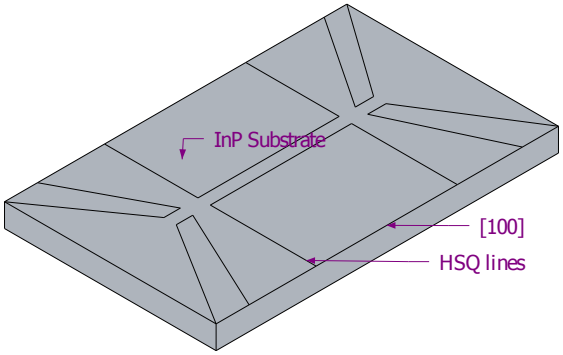
3.1.1 Electron Beam Lithography

Electron Beam Lithography is considered to be the basis of ultra high resolution and high density nano-fabrication. It is used to pattern high resolution nano-structures directly on to the substrate and also fabricate master masks for other high resolution lithography techniques like nano-imprint lithography and EUV etc[29].

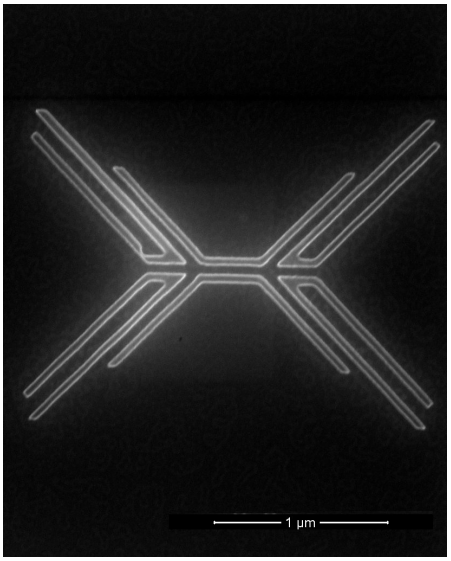
Our fabrication process starts with an epi-ready[1] 8×10 mm^2 *Fe-InP*(100) substrate. The substrate is pre-cleaned with ozone and spin-coated with hydrogen silsesquioxane (HSQ) diluted in Methyl isobutyl ketone (MIBK) at a ratio of (1:3/HSQ:MIBK). The

[1] epitaxy ready wafer with polished surface.

substrate is then loaded onto the Voyager commercial EBL system. HSQ is a high resolution negative tone resist, and after the first EBL exposure the patterned areas of the HSQ will cross-link and transform into a less soluble silicon di-oxide (SiO_2). Once after the exposed pattern is developed in Tetramethylammonium hydroxide (TMAH) the partial SiO_2 lines will serve as the regrowth mask as shown in Fig. 3.1.



(A) Illustration of the Fabrication process. An InP substrate with HSQ lines after the first EBL exposure. The NW will be parallel to [100] facet after regrowth.



(B) SEM image of HSQ lines after EBL exposure

FIGURE 3.1: Generation-One device fabrication

The HSQ lines in the pattern were (50±5) nm and the space between the lines ranged from (50±5) nm at the nanowire and gradually extends up to 200 µm at the contact pad.

3.1.2 Nanowire Selective growth

All the lateral nanowires in this thesis were grown in an Aixtron AIX 200/4 MOVPE by my practical coach and supervisor Mr. Cezar Zota. The patterned substrate is cleaned with diluted HCl and then transferred to Aixtron AIX 200/4 planetary horizontal MOVPE with its patented Gas Foil Rotation system; a schematic illustration is shown in Fig. 3.2.

The laminar flow design of the reactor avoids turbulence in the gas phase and ensures high reproducibility and uniformity[30]. The substrate was annealed to 500°C; unless otherwise stated this is the growth temperature used in this work. This is because at this growth temperature $InP/InGaAs$ is reported to exhibit good electrical characteristics[31].

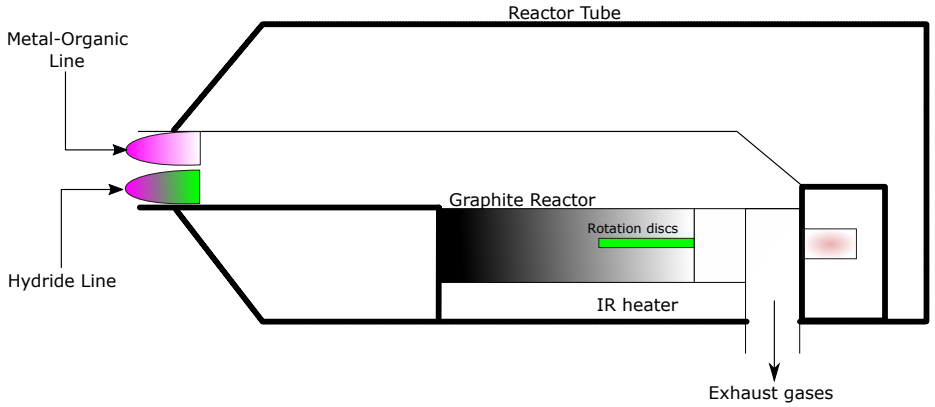


FIGURE 3.2: Schematic illustration of the AIX 200/4 Reactor.

TABLE 3.1: Precursor flow rates for selectively growing *InGaAs* thin films.

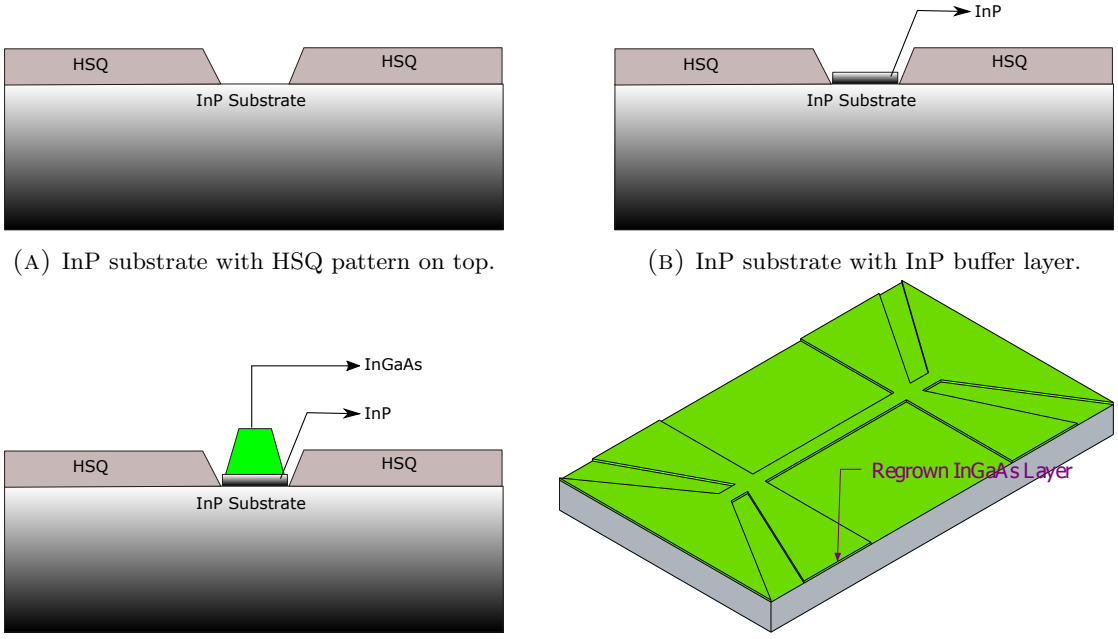
Precursor	Flow rate(µmol/min)
Trimethylgallium **(TMGa)**	25
Trimethylindium **(TMIn)**	46
Arsine (AsH_3)	6690

Purified hydrogen was used as the carrier gas, flowing at a rate of 625 µmol/min. The metal-organic precursors used in this process are Trimethylgallium **(TMGa)** and Trimethylindium **(TMIn)**, while Arsine **(AsH_3)** and Phosphine **(PH_3)** are the hydrides used. Initially TMIn and PH_3 lines are opened and a 4 nm *InP* buffer layer is grown in between the patterned HSQ lines. This is to isolate the defects in the substrate from the conducting channels. Then the PH_3 is switched with AsH_3 and the TMGa line is opened to grow an additional 16 nm of $In_{0.51-0.53}Ga_{0.49-0.47}As$ layer on top with a V/III ratio of 94. The regrown layer is not intentionally doped, as no dopant precursor was used during regrowth. There is no growth observed on the HSQ itself. The regrowth is illustrated by the Fig. 3.3.

3.1.3 Contact Layer

After regrowth, the HSQ lines are removed by an BOE *(Buffered Oxide Etch)* to form the isolation lines between the conducting *InGaAs* channels. The *InP* substrate is etched by a few nanometers to provide better contrast in the subsequent EBL exposure. Then the substrate is again spin-coated with a PMMA[2] double layer and loaded into the EBL Voyager for contact layer patterning. PMMA is a positive tone resist, so after exposure the the long polymer chains are broken down into smaller links that are easily soluble[29]. A double layer resist is used to create a unique profile which helps in lift-off after metal deposition. The substrate is then developed in Methyl isobutyl

[2]Poly methylmethacrylate



(A) InP substrate with HSQ pattern on top.

(B) InP substrate with InP buffer layer.

(C) InP substrate with epitaxial InGaAs on top of the buffer layer.

(D) Top View: InP substrate with epitaxial InGaAs on top of the buffer layer.

FIGURE 3.3: Schematic illustration of the selective area regrowth in an orthographic view.

ketone (MIBK): Iso-propyl alcohol (1:3) solution. After development, the substrate is cleaned with an oxygen plasma to get rid of the resist-residues. The substrate is then immediately loaded into the AVAC Evaporation chamber. Once the chamber is pumped down using a turbo pump, 10 nm of Titanium is thermally evaporated which is followed by another 90 nm of Gold as shown in Fig. 3.4. Titanium, apart from being a good contact material, it also promotes adhesion of gold[28]. And the metal layer thickness was kept constant for all samples, in both the device generations.

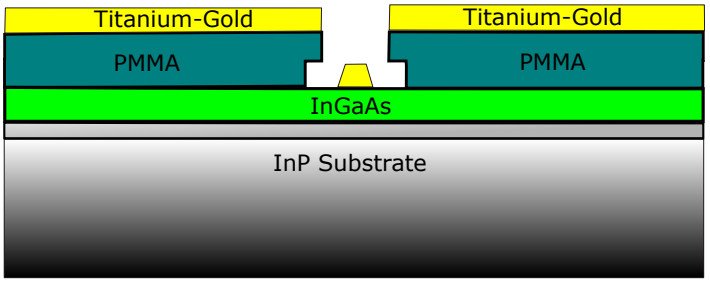
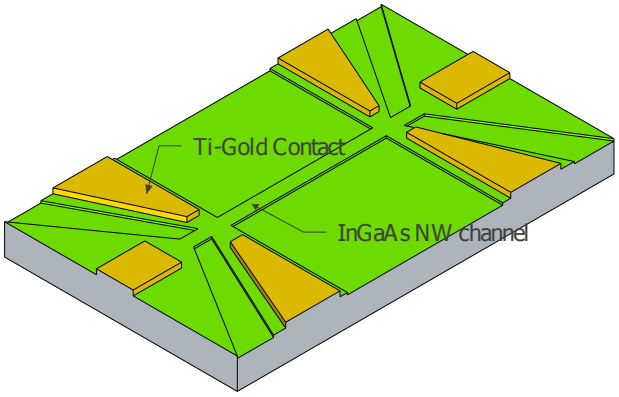


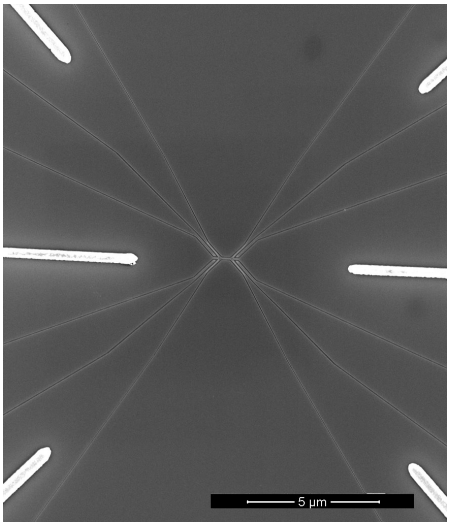
FIGURE 3.4: Illustration of contact metal layer being deposited on top of patterned PMMA. The undercut profile of PMMA is clearly visible in the illustration.

Metal deposition is followed by dissolving the PMMA under the metal layer. This is called **lift-off** and is achieved by placing the substrate in acetone for 12 hours; such a long time is required as the solvent should act on the resist via the undercut profile.

The solvent dissolves PMMA thereby releasing the deposited metal. Only the metal deposited directly to the substrate stays while the rest floats away. This happens as the thermally evaporated metal diffuses into the substrate for a negligible distance forming a nice contact layer. But once the resist is dissolved, there is no adhesion and this lifts the deposited metal up and hence the name *lift-off*. A completed Generation-one device is shown in Fig. 3.5.



(A) Illustration of contact metal layer after lift-off in acetone, the isolation between the conducting channel is less than 50 nm.



(B) SEM image of a completed Generation-one Hall device.

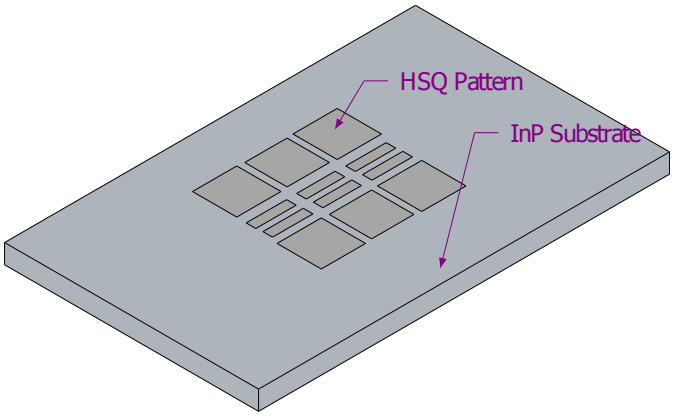
FIGURE 3.5: Generation-one Hall device.

3.2 Fabrication Process - Generation-Two

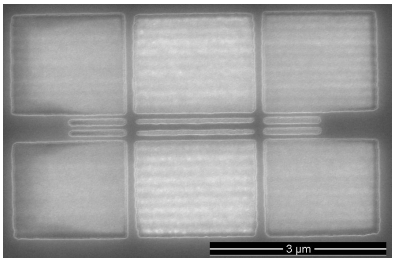
Generation-two Hall devices almost follows a similar fabrication process, but the new device design yielded positive results in terms of performance and reduction in leakage. A new design also required additional processing to keep the original idea intact. In generation-one devices, there was only ≈ 50 nm isolation between the conducting channels. Though the contact pads were separated by a relatively larger distance, it still lead to large leakage currents. So the new design should have adequate isolation to avoid such leakage signals. And having multiple nanowires instead of a single nanowire was found to improve the signal to noise ratio[7]. The mask design was modified to accommodate all the above mentioned changes. Instead of having the *InGaAs* thin films under the metal contact pads, the thin film was etched away everywhere except for the nanowire and Hall bars to provide better isolation. And three nanowires in parallel were used instead of one nanowire.

3.2.1 Electron Bean Lithography

Modifying the mask design with EBL was a simple task, as it involved making the necessary changes in the pattern file. The semi-insulating *InP* substrate follows a similar cleaning and resist coating as in generation-one. Then, after EBL patterning the substrate looks like Fig. 3.6.



(A) Illustration of InP substrate with Generation-two HSQ pattern.



(B) SEM image HSQ pattern on InP substrate after development in TMAH.

FIGURE 3.6: Generation-two Hall device fabrication process.

3.2.2 Nanowire Selective growth

Then the substrate is loaded in to the MOVPE reactor for regrowth. The regrowth process is similar to generation-one. After regrowth, the HSQ pattern is etched away and the substrate looks like Fig. 3.7.

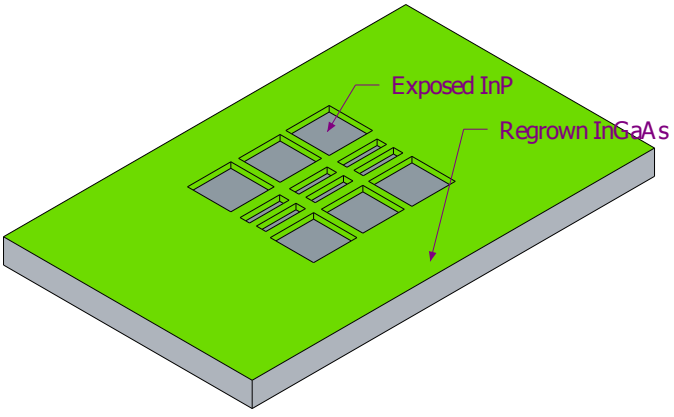


FIGURE 3.7: Schematic illustration of a Generation-two Hall device after regrowth of InGaAs.

The substrate is then subjected to HCl etching to remove a few nanometers of *InP* and HCl does not etch the regrown *InGaAs* layer.

3.2.3 Definition of mesa etch mask

The substrate is cleaned and then spin coated with undiluted HSQ. After spin coating, the substrate is loaded into the EBL voyager to define the etch mask. The purpose of this etch mask is to cover the area of interest so that the surplus *InGaAs* film can be chemically etched away. The second EBL pattern is just a rectangular area covering the nanowire and the Hall bars as shown in Fig. 3.8.

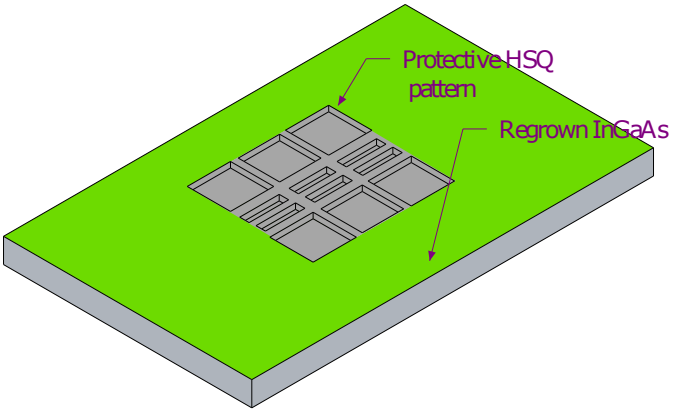
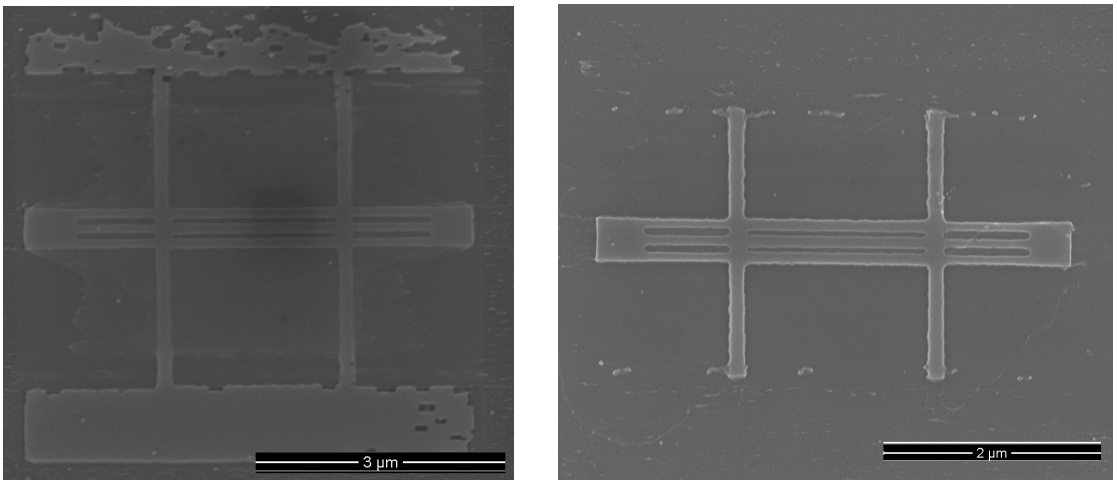


FIGURE 3.8: Schematic illustration of a Generation-two Hall device after an etch mask was patterned on top of the nanowire.

The residual *InGaAs* film is etched away with a solution of Hydrogen Peroxide : Phosphoric Acid : Water (1:1:25). Although the chemical etching is pretty accurate, the success also depends on proper placement of the protective HSQ pattern on top of the nanowires. Fig. 3.9a shows a SEM image of such a failure where the protective film has either moved or had an overexposure during the EBL.

The SEM image shows the Hall contacts on either side being short circuited, rendering the device useless in terms of Hall measurements. Fig. 3.9b shows another SEM image in which the etch mask has worked as intended. The free standing terminals of the Hall device will be contacted by metal in the subsequent steps.



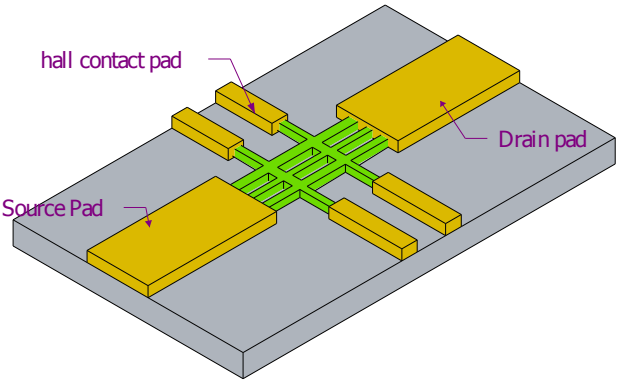
(A) SEM image of the substrate showing a failed mesa wet etch due to etch mask misalignment.

(B) SEM image HSQ pattern on InP substrate after development in TMAH.

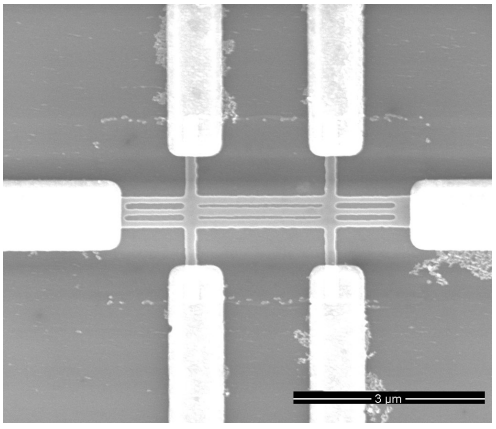
FIGURE 3.9: SEM images showing mesa wet etching of Generation-two Hall devices.

3.2.4 Contact Layer

The contact layer deposition is practically identical to Generation-one. The substrate is spun on with PMMA and patterned with EBL. Then Titanium-Gold bilayer is evaporated on to the substrate after an oxygen plasma cleaning. Fig. 3.10a shows a schematic illustration of completed device.



(A) Schematic illustration of a completed Generation-two Hall device.



(B) SEM image of a completed Generation-two Hall device with metal contacts on all pads. The PMMA resist residues are visible under the metal contacts

FIGURE 3.10: Completed Generation-two Hall device.

And Fig. 3.10b shows a SEM image of a completed device. The image also shows some resist residues under the metal contacts. This particular sample however was treated with oxygen plasma both before and after metal deposition, but failed to remove the

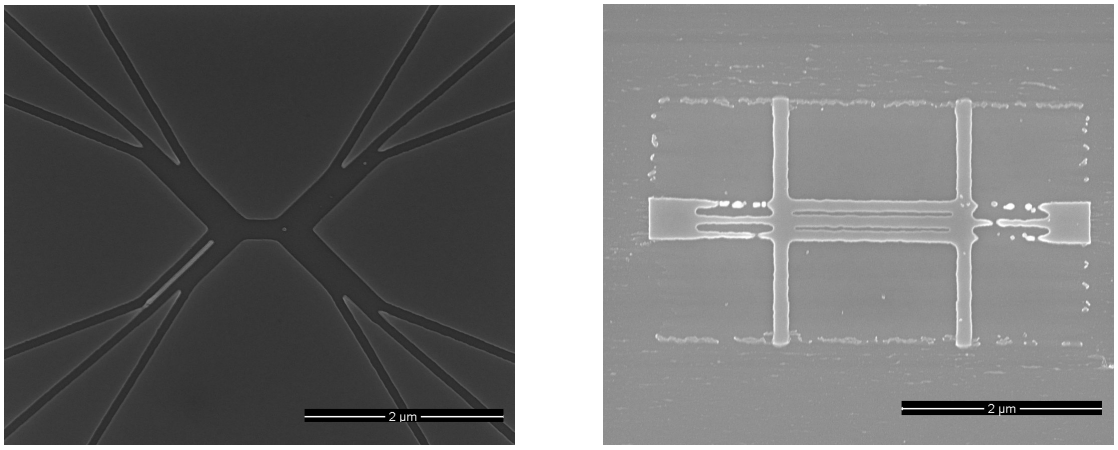
resist residues completely. Sufficient isolation is provided by the semi-insulating *InP* present in between the contacts.

3.3 Critical Issues in fabrication

There is always a probability for human error in any process involving a human operator. But in our fabrication process, apart from human error there were many parameters that needed precise control. This section addresses such critical issues which surfaced during the fabrication process.

3.3.1 EBL

Since all the mask patterns were designed and realised with EBL, the common parameters that affect the EBL exposure like exposure dose and pattern density came into play. The exposure dose affected the resolution while the pattern density gave rise to proximity effects. Apart from that, even a small change in the pattern required a dose test on a dummy substrate before it was used on an actual sample. The SEM images shown in Fig. 3.11 illustrates an overexposure due to improper exposure dose. It was also pretty challenging to asses the dosage for individual entities in the design, because when the entities come close together, proximity effect comes into play[29].



(A) SEM image of an overexposed Generation-one Hall device.

(B) SEM image of an overexposed Generation-two Hall device.

FIGURE 3.11: SEM images showing effect of exposure dose.

Apart from exposure dose, strenuous efforts were needed to align the subsequent EBL patterns to each other. This was due to the substrate material selected. The contact metal layer patterning required alignment of the current pattern to the previous pattern

of the *InGaAs* layer beneath PMMA. Under ideal conditions, this requires little effort to match the co-ordinate system of both the layers. But in our case, the *InGaAs* layer was only (14±2) nm in thickness, which was under more than 2 μm of PMMA resist. The poor contrast between the thin *InGaAs* layer and the *InP* substrate made it very difficult to align the layers to each other. Fig. 3.12 illustrates the above mentioned problem.

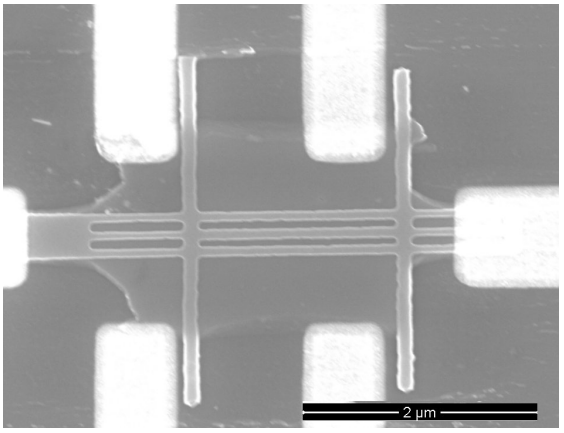


FIGURE 3.12: SEM image of a Generation-two Hall device with misaligned contacts.

Owing to these challenges, many samples belonging to both generations were not successful. Although dose assessment in EBL is a tedious process, it was solved with enough dose testing on dummy substrates. But alignment of subsequent EBL exposures was critical for a device to be successful. Many devices were deemed non-functional both before and after the contact metal deposition stage. Alignment with some samples were close to being impossible; the ones with a misaligned metal contact can't be processed any further.

3.4 Summary

1. Generation-one Hall devices had less than 50 nm isolation between the conducting pads.
2. Leakage signals dominated the generation-one devices due to its design.
3. A Generation-two Hall device is just an improved design with better isolation and additional processing.
4. Multiple wires in parallel were used in the second generation of devices to improve the signal to noise ratio.

Chapter 4

Experimental Setup

The motivation behind fabricating a Hall NW device, is to perform Hall measurements and characterize the transport properties in such complex architectures. This chapter gives a brief introduction about the experimental setup used to perform Hall measurements. It also explains how the sample was prepared for measurements. Both the Hall measurement setup and the control software was custom built at FTF. Though a cascade probe station was occasionally used to perform 4-Probe measurements, it was later replaced by the Hall setup without an active magnetic field.

4.1 Sample Preparation

After metal deposition, the substrate was cleaved into a suitable size and shape with the help of a scriber. The scriber is a diamond tip that can make precise cuts in a controlled manner. The device is operated manually by hand. A guide line is scribed on the sample at which it can be cleaved. After cleaving, the sample is mounted on a ceramic holder that looks like Fig. 4.1.

Colloidal silver paste is used to fix the sample onto the ceramic holder. This holder can be mounted on the socket present in the Hall measurement setup. After fixing the sample on ceramic holder, 0.25 µm gauge aluminium wire was used to make connections between contact pads of the device and the gold contacts on the ceramic holder using a bonding machine. Once connections were made, the ceramic holder is carefully mounted on to the socket in the measurement setup. The user is grounded at all times while performing the bonding and mounting. This is to avoid destruction of device by static discharge from the user.

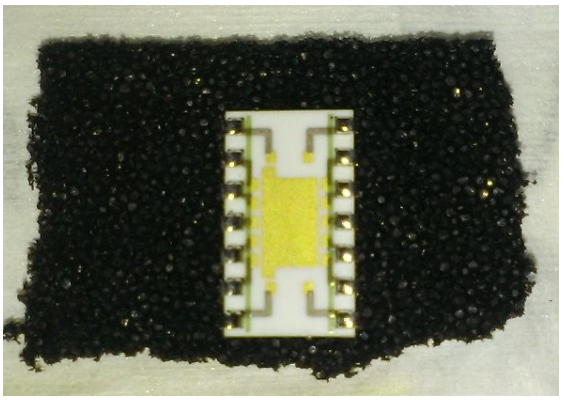


FIGURE 4.1: Picture of a ceramic holder with gold contact pads used to mount the Hall devices.

4.2 Hall Measurement Setup

The socket on which the ceramic holder is mounted can be positioned between two circular iron-core electromagnets. This way the sample plane is perpendicular to the magnetic field produced by the two electromagnets. The socket sits on a movable arm, that can be moved in and out of the magnetic field. The device orientation didn't matter as long as it is placed at the center of the two electromagnets. The socket houses cables from the relay controller. In order to switch the magnetic field values during measurement, large currents are pushed through the electromagnets, so the electromagnets were water cooled to protect the iron core from melting.

Fig. 4.2 depicts the measurement setup. The magnetic field is represented by **B** and is acting perpendicular to the sample plane. In order to perform Hall measurements, a constant current is passed through the *source* and *drain* terminals of the Hall device. Then the voltage across the Hall pairs are measured under the influence of the magnetic field sweep.

The current is sourced by Keithley 2602 source measure unit (SMU). The two channels of Keithley 2612 SMU is configured to sense the Hall voltage at the two Hall terminals. Both source meters are collectively addressed as SMU in Fig. 4.2. Only one opposite Hall pair (1-2/4-3) can be measured at a time with the Hall setup. The different Hall pairs can be selected via an electronic relay that is controlled by the Matlab program. The control program assigns the SMUs to the different relay positions and thereby to the contact pads. The two electromagnets are powered by a transformer that is controlled by Lakeshore DSP Gaussmeter. The transformer and the rest of the circuitry is isolated

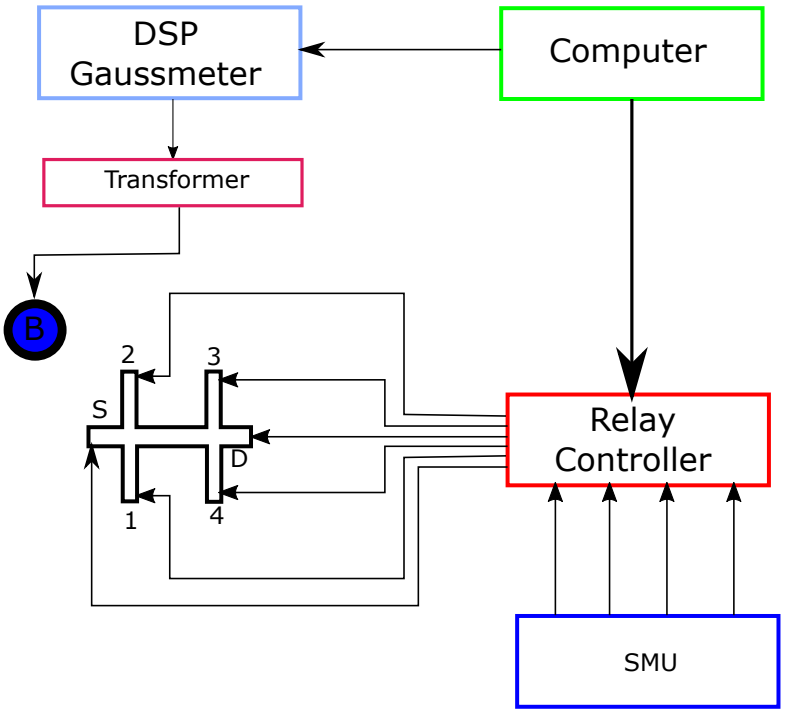


FIGURE 4.2: Schematic Illustration of Hall Measurement Setup.

from general power grid in order to avoid unwanted voltage spikes in the measurement setup.

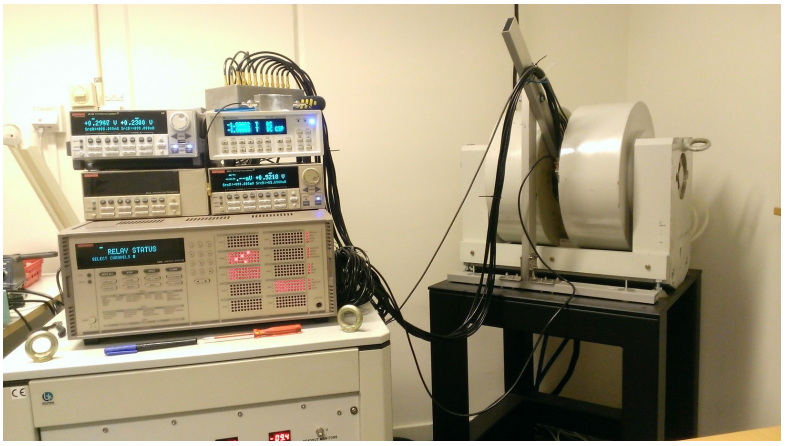


FIGURE 4.3: Custom built Hall Effect Measurement Setup.

The Gaussmeter can both sense and source magnetic field and is configured by the Matlab program. The magnetic field is swept non-sequentially between -2 T to 2 T in steps of 0.5 T. The magnetic field sweep starts at random multiple of 0.5 between -2 T and 2 T, and when its time for the next step, the magnetic field jumps to another multiple of 0.5 non-sequentially between -2 T and 2 T. A normal sweep tends to induce

a linear effect with time in the measurement. Non-sequential sweep of the magnetic field helps to verify the Hall measurement, so that such time-dependent effects seen during the normal sweep can be avoided. For each value of the magnetic field, 400 data points of the voltage are recorded. Once the magnetic field sweep is completed, the same process is repeated for a different value of current through the device. So multiple measurements were carried out on the same device using different Hall pairs and different values of current for computational accuracy. All measurements were carried out at room temperature.

4.3 Four-Probe Measurements

The same measurement setup was used to perform four-probe measurement in order to calculate the resistivity of the device. The magnetic field was switched off and a voltage sweep between -1 V to 1 V was applied between the *source* and *drain* contacts. Such a voltage sweep generates current along the NW. Then the voltage across the Hall probes on the same side (1-4/2-3) is measured. The same measurement was carried out with Hall probes on both sides of the sample. The resistance of the device can be found from a the I-V curve where V is the voltage difference between the two probes, from which the resistivity of the device can be calculated. The same Matlab control software is used in four-probe measurements as well.

Chapter 5

Results and Discussion

This chapter states the results obtained from the 4-probe measurements and Hall measurements performed on Generation-two Hall devices. The leakage data from both Generation-one and two is compared to establish the rationale for design modification. It also presents a critical analysis about the anticipated and obtained experimental results.

5.1 Resistivity Measurements

Resistivity measurements were carried out using a four-probe setup as previously explained. The purpose of extracting the resistivity profile of the device is to assist the calculation of transport parameters. As explained in section.4.3, the voltage between the two Hall probes is measured, while a voltage sweep of -1 V to 1 V is applied along the *source* and *drain* contacts. For simplicity, the Hall probe pairs on the same sides are named as *Hall pair 1* (1-4) and *Hall pair 2* (2-3). Fig. 5.1 shows the results of a sample device with single NW from Generation-one. The difference in voltage between the Hall probes on the same side is plotted against the current measured at the source contact. The slope of the curve gives the resistance of the device. The same measurement is performed with both the Hall pairs and the resistance vs Hall pair number is depicted as the sub-plot in Fig. 5.1.

The results from a similar measurement for another device from Generation-two can be seen in Fig. 5.2. The Generation-two devices are ≈75 % longer than that of Generation-one for design convenience. The current compliance for all the devices during four probe measurements was set to ±100 μA in order to avoid any accidental damage to the device. The *I-V* curves are relatively more linear in Fig. 5.2 and are of approximately equal magnitude in both forward and reverse bias. In theory, such characteristics are

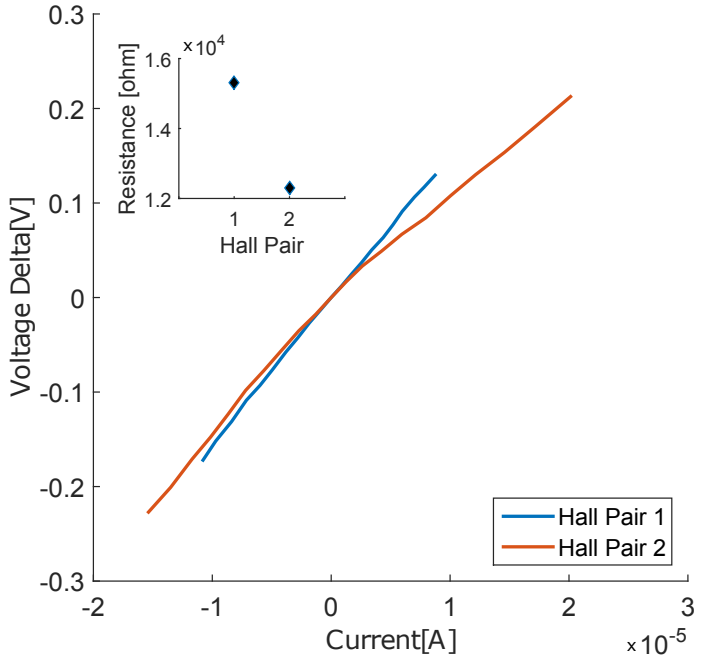


FIGURE 5.1: Results from four probe measurements carried out on single nanowire Hall device from Generation-one. A slope of the curves gives the resistance of the NW as shown in the sub-plot.

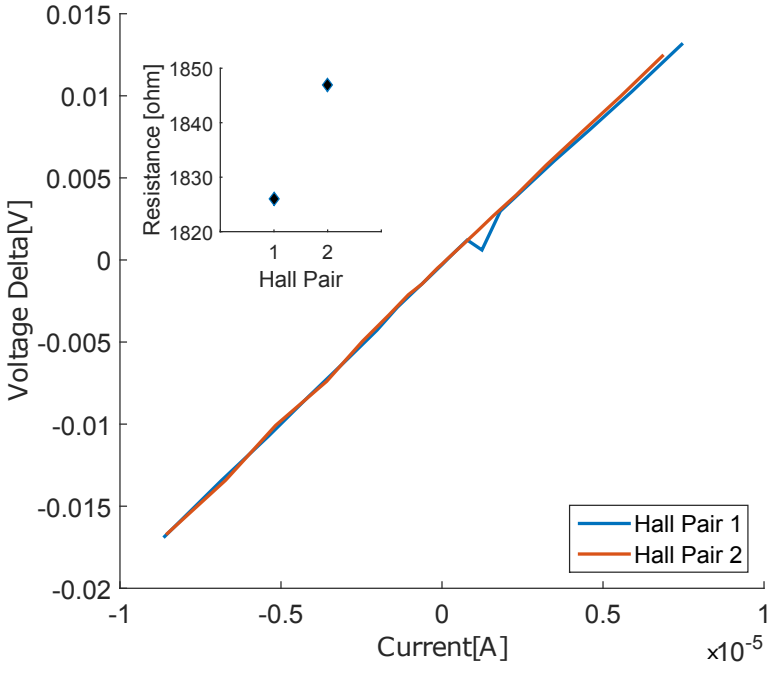


FIGURE 5.2: Results from four probe measurements carried out on multiple nanowire Hall device from Generation-two. Resistance vs Hall pair number are depicted as the sub-plot.

attributed to a proper ohmic metal-semiconductor contact[22]. A proper contact is very

crucial for accurate Hall measurements. The kink which is observed from Hall pair 1 data in Fig. 5.2, was seen in all the devices measured the same day. This might be an instrument artefact, however there is no adequate data to prove or disprove it. In Fig. 5.1 it is evident that device under forward bias conducts more current and also is non-linear. This might be due to the large surface area of the metal which is in contact with the semiconductor, and very small isolation between the different conducting channels. However, this generation of devices have very little relevance to the Hall results, as discussed in later sections.

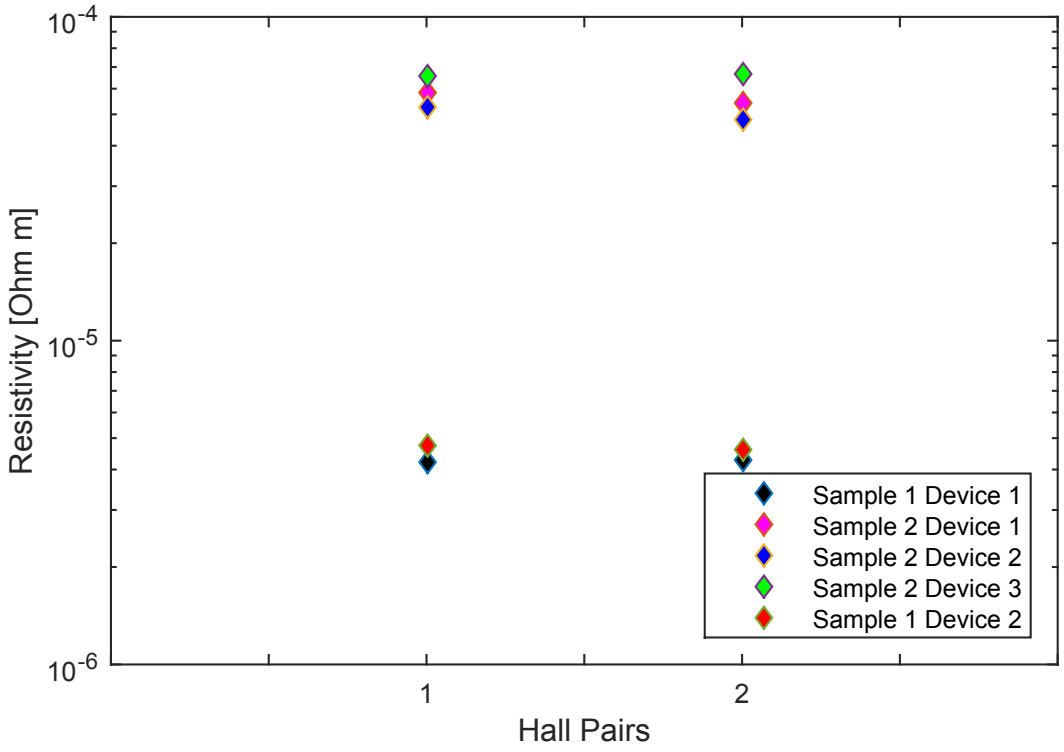


FIGURE 5.3: Resistivity values calculated for devices from two different samples plotted against the Hall pair numbers.

The resistances obtained from plots similar to Fig. 5.2, are used to calculate the resistivity using the equation. 5.1, where ρ is the resistivity, R is the resistance obtained from the plots, A is the cross-sectional area of the device and L is the distance between the two Hall probes on the same side.

$$\rho = \frac{RA}{L} \tag{5.1}$$

The effective width of the device (distance between the two Hall probes opposing each other) was calculated from the SEM images of all the devices. The thickness of the reference samples was measured using X-ray diffraction, which will be the height of the NW. The resistivity thus calculated from eq. 5.1 is plotted against the Hall pair number as shown in Fig. 5.3. The resistivity varies among the two samples by almost one order of magnitude; there might be various reasons for this. Although both the samples were subjected to growth at the same cycle in the MOVPE reactor, they were processed into a final device at different times. Any unintended variation during processing or an offset in the metal contacts might induce such differences. The regrown layer was not intentionally doped and is slightly doped only by the impurities present in the crystal lattice. Any contrast in the impurity concentration between the two samples might also be the reason for the difference in resistivity. Since, there is no relevant data about the un-intentional doping, it is difficult to draw conclusions about the low values of resistivity. Measurement error associated with instrument setup should also be considered. However, the prime motive behind resistivity measurements is to use the values thus obtained for calculating transport parameters like mobility. So, the average between the two Hall pair resistivity is used for calculating the respective mobilities.

5.2 Leakage Measurements

Leakage current was a major concern as it introduced a spread in the measured Hall voltages.

So acquiring a quantitative idea of the same was crucial in order to establish a proper strategy for further calculations. Leakage measurements were carried out between different contact pads of the same device and also between different devices on the same sample. A voltage sweep between -1 V to 1 V was sourced between two pads and the resulting current was measured. The process was same irrespective of the type of contact pad. Fig. 5.4 shows a representative leakage measurement of a Generation-two device. In this case the leakage was measured between the two Hall contacts (2-3) and between adjacent devices. The leakage curve between the pads is substantially linear as expected. It is evident that the current takes the only available path through the device. The crude resistance of the device path calculated from the I-V curve is in close agreement with the four-probe measurements. The leakage curve between the device is a straight line close to zero as the space between the devices is semi-insulating InP.

When mesa wet etching of the $InGaAs$ thin film is skipped and the devices are left with inadequate isolation between them, the leakage curves looks as shown in Fig. 5.5. The leakage curve for pad leakage is partly linear but around 0.4 V in both forward and

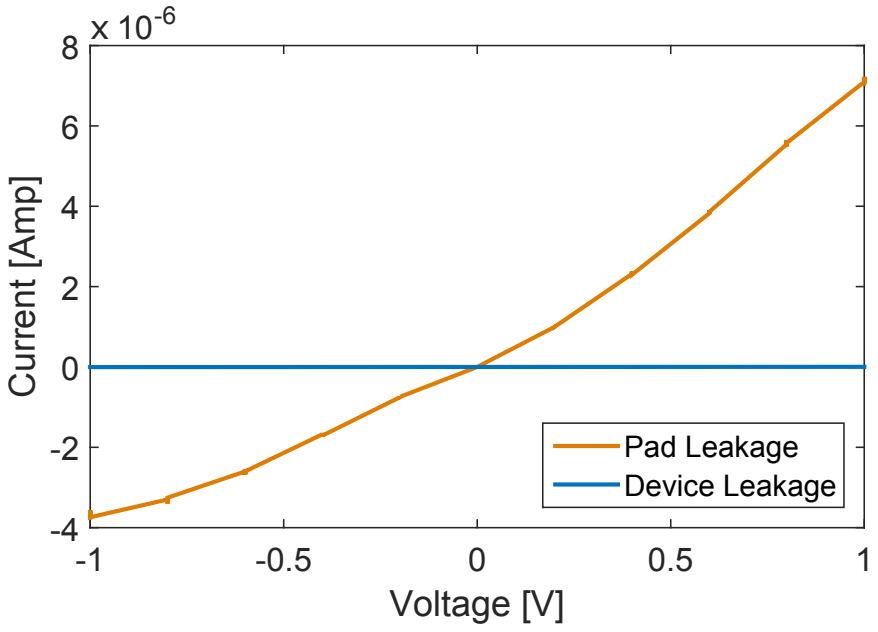


FIGURE 5.4: Leakage measurement from a Generation-two representative device showing both leakage between pads and also between devices on the same substrate. No magnetic field was applied during the measurement.

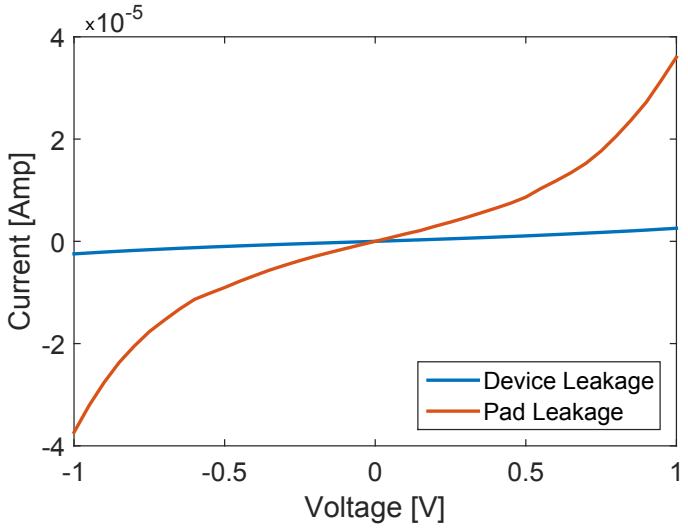


FIGURE 5.5: Leakage measurement from a Generation-one representative device showing both leakage between pads and also between devices on the same substrate.

reverse directions, the device conducts a huge current almost one order of magnitude more than Generation-two. This might be due to the fact that, at high enough voltage in both directions, the current takes a different path other than the one into the device. *InP* and *InGaAs* heterostructure forms a Type 1 - Straddling band alignment as shown in Fig. 5.6.

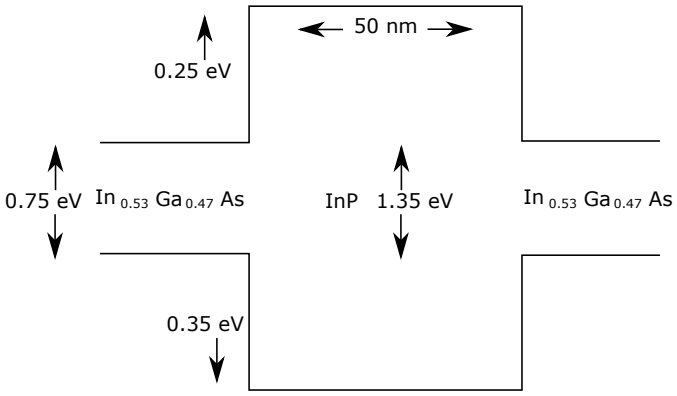


FIGURE 5.6: Band-structure of the 50 nm semi-insulating *Inp* in between two conducting *InGaAs* films.

Usually such a positive offset in the conduction band between *InGaAs* and *InP* blocks current flow[32]. But in reality, the band-alignment is not abrupt but more gradual in a lattice matched heterostructure[32][33]. This might make the current blocking effect of heterostructure less perceived over short distances like $\lesssim$ 50 nm. The crude resistance calculated from the leakage measurements is much less than the four-probe measurements. So, the leaky behaviour of the device design, has manifested itself as the high current flowing between the pads through the *InP* isolation. The leakage curve between adjacent devices also proves the above mentioned statement.

5.3 Hall Measurements

The previous measurements provided an overview of the successful devices. In this section the important results of this thesis will be discussed. Hall Measurements were performed using the same setup as shown in 4.2.

Fig. 5.7 shows the results obtained from a single Hall measurement performed on a device with low resistivity. Each data point in Fig. 5.7 is an average of 400 measured values of Hall voltage and the standard deviation of the data defines the symmetrical error bars. A current of 5 μA is applied between the source and drain contacts of the device and the voltage is measured between Hall probes 1-2 for different values of the magnetic field. Hall measurements were carried out on four successful devices from two different substrates, and each device contains two set of Hall pairs, totalling to 8 set of measurements.

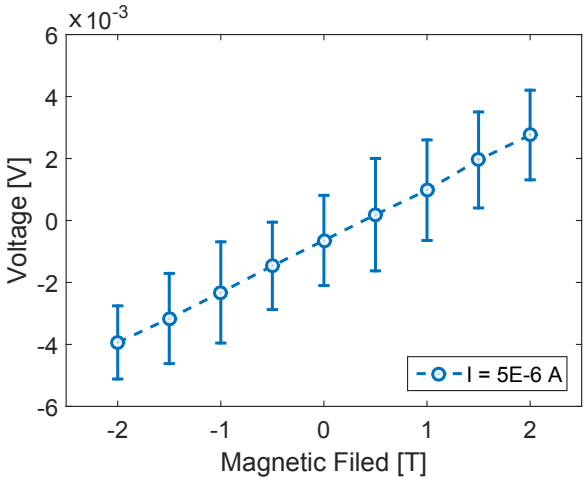


FIGURE 5.7: Representative Hall measurement results from a device with low resistivity. The measured Hall voltage is plotted against the applied transverse magnetic field.

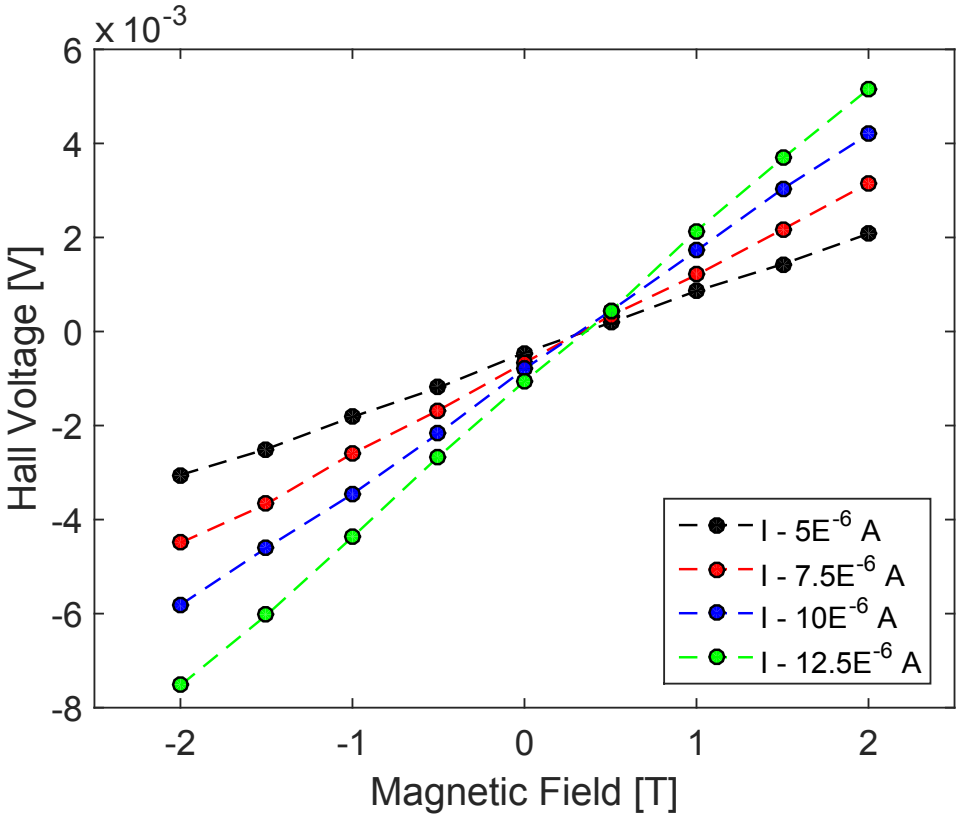


FIGURE 5.8: Hall measurement results from a single device with low resistivity. The Hall voltage is measured for different values of current through the device and is plotted against the applied transverse magnetic field.

Fig. 5.8 shows results from measurements carried out on a single device under different values of bias current. The average values of the Hall voltage is plotted against transverse

magnetic field, but without the error bars. The error bars were removed in order to make the plot more tangible. It can be seen that the Hall voltage approximately doubles when the bias current is doubled. And according to eq: 2.16 the Hall voltage has a direct relation to the applied current. This trend is followed by Hall data despite the spread observed in them. Interpretation of the data becomes more difficult, if the spread in the

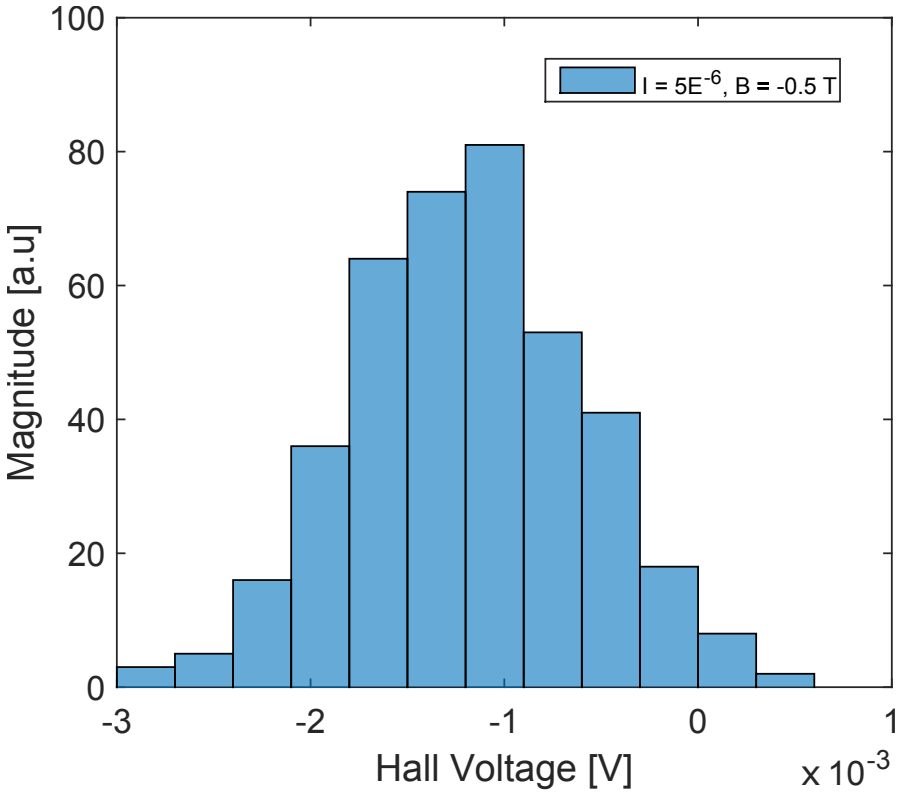


FIGURE 5.9: Hall measurement result from at a single magnetic field value. The 400 measured data points showing an approximate Gaussian distribution with the maximum peak around the averaged value.

data is random. In order to analyse the nature of this spread, the Hall voltage measured at a single magnetic field value at constant bias current is plotted as a frequency bar graph. Fig. 5.9 shows the distribution of the Hall voltage measured at a magnetic field of -0.5 T, for a bias current of 5 μA for the same device whose complete Hall data is given in Fig. 5.8, the black curve at -0.5 T corresponds to the frequency plot. Even though there is a spread, the data bear a resemblance to an approximate Gaussian curve. The peak value in Fig. 5.9 corresponds to the average value plotted in Fig. 5.8. This further proves the validity of the measured Hall data.

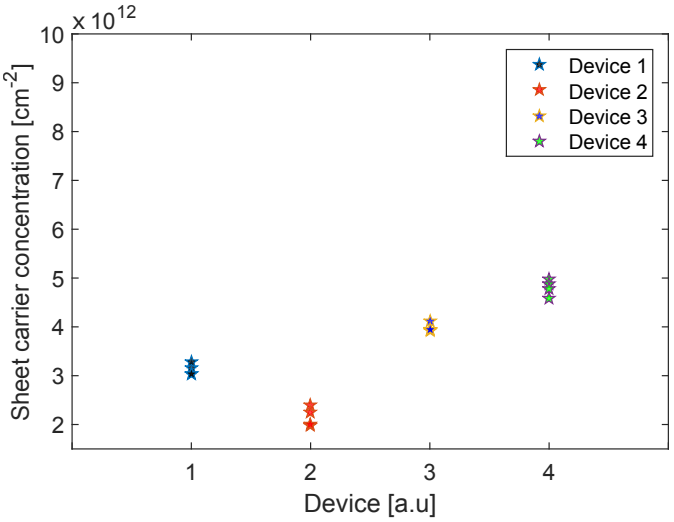


FIGURE 5.10: Sheet carrier density of the various Hall devices calculated from the Hall data. The carrier density obtained from the four different values of bias current is averaged and plotted.

5.4 η_s calculation

The Hall voltage thus obtained is used to calculate the sheet carrier density η_s using eq. 2.16. Fig. 5.10 shows the results from the calculation of carrier density for the four successful devices. The carrier density calculated for each bias current is averaged and is plotted for each device. 800 measured data points are averaged in order to get each data point in Fig. 5.10. Device four was the one with a relatively lower resistivity, which is reflected accordingly in the sheet carrier density of the same device. Similar experiments on Indium rich $InGaAs$-quantum well channels have shown comparable carrier densities[7]. But those channels are under an high-k dielectric with better isolation. High-k dielectric reduces the leakage currents associated with tunnelling, thereby providing better isolation[34]. Absence of a dielectric layer in our devices might explain the spread in our data.

5.5 Hall Mobility calculation

The sheet carrier concentration obtained in the previous calculation was used to calculate the Hall mobility from eq. 2.14.

Fig. 5.11 shows the mobility calculated for a single device as a function of sheet carrier density. A monotonic reduction in mobility is observed with increasing carrier density. This monotonic degradation of mobility is well explained by the fact that, as

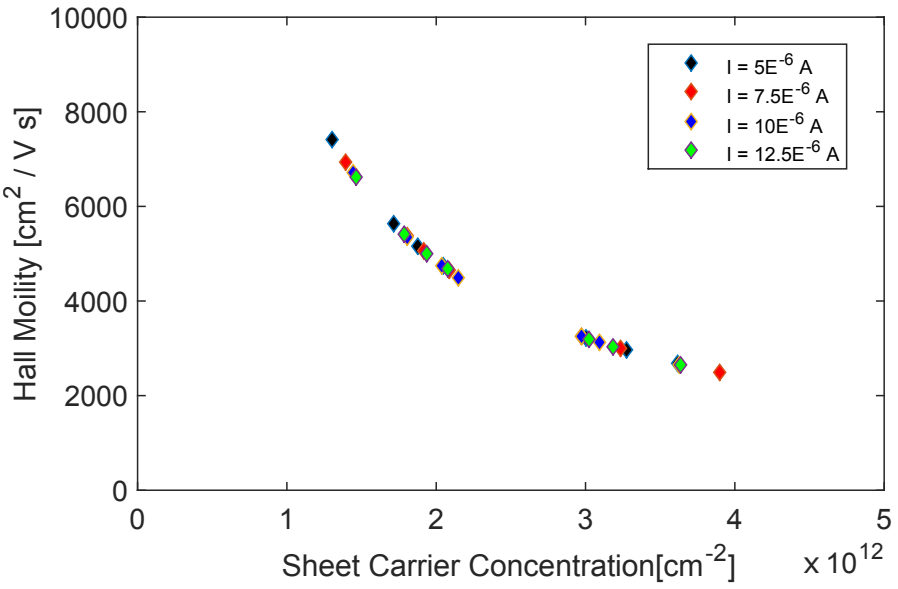


FIGURE 5.11: Experimental results of electron mobility as a function of sheet carrier density. The sheet carrier densities for each bias current is averaged. The different data points for the same bias current correspond to the different applied magnetic field.

the carrier concentration increases, the probability of scattering events also increases, thereby degrading the carrier mobility[35].

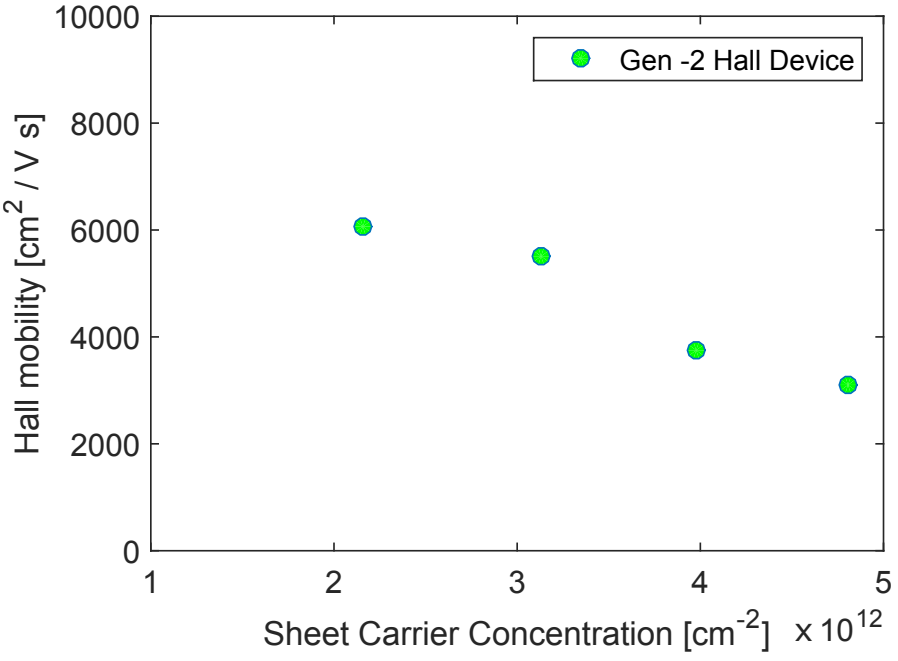


FIGURE 5.12: Experimental results of electron mobility as a function of sheet carrier density. Each data point represents the mobility calculated using the average carrier density of the device.

Fig. 5.12 shows the average mobility for each device measured as a function of carrier density. At a sheet carrier concentration of 2×10^{12}, the carriers attain highest mobility. Previous experiments for $InGaAs$ channels of comparable dimensions also agree with the peak mobility result presented[7].

The measured devices had an average carrier mobility around (5000±800) cm^2/Vs. The minor fluctuations in measured carrier mobility might be due to localized imbalance in stoichiometry during MOCVD growth. The measurements were carried out at room temperature, so the mobility fluctuations observed in this work are independent of temperature. The multi-gated NWFETs made from $InGaAs$-QW channel with integrated Hall probes, demonstrated a similar performance[7]. However the devices differed from the ones being experimented here by their material composition and by the presence of a di-electric below the gate. And the mobility deterioration in their work was attributed to their fabrication process. Top-Down pattern transfer carried out by etching the crystal lattice introduced additional scattering, as proved by their depletion mode device. In the absence of such additional scattering, the channel material was expected to achieve considerable boost in its transport properties. Improved transport properties in principle will offer improved device performance.

Chapter 6

Conclusion and Outlook

In this thesis, Hall measurements were performed on a III-V $InGaAs$ NW array with integrated Hall probes. The device was designed and fabricated using a novel area regrowth technology to avoid performance degradation present in the conventional top-down fabrication.

The novel selective area regrowth was perfected and well established for multi-gated FinFET architectures[8]. But implementing the same technology for new architectures like a Hall device, invoked many unprecedented complications. Integrating the the fabrication technology to our Hall device was not an impossible task. However it consumed a lot of time and resources; time, that would have otherwise been spent in additional data collection and validation. Generation-one Hall device performance was found to be very leaky. The leakage currents dominated the measurements and the devices failed to provide any fruitful Hall data. It was found that the design is flawed and failed to provide adequate isolation, which lead to their poor performance. Several trails failed before successful devices were fabricated. Most of the devices faced critical issues in the contact layer alignment. This was created by poor contrast between InP substrate and $InGaAs$ regrown layer. And no Hall data was obtained from the successful devices due to their leaky behaviour.

In Generation-two the design flaw was corrected and the poor contrast was compensated by wet etching and implementing positive markers that aided in alignment. The experimental Hall mobility presented in this report agrees both with planar $InGaAs$ data and data from devices with comparable attributes. The mobility of the material is found to degrade with the increase in the carrier concentration. However, the main motivation for this work is to make a relevant technological statement, by performing

gated Hall measurements with a scaled high-k dielectric on top of the channel. Mobility modulation in response to the gate bias is more relevant to the current phase of semi-conductor industry[7]. The idea was to characterise the transport properties under relevant conditions and prove the ballisticity of $InGaAs$ channel. Through continuous trails, the selective area growth was successfully implemented for the new Hall device architecture. But, due to lack of time, gated Hall measurement was not performed.

Though proper care was taken while performing measurements and during calculation of transport characteristics, the sample set was quite small to make a strong statement. The time spent on perfecting the fabrication process left very little time to measure and organize the acquired data. To create even a small impact on the scientific community, the first order of business is to have a large enough sample set and reliable measurement techniques.

In a future perspective, the same measurements should be performed on a larger sample set for more accurate conclusions. And the data must be checked for its validity and to see if they provide a rationale for using selective area growth. The fabrication process is now reliable and can be repeated with a larger success rate. Another more relevant experiment is to perform gated Hall measurements and look for an improvement in the transport characteristics of $InGaAs$. Apart from the gate, a scaled dielectric will improve the surface passivation and hence the device performance. And the device can be simulated in a finite element simulation in order to further validate the design and data. There is a possibility that the spread in the measured Hall data may be due to the measurement setup. But there is not enough data either to prove or to disprove that statement. A reference measurement for the current Hall measurement setup can indeed improve its authenticity. III-V materials have a huge potential, quantitative characterization of them will allow us to properly use that potential. Further measurements are needed to ascertain their true calibre.

Bibliography

[1] Jesús A. del Alamo. Nanometre-scale electronics with iii-v compound semiconductors. 2011. URL http://www.nature.com/nature/journal/v479/n7373/abs/nature10677.html.

[2] ITRS. International techonology roadmap for semiconductors, 2013. URL http://www.itrs.net/home.html.

[3] Scott E. Thompson and Srivatsan Parthasarathy. Moore's law: the future of si microelectronics. *Materials Today*, 9(6):20 – 25, 2006. ISSN 1369-7021. doi: http://dx.doi.org/10.1016/S1369-7021(06)71539-5. URL http://www.sciencedirect.com/science/article/pii/S1369702106715395.

[4] Vikram Jagannathan. Ballistic devices. 2004.

[5] A. M. Song. Room-temperature ballistic nanodevices. In *Encyclopedia of nanoscience and Nanotechnology*. (2004).

[6] Kristian Storm, Filip Halvardsson, Magnus Heurlin, David Lindgren, Anders Gustafsson, Phillip M. Wu, Bo Monemar, and Lars Samuelson. Spatially resolved hall effect measurement in a single semiconductor nanowire. *Nature Nanotechnology*, 7(11):718–722, 2012.

[7] Arun V. Thathachary, Nidhi Agrawal, Lu Liu, and Suman Datta. Electron transport in multigate inxga1–x as nanowire fets: From diffusive to ballistic regimes at room temperature. *Nano Letters*, 14(2):626–633, 2014. doi: 10.1021/nl4038399. URL http://dx.doi.org/10.1021/nl4038399. PMID: 24382089.

[8] Cezar Zota, Lars-Erik Wernersson, and Erik Lind. In0.53ga0.47as multiple-gate field-effect transistors with selectively regrown channels. 35(3):342–344, 2014. ISSN 0741-3106. URL http://dx.doi.org/10.1109/LED.2014.2301843.

[9] Oliver Hayden, Ritesh Agarwal, and Wei Lu. Semiconductor nanowire devices. *Nano Today*, 3(5–6):12 – 22, 2008. ISSN 1748-0132. doi: http://dx.doi.org/10.1016/S1748-0132(08)70061-6. URL http://www.sciencedirect.com/science/article/pii/S1748013208700616.

[10] D.J. Frank. Power-constrained cmos scaling limits. *IBM Journal of Research and Development*, 46(2.3):235–244, March 2002. ISSN 0018-8646. doi: 10.1147/rd.462.0235.

[11] Ritesh Agarwal Xiangfeng Duan, Yu Huang. Single-nanowire electrically driven lasers. *Nature*, 2003/01/16/print.

[12] Mark Lundstrom. Moore's law forever? *Science*, 299(5604):210–211, 2003. doi: 10.1126/science.1079567. URL http://www.sciencemag.org/content/299/5604/210.short.

[13] Fredrik K. Olsson, Amandine Aubert, Manuel Avella, Juan Jiménez, Carlos A. Barrios, Jesper Berggren, and Sebastian Lourdudoss. Heteroepitaxy of inp on silicon-on-insulator for optoelectronic integration. *ECS Transactions*, 3(39):23–29, 2007. doi: 10.1149/1.2818558. URL http://ecst.ecsdl.org/content/3/39/23.abstract.

[14] Karen L Kavanagh. Misfit dislocations in nanowire heterostructures. *Semiconductor Science and Technology*, 25(2):024006, 2010. URL http://stacks.iop.org/0268-1242/25/i=2/a=024006.

[15] K.J. Kuhn. Cmos transistor scaling past 32nm and implications on variation. In *Advanced Semiconductor Manufacturing Conference (ASMC), 2010 IEEE/SEMI*, pages 241–246, July 2010. doi: 10.1109/ASMC.2010.5551461.

[16] N. Wang, Y. Cai, and R.Q. Zhang. Growth of nanowires. *Materials Science and Engineering: R: Reports*, 60(1–6):1 – 51, 2008. ISSN 0927-796X. doi: http://dx.doi.org/10.1016/j.mser.2008.01.001. URL http://www.sciencedirect.com/science/article/pii/S0927796X08000028.

[17] Richard G. Hobbs, Nikolay Petkov, and Justin D. Holmes. Semiconductor nanowire fabrication by bottom-up and top-down paradigms. *Chemistry of Materials*, 24(11):1975–1991, 2012. doi: 10.1021/cm300570n. URL http://dx.doi.org/10.1021/cm300570n.

[18] *McGraw-Hill Encyclopedia of Physics*. McGraw-Hill Companies, 1994.

[19] B. Van Zeghbroeck. Principles of electronic devices, 2011. URL http://ecee.colorado.edu/~bart/book/book/append/quick.htm.

[20] J. W. Turrentine. The meaning of current density. *The Journal of Physical Chemistry*, 14(2):152–157, 1909. doi: 10.1021/j150110a002. URL http://dx.doi.org/10.1021/j150110a002.

[21] Massimo V. Fischetti and Steven E. Laux. Monte carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects. *Phys. Rev. B*, 38:9721–9745, Nov 1988. doi: 10.1103/PhysRevB.38.9721. URL http://link.aps.org/doi/10.1103/PhysRevB.38.9721.

[22] *Physics of Semiconductor Devices*. John Wiley and Sons, 2006.

[23] U.S. Department of Commerce. Hall effect measurements, 2008. URL http://www.nist.gov/pml/div683/hall_effect.cfm.

[24] Edwin Hall. On a new action of the magnet on electric currents, 1879. URL http://web.archive.org/web/20110727010116/http://www.stenomuseet.dk/skoletj/elmag/kilde9.html.

[25] Hall effect history, 2015. URL http://phareselectronics.com/products/hall-effect-sensors/hall-effect-history/.

[26] Fredrik Lindelöw. Doping evaluation of inp nanowires for tandem junction solar cells, 2014. Student Paper.

[27] Adam M. Crook, Erik Lind, Zach Griffith, Mark J. W. Rodwell, Jeremy D. Zimmerman, Arthur C. Gossard, and Seth R. Bank. Low resistance, nonalloyed ohmic contacts to ingaas. *Applied Physics Letters*, 91(19):192114, 2007. doi: http://dx.doi.org/10.1063/1.2806235. URL http://scitation.aip.org/content/aip/journal/apl/91/19/10.1063/1.2806235.

[28] A. K. Baraskar, M. A. Wistey, V. Jain, U. Singisetti, G. Burek, B. J. Thibeault, Y. J. Lee, A. C. Gossard, and M. J. W. Rodwell. Ultralow resistance, nonalloyed Ohmic contacts to n-InGaAs. *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, 27:2036, 2009. doi: 10.1116/1.3182737.

[29] MohammadAli Mohammad, Mustafa Muhammad, StevenK. Dew, and Maria Stepanova. *Fundamentals of Electron Beam Exposure and Development*. Springer Vienna, 2012. ISBN 978-3-7091-0423-1. doi: 10.1007/978-3-7091-0424-8_2. URL http://dx.doi.org/10.1007/978-3-7091-0424-8_2.

[30] Aixtron AG. Aix 200/4 operational manual, 2015.

[31] Kenji Kurishima, Takashi Kobayashi, and Ulrich Ito, Hiroshi. Control of zn diffusion in inp/ingaas heterojunction bipolar transistor structures grown by metalorganic vapor phase epitaxy. *Journal of Applied Physics*, 79(8), 1996.

[32] Su Yongbo, Jin Zhi, Cheng Wei, Liu Xinyu, Xu Anhuai, and Qi Ming. Ultra high-speed inp/ingaas dhbts with f t of 203 ghz. *Journal of Semiconductors*, 30(1): 014002, 2009. URL http://stacks.iop.org/1674-4926/30/i=1/a=014002.

[33] Nien-Tze Yeh, Pei-Chin Chiu, Jen-Inn Chyi, Fan Ren, and Stephen J. Pearton. Sb-based semiconductors for low power electronics. *J. Mater. Chem. C*, 1:4616–4627, 2013. doi: 10.1039/C3TC30585F. URL http://dx.doi.org/10.1039/C3TC30585F.

[34] G. D. Wilk, R. M. Wallace, and J. M. Anthony. High-Îº gate dielectrics: Current status and materials properties considerations. *Journal of Applied Physics*, 89(10), 2001.

[35] D Chattopadhyay, S K Sutradhar, and B R Nag. Electron transport in direct-gap iii-v ternary alloys. *Journal of Physics C: Solid State Physics*, 14(6):891, 1981. URL http://stacks.iop.org/0022-3719/14/i=6/a=014.