Digital communication system for a proton accelerator

A popular science summary of master's thesis:
High speed backbone for FPGA at ESS

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What we have done is to reverse engineer a PCI Express (PCIe) communication system between customized hardware and a Linux computer. The original hardware design is non-modifiable and our goal is to create a system open for customization. We have successfully re-created the original design and researched possible improvements. This system will be installed in 150 different parts of the European Spallation Source (ESS)[1]. Although it is a small part, it will be vital for the overall performance of the facility.

The European Spallation Source will be a top research facility in the field of material science. 17 countries has come together to create the most powerful microscope ever built. This is done with help of a particle accelerator that acts as a huge beam cannon that shoots particles at a target. When the beam hits the target, it will send out small particles called neutrons. These neutrons have good quality's that can be used when investigating the structure of different materials.

The accelerator contains so called cavities that are responsible for speeding up the particles that are fired towards the target. These will be fired in pulses lasting only a few nanoseconds and reaching speeds up to 96% of the speed of light. During these pulses measurements of the electric field, used to accelerate the particles, need to be saved so that they can be used to regulate the field. The system that controls data movement between measurement inputs, memory and computer is the design covered in this project and acts as the central nerve system for the field regulator.

To connect a computer to the regulator a communication system called PCIe is used. PCIe is a common interface which is used in a large amount of computers today. It is mainly used to connect external parts such as graphic-, network- and memory cards to the motherboard of the computer. Because of the high speed of the particle beam and the short time frame, data transfers in and out of memory have to be fast enough to cope with the regulator. PCIe is a high speed interface which makes it a perfect match for this job.

The predecessor to our system was a black box which means that it couldn't be altered because we didn't have access to its content. What we did was to observe the system by looking at what was going in and what was coming out. By doing this, features of the implementation could be extracted. We found that the system needed: a PCIe interface, a memory interface, an write arbiter and a direct memory access handler. We could also see that the data transfer speed, when sending data from the computer to our system, wasn't fast enough.

When comparing the predecessor to our final design the functionality is the same. We have successfully recreated the design with equal performance. We also researched possible improvements and possibilities to increase the transfer speed.

When sending data from the computer, two special cases prevent us from accelerating the transfer. The first one is when data is split into two smaller parts. The other one is when the data sent is reordered. This means that if the data is sent in the order one, two and three, it could be received in order one, three and two. These issues were not resolved in the original design which greatly reduced the performance. In our case, we could now take these cases into consideration and in the future increase the throughput of data to better fit the needs at ESS.

[1] https://europeanspallationsource.se