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Simulation and Analysis of a Power Supply Circuit for Frequency Inverter Controlled AC-Induction Motors

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Abstract
For variable-frequency drives, the most common way to apply the desired power to an electrical motor is using PWM modulated signals. Due to high-frequency components, those signals give rise to reflections in the motor cables, radiated noise around the cables and acoustic noise in the motor. In order to avoid those problems, NFO Drives AB develops and produces an alternative to PWM modulation called sinus switch for use with AC induction motors. The sinus switch can produce sinusoidal signals at its output, so that no high-frequency components are transmitted over the motor cables. To extend the range of powers the sinus switch can be used for, to reduce ripple on the output voltage and to reduce the range of switching frequencies used, an idea has been developed about how to extend the sinus switch by connecting several modules in parallel. In this thesis, a simulation model of the sinus switch is developed and implemented in Matlab/Simulink. This simulation model is expanded to simulate the sinus switch with parallel modules. A solution to a synchronization problem arising with this extension is being tested and modified successfully. The overall functioning of the extended sinus switch is tested using a DC motor as a load as an example. The simulation shows the expected behavior. Furthermore, the performance concerning parameter inaccuracies and the stability concerning inaccurate solutions to the synchronization problem are analyzed.

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Contents

1. Introduction

There are a variety of applications, for which it is necessary to control the speed of electrical motors like AC induction motors or synchronous motors. To do so, control methods like U/f-control or field oriented control are used [Leo90]. These methods determine the amplitude and frequency of the voltage that has to be applied to the motor (e.g., 3-phase AC induction motor), so that it runs with the desired speed. Power electronic converters are used as an interface between the reference voltage calculated by the controller and the electrical motor [MUR89]. Pulse wide modulated (PWM) power converters are widely used today. However, their disadvantage si that they contain high-frequency components [KWS02], which lead to radiated noise around the motor cables, reflections in the motor cable and accoustic noise in the motor. Extra filters and screened cables are needed to cope with those problems.

By transmitting sine-wave signals to the motor instead of PWM modulated signals, the problems mentioned above could be avoided [Jön09]. The company NFO Drives AB developed an alternative to PWM called “sinus switch” for their frequency inverters, that outputs sin-wave signals to the motor [Jön88]. The sinus switch consists of a transistor half-bridge and an LC-filter. The transistors are switched in a special way, so that the voltage at the output of the LC-filter can be sine shaped. Using sin-wave signals instead of PWM modulated signals can then save energy. This “sinus switch” is currently included in frequency inverters in the range of $0.73 - 15\,kW$ using MOSFET transistors in the transistor half-bridge included in the sinus switch [Jön09].

For some applications, higher powers than 15 kW are needed. To develop the sinus switch for those higher powers, IGBT transistors should be used instead of MOSFET [Leo90]. Since for IGBT transistors the range of switching frequencies available is smaller than for MOSFET transistors [MUR89], the frequencies used to switch the transistors in the sinus switch have be limited. A possibility to reduce the switching frequency of the transistors while still delivering power high enough is to connect several modules in parallel, each comprised of a transistor half-bridge and an LC-filter [Jön05].

One part of this thesis is to simulate the sinus switch circuit with the help of MATLAB and Simulink. The basic sinus switch as described in [Jön88] is simulated for one phase of the motor and extended according to [Jön05]. This extended version of the sinus switch is tested in the simulation whether is has the expected behaviour. Its inductor currents are synchronized for certain operation ranges of the motor und unsynchornized for others. The seconds purpose of this thesis is to test a synchronization algorithm for those unsynchornized cases presented in [Jön05] and, if necessary, modify it. Furthermore, a third purpose is to analyze the switch circuit including the extension and synchronization and find out some constraints for the operation.

Although the sinus switch is supposed to be used with AC induction motors, in this thesis one phase of a DC-motor is used for the simulations. For the purpose of this thesis, a DC-motor is sufficient to test the functioning of the sinus switch and analyze its behaviour.

The basic sinus switch circuit as presented in [Jön88] is described in Section 2. The model of the DC-motor used for the simulations is developed in Section 3. The simulation model for the basic sinus switch [Jön05] is developed in Sections 4 and 5. A voltage control loop including the capacitors of the LC-circuit is developed in Section 5. The connection of two modules as simulated in 4 in parallel and the synchronization are discussed in Section 6. In this section, also constraints of the

modified sinus switch like non-exact synchronization and the effect of inaccurate inductances are tested with the help of the simulation. A conclusion of the work is given in Section 7.

2. The Sinus Switch

This chapter gives a review on the basic Sinus Switch circuit as described in [Jön88], [Jön05] and [Jön09]. First the setup is given and then the function is explained. Simulations, further development and analysis are based on this circuit.

2.1 Setup

Figure 2.1.1 shows the setup of the basic switch circuit. A single phase of the converter is considered. The switch circuit consists, as in PWM, of a transistor half-bridge, connected to a DC-link with the voltage $\pm V$. In parallel to the transistors TR_1 and TR_2 a free-wheel diode is connected. As seen in figure 2.1.1, the transistors are assumed to be ideal switches in this thesis [MUR89].

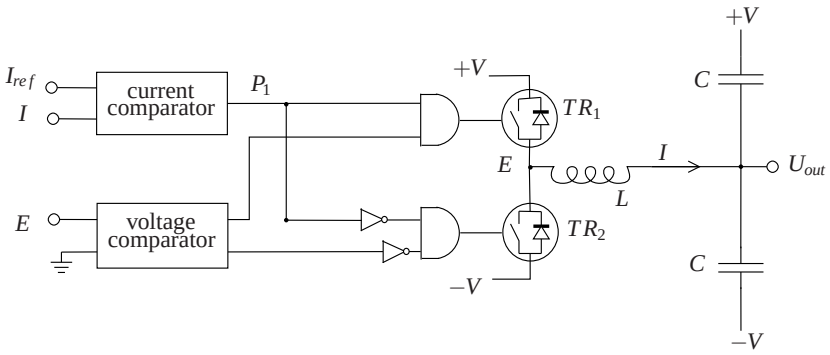


Figure 2.1.1 The switch circuit

The switching of the transistors is controlled by a control logic, whereas the switching frequency of the transistors is variable. The control logic consists of a current comparator, controlled by a reference current I_{ref} and the current I through the inductor L, and a voltage comparator, controlled by the bridge voltage E. At the output of the transistor bridge, a LC-filter is connected. This filter serves several tasks. It isolates the bridge and the load current from another. Then the bridge current can go to zero, although the load current has a value unequal to zero. Also, switching transients occurring in the transistor bridge are isolated from the output and the transistor bridge is protected from electric transients coming from the output. Furthermore, the output voltage U_{out} of the switch circuit is already filtered through the LC-filter, so that it has, for example, a sinusoidal shape. Though, the shape of the output voltage is dependent on how the control logic controls the switching of the transistors.

2.2 Operation

The shape of the output voltage is dependent on the inductor current I. Therefore, the shape of the inductor current is described first, before explaining how the output voltage results from it.

To explain the operation of the switch circuit, a constant reference current I_{ref} at the current comparator is assumed. Figure 2.2.1 shows the shape of the inductor

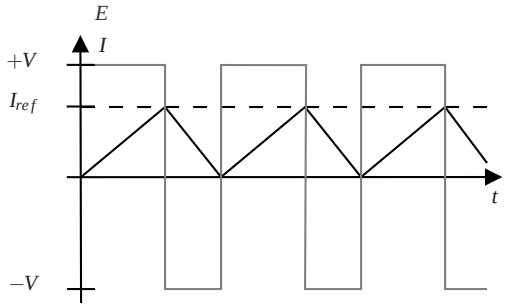


Figure 2.2.1 Bridge voltage E and inductor current I

current and the bridge voltage. Three cycles of the inductor current are shown in the figure.

A cycle starts with the inductor current at zero and the upper transistor TR_1 in figure 2.1.1 being switched on while TR_2 is switched off. Thus, the bridge voltage is $E = +V$ for a positive reference current at the beginning of a cycle, which leads to a rising inductor current I. One cycle can then be divided into four intervals.
During the first interval, the inductor current is smaller than the reference current. The current comparator compares those two currents and lets the transistor TR_1 be switched on. Transistor TR_2 is switched off. Therefore, the bridge voltage is now $E = +V$, so that the voltage over the inductance L is $+V - U_{out}$, which is positive since $V > U_{out}$. Hence, the inductor current I rises. An ideal inductor is assumed, hence the current rises linearly.

At interval two, the current comparator sees, that reference current and inductor current are equal and turns the transistor TR_1 off.

During the third interval, the inductor current I has to go another way after TR_1 got turned off, since it cannot stop abruptly. It now flows through free-wheel diode parallel to TR_2, while TR_2 remains closed. Now the bridge voltage is $E = -V$. Therefore, the voltage over the inductance L is in the opposite direction compared to interval one and the inductor current I decreases.

In interval four, the inductor current reaches zero. The diode does not close when the current is zero, because of its reverse recovery character [Phi92]. It stays open in negative direction until its reverse recovery charge is reached. Then, the diode closes and the current is forced through the upper free-wheel diode. Again, the current through the inductor cannot stop abruptly. The bridge voltage is pulled up to $E = +V$ by this. The voltage comparator realizes this rising edge of the bridge voltage and switches on the transistor TR_1 again, so that the the bridge voltage stays at the positive value and a new cycle starts with the interval one.

2.3 Equivalent Circuit

To see how the output voltage U_{out} of the switch circuit looks like dependent on the inductor current I, an equivalence circuit for the LC-filter at the output of the transistor half-bridge can be calculated. For detailed calculations see appendix A. For both cases that the bridge voltage is $E = +V$ and $E = -V$, the equivalence circuit is a basic LC-circuit as shown in figure 2.3.1, with the inductance L and the capacitance $2C$.

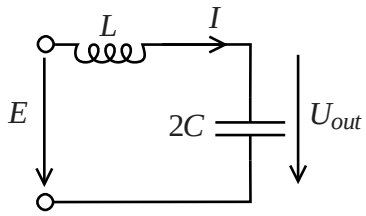


Figure 2.3.1 Basic, ideal LC circuit

It can be seen in this figure, that the output voltage U_{out} results from [KSW00]:

$$U_{out}(t) = \frac{1}{2C} \int I(t)\, dt.$$

Therefore, appart from the constant, the output voltage results from integrating the inductor current. In the case with a constant reference current, as described above, the output voltage would rise linearly containing a ripple. Without the ripple, the output voltage would be the same as when integrating the average value of the inductor current, which is half the reference current.

Different shapes of the output voltage U_{out} can now be obtained by changing the reference current I_{ref}. A higher or lower reference current leads to a longer or shorter cycle time for the inductor current and therefore to a smaller or bigger switching frequency of the transistors. Limits in the switching frequency limit also the available range of reference currents. In order to get a certain, desired shape of the output voltage U_{out}, e.g. sinus-shaped, a voltage control loop is closed around the switch circuit. The voltage controller determines dependent on the desired voltage and the output voltage how the reference current has to be in order to get the output voltage the same as the desired voltage. For details to this see chapter 5.1.

3. The DC-Motor

The mathematical model of the DC-motor needed for the simulations is derived in this section. Furthermore, this model is implemented into MATLAB and Simulink.

3.1 Design and Basic Principle of the DC-Motor

A DC-motor is an electric motor, that is driven by direct current. It converts electrical energy into mechanical energy.

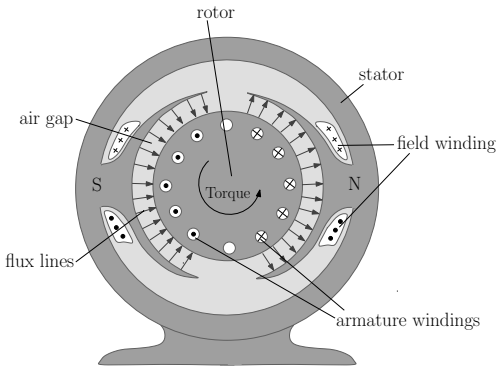


Figure 3.1.1 schematic sketch of a DC motor

It consists of a stator, which generates a static magnetic field of strength B using permanent magnets or electromagnets. In Figure 3.1.1 a motor with two poles is shown, where the poles are composed of electromagnets. In this thesis though, a permanent magnet DC-motor is assumed, which has a constant magnetic field. A rotor, that can turn around its longitudinal axis, is located inside the stator. Armature windings are arranged in slots around the periphery of the rotor. Each winding consists of two conductors. Several windings in one slot make up a coil, so that there are several coils along the perimeter of the rotor. The beginning and the end of each of those coils are connected to commutator brushes of a commutator. The commutator is not shown in figure 3.1.1. It is connected to the shaft of the rotor. It periodically reverses the current in the armature windings, so that the torque created is always acting in the same direction on the rotor. More information about commutation can be found, for example, in [Leo90]. Since the windings are all connected through the commutator, the coils on the rotor can be seen as connected in series. They are supplied with the armature current I_A through the commutator.

When the voltage U_A is applied to the rotor through the commutator, the armature current I_A is flowing through the armature windings. Since the windings are placed in a magnetic field, a force and a torque a generated, that turn the rotor.
If instead the rotor is being turned around its longitudinal axis in the magnetic field, the voltage U_A is induced into the coils and can be accessed through the commutator.

3.2 Mathematical Model of the DC-Motor

The voltage of the commutator brushes is the armature voltage U_A, that consists of a voltage drop caused by the resistance of the rotor R_A , a voltage drop evoked by

the inductance L_A of the rotor, which is generated by air gap- and leakage fields, and the armature emf [Leo90]. The emf is a voltage induced in the armature windings due to the magnetic field B . The armature voltage can therefore be described in the following equation [Fis06]:

$$U_A = U_q + R_A \cdot I_A + L_A \cdot \frac{dI_A}{dt}. \tag{3.2.1}$$

The emf can be calculated according to [Fis06]:

$$\begin{aligned} U_q &= 4\,N\,p\,\Phi\,\frac{60}{2\pi}\cdot\omega \\ &= k_1 \cdot \Phi \cdot \omega. \end{aligned} \tag{3.2.2}$$

It is proportional to the flux and the speed of the motor. Since a permanent magnetic DC-motor is assumed, the flux Φ is constant.

The torque on the rotor is dependent on the current through the armature windings. A force is affecting the windings, which leads to a torque [Smi94]:

$$\begin{aligned} M &= \frac{N \cdot p}{\pi} \cdot \Phi \cdot I_A \\ &= k_2 \cdot \Phi \cdot I_A \end{aligned} \tag{3.2.3}$$

The acceleration torque M_a, which in the difference between the torque M of the rotor and the load torque applied to the motor, leads to rotation of the motor. According to newtons law [Fis06] it is:

$$M_a = M - M_L = J \cdot \frac{d\omega}{dt}. \tag{3.2.4}$$

The constants k_1 and k_2 are equal [Leo90]:

$$\begin{aligned} k_1 &= k_2 \\ \Rightarrow k_1 \cdot \Phi &= k_2 \cdot \Phi \\ &= K \end{aligned}$$

Therefore equations (3.2.2) and (3.2.3) are now:

$$U_q = K \cdot \omega \tag{3.2.5}$$

$$M = K \cdot I_A \tag{3.2.6}$$

Transforming the equations 3.2.4 and 3.2.1 into the s-domain gives the transfer functions:

$$I_A = \frac{1}{R_A + L_A\,s} \cdot (U_A - U_q) \tag{3.2.7}$$

$$\omega = \frac{1}{J\,s} \cdot (M - M_L) \tag{3.2.8}$$

This leads to the model shown in figure 3.2.1.

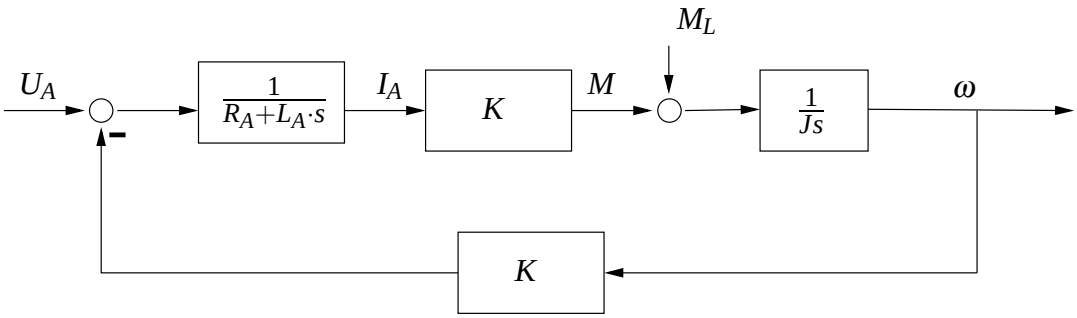


Figure 3.2.1 Model of the DC motor

3.3 Simulation Parameters of the DC-Motor

For simulating this model of a 2-pole permanent magnet DC-motor with Simulink, it is assumed that the motor has a rated power of $P_n = 500W$ and a rated voltage of $150V$. The motor is assumed to have a rated speed of $n_n = 3000\ rpm$.

For calculating the parameters of the motor needed in the simulation, the assumed rated operation point is considered. This is when the motor is running with its rated speed n_n, delivering the rated power P_n and using rated voltage U_n and rated current I_n.

With the assumption, that the losses are small the resistance voltage drop can be neglected. Furthermore, the inductive voltage drop is very small if the motor operates in a stationary state. Then the constant K can be calculated with equation (3.2.5), since then $U_A = U_q = U_n$:

$$K = \frac{U_n}{\omega_n} = \frac{150}{3000 \cdot \frac{2\pi}{60}} \simeq 0.5$$

Rated operation is considered to calculate the parameters.

The torque is connected to the power of the motor by its speed [Fis06]:

$$P_n = M_n \cdot \omega_n \cdot 0.9.$$

The factor 0.9 is added, because the speed with rated load is assumed to be 90% of the speed without a load on the motor. The motor is assumed to have 90% efficiency. The torque at the assumed speed n_n gives the assumed power P_n. Therefore, the torque can be calculated to:

$$M_n = \frac{500}{3000 \cdot \frac{2\pi}{60} \cdot 0.9} \simeq 1.768\ Nm.$$

With the help of equation (3.2.6), the current necessary for the torque $M = 1.768$ can be calculated:

$$I_n = \frac{M_n}{K} = 3.536\ A.$$

The voltage drop over the resistor R_A is 10% of the input voltage to the motor U_A, since the motor is assumed to have an efficiency of 90%. With $U_{A10\%} = 15V$, the resistor R_A can be calculated to:

$$R_A = \frac{U_{A10\%}}{I_n} = 4.24\ \Omega$$

A typical cut-off frequency of the transfer function (3.2.7) is $\omega_0 = 30\ Hz$. Depending on armature resistor and inductance this cut off-frequency is:

$$\omega_0 = \frac{R_A}{L_A}.$$

The inductance of the rotor is then:

$$L_A = \frac{R_A}{\omega_0} = \frac{4.24\ \Omega}{30\ Hz \cdot 2\pi} = 0.021\ H.$$

In summary, the calculated parameters used for simulating the DC-motor are shown in table 3.3.1.

K	0.5	**R**	$4\ \Omega$
J	0.0005	**L**	$0.02\ H$

Table 3.3.1 Motor data used for the simulation

3.4 Simulation Results of the DC-motor

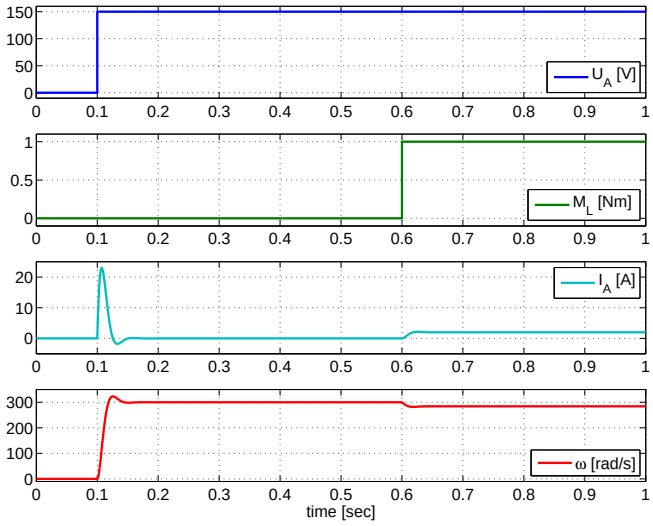


Figure 3.4.1 Input voltage U_A, load torque M_L, motor current I_A and speed ω of the DC motor

The DC motor was simulated implementing the model shown in figure 3.2.1 in Simulink with the parameters from table 3.3.1.
A step to $U_A = 150\ V$ is applied to the input of the motor at $0.1\ s$. At that time, no load is connected to the motor. At $0.6\ s$, a load of $1\ Nm$ is connected to the DC-motor. In figure 3.4.1 it can be seen, that the motor current has a peak when the voltage at its input changes from 0 to $150\ V$ and goes back to zero once the voltage stays constant. When the load is applied to the motor, the current gets a constant value unequal zero. The speed of the motor goes to $\omega = 300\frac{rad}{s}$, which equals $n = 2865\ rpm$. The speed

n is slightly lower than the desired speed of $n = 3000$, because the parameters used for the simulation have been rounded during their calculation. When the load step occurs, the speed of the motor decreases to a lower, constant value.
The results of this simulation confirm, that the motor model developed in this section is realistic [Leo90].

4. Simulating the inner loop for the current

The inner part of the switch circuit from figure 2.1.1, which has the current of the inductance as an output, is simulated in this section.

4.1 Simulation Setup

The inner current loop of the switch circuit is simulated as seen in figure 4.1.1. Figure 4.1.2 shows the subsystem containing the control logic, comprised of current and voltage comparator.

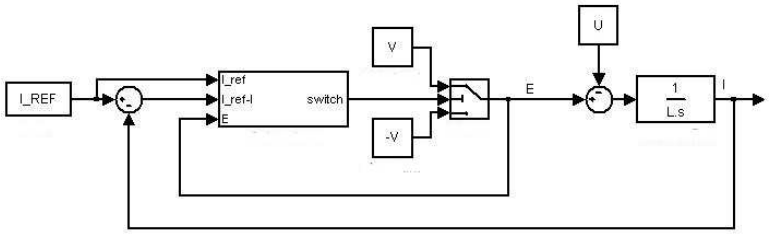


Figure 4.1.1 Simulation of the inductor current in the switch circle

For the simulation, it is assumed that the inductor is ideal, i.e. it has no iron and copper losses. Therefore, it is simulated as an integrator with a voltage at the input and a current at the output. The voltage over the inductor, which is the input to the mentioned integrator, is $E - U_{out}$. For developing the simulation model, a constant voltage U is assumed instead of the output voltage U_{out}. Therefore, the integrator simulating the inductor has the the voltage difference $E - U$ as an input.
The bridge voltage E can be $+V$ or $-V$, which is determined by the logic in the subsystem of the simulation model. This subsystem takes the given value for the inductor current I_{ref}, the actual inductor current I and the bridge voltage E of the actual time-step as an input and outputs a switching signal for the bridge voltage E_{next} for the next step.

The switch behind the subsystem simulates transistor half-bridge. It gets the switching signal and switches E_{next} to $\pm V$, depending on the output of the subsystem.

For simulating the control logic, the behavior of the sinus switch is analyzed. Therefore, the simulation model is developed from the behavioral pattern rather than from the physical functioning. The behavioral pattern, derived from the explanations in section 2.2, is as follows:

1. If $E = +V$ and $I_{ref} > I$, then $E_{next} = +V \Rightarrow I$ rises
2. If $E = +V$ and $I_{ref} = I$, then $E_{next} = -V \Rightarrow$ falling slope of I starts
3. If $E = -V$ and $I_{ref} > I$, then $E_{next} = -V \Rightarrow I$ falls

4. If $E = -V$ and $I = 0 \Leftrightarrow I_{ref} - I = I_{ref}$ then $E_{next} = +V \Rightarrow$ rising slope of I starts

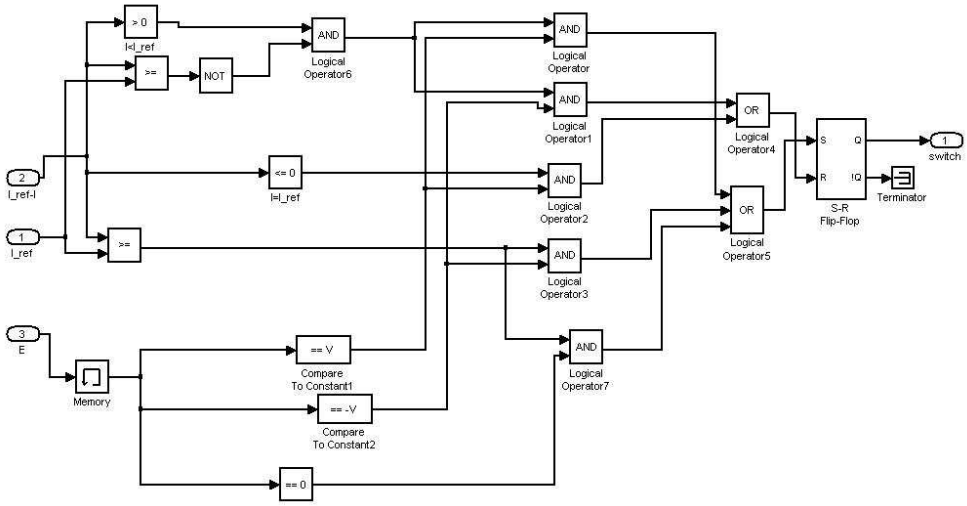


Figure 4.1.2 switching logic of the inductor current in the switch circle

The model of the control logic is shown in figure 4.1.2. It is composed of logic blocks, which are connected according to the behavioral pattern described above.
The switching signal, which is the output of the subsystem, is set by an R-S-Flipflop block provided by Simulink. If the set-input is set to one,the output of the subsystem is one. If the reset-input is set to one, then the output of the subsystem is zero. The switch that the output of the subsystem is connected to (figure 4.1.1), sets $E = +V$ if the switch signal at the output of the flip-flop is one and$E = -V$ if it is zero. Thus, the set-input of the flip-flop has to be set to one when $E = +V$ is required and to zero when $E = -V$ is required. Therefore, the results of the cases from the behavioral pattern are connected to the set- and reset-inputs through OR-blocks.

So far, only positive reference currents I_{ref} were considered. To include negative currents the logic has to be extended. For negative currents, the behavior follows the following pattern, which is similar to above:

1. If $E = -V$ and $I_{ref} - I < 0$ then $E_{next} = -V$
2. If $E = -V$ and $I_{ref} - I = 0$ then $E_{next} = +V$
3. If $E = +V$ and $I_{ref} - I < 0$ then $E_{next} = +V$
4. If $E = +V$ and $I_{ref} - I = I_{ref}$ then $E_{next} = -V$

By comparing this to the case of positive currents, it can be seen that the signs have been changed. Therefore, the signals for the currents and the Voltage at the input of the subsystem are multiplied by the sign of the reference current. For positive reference currents, a $'1'$ at the output of the OR-Block connected to the reset-input of the RS-flipflop means that the Voltage E should be $-V$ in the next time step, since the output of the flip-flop is set to zero. For negative currents, a $'1'$ at the output of the same OR-block is supposed to set the output of the flip-flop to $'1'$ so that $E = +V$. To achieve this, the output of the OR-Blocks has to be inverted for $I_{ref} < 0$.

That is done by an extra logic circuit shown in figure 4.1.3. The truth table for this logic circuit is shown in table 4.1.1. It can be seen, that the output of the OR-block remains unchanged for $I_{ref} > 0$. For $I_{ref} \leq 0$ the output of the OR-blocks is

inverted. This is also the truth table of an XNOR function. Hence, the output of the OR-blocks and the sign of the reference current are connected through and XNOR. This is implemented in Simulink as shown in figure 4.1.3.

$\mathbf{I_{ref} > 0}$	**OR-out**	$\mathbf{I_{ref} > 0}$ **AND OR-out**
0	0	1
0	1	0
1	0	0
1	1	1

Table 4.1.1 Logic for inverting the output of the OR-Blocks if $I_{ref} < 0$, rearranged.

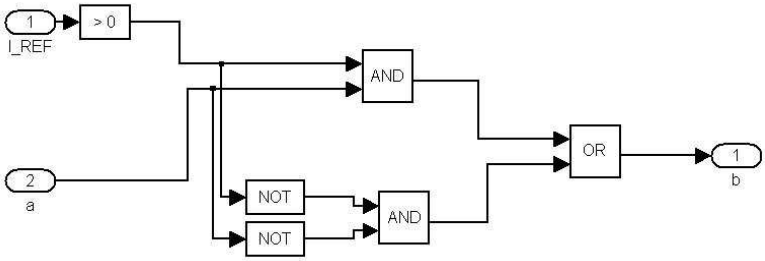


Figure 4.1.3 XNOR to invert the output of the OR-blocks if $I_{ref} < 0$

4.2 Simulation Results

To simulate the model for the inner loop of the switch circuit, a reference current of $I_{ref} = \pm 5\ A$ and a constant voltage of $U = 5\ V$ are chosen. The parameter for the inductance used is $L = 80 \cdot 10^{-6}\ H$, based on the value from [Jön88]. The parameter for the bridge voltage is chosen to $E = 178.5\ V$. By choosing the value for the bridge voltage to this value, the rated voltage $U_A = 150\ V$ of the DC-motor is 80% of the bridge voltage. At this point, the rated operation of the motor is supposed to be. The simulation is done with positive and with negative reference current.

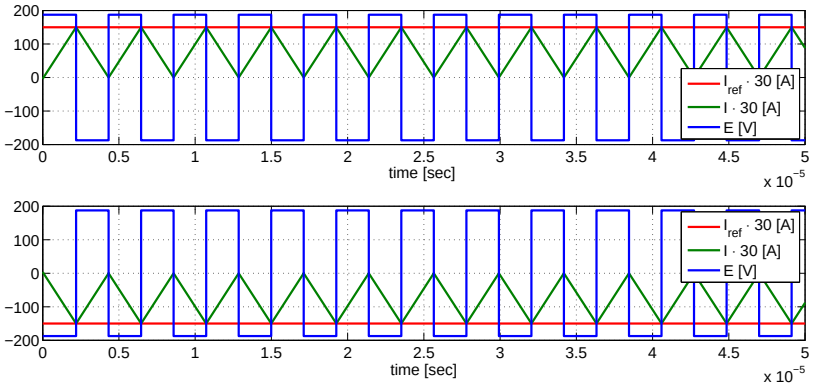


Figure 4.2.1 Simulation results for the inner loop of the current circuit

The inductor current I, the reference current I_{ref} and the bridge voltage E of the simulations are shown in figure 4.2.1. The upper part of figure 4.2.1 shows the results for a positive reference current. The inductor current rises linearly while $E = +V$. When it reaches the maximum value I_{ref}, then the bridge voltage switches to $E = -V$. After that the inductor current I decreases linearly until it reaches zero. Then the bridge voltage is switched to $E = +V$ again.
The lower part of figure 4.2.1 shows the simulation results for a negative reference current. In this case, the current I decays linearly while $E = -V$. When it reaches the reference value, the bridge voltage changes to its positive value $E = +V$, so that the current I rises until it reaches zero. The bridge voltage is then switched to its negative value again. This shows, that the simulation is working for constant positive and negative reference currents.

To test with a non-constant reference current, a ramp signal was chosen. This reference signal crosses zero. The parameters for this simulation are the same as above

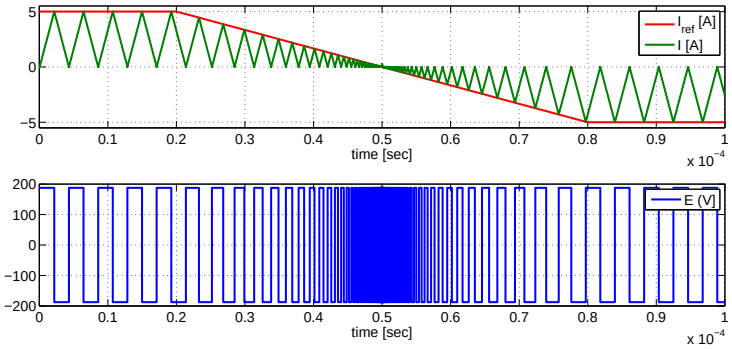


Figure 4.2.2 Reference current and current through the inductor

with constant reference current. The only difference is, that the reference current now goes linearly down from $+5\,A$ to $-5\,A$. Figure 4.2.2 shows the results. It can be seen, that the behavior is the same as for a constant reference current. But since the reference current passes zero, the frequency of the current through the inductor increases when the reference current gets smaller. This means, that the switching frequency of the transistors in the current circuit increases as well. In reality, the switching frequency of the transistors is limited due to e.g. switching time delays. Therefore, there should be set a limit to how much the frequency of the inductor current I can increase. This is done in the next section.

4.3 Hysteresis

To prevent the switching frequency of the transistors from getting too high, a hysteresis is included. For that purpose a comparator with hysteresis is included in the real circuit, as shown in figure 4.3.1. The resistances R_{H1} and R_{H2} can be chosen to adjust the hysteresis.

Applying the rule of voltage divider leads to:

$$\frac{u_I - V_1}{R_{H1}} = \frac{V_1 - V_{out}}{R_{H2}}. \tag{4.3.1}$$

Hence the voltage at the non-inverting input of the comparator depend on the output

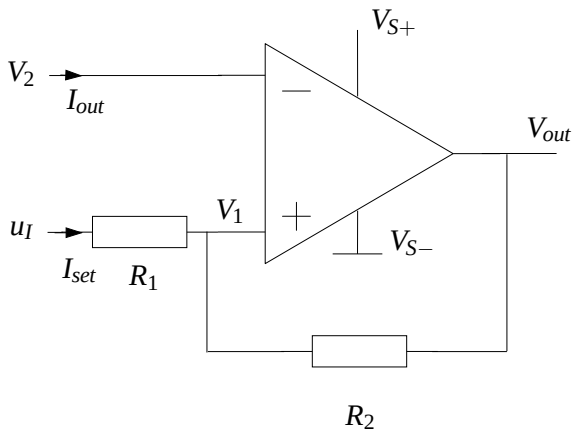


Figure 4.3.1 The comparator with hysteresis

voltage V_{out} and the voltage u_I:

$$V_1 = \frac{R_{H2}}{R_{H1}+R_{H2}} \cdot u_I + \frac{R_{H1}}{R_{H1}+R_{H2}} \cdot V_{out}. \tag{4.3.2}$$

For $V_2 < V_1$, the output voltage of the comparator ist $V_{out} = V_{S+}$. The the voltage at the non-inverting input is for this case:

$$V_{1H} = \frac{R_{H2}}{R_{H1}+R_{H2}} \cdot u_I + \frac{R_{H1}}{R_{H1}+R_{H2}} \cdot V_{S+}. \tag{4.3.3}$$

When V_2 grows larger than V_{1H}, the output voltage of the comparator switches to $V_{out} = V_{S-}$.

For $V_2 > V_1$, the output voltage is $V_{out} = V_{S-}$. The voltage at the non-inverting input is for this case:

$$V_{1L} = \frac{R_{H2}}{R_{H1}+R_{H2}} \cdot u_I + \frac{R_{H1}}{R_{H1}+R_{H2}} \cdot V_{S-}. \tag{4.3.4}$$

The output voltage switches back to $V_{out} = V_{S+}$, when V_2 gets smaller than V_{1L}. Since $V_{S+} > V_{S-}$, this leads to a hysteresis as seen in figure 4.3.2 .

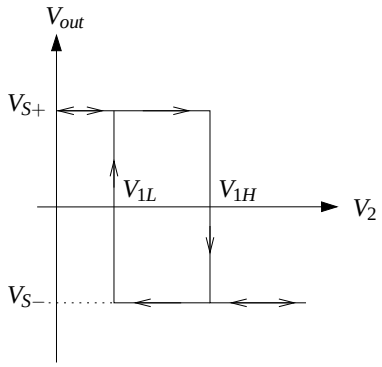


Figure 4.3.2 The Hysteresis

The effect of the hysteresis is, that the signal to switch the transistor at the value of the reference current is given slightly later as without hysteresis. The inductor current I changes its slope therefore at a slightly bigger absolute value than the reference current.
The advantage of the hysteresis shows when the reference current passes zero. The frequency of the current I through the inductor L can just increase until a value predetermined through the hysteresis. This prevents the transistors from too high switching frequencies. Furthermore, the simulation gets too slow when the frequency of I gets too high.

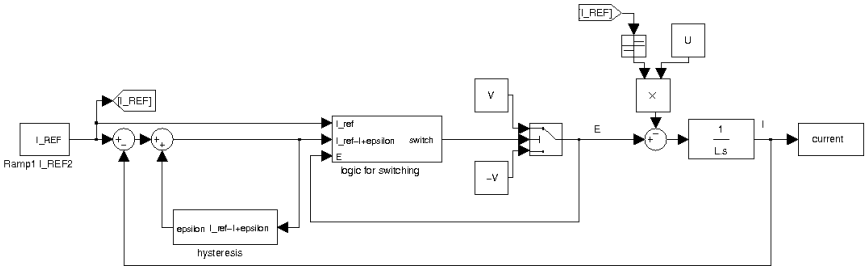


Figure 4.3.3 Simulink model of the current loop with hysteresis.

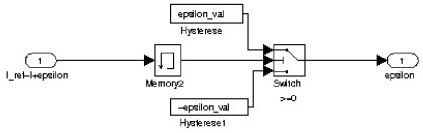


Figure 4.3.4 The hysteresis block in figure 4.3.3

In the simulation, the hysteresis is implemented by adding a small constant to the difference between the reference current and the output current. The sign of this constant depends on the sign of the reference current I_{ref}. This will increase the reference current , which simulates the fact that the inductor current I increases until a value slightly higher than the reference value due to the hysteresis. The model for the hysteresis is shown in figure 4.3.4. How this model is included in the simulation model for the inner sinus switch loop is shown in figure 4.3.3.

The results of the simulation of the inner sinus switch circuit including hysteresis is shwn in figure 4.3.5.

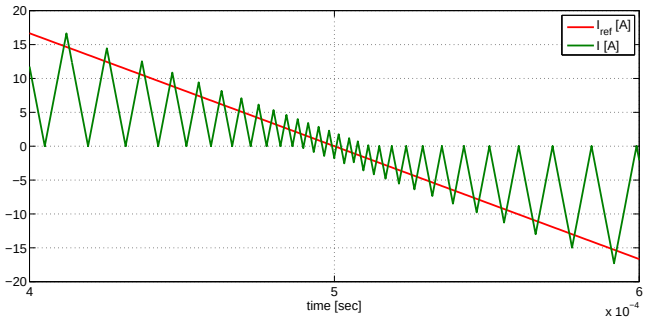


Figure 4.3.5 Reference current and current through the inductor with hysteresis

It can be seen, that the frequency of the inductor current I increases until a certain value when the reference current I_{ref} approaches zero. The frequency stays at this value while I_{ref} passes zero. When the reference current leaves the hysteresis region into negative currents, the frequency increases again. This shows, that the hysteresis is included in the simulation model as intended.

4.4 Internal feedback of the Output Voltage

So far, the voltage U has been added to the simulation as a constant. But in the real circuit, the voltage over the inductor is $E - U_{out}$, including the output voltage of the sinus switch U_{out}. To simulate the output voltage, the model is extended by a capacitance C representing the capacitors in the real circuit (compare to figure 2.3.1).

In the s-plane, a capacitor is represented as an integrator:

$$U = \frac{1}{C \cdot s} \cdot I. \tag{4.4.1}$$

Therefore, an integrator block and a constant $\frac{1}{C}$ are added to the model in the simulation. The output of this integrator, which represents the output voltage U_{out}, is fed back into the model as shown in figure 4.4.1. This internal feedback replaces the constant voltage U.

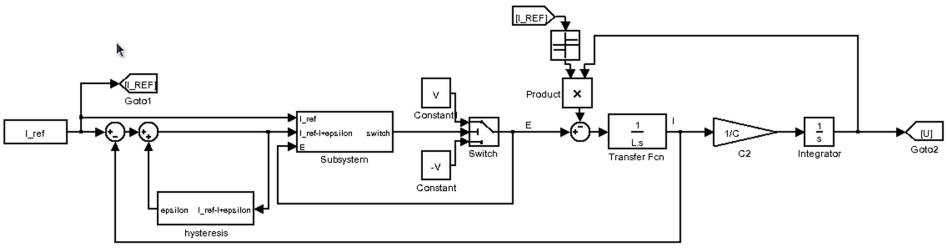


Figure 4.4.1 simulink model of the current circuit with output voltage fed back

To simulate this model, the parameters for inductance, power supply voltage and hysteresis constant have been chosen to the same values as in previous simulations. The capacitance has been chosen to $C = 1.2\ mF$, which is higher than is [Jön88], but should be used for simulations because the voltage ripple is reduced more than with a smaller capacitor. Figure 4.4.2 shows the result of this simulation. The upper part shows the reference current and the inductor current. The reference current is constant and changes sign from $I_{ref} = +10\ A$ to $I_{ref} = -10\ A$ when half the simulation time has passed. Because of the hysteresis, the inductor current has its peak at $\pm 12\ A$.
The lower part shows the output voltage U_{out}, which is fed back into the switch circuit. While the reference current is positive, the output voltage rises linearly including a ripple, as mentioned in section 2.2. When I_{ref} is negative, the output voltage falls linearly, again containing a ripple.

This shows that the simulation including internal feedback of the output voltage works as intended.

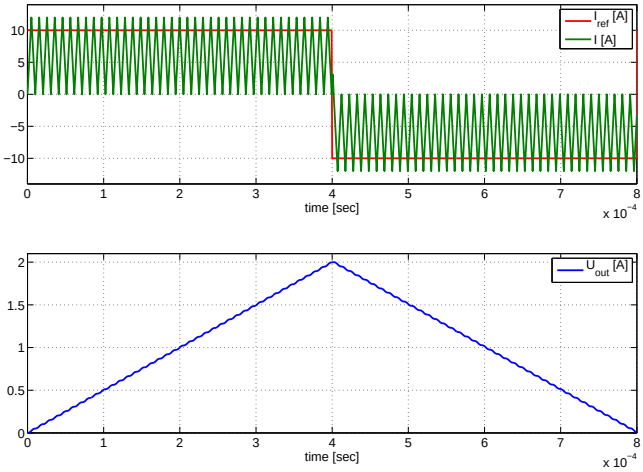


Figure 4.4.2 Reference current and inductor current in the current circuit with the output voltage fed back.

4.5 Optimizing the Simulation Time

To achieve a real time of 1.5 minutes to simulate a simulation time of $1 \cdot 10^{-4}$ seconds, some properties in Simulink have been changed in contrast to the default properties. The default solver called 0*de*45 has been used, where the parameters for maximal, minimal and initial step size have been changed to *minimal step size* = $1 \cdot 10^{-9}$, *maximal step size* = $1 \cdot 10^{-2}$ and *initial step size* = $1 \cdot 10^{-4}$ to optimize the simulation time. Furthermore, zero crossing detection has to be activated for the respective blocks. Without activating the zero crossing detection the simulation result may be wrong, because the solver is not able to detect discontinuities in the simulation [Inc09].
To accelerate the simulation, the simulation is run in Accelerator Mode. When using this mode instead of the Normal Mode, the Simulink model is first translated into a C-Mex S-Function (C-Code). Then, this S-Function is executed in Matlab to run the simulation [Inc09]. Using this accelerator seemed to speed up the simulation slightly.

Since despite all these changes of the Simulink properties the real time for running a simulation of $1 \cdot 10^{-4}$ seconds is still about 1.5 minutes, an alternative model for the current circuit is developed in chapter 4.6.

4.6 Alternative model for the Current Loop

To decrease the the real time needed for a simulation, a model for the current circuit using less Simulink blocks than the model derived in the previous chapters is developed. The Simulink block diagram of this model is shown in figure 4.6.1.

The idea behind this model is, that the inductor current should determine when the Voltage E changes sign. This is possible, because it is known from the real circuit how the voltage E behaves depending on the inductor current. The model does not simulate the physical behavior of the transistors switching and the free-wheel diodes, it rather simulates the behavior of the voltage E dependent on the output current of the circuit. The bridge voltage E is not used to determine the switching signal for itself and thus there is no feedback of it in the model. Here again the reverse-recovery

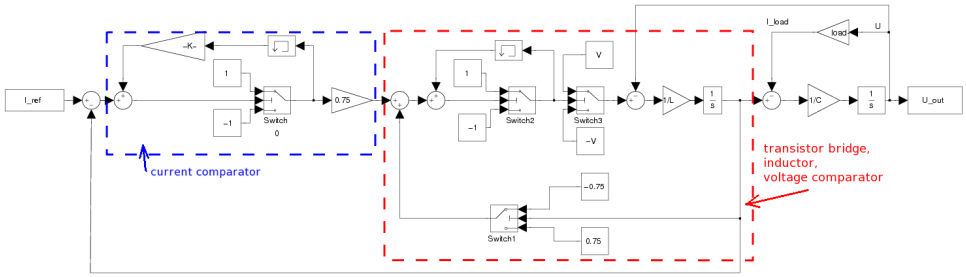


Figure 4.6.1 Alternative model to simulate the current circuit

current is neglected, since it is possible to make it very small [Jön88]. Furthermore, this model includes hysteresis as well, based on section 4.3.

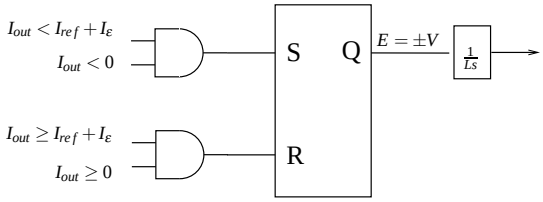


Figure 4.6.2 SR flip-flop that models the behaviour of the current circuit.

Assuming that the behavior of the bridge voltage E depending on the output current is known, the behavior of the current circuit can be modeled with an RS-flip-flop. The flip-flop is shown in figure 4.6.2. That it models the behavior of the inner part of the sinus switch correctly is shown with the help of an example. Figure 4.6.3 shows an example shape of the reference current I_{ref}, the output current I_{out} and the bridge voltage E. As already mentioned in section 2.2, each cycle of the inductor current can be divided in 4 phases, which are labeled (1), (A), (2) and (B) here. Phase (1) is the rising slope of the output current, phase (2) the falling slope, phase (A) is the point at the reference current, where the rising slope changes into the falling slope and phase (B) where the falling slope changes into the rising slope again.

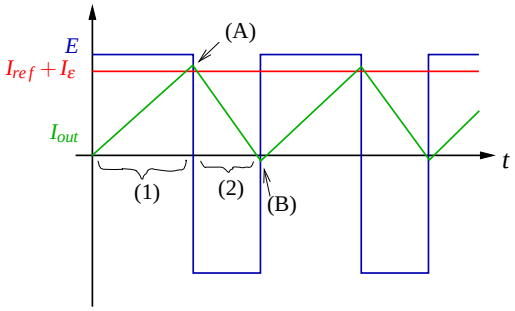


Figure 4.6.3 An example of the behavior of E dependent on th output current of the model.

(1): At the start of the cycle, the bridge voltage is $E = +V$. The inductor current I rises therefore. It is $I \geq 0$ and $I < I_{ref} + I_\varepsilon$. It is known that in this phase $E(k) = E(k-1)$, where k is the actual time point and $k-1$ is the previous time point. Comparing to figure 4.6.2, it can be seen that in this phase both inputs of the flip-flop are zero. Thus, the flip-flop keeps its output at the same value as in the previous time point, so

that $E(k) = E(k-1)$ is fulfilled.
(A): In this phase, the inductor current reaches the reference current. The bridge voltage has to change its sign from $+V$ to $-V$ at this point. Since it is $I > 0$ and $I \geq I_{ref} + I_\varepsilon$, the signal at the set-input of the flip-flop is zero, while the signal at the reset-input is one. Hence the output of the flip-flop is reset to zero, so that the bridge voltage changes to $E = -V$.
(2): Since the bridge voltage in negative, the inductor current is falling. It is again $I > 0$ and $I < I_{ref} + I_\varepsilon$, as in phase (1), so that the output value of the flip-flop remains unchanged at zero. The bridge voltage is therefore kept at $E = -V$.
(B): In this phase, the inductor current passes zero. The bridge voltage has to change back to $E = +V$, so that a new cycle can start. It is $I < 0$ and $I < I_{ref} + I_\varepsilon$ and thus the set-input of the flip-flop is one and the reset-input is zero. The output of the flip-flop is set to one again. So the bridge voltage is set to $E = +V$.

This flip-flop has been implemented in Simulink using switch-blocks, as seen in figure 4.6.1. In this model, the Switch 1 determines the sign of the inductor current I and the Switch 0 decides if the output current is bigger or smaller than the reference current I_{ref} plus the current from the hysteresis loop I_ε. Those two signals are then connected through a plus sign similar to an AND function. The Switch 2 simulates the flip-flop, which can be in “set”, “reset” or “keep output state” mode. The output value of Switch 2 is translated into $\pm V$ by Switch 3, which gives out the bridge voltage E. Because the voltage over the inductor is the difference between the bridge

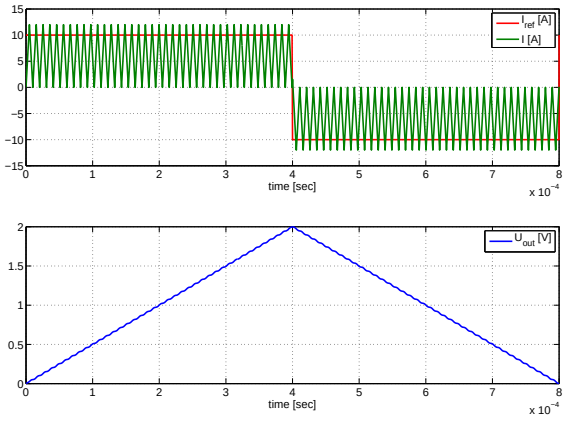


Figure 4.6.4 Simulation of the current circuit with the alternative model

voltage E and the output voltage U_{out}, the output voltage is subtracted from the bridge voltage. Multiplying this voltage difference by $\frac{1}{LS}$ results in the inductor current I. The inductor current is superposed by the current of the load. Here, the load is a resistor with the resistance R, so that the superposed load current is $I_{load} = \frac{U}{R}$. Those two superposed currents result in the output voltage U_{out} over the load through integration due to the capacitors.

To simulate the model, the parameters are the same as in chapter 4.4. No load has is connected to the output for this simulation. As can be seen in figure 4.6.4, the simulation results are similar to those in chapter 4.4. The difference is however, that the simulation takes less time than with the previous model.

For further simulations, the model developed in this section is used, since it is less complex and thus easier to handle and to oversee for further extensions.

5. Simulating the Outer Loop for the Voltage

This chapter describes, how an outer voltage control loop is added around the inner sinus switch circuit to control the output voltage U_{out} of the sinus switch.

5.1 The Voltage Controller

To control the output voltage U_{out}, an error amplifier is introduced before the sinus switch circuit [MUR89], which takes the desired voltage U_{ref} and the output voltage of the current circuit U_{out} as inputs. The amplifier is shown in figure 5.1.1, with general input voltages U_{a1} and U_{a2} and a general output voltage U_b.

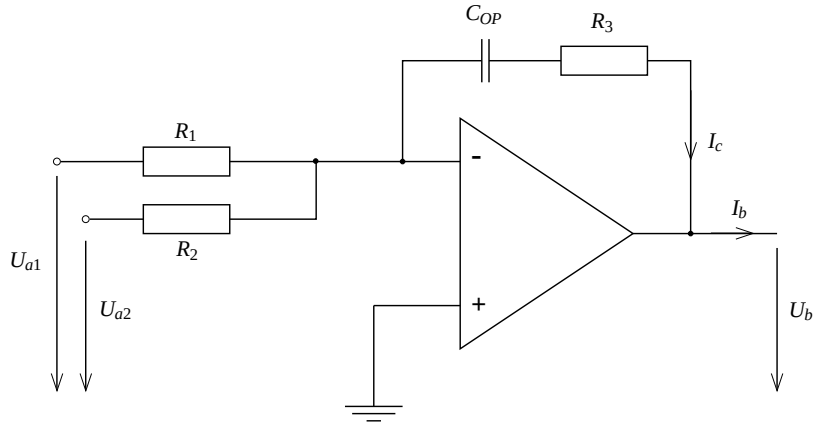


Figure 5.1.1 The operational amplifier for voltage control of the switch circuit/motor.

For this operational amplifier circuit, the output voltage U_b depending on the input voltages U_{a1} and U_{a2} is:

$$U_b = -\frac{1+T_{c3}\cdot s}{T_{c1}\cdot s}\cdot U_{a1} - \frac{1+T_{c3}\cdot s}{T_{c2}\cdot s}\cdot U_{a2}.$$

With $T_{c1} = R_1 \cdot C_{OP}$, $T_{c2} = R_2 \cdot C_{OP}$ and $T_{c3} = R_3 \cdot C_{OP}$

The last equation is equivalent to:

$$U_b = \frac{1+T_{c3}\cdot s}{T_{c1}\cdot s}\cdot\left(\left(-\frac{T_{c1}}{T_{c2}}U_{a2}\right) - U_{a1}\right). \tag{5.1.1}$$

If now the reference voltage U_{ref} and the output voltage of the sinus switch circuit U_{out} are chosen to:

$$\begin{aligned} U_{out} &= U_{a1} \\ U_{ref} &= -\frac{T_{c1}}{T_{c2}}\cdot U_{a2} \\ &= -\frac{R_1}{R_2}\cdot U_{a2}, \end{aligned} \tag{5.1.2}$$

the operational amplifier circuit gives a transfer function, that takes the difference between the reference voltage U_{ref} and the output voltage of the current circuit U_{out} as an input and can thus be used as a controller for the motor voltage. Equations (5.1.1) and (5.1.2) together then result in:

$$U_b = \frac{1 + T_{c3} \cdot s}{T_{c1} \cdot s} \cdot (U_{in} - U_{out}) . \tag{5.1.3}$$

Equation (5.1.2) can for example be realized by an inverting amplifier [KSW00].

5.2 The Voltage Control Loop

Using a voltage controller as shown in the previous section to control the output voltage of the sinus switch current circuit leads to a block circuit as in figure 5.2.1.

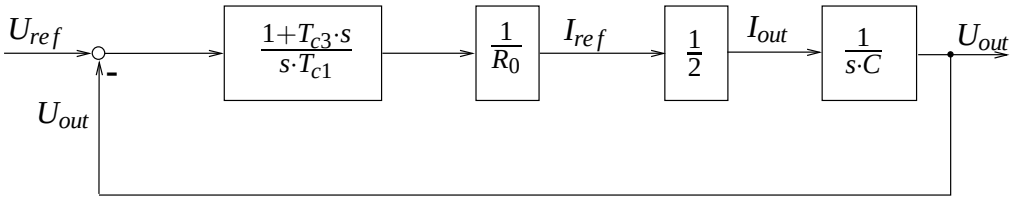


Figure 5.2.1 The voltage loop.

The true inductor current has a sawtooth shape. Therefore, the average value of the inductor current I is half its peak value. For the switch circuit, the peak value of the inductor current is always the value of the reference current plus the hysteresis. For the purpose of analyzing the voltage control loop, the hysteresis is neglected. The average value of the inductor current I is then half the reference current I_{ref}. The current circuit is thus replaced by the constant $\frac{1}{2}$ for dimensioning the voltage control loop.

The open-loop transfer function of the model in figure 5.2.1 is:

$$L(s) = \frac{1}{2} \, \frac{1 + T_{c3} \cdot s}{s^2 \cdot T_{c1} \, R_0 \, C} . \tag{5.2.1}$$

This gives an approximate bode diagram as seen in figure 5.2.2. For low frequencies the transfer function has the behavior of a double integrator, thus the bode diagram for low frequencies has a slope of $-40 \, \frac{dB}{decade}$. For high frequencies the transfer function behaves like a single integrator. Hence the bode plot for high frequencies has a slope of $-20 \, \frac{dB}{decade}$. The intersection point of those two asymptotes ω_1 and the intersection of the high frequency asymptote with $0 \, dB$ ω_2 can be calculated to:

$$\omega_1 = \frac{1}{T_{c3}} \quad \text{and} \quad \omega_2 = \frac{T_{c3}}{2 T_{c1} R_0 C}$$

When the desired open loop characteristics of the voltage loop are given through the frequencies ω_1 and ω_2, the parameters in the transfer function 5.1.3 can be determined as the following:

$$T_{c1} = \frac{T_{c3}}{2 \, \omega_2 \, R_0 \, C} \quad \text{and} \quad T_{c3} = \frac{1}{\omega_1}$$

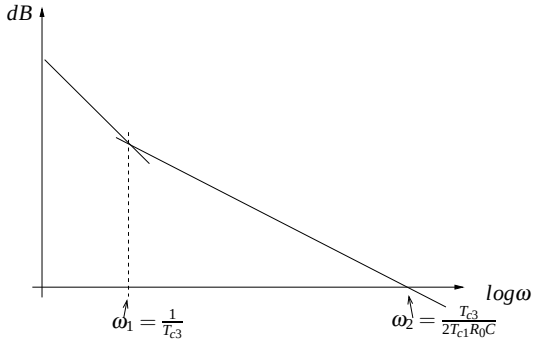


Figure 5.2.2 Approximate Bode diagram of the voltage loop.

The resistor R_0 gets chosen to e.g. 400Ω. After calculating T_{c1} and T_{c3} according to the equations above, all parameters for the simulation are known. Also, from this the values for the resistors in the operational amplifier circuit from figure 5.1.1 can be determined. The values chosen for the simulation might not be realistic, but for the purpose of this thesis they are sufficient. Important here are stable dynamics of the voltage control loop to be able to use it for further simulation. The optimization of the voltage controller is not part of this thesis.

5.3 Simulating the Voltage Loop

First, the voltage control loop is simulated with a constant of $\frac{1}{2}$ instead of the current circuit. The parameters shown in table 5.3.1 are used. The simulink model is implemented according to figure 5.2.1.

The simulation results are shown in figure 5.3.1. As the reference voltage U_{ref}, a

L	$80 \cdot 10^{-6}\ H$	**V**	$150\ V$
C	$1.2\ mF$	$\mathbf{R_0}$	400Ω
ω_1	1000	ω_2	3000

Table 5.3.1 Parameters for simulation of the voltage loop.

step from $0\ V$ to $5\ V$ has been chosen. No load is connected to the output. Figure 5.3.1 shows the reference voltage U_{ref} and the output voltage U_{out} in its lower part. The output voltage settles at the value of the reference voltage in steady state with a settling time of $t_s = 3.6\ ms$. It needs a rising time of $t_r = 0.45\ ms$. The overshoot of the output voltage is approximately 16% of the reference voltage. For real application this overshoot is too high, but for this thesis it is sufficient to have a stable behaviour. The dynamics could be optimized by, for example, increasing the difference $\omega_2 - \omega_1$. This would increase the phase margin of the voltage control loop. The Damping inchreases when the phase margin inchreases [Wer09]. Thus, increasing the difference $\omega_2 - \omega_1$ would lead to a smaller overshoot. However, this is not part of the thesis.

For further simulations the reference voltage should be restricted to a maximum value, so that the output voltage in spite of its overshoot does not exceed the bridge voltage E. This is because the switch circuit only works properly for output voltages smaller than the bridge voltage. Also, the dynamics of the output voltage might

change, when a load is connected to the output of the switch circuit.
The upper part of figure 5.3.1 shows the reference current of the switch circuit and

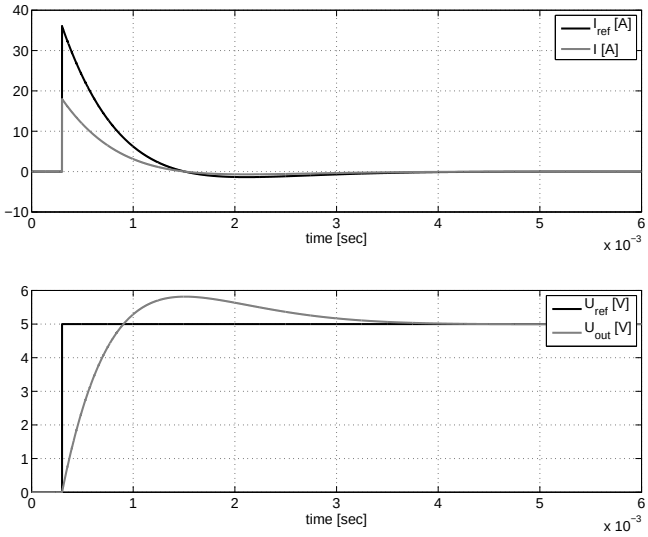


Figure 5.3.1 Simulation result to a step on the voltage loop.

its inductor current. Since the switch circuit is substituted with a constant of $\frac{1}{2}$ for this simulation for reasons mentioned above, the inductor current is always half the reference current. The reference current has an overshoot of 36 A when the step of 5 V of the reference voltage occurs and settles at zero current again after 3.5 ms. This is as well too high for real applications, but for this thesis sufficient. By choosing ω_2 smaller, the overshoot in the reference current should decrease.
According to this simulation, the voltage control loop is stable.

5.4 Simulating the Voltage Loop Including the Current Circuit

Now the current circuit according to section 4.6 is added to the voltage control loop. In the model as shown in figure 5.2.1, the constant $\frac{1}{2}$ is exchanged with the model of the current circuit. The Simulink model is shown in figure 5.4.1.

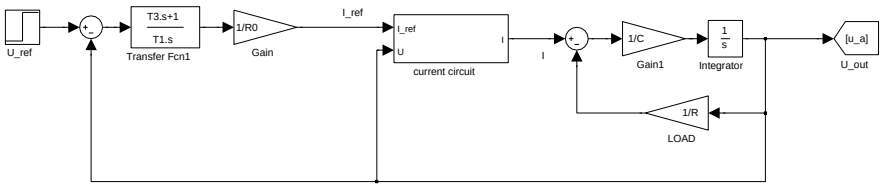


Figure 5.4.1 Simulink model for the voltage loop including the model for the current circuit.

The parameters used for simulating the outer voltage loop are again those from table 5.3.1. For the current circuit, the hysteresis is set to $\varepsilon = 2$. In figure 5.2.1, a load R is connected to the output of the switch circuit. For this simulation though, no load is connected to the output ($R \to \infty$).

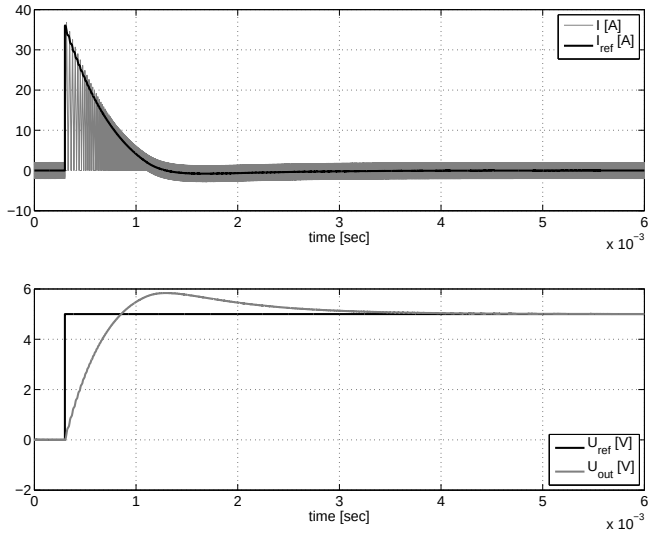


Figure 5.4.2 Simulation results for the voltage loop including the model for the current circuit.

Figure 5.4.2 shows the simulation results. The dynamic behavior is similar to that with a constant instead of the current circuit. The reference current, shown in the upper part of the figure, has an overshoot of ca. 36 A when the step in the reference voltage occurs. It settles down to zero after ca. 2.54 ms, when the output and reference voltages are approximately equal. As expected, the output current of the circuit, which is the inductor current I, is sawtooth shaped having a maximum value of the reference current plus the hysteresis. The lower part of figure 5.4.2 shows the output and reference voltage. As a reference voltage, a step to 5 V is applied to the voltage loop. The output voltage settles down after $t_s = 3.8$ ms. The rise time here is $t_r = 0.42$ ms and the overshoot is ca. 17% of the reference voltage. All of that is is comparable to section 5.3.
This means, that even with the current circuit included, the behavior of the voltage control loop is stable and sufficient for this thesis.

5.5 Simulating the Voltage Loop with a DC-motor as Load

After doing a basic dimensioning of the voltage control loop and testing it with the current circuit, a DC-motor is added to the output as a load. Figure 5.5.1 shows the

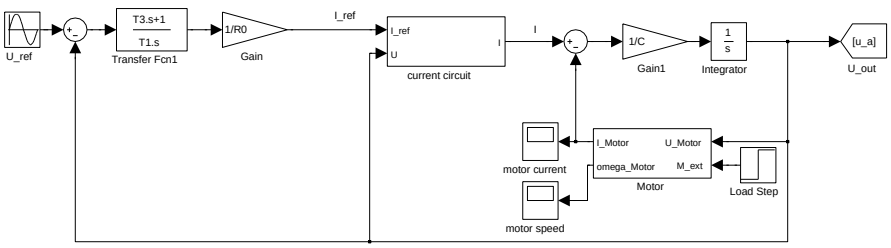


Figure 5.5.1 Simulink model for the voltage loop including the model for the current circuit.

model used in Simulink for the simulation. The model of the DC-motor is that developed in section 3.

The parameters used for the simulation are the same as in the previous sections. For the motor, the parameters used are those from section 3. The input signal to the voltage loop is a pulse signal with an amplitude of 5 V and a period of 0.03 sec. At 0.02 seconds, a load step of 5 Nm is applied to the motor This is a very big torque for the used motor, but it helps to emphasize the effect of a torque applied to the DC-motor. The results of the simulation are shown in figure 5.5.2. This figure shows the reference current and output current of the switch circuit in its first, most upper part and the reference voltage and output voltage of the voltage control loop in its second part. Furthermore, it shows the current and the speed of the DC-motor.

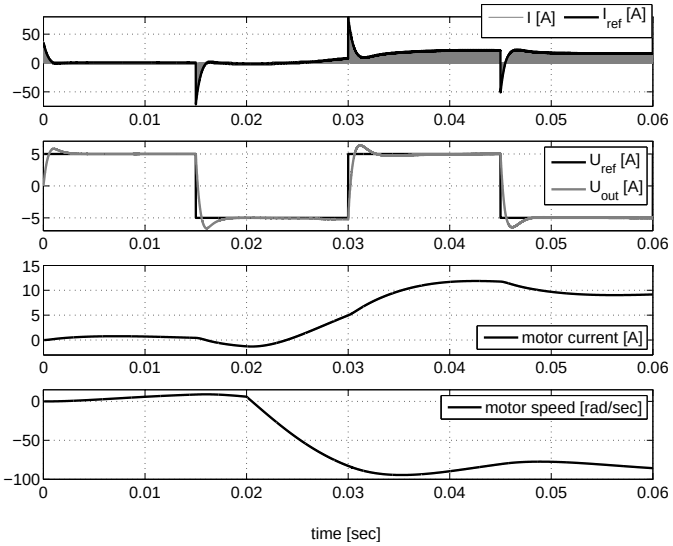


Figure 5.5.2 Simulation results for the voltage loop including the model for the current circuit with a dc motor as load.

It can be seen in figure 5.5.2, that the behavior of the motor is similar as in section 3 for each pulse, also for a negative input voltage. When the sign of the reference voltage changes, the reference current of the current circuit has an overshoot, since the output voltage has to be adjusted to the reference voltage. Because of the tuning of the voltage controller in section 5.2, the output voltage does not follow the reference voltage immediately, as already seen in the previous section. Since the output voltage U_{out} of the sinus switch changes a lot slower than its reference voltage, the motor current does not have as high peaks as the reference current. However, it can be seen that the motor current rises when the voltage pulse is positive. This is described by equation (3.2.7). According to equations (3.2.8) and (3.2.6), the motor speed results from the motor currents from integration.
The load step applied to the motor decreases the speed of the motor (equation (3.2.8)) and therefore increases the motor current (equations (3.2.5) and (3.2.7)). In order to keep the voltage at the desired value, the voltage controller increases the reference current for the switch circuit.

Simulating the voltage control loop including the current circuit with a DC-motor as a load leads to the expected behavior of the motor.

6. Adding a Slave Circuit

In the previous section, a single current circuit has been used to provide the load at the output with voltage and current. The switching frequency of the transistors in the transistor half-bridge changes with the output voltage and the reference current. The optimal range for this switching frequency is between 10 and 20 kHz [Jön09], which limits the power range that can be used. To extend those limits, several switch circuits can be connected in parallel. Each switch circuit connected in parallel increases the output current, whereas the switching frequency of each transistor can be kept in the limits of 10 and 20 kHz.

This chapter describes how a second current circuit is connected in parallel with the one described in section 4. A time shift between the two inductor currents is implemented, which can reduce the ripple of the output voltage. Furthermore, a method to synchronize these two inductor currents for all voltage and current combinations is introduced. Also, the effect of non-exact synchronization and inequal inductances are analyzed in this section.

6.1 The Slave Circuit

The slave switch circuit is connected in parallel to the master switch circuit as shown in 6.1.1.

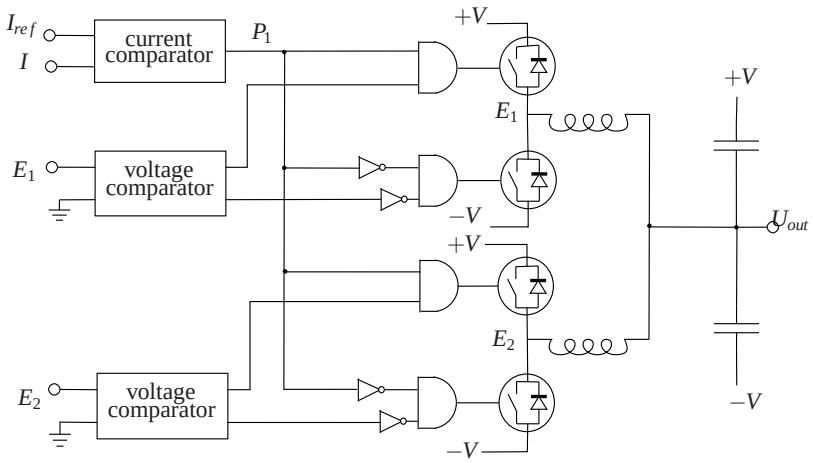


Figure 6.1.1 The switch circuit with a master and a slave module in parallel.[Jön05]

Slave and master module consist of identical components, which are those from section 4. They are comprised of a transistor half-bridge connected to $\pm V$ and a inductor delivering current to the output. By connecting the two modules in parallel as shown in figure 6.1.1, the inductor currents of both modules add up to an output current. Both parallel modules share a common pair of capacitors, also connected to $\pm V$. Those capacitors are the same as in sections 2 and 5.
The modules get the same switch-off signal for the transistors from the current comparaor, but the switch-on signal is given individually for each module by the voltage comparators. Similar to the previous section, the master and slave module get a switch-off signal for their transistors, when the inductor current of the master circuit reaches its reference value, shown as signal $P1$ in figure 6.1.1. The switch-on signal

is generated by the voltage comparator of each module when its inductor current goes through zero.

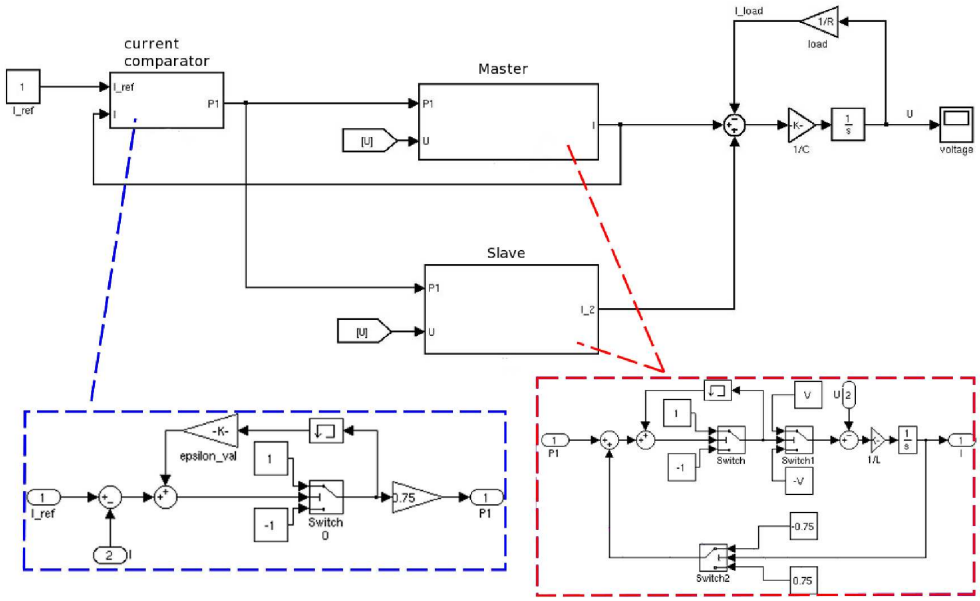


Figure 6.1.2 The switch circuit with a master and a slave module in parallel modeled in Simulink.

Figure 6.1.2 shows how the switch circuit including master and slave module is modelled in Simulink. The basis for this is the model for the current circuit from section 4.6 as seen in figure 4.6.1. The part taking the reference current and the inductor current of the master module as an input and having the signal P_1 as an output represents the current comparator. It determines whether the inductor current of the master module is equal to the reference current and outputs this information as the signal P_1. Both master and slave module use this signal. Everything in 4.6.1 except the current comparator part is copied to make up the master and the slave module. The inductor currents of those two modules, the master and slave current, are then added together with the load current. This total output current is then integrated by a capacitance that equals the combined value of the two output capacitances shown in figure 6.1.1. According to section 2.2 they can be merged to one capacitance. The integration of the output current by the capacitance leads to the output voltage U_{out}.

As seen in figure 6.1.2, the master module is operated in a closed-loop system, since its inductor current is fed back through the current comparator. The feedback results in a stable operation of the master module. The slave module in contrast does not have a feedback. It takes the output of the current comparator as a switching signal. Therefore, the slave module operates in open-loop.

Simulation with the Slave Circuit

For testing its functioning, the described model is simulated with a constant reference current of $I_{ref} = 1\ A$. No internal feedback of the output voltage U_{out} is used, to show the effect of a slave module in parallel to the master module. The voltage used by master and slave module is set to a constant value of $U = 110\ V$ instead of feeding back the output voltage. Since there is no load connected, the load current here is zero. The value of the hysteresis is set to $\varepsilon = 0.001$.

Figure 6.1.3 shows the switching signal P_1 in the upper part, the master current in the middle part and the slave current in the lower part. It can be seen, that master and

slave current have the same shape. The pulse P_1 triggers both to change from positive to negative slope. The slope of the master and slave current is changed internally by the modules themselves when the currents reach zero. This models the individual voltage comparators.

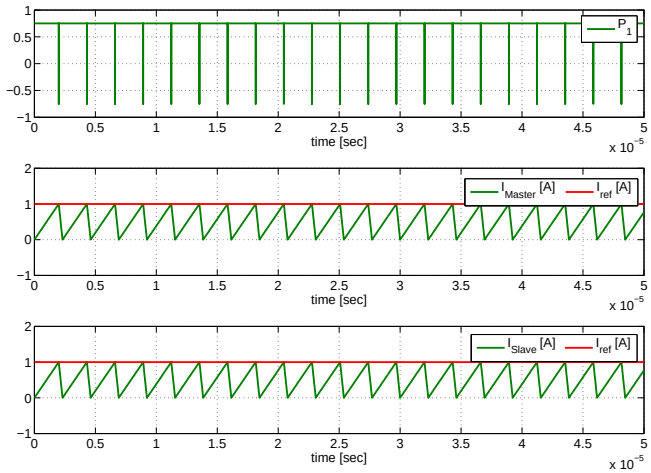


Figure 6.1.3 The switch-off signal P_1 and the currents of the switch circuit's master and slave module.

Since there is no internal voltage feedback and no load connected to the switch circuit, the voltage rises linearly with a constant reference current. The output voltage is shown in figure 6.1.4, when only the master module is active and when master and slave module are active. It can be seen, that the output voltage is higher for the second case although the reference current is the same for both cases. in both cases, the voltages are not smooth, but contain a ripple. This is due to the fact, that the current integrated by the conductor is not constant, but triangular shaped.

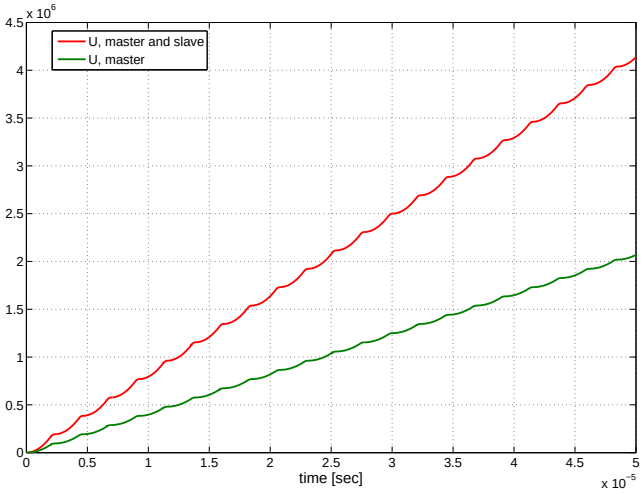


Figure 6.1.4 Output voltages of the switch circuit with only master module and with master and slave module.

6.2 Time Shift for the Slave Circuit

The inductor currents of the master and slave module are triangular shaped. With the setup described in section 6.1, both currents are in phase, i.e., they reach the reference current and zero at the same time. This leads to a higher output voltage as in the case without the slave module. Since the two inductor currents and also the total current are triangular shaped, the output voltage will not be smoth but contain a ripple, see section 6.1.

The slave circuit can also be used to reduce the ripple of the output voltage [Jön05]. To do so, a time delay is introduced between the inductor currents of the master and the slave in such a way, that the maximum of the slave current is half way between two maxima of the master current in the case of one slave module. This corresponds to a time shift of half a switch cycle. Figure 6.2.1 shows the principle of this Idea.

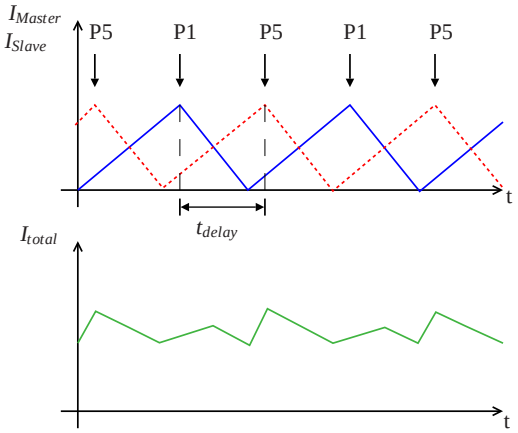


Figure 6.2.1 Time shifted currents of master and slave module and the total current.

The solid line in the upper part of figure 6.2.1 is the master modules current and the broken line the slave modules time shifted current. The arrows pointing on the tops of the currents indicate when a falling edge of the respective switch-off signal P_1 or P_5 occurs. The signal P_5 is the switch-off signal for the time-shifted slave current, which is generated from P_1. Adding up the two currents gives a total current as shown in the lower part of figure 6.2.1. The total current is not smooth, but the amplitude is smaller than in the case without a slave module. Integrating this current through the conductor then leads to less ripple compared to the case with only a master module.

The Time Shift

A time shift between the two inductor currents as described above can be obtained by a time shift between the switch-off signals P_1 and P_5 for the master and the slave module [Jön05]. The master module still gets the switch-off signal P1 as before. The slave module now receives the signal P5, which is derived from the signal P1 by time-shifting it half a switch cycle. Figure 6.2.2 shows how this time-shift is done by using a digital circuit.

An XOR inverts the signal P1 in case the reference current I_{ref} changes sign. Then P_1 is synchronized to a clock signal by a synchronizer. The synchronized signal P_1 resets a counter at every falling edge of the clock signal. Since the falling edge of P_1 falls together with the time that the inductor current reaches the reference current I_{ref}, this counter counts the time for one switch cycle. The pulse P_1 rises again at the next time instance. On this rising edge, the value of the counter is stored in a buffer.

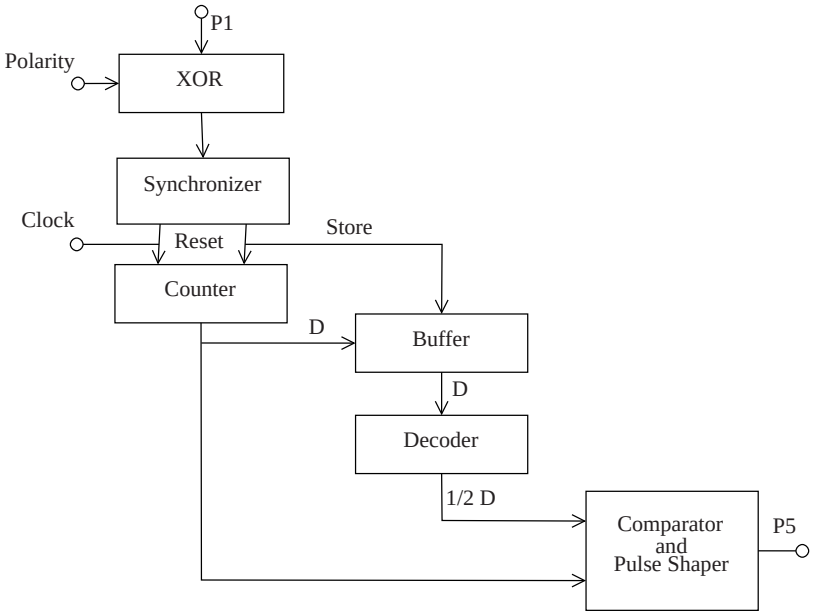


Figure 6.2.2 Time shifting the turn-off signal for the slave module. [Jön05]

That way the value of the time for one switch cycle is stored in the buffer. A decoder generates the time value for the time-shift from the time for one switch cycle stored in the buffer. In the case of only one slave circuit, the buffer value is divided by two, so that the output of the decoder is the time for half a switch cycle. A comparator takes this value and compares it to the actual counter value. The falling edge of the pulse P5 is given out by the comparator when the counter value is equal to the value for half the switch cycle. This signal is the time-shifted switch-off signal P_5 for the slave modules transistor that triggers the inductor current to change to a negative slope.

Simulink-Model for the Time Shift

The realization of the time shift as described in section 6.2 in Simulink is shown in figure 6.2.3. To invert the signal P1 when the reference current I_{ref} is negative,

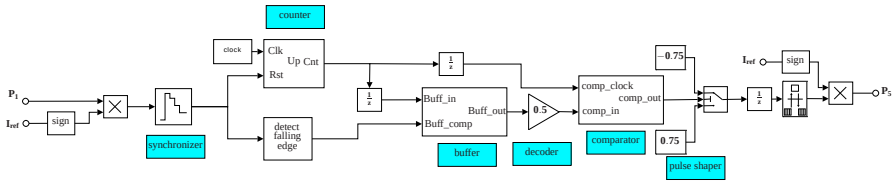


Figure 6.2.3 The time shift realized in Simulink

the sign of I_{ref} is multiplied with the signal P_1 provided by the current comparator (see section 6.1). To synchronize this signal, a zero-order-hold block provided by Simulink is used. By discretizing the signal P1, it gets synchronized to a clock running with the sample time used for the discretization. The digitalized and synchronized signal P1 is connected to the reset input of a counter. The clock input of the counter is connected to a clock with double the sample time as its period. Since the counter counts upwards at every falling and rising edge of the clock signal, it counts up one at every sampling instance. A falling edge of the synchronized signal P1 resets the counter. That means, that one time step before it gets reset, the output is the the time for a cycle of the master current.

The falling edge of the synchronized P1 also triggers the buffer to store the value connected to its upper input. Because of the unit delay block between counter and buffer, this is the counter value at the previous time instant. At the time step the falling edge of the synchronized P1 occurs, the counter gets reset to zero. So the value at the time instance before that is the counted time for the switch cycle.
The buffer outputs the time for one switch cycle. This output value is multiplied by 0.5, which represents the decoder. The decoded value is then compared with the counter value of the previous time instance. This is because the input value of the buffer also contains a delay of one time instance. Like this, the two values compared by the comparator originate from the same time point. The comparator determines whether its two input values are equal. If they are, then the comparator gives out a $'1'$. At the next time step the comparators output changes back to zero. This causes the switch behind the comparator to change its value from 0.75 to -0.75 and back. The output of this switch is the signal P1 time shifted half the time of the switch cycle, giving the signal P5. But this signal is still a discrete signal with the sampling time that was used for the synchronization of P1. To transform the signal P5 back into the continuous domain, a unit delay together with a rate transition block is used [Inc09]. The continuous signal P5 is then multiplied by the sign of the reference current to assure a correct signal for the slave module also for negative reference currents.

This signal P_5 is used as a switching signal for the slave module, similar as P_1 is the switching signal for the master module. It triggers the slave current to change its slope from positive to negative half way between the peaks of the master current.

Simulation of the Time Shifted Slave Current

To simulate the time-shifted slave current described above, the simulation model from figure 6.1.2 is extended by the time-shifting model in figure 6.2.3. The output of the current comparator in figure 6.1.2 is connected to the input of the time-shifted model in figure 6.2.3. The output of the time-shifted model is then connected to the upper part of the slave module in figure 6.1.2. The parameters used for the simulation are the same as in section 6.1. The reference current is positive and constant and a constant, positive voltage U is used instead of internal feedback of the output voltage.

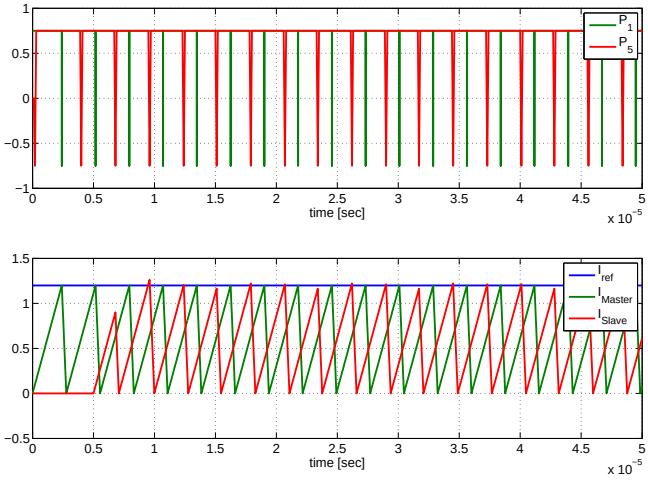


Figure 6.2.4 Switching signals P_1 and P_5 and master and slave currents of the switch circuit with time shifted slave current.

Figure 6.2.4 shows the simulation results. The upper part shown the switching

signal P_1 and its time shifted version P_5. It can be seen, that the pulses P_5 are approximately half way between two pulses P_1. Due to numerical reasons, P_5 is not always exactly in the middle between two P_1 pulses.
The slave module is activated after $5 \cdot 10^{-6}$ seconds. Since the start of the slave current is not half way between two points where the master current hits zero, it changes slope from positive to negative before it reaches the reference current. But the slave current synchronizes itself to reach the reference current and change its slope half way between two maxima of the master current.

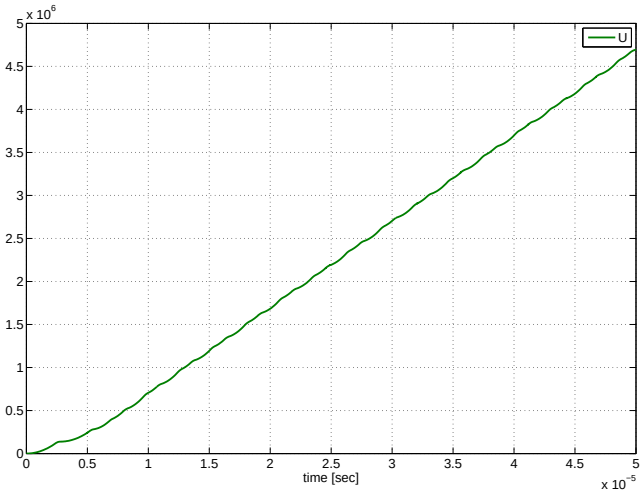


Figure 6.2.5 Output voltages of the switch circuit with time shifted slave current.

Figure 6.2.5 shows the output voltage, which is again linearly rising due to a constant reference current (compare to section 6.1). Compared to the output voltage when the slave current is not time shifted (figure 6.1.4), one can see that the ripple seems to be less now, as was intended for the time shifted slave current.

6.3 Synchronizing the Slave Circuit

This section treats the synchronization of the slave current.

Why Synchronization is necessary

As mentioned in section 6.1, the slave module is operated in open-loop. Hence, it is not necessarily stable during all operations and needs to be stabilized through synchronization.
Figure 6.3.1 [Jön88] shows the optimal slave current as a continuous line and the non-synchronized current as a dashed line. It can be seen, that a time error t_1 in the switching at zero current results in an error ΔI for the slave current. This current error again leads to an error t_2 when the current reaches zero the next time. Depending on the slopes of the current-triangles, the non-synchronized current either stabilizes itself or is instable. The current error ΔI dependent on the time errors t_1 and t_2 is [Jön88]:

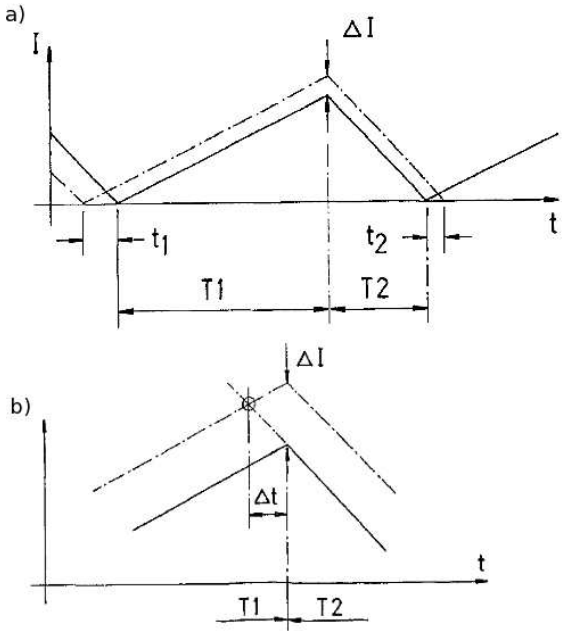


Figure 6.3.1 a) optimal slave current (continuous line) and non-synchronized slave current (dashed line); b) Zoom

$$\begin{aligned} \Delta I &= \frac{E-U}{L} \cdot t_1 \\ -\Delta I &= \frac{-E-U}{L} \cdot t_2 \end{aligned}$$

This can be derived from geometry in figure 6.3.1, where the slopes of the triangles are $\frac{E-U}{L}$ for the rising slope and $\frac{E+U}{L}$ for the falling slope.
Eliminating the current error ΔI in the equations above leads to:

$$t_1 = \frac{E-U}{E+U} \cdot t_2 \tag{6.3.1}$$

In order to see how the error of the slave current in comparison to its optimal shape develops over time, equation (6.3.1) is examined for three different cases of the voltage U.

- $U = 0$: The time errors are equal $t_1 = t_2$. That means the time error stays the same and the current error ΔI oscillates between a negative and a positive value, while keeping the same amplitude.

- $U > 0$: it is $\frac{E-U}{E+U} < 1$ and hence $t_2 < t_1$. Therefore, both time error and current error get smaller over time, so that the slave circuit stabilizes itself.

- $U < 0$: it is $\frac{E-U}{E+U} > 1$ and therefore $t_2 > t_1$. Since the time error grows over time, the slave circuit does not synchronize itself in this operating condition and must thus be stabilized.

In all the cases, it is assumed that the reference current is positive. With a motor as a load, this would correspond to motoring mode when $U > 0$ and to regenerative mode when $U < 0$ [Jön88]. In motoring mode, the switch circuit delivers power to the motor. In regenerative mode, the switch circuit receives power from the motor. The latter is the unstable mode that needs to be synchronized.

The Synchronization

The time error t_2 can be eliminated, if the down-slope of the slave current starts Δt earlier [Jön88], see figure 6.3.1 b). Then, the down-slope of the slave current coincides with the down-slope of its optimal shape. The time Δt, that the down slope has to start earlier, can be calculated in dependence of the time error t_1:

$$\Delta t = \frac{E - U}{2E} \cdot t_1 \tag{6.3.2}$$

The signal P_5 triggers the slave current to change its slope from positive to negative. With the introduces time-shift, this happens half way between two peaks of the master current. In order to synchronize the slave current, the switching signal P_5 is moved by Δt from its original position, so that its down-slope falls together with the optimal down-slope.

In order to calculate the adjustment time Δt as given in equation (6.3.2), the time error t_1 between the optimal shape of the inductor current in the slave circuit and the actual inductor current is needed. In reality this time can be measured by detecting the rise of the bridge voltage when master and slave current pass zero.
To simulate the measurements of this time, the bridge voltages of the master and slave module and the switching signal P_1 are used. Using P_1, half the time for one cycle of the master current is determined. The bridge voltage is then used to calculate the time difference between the zero crossings of the master current and those of the actual slave current. Subtracting this from half the cycle time gives the time error t_1. A block diagram of this calculation can be seen in figure 6.3.2. The Counter 1 starts counting

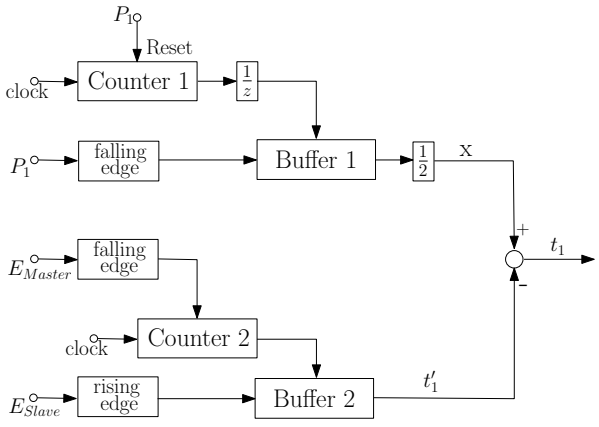


Figure 6.3.2 Calculating the time error t_1 for the synchronization

when the signal P_1 triggers the master current to change slope. At each falling edge of P_1, the counter value of the previous time point is saved in buffer 1, which is the cycle time. The output of the buffer is multiplied by $\frac{1}{2}$, so that x is half the cycle time. In the optimal case, the slave current should hit zero half way between two time points that the master current hits zero. The difference between the times that master and slave module go to zero in the optimal case is thus x.
The rising edge of the bridge voltage in the master circuit E_{Master} starts the counter 2.

Its value is saved in buffer 2 at the rising edge of the bridge voltage in the slave circuit E_{Slave}. Thus the buffer 2 saves the time difference t_1' between the master current and the actual slave current passing zero. This time difference subtracted from half the cycle time x gives the time error t_1.
The signals used to calculate t_1 have to change sign in case the reference current I_{ref} is negative.

Simulation of the Synchronization

The synchronization part is added to the discretized part of the Simulink model, which so far consists of the time-shifting model.
As described above, the time Δt is subtracted from the precalculated value of the time, that the signal P_5 should trigger the slave current to change slope. The equation (6.3.2) is implemented in Simulink as seen in figure 6.3.3.

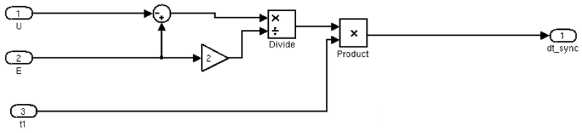


Figure 6.3.3 The Simulink model for equation (6.3.2)

The time error t_1 can be determined according to figure 6.3.2, as described above. The implementation in Simulink is shown in figure 6.3.4. The figure does not show how the sign of the input signals is changed when the reference signal is negative. This is done by multiplying every input signal by the sign of the reference current.

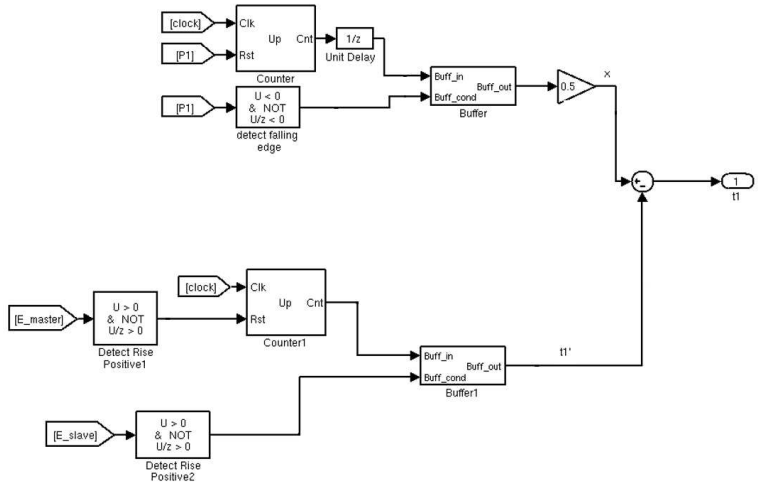


Figure 6.3.4 Calculating the time error t_1 according to figure 6.3.2

The output of the model in figure 6.3.4, which is the time error t_1, is the lowest input of the model in figure 6.3.3. The output of the model in this figure is the time Δt. The signal for Δt is an input to the time-shifting model in figure 6.2.3. It is subtracted from the calculated time for the time-shift, which is the output of the 0.5-block after the buffer.

In order to test the synchronization algorithm, the master and slave circuits are simulated without the voltage control loop.
The reference current is chosen to $I_{ref} = 1\,A$ and the voltage has been set constant to $U = -110\,V$ instead of internal feedback of the output voltage. The constant for the

hysteresis has been set to $\varepsilon = 0.001$.
The slave circuit is started arbitrarily at the time $5 \cdot 10^{-6}$ seconds. Simulating the current circuit including master and slave circuit in the unstable mode without synchronization leads to a non-synchronized behavior, as shown in figure 6.3.5. The start of the slave circuit at an arbitrary time point leads to the first time error t_1, which results in an error of the peak value of the current. This leads to further time and current errors in the slave current, which do not synchronize themselves.

When the synchronization is added as described above, the slave current gets synchronized as shown in figure 6.3.6. The peaks of the slave current are again half way between two peaks of the master current.

It should be noted, that the synchronization does not work well anymore, when the reference current is in the range of the hysteresis. But since the slave module is, as described later, only supposed to be used for bigger currents, only the master module is active when the reference current is close to zero. Therefore, synchronizing the slave current close to zero reference current in the range of the hysteresis constant can be neglected.

6.4 A Synchronization Algorithm Depending on Times

The algorithm for synchronizing the slave current to the current of the master circuit as described needs the bridge voltage E of the master current and the the output voltage U_{out} to be available. In this section, an algorithm is presented, that uses measured times instead of voltages.

The times for the rising and falling slope T_1 and T_2 are used as well as the time error t_1 to calculate Δt. With geometry, the following equations can be derived with the help of figure 6.4.1:

$$\frac{I_0 + \Delta I}{I_0} = \frac{T_2 + \Delta t}{T_2} \tag{6.4.1}$$

$$\frac{I_0 + \Delta I}{I_0} = \frac{T_1 - \Delta t + t_1}{T_1} \tag{6.4.2}$$

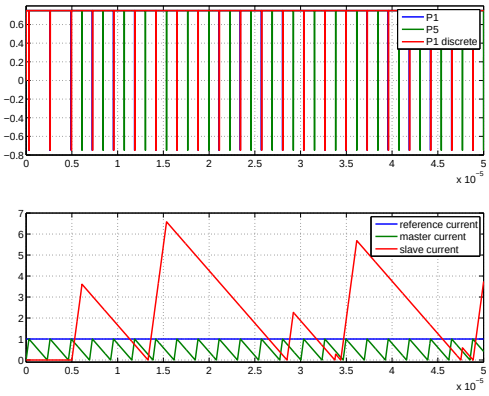


Figure 6.3.5 Switching Signals P_1 and P_5; reference current, master current and slave current **un**synchronized

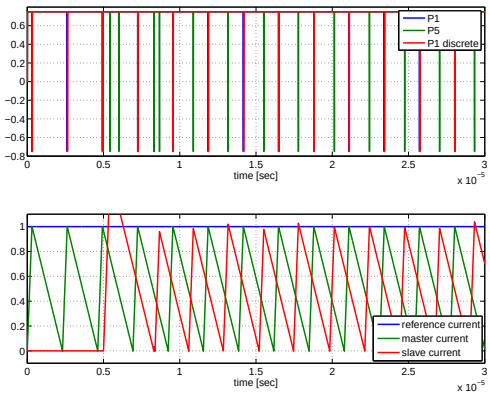


Figure 6.3.6 Switching Signals P_1 and P_5; reference current, master current and slave current synchronized

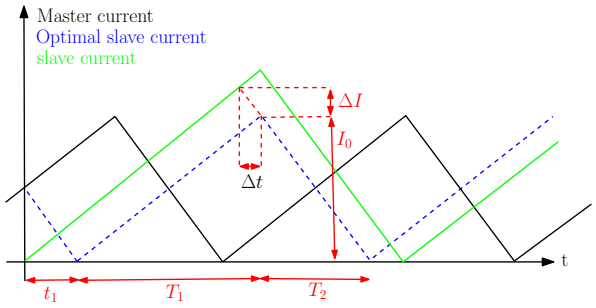


Figure 6.4.1 Alternative method to synchronize the slave current

They can be solved to:

$$\Delta t = t_1 \cdot \frac{T_2}{T_1 + T_2} \tag{6.4.3}$$

In the Simulink model, this is implemented as shown in figure 6.4.2. The times T_1, T_2 and t_1 are calculated by the simulation as before. The time Δt is added to the calculated time for the pulse P_5 as in section 6.3.

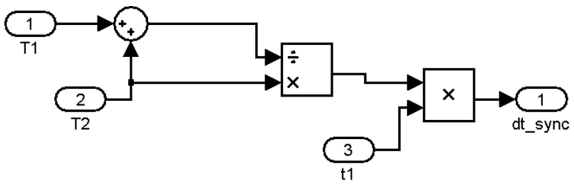


Figure 6.4.2 Alternative algorithm to synchronize the slave current.

The simulation results of this synchronization are the same as in section 6.3. For further simulations, this algorithm is preferred.

6.5 Activation of the slave circuit

This section describes, how the activation and deactivation of the slave module is done. Furthermore, a method to activate the slave module synchronized to the optimal case is implemented in the simulation.

Activation Depending on Frequency

In order to keep the switching frequency of the transistors in the sinus switch in a certain limit, the slave module should be activated when he frequency of the master current falls under 10 *kHz* and deactivated when the frequency rises over 20 *kHz*. For the purpose of simulations without internal feedback of the output voltage, the easier case that the slave module is activated when the frequency is under a certain value f_{act} and deactivated when it is over this value is considered first. To be able to implement this in the simulation, the frequency of the master current has to be determined. For this, the calculation of the time for one cycle of the master current, which is already implemented for the calculation of the time t_1 (see section 6.3), can be used. The cycle time is inverted and divided by $1 \cdot 10^3$ to get the frequency in *kHz*. This frequency is then used to determine if the slave circuit should be active. The realization of this in Simulink is shown in figure 6.5.1.

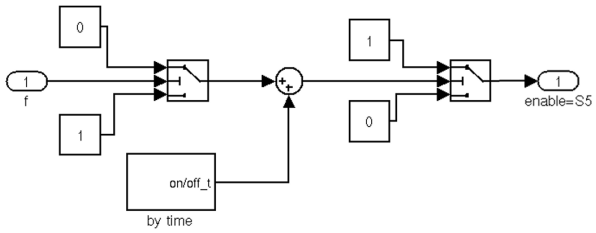


Figure 6.5.1 Part of the model that activates the slave circuit depending on the frequency of the master current

If the frequency of the master current is bigger than the activation frequency f_{act}, then the leftmost switch gives out $'0'$ and when the frequency is smaller than f_{act}, then the same switch gives out a $'1'$. An additional block gives out $'1'$ after a certain time has passed. Those two signals are added. If the frequency of the master current is smaller than f_{act} and the predetermined time has passed, the output of the addition is $'2'$. Only then should the slave circuit be activated. Therefore, another switch sets its output to $'1'$ if this addition is greater than 1.5 and to $'0'$ otherwise. So the output of this second switch is $'1'$, when a desired time has passed and the frequency of the master current has fallen under a certain value. This is the enable signal for the slave circuit.

This enable signal is then passed to the slave circuit. When it changes from zero to one, it resets the integrator modeling the inductance, so that the inductor current starts from zero. Furthermore, the enable signal enables the inductor current to be unequal to zero while it is $'1'$. When it falls back to zero, the slave current is set to $'0'$. The signal P_5 for the slave circuit is also calculated while the slave circuit is not running, so that it can be used for further calculations, for example for the synchronized switch-on of the slave circuit.

Synchronized Activation using P5

The idea of synchronized activation of the slave current [Jön05] is to start the slave module at that time point, that the optimal slave current would cross zero. The block model in figure 6.5.2 shows the method used.

A counter counts the time between two pulses P_5. This time is compared to the time T_2 of the master current (see figure 6.3.1). The comparator gives out a pulse, when the clock value is equal to the time T_2. By setting the comparator output to $'1'$ at the time T_2 after the the last pulse P_5, the slave module gets switched on or off when its current would optimally get zero. This is because the time T_2 is the

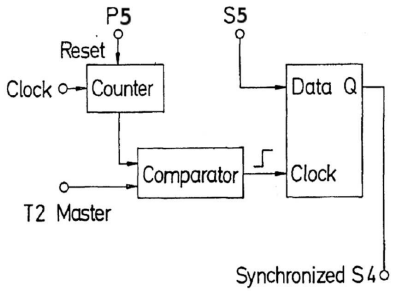


Figure 6.5.2 Synchronizing the start of the slave circuit, from [Jön05]

time the inductor current needs to fall from its peak value to zero. The output of the comparator is connected to the clock input of a D-Flip-Flop and the enable signal from the subsection 6.5 is connected to the data input. The output *Q* of the flip-flop is changing to one, when the enable signal as well as the synchronization signal is one. If the enable signal is zero, then the output of the flip-flop changes back to zero again when the synchronizing signal gets one. With this, the turn-on and turn-off of the slave circuit is synchronized to the synchronization signal.

The synchronized starting of the slave current is implemented in Simulink as seen in figure 6.5.3. The output signal seen in this figure is connected to the clock input of a D-flip-flop. The data input of that flip-flop is connected to the enable signal from figure 6.5.1. A D-flip-flop block is available in Simulink. The output of the flip-flop is the new enable signal for the slave module.

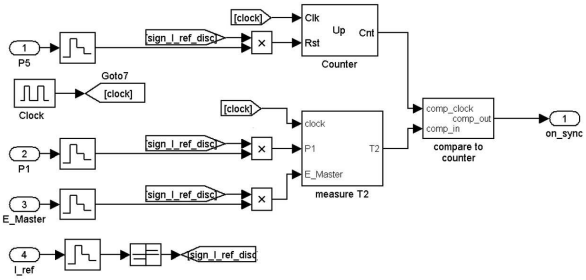


Figure 6.5.3 Synchronizing the start of the slave circuit, modeled in Simulink

The time T_2, which can be measured in the real circuit, can be calculated for the simulation from the pulse P_1 and the master circuit's bridge voltage, as shown in figure 6.5.4.

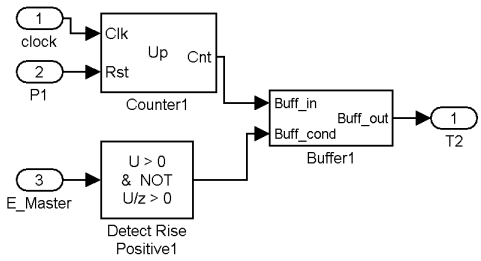


Figure 6.5.4 Calculating T_2

Due to, e.g. numerical errors because of the sampling and calculations errors, the pulses P_5 might not be at their optimal position. In this case, the calculated starting point of the slave current is not the optimal starting point either which leads to a time error in the slave current. Then, the described algorithm for synchronizing the time error of the slave current should minimize this error.

Synchronized Activation using P1

By using the pulse P_1 for calculating the synchronization pulse for the starting synchronization of the slave circuit, the problem with imprecise pulses P_5 can be avoided. The slave current should optimally cross zero in the middle of a cycle of the master current. This optimal point can be calculated to t_{act}:

$$t_{act} = T_2 + \frac{T_1 + T_2}{2} = \frac{1}{2}T_1 + \frac{3}{2}T_2$$

This is the optimal starting time for the slave current with respect to the last pulse of P_1. It can be seen in figure 6.5.5, that this optimal time is the time T_2 plus half the cycle time after the pulse P_1 occurs.

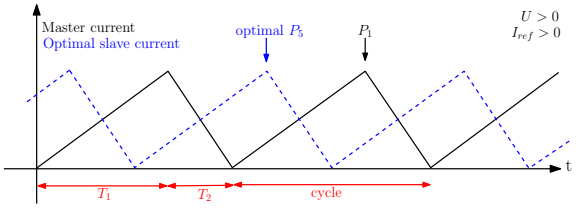


Figure 6.5.5 Synchronizing the start of the slave circuit, alternative model in Simulink

This activation is implemented in Simulink as shown in figure 6.5.6. The time T_2 is calculated like in figure 6.5.4. The time T_1 is calculated in a similar way by exchanging the signals P_1 and the master modules bridge voltage E_Master.

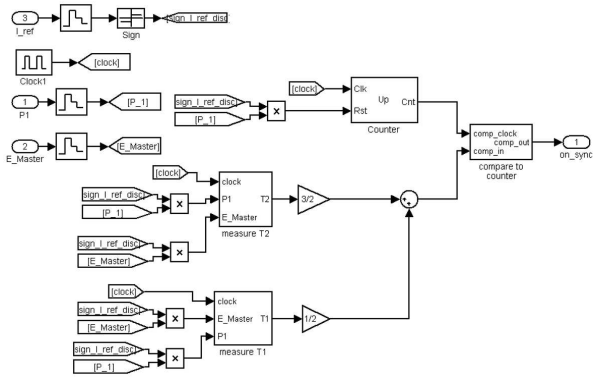


Figure 6.5.6 Synchronizing the start of the slave circuit, alternative model in Simulink

This algorithm for synchronized activation is allowing the slave module to only start synchronized with the optimal shape of the slave current.

6.6 Switching Between Master and Slave Module

According to [Jön05], the switching frequency of the modules should be between 10 *kHz* and 20 *kHz*. When the frequency of the master module's inductor current

drops under 10 *kHz*, the slave module is supposed to be activated. In closed-loop with a voltage controller, the reference current will drop in this case, since the output voltage is held at the reference value by the voltage controller. Consequently, the frequency rises to its double value 20 *kHz* and decrease as the reference current increases. When it decreases again, the slave is deactivated when the frequency of I_{Master} falls under 20 *kHz*.
Here, only the activation and deactivation of one slave module is observed. The cases when the frequency of the master current for activated slave falls under 10 *kHz* and when this frequency goes over 20 *kHz* for deactivated slave is neglected.

The Frequency of the Master Current

The frequency of the master current can be calculated dependent on the output voltage and the reference current of the switch circuit. Figure 6.6.1 shows a sketch for one cycle of the master current.

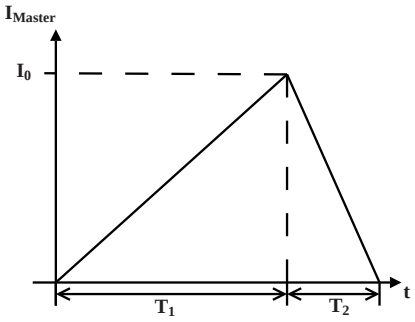


Figure 6.6.1 Sketch of one cycle of the master module's inductor current

In general, the voltage over the inductor of the master module is:

$$U_L(t) = L \cdot \frac{dI_L(t)}{dt}$$

The voltage $U_L(t)$ is the voltage over the inductor and the current $I_L(t)$ is flowing through the inductor.

For a constant voltage, the inductor current is rising linearly [KSW00]. The slope of the rising current can hence generally be expressed as the following:

$$\frac{dI_L}{dt} = \frac{U_L}{L}.$$

Comparing to figure 6.6.1, the rising slope of the inductor current can be expressed as:

$$\frac{I_0}{T_1} = \frac{E-U}{L}, \tag{6.6.1}$$

since the voltage over the inductor is the difference between the bridge voltage and the output voltage. The bridge voltage is positive when the slope is rising. For a falling slope, the bridge voltage is negative:

$$\begin{aligned} \frac{I_0}{T_2} &= -\frac{(-E-U)}{L} \\ &= \frac{(E+U)}{L}. \end{aligned} \tag{6.6.2}$$

By solving equations (6.6.1) and (6.6.2) for T_1 and T_2 respectively, the cycle time can be calculated:

$$\begin{aligned} T = T_1 + T_2 &= \frac{L}{E-U} \cdot I_0 + \frac{L}{E+U} \cdot I_0 \\ &= \frac{2E}{E^2 - U^2} \cdot LI_0. \end{aligned}$$

The frequency of the master current is the inverse of the cycle time T:

$$f_M = \frac{1}{T} = \frac{E}{2 \cdot L \cdot I_0} \cdot \left(1 - \left(\frac{U}{E}\right)^2\right) \tag{6.6.3}$$

Figure 6.6.2 shows the level curves for $f_M = 20\ kHz$ and $f_M = 10\ Hz$ dependent on the reference current and the output voltage of the sinus switch circuit. The level curves are plotted according to formula (6.6.3) with the same values for the parameters as for the simulation in section 6.7.

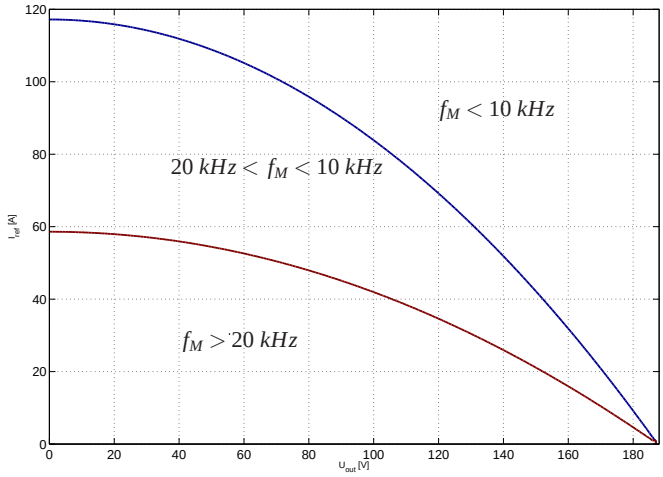


Figure 6.6.2 Level curves of the master current's frequency f_M for 10 and 20 kHz

The desired operation range for the frequency of the transistors is between the level curves in figure 6.6.2. Frequencies higher than 20 kHz are not examined in this thesis. Important is, that the slave module is activated when the frequency of the master current drops to 10 kHz, so that the switching frequency of the master and slave module stays in the range of 10 and 20 kHz.

6.7 Simulation of the model

In this section, the simulation results of the model so far are shown. This includes a master and slave current circuit, where the current of the slave circuit is shifted as described in the sections above. For the synchronization algorithm, the one from section 6.4, that uses times instead of voltages, is used. To start the slave circuit, the methods described in section 6.5 are used.

Current Circuit

First, only the sinus switch circuit is simulated without the voltage control loop. Figure 6.7.1 shows the results for a simulation using a constant voltage of 10 V for the master and slave circuit instead of internal feedback of the output voltage. The hys-

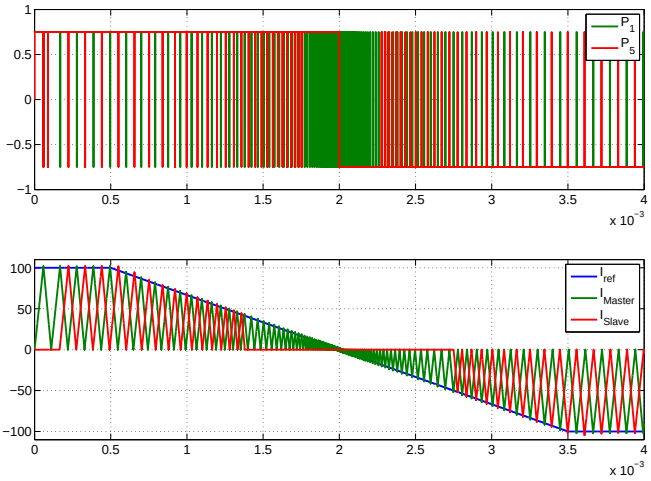


Figure 6.7.1 Switching signals; reference, master and slave current without internal voltage feedback

teresis constant is chosen to $\varepsilon = 0.001$ and the slave module is switched on, when the frequency of the master current drops under $f = 20\ kHz$. The reference current, as seen in figure 6.7.1, is a slope starting at 100 A and ending at $-100\ A$. The slave current gets time shifted to have its maximum half way between two maxima of the master current. For both negative and positive currents, the slave current gets synchronized correctly. It gets deactivated for lower reference currents, i.e. when the master currents frequency is higher than the preset 20 kHz.

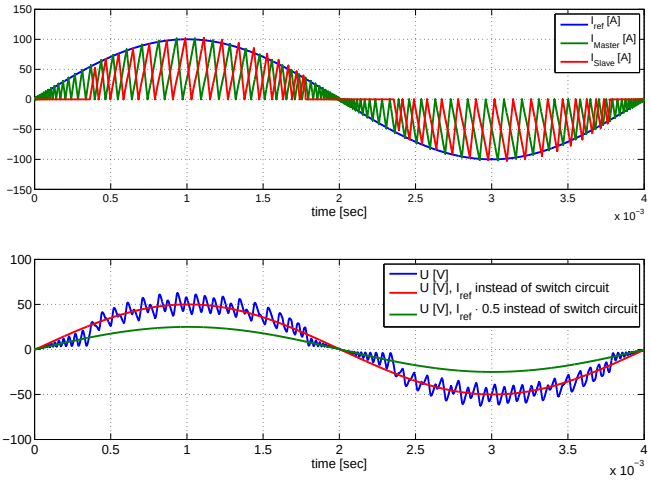


Figure 6.7.2 reference, master and slave current without internal voltage feedback and output voltage U_{out}

With internal feedback of the output voltage, the reference current has to be chosen differently. Master and slave module can only work correctly, when $U_{out} < V$.

Therefore, the reference current has to be chosen in such a way, that the output voltage does not go over the value $\pm V$ for the bridge voltage. For testing purposes, a sinusoidal signal is chosen as a reference current. Although in this thesis a DC-motor is used as a load, in general the switch circuit is supposed to work with AC induction motors, which have sinusoidal current and voltage. Hence, sinusoidal signals are tested in the simulation. A load helps further to keep the voltage from getting too high. Here, a resistor of 0.5Ω has been connected to the output of the switch circuit as a load. The results can be seen in figure 6.7.2. The hysteresis constant has again been chosen to $\varepsilon = 0.001$. The slave module is active when the master modules inductor current has a frequency lower than $f = 20kHz$.
As shown in figure 6.7.2, the slave current gets synchronized to the master current for both negative and positive currents. Around the zero crossing of the reference current, the frequency of the master current gets very high. To reduce this switching frequency, the hysteresis can be increased.
The output voltage U is shown in the lower part of figure 6.7.2. Together with the output voltage, two other voltage curves are plotted. The red curve is the voltage after the conductor, when the switch circuit is substituted by the constant 1. If the switch circuit is instead substituted by the constant $\frac{1}{2}$, the output of the capacitor results in a voltage shown by the green curve. With half the reference current, the amplitude of the voltage is only half as big as with the full reference current. It can be seen, that the output voltage U_{out} follows the lower curve as long as only the master module is active and the upper curve while the slave module is active. So activating the slave circuit results not only in reduced ripple, but also in doubled output effect.

The Voltage Loop Including the DC-motor

In this simulation, the sinus switch circuit is used together with the voltage control loop loop. The DC-motor from section 3 is used as a load. This simulation is done with a load of 100 Nm is connected to the motor during the first 0.01 seconds. After that, the motor load is set to zero. The frequencies ω_1 and ω_2 for the voltage controller are chosen to $\omega_1 = 1000$ and $\omega_2 = 3000$ (see section 5.2). The reference voltage is chosen to be sinusoidal with an amplitude of $50V$. It should be noted, that the parameters chosen for the simulation might not be realistic, but sufficient for the purpose of this simulation. Furthermore, sinusoidal curves are used for this simulation, since the sinus switch is supposed to work with AC motors.
For the switch circuit, the inductances of master and slave circuit are as is previous sections 80 μH, and the capacitor value has been set to 1.2 mF. The bridge voltage has been chosen to 187.5 V, so that a voltage of 150 V equals 80% of the bridge voltage.
Figure 6.7.3 shows the reference voltage U_{ref} and the output voltage U_{out} of the voltage loop in its first part. The second part of the picture shows the reference current I_{ref} set to the switch circuit by the voltage controller and the output current I_{out} of the switch circuit. The output current I_{out} is the addition of master and slave current. The inductor currents I_{Master} and I_{Slave} of the master and slave module are shown in the third part of the figure. When the slave module is inactive, its inductor current is shown as zero. The lowest part of figure 6.7.3 shows the frequency of the current I_{Master}.
At the start of the simulation, only the master module is active. As the reference current rises, the frequency of the master current I_{Master} decreases. When it reaches 10 kHz, the slave circuit gets activated. Since the voltage controller is holding the ouput voltage at the value given by the reference voltage, the referece current is decreased. This results in an increase of the master current's frequency. Once this frequency exceeds 20 kHz, the slave module is tuned off again, which results in a

increase of the reference current. While the slave module is active, the output current I_{out} does not go down to zero anymore. This is due to the fact, that the output current is the addition of the master and the time shifted slave current.
When the slave module is activated, there is a small error in the output voltage. This is due to the fact, that the voltage controller should not be very fast. With a faster voltage controller, the reference current would be decreased too much, so that the frequency of the master current rises over 20 kHz immediately. As a result, the slave circuit would switch itself off again. Then, the reference current would rise again to a value, where the frequency of the master current is lower than 10 kHz, where the slave module would get active again. This can cause oscillations of the output voltage. In worst case, the system can loose stability with a too fast voltage controller.

Figure 6.6.2 can be compared to this simulation. In the simulation shown in figure 6.7.3, the slave module gets switched on when the output voltage is approximately 50 V and the current reaches a bit over 100 A. In figure 6.6.2, the level curve for $f_M = 10\ kHz$ is for $U_{out} = 50\ V$ approximately at $I_{ref} = 110\ A$. In the simulation, the reference current falls down to approximately 60 A after activating the slave module. In figure 6.6.2, the level curve for $f_M = 20\ kHz$ is at $U_{out} = 50\ V$ slightly lower as $I_{ref} = 60\ A$.
The motor used for the simulations has a rated voltage of 150 V (see section 3). It is assumed that the rated operation of the motor is supposed to be at $0.8 \cdot E$. Then, the value of the bridge voltage is $V = 187.5\ V$. Comparing this to figure 6.6.2 it can be seen, that at $U_{out} = 150\ V$ the reference current for the switch circuit is between 20 and 40 A for $20\ kHz < f_M < 10\ kHz$.

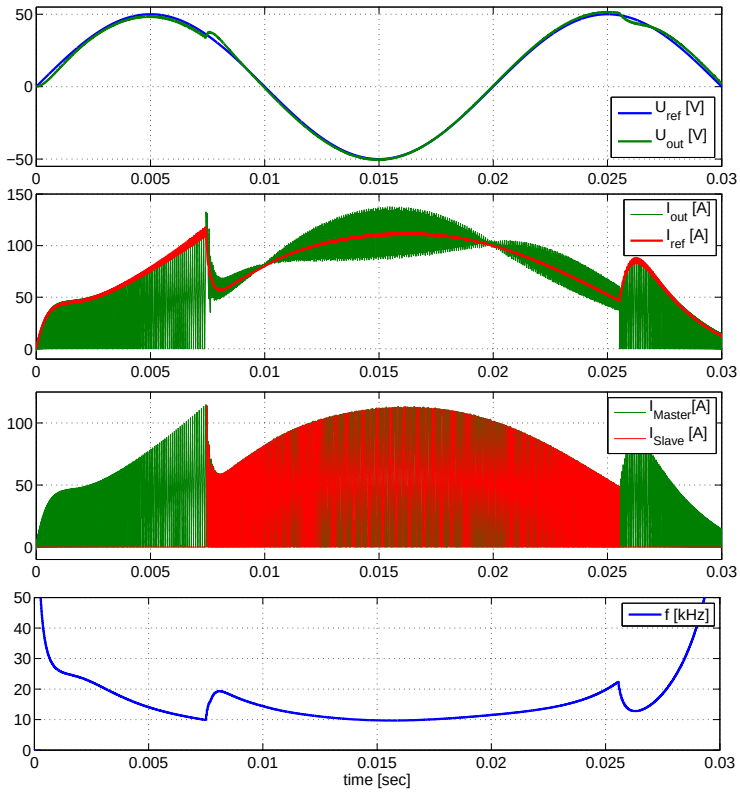


Figure 6.7.3 Voltages, currents and inductor frequency for simulation of the voltage controlled switch circuit with a dc motor as a load

In spite of the not realistic parameter assumptions, this simulation shows that the sinus switch with the synchronization works as desired. Between 0.01 and 0.02 seconds, the reference voltage is negative while the reference current is positive. This is the mode, where the slave current gets unstable without synchronization. With the used synchronization however, the slave current is stable, as seen in figure 6.7.3. Furthermore, this simulation shows that the slave module gets activated so that the frequency of the master current does not fall under 10 kHz and the slave module operated in the range between 10 and 20 kHz as desired.

6.8 Non-exact Synchronization

The synchronization algorithm as described in section 6.4 synchronizes the slave current immediately, i.e. a time error in the slave circuits inductor current is set to zero in one cycle of the inductor current. But because of e.g. numerical errors during the calculation of Δt it might happen, that the synchronization is done with a slightly different value. Also one might want that the synchronization is not done in one step and therefore synchronize the slave current with a value different from Δt. This and the difference of exact and non-exace synchronization at the presence of measurement noise is discussed in section 6.8.

In this section, the non-exact synchronization is described and its constraints are examined. Figure 6.8.1 shows an outline of the master current, the synchronized and unsynchronized slave current. The black, solid line is the master current. The blue, dashed line shows the slave current in the case of optimal synchronization. This is how the slave current should look like after synchronization. The green, solid line shows the unsynchronized slave current. As an example, the slave current starts t_1 to early compared to the case of optimal synchronization. For exact synchronization as in chapter 6.4, the slave current gets synchronized with Δt and follows the optimal case immediately. If non-exact synchronization is applied to the slave current, the synchronization is done with $\alpha \cdot \Delta t$ instead of Δt. In the case shown in figure 6.8.1, it is $0 < \alpha < 1$ in (a) and $\alpha > 1$ in (b). The synchronized current following from that is shown as a red, solid line. It reaches zero with a time error t_3 compared to the optimal case. This time error depends on the value of α. The error in the current peak between the optimal case and the case of non-exact synchronization is $\Delta I'$.

In oder to observe constraints for this non-exact synchronization, an expression for t_3 dependent on T_1, T_2, t_1 and α is developed. It is observed, for which cases the non-exact synchronization is stable. It is stable, if the time error t_3 goes to zero.

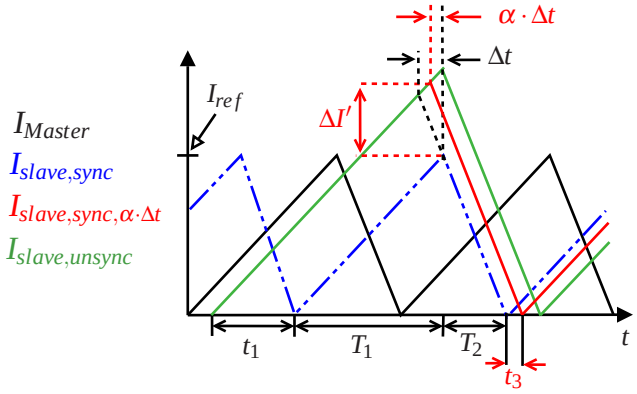
From figure 6.8.1 it can be calculated with geometry that:

$$\frac{I_0 + \Delta I'}{I_0} = \frac{t_3 + T_2 + \alpha \cdot \Delta t}{T_2} = \frac{t_1 + T_1 - \alpha \Delta t}{T_1}.$$

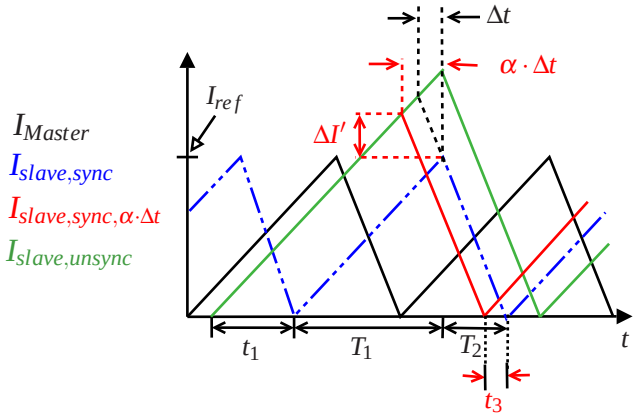
Combined with equation (6.4.3), this results in:

$$t_3 = (1 - \alpha) \cdot \frac{T_1}{T_2} \cdot t_1. \tag{6.8.1}$$

With the help of this equation, the stability of the synchronization is observed for different cases of T_1, T_2 and α. In section B, the detailed calculations are shown. In table 6.8.1 , a Summary of the results is presented. The table shows the dependence of the stability of the non-exact synchronization for a specific α on the rise- and fall times T_1 and T_2 of the inductor current. Figure 6.8.2 shows the curve for $\frac{T_2}{T_1} = \frac{1}{|1-\alpha|}$



(a) $0 < \alpha < 1$



(b) $\alpha > 1$

Figure 6.8.1 master current, optimal slave current, slave current for non-exact synchronization, unsynchronized slave current

		$0 < \alpha < 1$	$1 < \alpha < 2$	$\alpha > 2$
$T_2 < T_1$	$T_2 < \frac{1}{\lvert 1-\alpha \rvert} T_1$	stable	stable	stable
	$\frac{1}{\lvert 1-\alpha \rvert} T_1 < T_2 < T_1$			unstable
$T_2 = T_1$		stable	stable	unstable
$T_2 > T_1$	$\frac{1}{\lvert 1-\alpha \rvert} T_1 < T_2 < T_1$	stable	stable	unstable
	$T_2 > \frac{1}{\lvert 1-\alpha \rvert} T_1$	unstable	unstable	

Table 6.8.1 Stability of non-exact synchronization depending on T_1, T_2 and α

over α. Comparing with table 6.8.1, it can be seen that the area where the non-exact synchronization is stable is the area under the curve. For combinations of T_1 and T_2 that lie above the curve for a specific α, the non-exact synchronization is unstable. The red, constant line in figure 6.8.2 shows $\frac{T_2}{T_1} = 1$ to make it easier to compare with table 6.8.1.

Since the slopes of the inductor current changes with the voltage U, the times T_1 and T_2 also do. Therefore, the condition for the synchronization to get unstable in the case of $0 < \alpha < 2$ can be recalculated in a condition for the voltage U (for details see

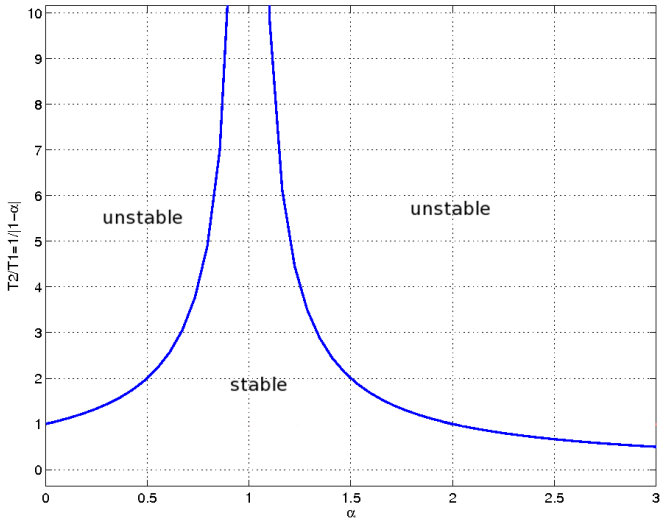


Figure 6.8.2 Stability of non-exact synchronization depending on the rise- and fall times T_1 and T_2 of the inductor current

section B):

$$\frac{U}{E} < \frac{|1-\alpha|-1}{|1-\alpha|+1} \tag{6.8.2}$$

The right hand side of equation 6.8.2 is drawn over alpha in figure 6.8.3. Since equation 6.8.2 states for which voltages U the non-exact synchronization is unstable, the areas under the curve in figure 6.8.3 correspond to the unstable case. The area over the curve is, in contrast, the area for which non-exact synchronization is stable.

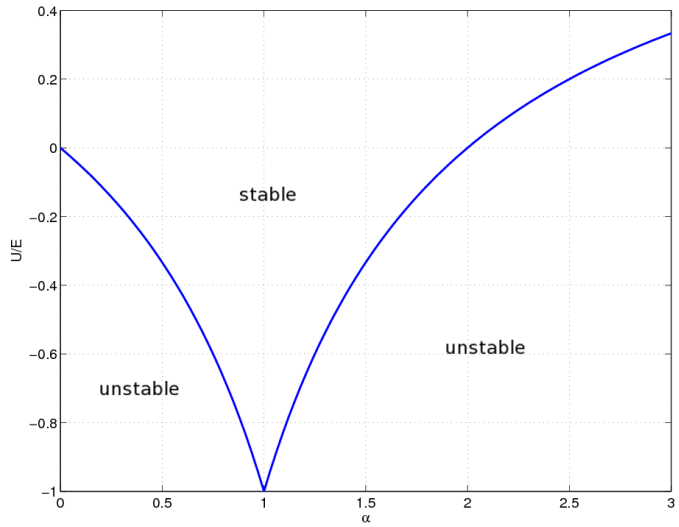


Figure 6.8.3 Stability of non-exact synchronization depending on the voltage U

For $\alpha = 0$, the non-exact synchronization is unstable for $\frac{U}{E} < 0$, which corresponds to the unsynchronized case when the slave current is unstable for all fed back output voltages smaller than zero. When $\alpha = 1$, the slave current is stable for all

voltages $-U$ until the value of the bridge voltage E. This is the case of exact synchronization. For all other values of α, the current gets unstable for voltages between 0 and $-E$, depending on the value of α. With non-exact synchronization, the range of stable operation is reduced compared to the case of exact synchronization, as can be seen in figure 6.8.3.

Effect of Measurement Noise

With the help of a simulation, the effect of noisy measurements on the times T_1, T_2 and t_1 is investigated. Also, it is testet if it is possible to improve the synchronization at the presence of noise by using $\alpha \cdot \Delta t$ instead of Δt to synchronize the slave current.

One possible source of measurement noise could be because of an A/D-converter that is assumed to be used in practic to convert the measured times T_1, T_2 and t_1 into discrete signals. In the simulation, the time is sampled, but the signal values are not quantized. But in practice, an A/D-converter quantizes the signal values additional to sampling the time, which leads to a quantization error depending on the resolution of the A/D-converter. The quantization error of an A/D-converter is 1 LSB. Assuming a resolution of 8bit leads to $1\ LSB = \frac{1}{256} = 0.0039$. This is approximately an error of 0.4 % of the total operation range of the A/D-converter. To account for other unknown noise factors, the simulation is done with approximately 1 % of the total operation rance of the A/D-converter.
The maximum operation range of the assumed A/D-converter would in practice be the maximum value of the signal to be converted. In this case, the maximum values for T_1 and T_2 should determine the maximum operation range. The maximum value, that both T_1 and T_2 can theoretically take is the value of the cycle time $T = T_1 + T_2$. This is when either the up- or the downslope of the slave current takes the whole cycle time T and the respective other slope takes place in zero seconds (compage e.g. to figure 6.8.1). The cycle time, though, is dependent on the the reference current and the voltage U, which is supposed to be the output voltage of the system. The up- and downslope of the the synchronized slave current can be expressed in the following way:

$$\frac{I_{ref}}{T_1} = \frac{E-U}{L} \text{ and } \frac{I_{ref}}{T_2} = \frac{E+U}{L}.$$

From that, the cycle time $T = T_1 + T_2$ can be calculated to:

$$T = I_{ref} \cdot L \cdot \frac{2E}{E^2 - U^2}.$$

From the last equation, it can be seen, that the cycle time T rises when the reference current I_{ref} rises and when the voltage U approaches the value E of the bridge voltage. According to the formula, the cycle time would get ifinitively big when $U = E$. But to determine the maximum operation range of the A/D-converter, a finite upper bound for T is necessary. If assuming, that not more than 99 % of the whole range for U from zero to E are used, the maximum value for the voltage can be set to $U = 0.99 \cdot E$. For the reference current $I_{ref} = 10\ A$ is assumed. The frequency of the inductor current would then be $f = \frac{1}{T} = 2.3\ kHz$, which is alot under the supposed minimum of $10\ kHz$ for the inductor current. The cycle time is then $T = 4.28 \cdot 10^{-4}$ seconds. As stated above, 1% of this assumed maximum value for the cycle time is taken as an indication for the amplitude of the measurement noise, which is $T_{1\%} = 4.28 \cdot 10^{-6}$.

Figure 6.8.4 shows the synchronization time Δt corrupted by noise. This is because in the simulation, white noise with zero mean and a variance of 500 samples are added to the calculeted times T_1, T_2 and t_1. This leads approximately to an amplitude of $6 \cdot 10^{-6}$ seconds of the noise on T_1, T_2 and t_1. As seen in figure 6.8.4, this

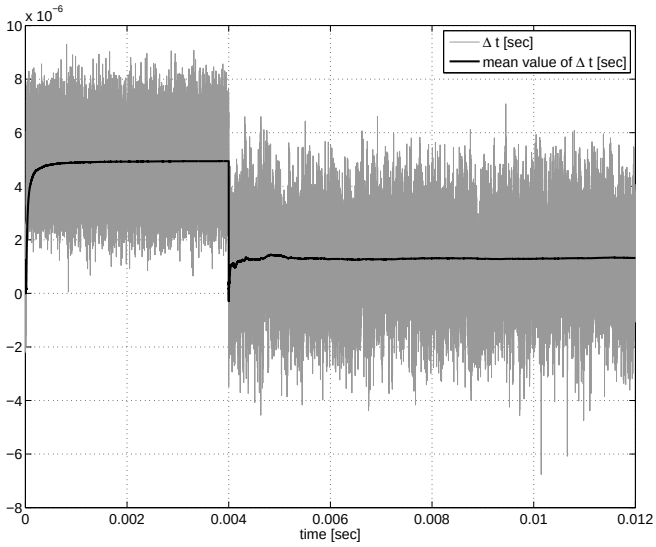


Figure 6.8.4 reference current, master current and slave current with exact and non-exact synchronization.

results in noise with an amplitude of approximately $3 \cdot 10^{-6}$ around the synchronization time Δt. That this is a little more than the calculated value does not matter for the purpose here. The purpose of this section is to investigate if in general the slave current gets less effected by measurement noise when using $\alpha \cdot \Delta t$ instead of Δt for the synchronization. Therefore, the exact value of the noise is unimportant here.

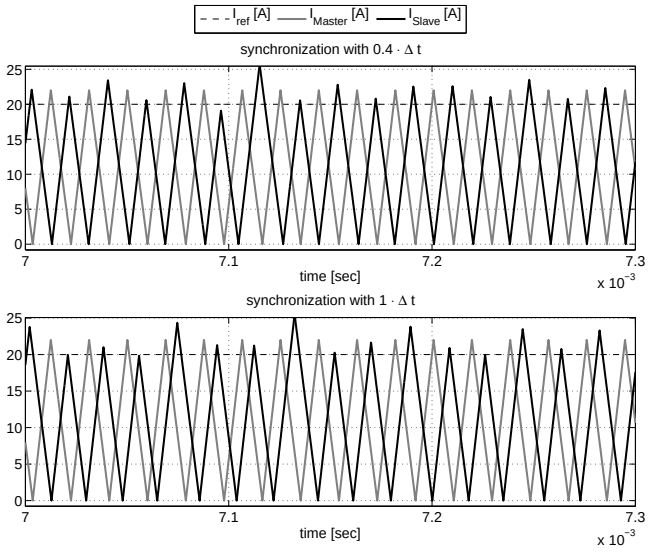


Figure 6.8.5 reference current, master current and slave current with exact and non-exact synchronization.

Figure 6.8.5 shows the results for this simulations. The upper part shows the master and slave current with non-exact synchronization $0.4\Delta t$ and the lower part with exact synchronization. As seen in the lower part of figure 6.8.5, the synchronization of the slave current can get effected by corrupted time measurements. The peaks of

the slave currents are no longer synchronized to the middle between two peaks of the master current, but rather shifted away slightly from the middle. Additionally, the peaks of the slave current dont reach the reference value exacty.
As can be seen comparing the upper part of figure 6.8.5 with the lower part, the pattern of the currents looks more regular in the upper part. The peaks of the slave current are still not exactly at the reference current plus hysteresis, but they are synchronized to the middle between two peaks of the master current.
According to this simulation, there is a possibility improving the synchronization of the slave current at the presence of measurement noise. However, further investigation of this is necessary to make a general statement.

Even if non-exact synchronization improves the synchronization when measurement noise is present, it remains the drawback stated earlier in this section. The more the factor α differs from 1, the less of the range $0 < U < E$ can be used to maintain a stable synchronization.

6.9 Effect of Inaccurate Inductances

For all simulations in the previous section it was assumed, that the inductances for the master and slave modules are exactly the same. However, this is not necessarily the case. The inductances can differ with $\pm 5\%$. In this section, the effect of non-equal inductances is analized both in theory and in simulation.

Effect on Slave Current

For analysis, it is assumed, that the inductance of the master module is slightly bigger than the inductance of the salve circuit, so that $L_M > L_S$. The slope of the inductance current is inversely proportional to the inductance. Therefore, the slope of the slave current is bigger than the slope of the master current in the case of $L_M > L_S$. Figure 6.9.1 outlines the effect.

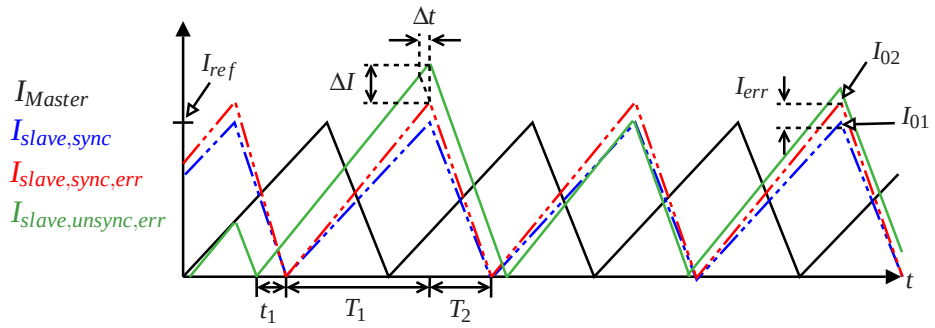


Figure 6.9.1 master current, optimal slave current, optimal slave current with $L_M > L_S$, unsynchronized slave current with $L_M > L_S$

The black solid line shows the master current. The blue, dashed line shows the slave current when it is synchronized and the inductances are $L_M = L_S$. This is used as a reference to the case with unequal inductances. The synchronized slave current with $L_M > L_S$ is shown with a dashed, red line. Without changing the switching signal P_5 for the slave module, the maximum slave current is higher in this case with unequal inductances. The unsynchronized case $L_M > L_S$ is shown with a solid, green line. Exact synchronization is used here. The synchronization algorithm is adjusting the time for the falling edge of the signal P_5 to synchronize the slave current. Therefore,

the slave current gets synchronized to the red, dashed line in figure 6.9.1. When the slave current is synchronized, the times t_1, T_1 and T_2 are the same as for the case with equal inductances, but the amplitude of the triangular inductor current is slightly higher.

The rising and falling slope of the slave current, when both inductances are equal $L_M = L_S$, are:

$$\frac{I_{01}}{T_1} = \frac{E-U}{L_M} \text{ and } \frac{I_{01}}{T_2} = \frac{E+U}{L_M}.$$

Since $L_M = L_S$, the master module's inductance is used .
For the case of unequal inductances with $L_M > L_S$, the rising and falling slope of the slave current is now dependent on L_S:

$$\frac{I_{02}}{T_1} = \frac{E-U}{L_S} \text{ and } \frac{I_{02}}{T_2} = \frac{E+U}{L_S}.$$

From this, the error between the peaks of the slave current with equal and unequal inductances can be calculated for the synchronized case:

$$\begin{aligned} I_{err} = I_{02} - I_{01} &= \frac{E-U}{L_S} \cdot T_1 - \frac{E-U}{L_M} \cdot T_1 \\ &= \frac{E-U}{L_M} \cdot T_1 \cdot \left(\frac{L_M - L_S}{L_S} \right) \\ &= I_{01} \cdot \left(\frac{L_M - L_S}{L_S} \right). \end{aligned}$$

It can be assumed, that the the maximum value of the synchronized slave current for equal inductances I_{01} is equal to the reference current I_{ref} plus hysteresis. The relative error of the inductance L_M to the inductance L_S is then equal to the the relative error of the slave current's peak value with $L_M = L_S$ to the peak value with $L_M > L_S$:

$$\delta I_0 = \frac{I_{err}}{I_{ref}} = \frac{I_{02} - I_{ref}}{I_{ref}} = \frac{L_M - L_S}{L_S}. \tag{6.9.1}$$

The relative error of the inductances that can occur is assumed to be $\pm 5\%$. According to equation (6.9.1), the maximum error δI_0 for the slave current's peak value is also $\pm 5\%$ for synchronized slave current.

The relative error of the slave currents peak value is also determined by simulation. For that, the sinus switch circuit is simulated with a constant reference current of $I_{ref} = 50\ A$ and a hysteresis constant of $\varepsilon = 2$. The output voltage is not fed back to the input. Instead, a constant voltage of $U = 110\ V$ is used for the master and slave module. No load is connected to the output of the switch circuit. The simulation is run one time with equal inductances and another time with unequal inductances. In both simulations, the inductance $L_M = 80 \cdot 10^{-6}$ of the master module is held constant. The inductance for the slave module is $L_S = L_M = 80 \cdot 10^{-6}$ in the first simulation and $L_S = L_M + 0.05 L_M = 84 \cdot 10^{-6}$ in the second simulation. The inductor current of the slave module for both simulations is compared. Figure 6.9.2 shows in its upper part the reference current plus hysteresis, the slave current for $L_S = L_M$ and the slave current for $L_S > L_M$. It can be seen, that the slave current does not reach the reference current in the second case of unequal inductances. There is an error in the peak value of the slave current in those two cases. This error is shown in the lower part of figure 6.9.2. For each peak value of the slave current, the difference between the unequal and the equal case is calculated and divided by the equal case, as in equation (6.9.1).

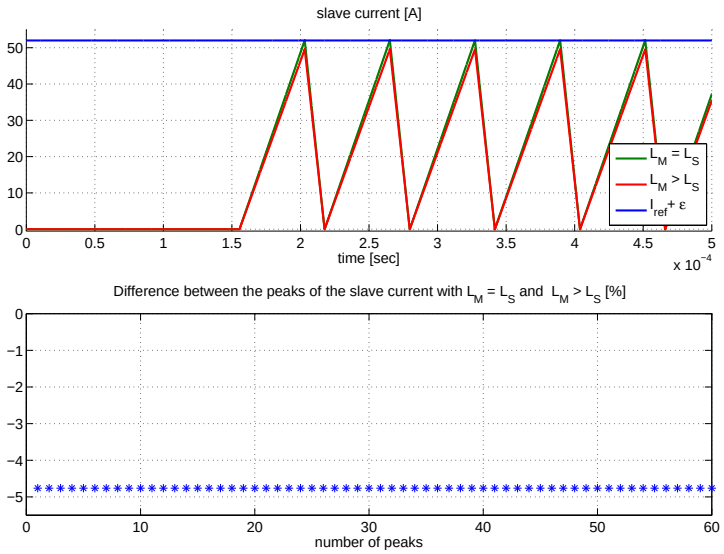


Figure 6.9.2 Error in the peak value of the slave current between $L_S = L_M$ and $L_S > L_M$

This result is then multiplied by 100 to gain the percentage error of the slave circuit for unequal master and slave inductances.

It can be seen, that the error is slightly over -5%. The inductances used in the second simulations are $L_M = 80 \cdot 10^{-6}$ and $L_S = L_M + 0.05L_M = 84 \cdot 10^{-6}$, where as L_M is held constant in both simulation. If L_S was held constant and L_M had been changed, it would have been hard to compare the two simulations because the slope of the master current would have changed. This would have caused the cycle time of the master current to change. By keeping L_M constant, it is possible to keep the time for a switch cycle of the master current constant in both simulations. Calculating the relative error of the inductances as in equation (6.9.1) with the inductances as used in the simulation gives:

$$\frac{L_M - L_S}{L_S} = -0.00476.$$

This means that the simulation result coincide with equation (6.9.1). Hence, the maximum error for the slave current with unequal inductances in master and slave module is the same as the error of the inductances for a synchronized slave current.

So far, the switch circuit was simulated in this section with a constant voltage on master and slave module. Now, internal feedback of the output voltage U_{out} is introduced. When the output voltage is fed back into the master and slave module, the slope of the slave current for the cases $L_S = L_M$ and $L_S \neq L_M$ is

$$\frac{I_{01}}{T_1} = \frac{E - U_{out}}{L_M} \quad \text{and} \quad \frac{I_{02}}{T_1} = \frac{E - \hat{U}_{out}}{L_S},$$

where U_{out} is the output voltage when the inductances are equal and $\hat{U}_{out}$ is the output voltage when the inductances are unequal. With this, the relative error of the peaks of the slave current becomes:

$$\delta I_0 = \frac{I_{02} - I_{01}}{I_{01}} = \frac{L_M\left(E - \hat{U}_{out}\right) - L_S\left(E - U_{out}\right)}{L_S\left(E - U_{out}\right)}.$$

Because of the voltage control loop, U_{out} and $\hat{U}_{out}$ can be set equal. Hence, also in the case of internal feedback of the output voltage, the error δI_0 is as in equation (6.9.1). So for unequal inductances in master and slave module, the error of the inductor current is depending on the error between the inductances, if assumed that the output voltage is controlled by the voltage control loop. This is sufficient for the supposed application of the switch circuit.

7. Summary

In this thesis, first the basic sinus switch accorning to [Jön88] has been simulated. The simulation model developed showed the expexted behaviour. Also, a hysteresis has been implemented in the simulation, which sucessfully limits the frequency of the master module's inductor current to a specifiy value. Thereafter, a module similar to the first one has been connected in parallel and a phase shift between the triangular inductor currents has been implemented. Again, the desired behaviour could be shown in simulations. The simulations could also show, that the ripple in the output voltage was reduced and the switching frequency of the transistors is reduced using two parallel modules. Furthermore, the simulations showed that the slave module's inductor current is unstable for certain operating points. A synchronizations algorithm based on the ideas in [Jön05] was implemented in the simulation to solve the problem. It could be seen in the simulations, that with this synchronization, the inductor current of the slave module is behaving stable. An alternative synchronization algorithm was developed, which has the advantage to be based on measured times rather than voltages. This was as well tested to be sucessful in simulations. With the synchronization, the time error resulting from the unsynchronized current gets to zero immediately. Because of e.g. numerical errors the synchronization might not be exact. An anlysis was therefore done to find out about the stablility of the synchronization in case of such a non-exact synchronization. It could be shown, that in this case the stability range regarding the output voltage is decreased. When the size of the deviation from the exact synchhronization increases, the region of output voltages to which the stability is restricted decreases. It was also tested with the help of a simulation, if using non-exact synchonization instead of exact synchonization can help to improve the performance of the synchronization in the present of measurement noise on the measured times. The simulation performed indicated, that there might be a possibility to improve the synchonization for this case. However, further investigations are needed to make a clear statement. Furthermore, an analysis was done concerning the effect of unequal inductances in master and slave module. It could be shown that, under the assumption that the voltage control loop control the output voltage accurately, the error between the inductor currents of master and slave module is limited, depending on the error between the inductances.

8. Conclusion

The first purpose of this thesis was to simulate the sinus switch circuit with two modules in parallel. The expected behaviour could be verified.

The second part was to test and eventually modify and algorithm synchronizing both parallel modules. The simulations showed, that the algorithm is functioning. It could be modified to be depending on measured times rather than voltages. In accuracies in the synchronization algorithm could be shown to limit the stable operation range of the sinus switch.

Furthermore, it could be shown in this thesis that in case of parameterinaccuracies in the inductances of both modules, the current error is limited by the error of the inductances.

9. Prospects

In this thesis, a DC-motor was used as a load to the sinus switch. Since the intention of the sinus switch is to be included in a frequency inverter controlling AC induction motors, the simulations should be done with such a motor as a load to see the behaviour. It is, however, expected that the behaviour is not changing significantly. Furthermore, the voltage controller used in this thesis is not optimal. An optimized controller could improve the performance of the sinus switch. Moreover, the extension of the simulation model to more than two modules in parallel could be useful to investigate the behaviour. A hysteresis, which is not constant but leads to a maximum switching frequency of 20 kHz, is under development. This is important, since the transistors used have a limited range of switching frequency and the slave circuit only takes care about the lower bound. Finally, implementation of the synchronization algorithm into a real system is necessary. This should be compared to the results from the simulations. Also, the effect of non-exact synchonization in the real system compared to the analysis done in this thesis could be interesting to analyze.

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A. Equivalence Circuit for the LC Circuit

This section describes, why the inductances and capacitors at the output of the transistor half-bridge can be modeled as an LC-circuit as shown in figure 2.3.1.

During ideal operation of the switch circuit, either the upper transistor is open and the lower one closed, or the other way around.

Figure A.0.1 shows the case when the upper transistor is turned on and the lower one is turned off. Then, the current flows from $+V$ to the inductor L. Figure A.0.1 also shows how the circuit at the output of the transistor half-bridge can be re-drawn to make calculations easier. The right-hand side is used to make the calculations.

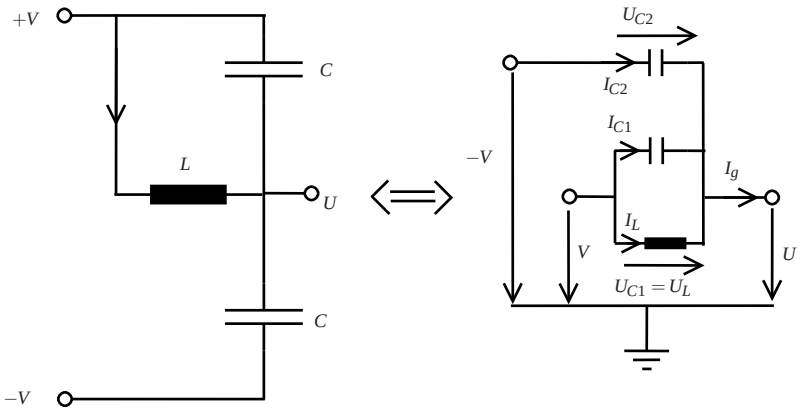

Figure A.0.1 Equivalent circuit of the Sinus Switch for $E = +V$

The total current I_g is the sum of the currents through the conductors and the current through the inductor:

$$I_g = I_{C1} + I_{C2} + I_L.$$

Those currents can be calculated to:

$$\begin{aligned} I_{C1} &= j\omega C \cdot U_{C1} \\ &= j\omega C \cdot (V - U) \\ I_{C2} &= j\omega C \cdot U_{C2} \\ &= j\omega C \cdot (-V - U) \\ I_L &= \frac{1}{j\omega L} \cdot U_L \\ &= \frac{1}{j\omega L} \cdot (V - U) \end{aligned}$$

With that, the total current I_g gets:

$$I_g = \frac{1}{j\omega L} \cdot V - \left(\frac{1}{j\omega L} + j\omega 2C \right) \cdot U.$$

With no load at the output of the circuit, the total current is $I_g = 0$. Then, the equation above becomes:

$$\begin{aligned} \frac{1}{j\omega L} \cdot V &= \left(\frac{1}{j\omega L} + j\omega 2C \right) \cdot U \\ \Leftrightarrow U &= \frac{\frac{1}{j\omega L}}{\frac{1}{j\omega L} + j\omega 2C} \cdot V \\ &= \frac{\frac{1}{j\omega 2C}}{j\omega L + \frac{1}{j\omega 2C}} \cdot V \end{aligned}$$

This is the transfer function from E to U of the LC circuit in figure 2.3.1 with $E = V$.

For the case that the upper transistor of the transistor half bridge is open and the lower one is closed, the current flows from $-V$ to the output, as shown in figure A.0.2. Again, calculations are done with the help of the right hand side of figure A.0.2.

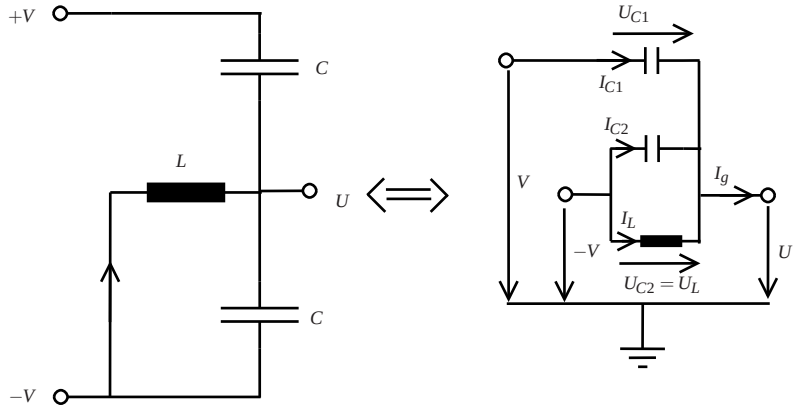

Figure A.0.2 Equivalent circuit of the Sinus Switch for $E = -V$

Similarly, the total current I_g is:

$$\begin{aligned} I_g &= j\omega C \cdot (V - U) + j\omega C \cdot (-V - U) + \frac{1}{j\omega L} \cdot (-V - U) \\ &= -\frac{1}{j\omega L} \cdot V - \left(j\omega 2C + \frac{1}{j\omega L} \right) \cdot U \end{aligned}$$

With no load at the output, the total current is $I_g = 0$. The transfer function from V to U is then:

$$U = \frac{\frac{1}{j\omega 2C}}{j\omega L + \frac{1}{j\omega 2C}} \cdot (-V) \,.$$

The transfer function of the LC-circuit in figure 2.3.1 with $E = -V$ gives the same result.

Thus, the circuit at the output of the transistor half bridge can be represented as an LC-circuit when changing the bridge voltage E between $+V$ and $-V$ accordingly.

B. Calculations for Non-exact synchronization

For the case of non-exact synchronization of the slave current as described in section 6.8, the calculations leading to table 6.8.1 are given.

- $0 < \alpha < 1 \Leftrightarrow 0 < 1-\alpha < 1$:
  - $T_1 = T_2$:
    $t_3 = (1-\alpha)\cdot t_1 \Rightarrow$ stable, since $0 < 1-\alpha < 1$
  - $T_2 < T_1$:
    $\frac{T_2}{T_1} < 1 \Rightarrow (1-\alpha)\frac{T_2}{T_1} < (1-\alpha) < 1 \Rightarrow t_3 = (1-\alpha)\frac{T_2}{T_1}\cdot t_1 < t_1 \Rightarrow$ stable
  - $T_1 < T_2 < \frac{1}{1-\alpha}T_1$:
    $1 < \frac{T_2}{T_1} < \frac{1}{1-\alpha} \Rightarrow (1-\alpha) < (1-\alpha)\frac{T_2}{T_1} < 1 \Rightarrow (1-\alpha)t_1 < t_3 < t_1 \Rightarrow$ stable
  - $T_2 > \frac{1}{1-\alpha}T_1$:
    $\frac{T_2}{T_1} > \frac{1}{1-\alpha} \Rightarrow (1-\alpha)\frac{T_2}{T_1} > 1 \Rightarrow t_1(1-\alpha)\frac{T_2}{T_1} > t_1 \Rightarrow t_3 > t_1 \Rightarrow$ unstable
- $1 < \alpha < 2 \Leftrightarrow 0 < |1-\alpha| < 1$:
  - $T_1 = T_2$:
    $t_3 = (1-\alpha)\cdot t_1 \Rightarrow |t_3| = |1-\alpha|\cdot|t_1| \Rightarrow$ stable, since $0 < 1-\alpha < 1$
  - $T_2 < T_1$:
    $\frac{T_2}{T_1} < 1 \Rightarrow (1-\alpha)\frac{T_2}{T_1} < (1-\alpha) \Rightarrow |t_3| < |1-\alpha||t_1| < |t_1| \Rightarrow$ stable
  - $T_1 < T_2 < \frac{1}{|1-\alpha|}T_1$:
    $1 < \frac{T_2}{T_1} < \frac{1}{|1-\alpha|} \Rightarrow |1-\alpha| < |1-\alpha|\frac{T_2}{T_1} < 1 \Rightarrow |1-\alpha||t_1| < |t_3| < |t_1| \Rightarrow$ stable
  - $T_2 > \frac{1}{|1-\alpha|}T_1$:
    $\frac{T_2}{T_1} > \frac{1}{|1-\alpha|} \Rightarrow |1-\alpha|\frac{T_2}{T_1} > 1 \Rightarrow |t_3| > |t_1| \Rightarrow$ unstable
- $\alpha > 2 \Leftrightarrow |1-\alpha| > 1$:
  - $T_1 = T_2$:
    $t_3 = (1-\alpha)\cdot t_1 \Rightarrow |t_3| = |1-\alpha|\cdot|t_1| \Rightarrow$ unstable, since $|1-\alpha| > 1$
  - $T_2 < \frac{1}{|1-\alpha|}T_1$:
    $\frac{T_2}{T_1} < \frac{1}{|1-\alpha|} \Rightarrow |1-\alpha|\frac{T_2}{T_1} < 1 \Rightarrow |t_3| < |t_1| \Rightarrow$ stable
  - $\frac{1}{|1-\alpha|}T_1 < T_2 < T_1$:
    $\frac{1}{|1-\alpha|} < \frac{T_2}{T_1} < 1 \Rightarrow 1 < |1-\alpha|\frac{T_2}{T_1} < |1-\alpha| \Rightarrow |t_1| < |t_3| < |t_1||1-\alpha| \Rightarrow$ unstable

– $T_2 > T_1$:
  $\frac{T_2}{T_1} > 1 \Rightarrow |t_3| > |1-\alpha||t_1| \Rightarrow$ unstable

Now the calculations leading to equation (6.8.2) are given. The down- adn up-slople of the slave current are:

$$\frac{I_{ref}}{T_1} = \frac{E-U}{L} \text{ and } \frac{I_{ref}}{T_2} = \frac{E+U}{L}$$

Those two equations together lead to:

$$T_2 = \frac{E-U}{E+U} T_1.$$

Now, the case from the calculations above when $T_2 > \frac{1}{|1-\alpha|} T_1$ is considered and combined with the last equation. This results in:

$$\begin{aligned} \frac{E-U}{E+U} T_1 &> \frac{1}{|1-\alpha|} T_1 \\ \Leftrightarrow \frac{E-U}{E+U} &> \frac{1}{|1-\alpha|} \\ \Leftrightarrow E\left(|1-\alpha|-1\right) &> U\left(|1-\alpha|+1\right) \\ \Leftrightarrow U &< \frac{|1-\alpha|-1}{|1-\alpha|+1} \cdot E \end{aligned}$$

C. List of Symbols

B	magnetic field in the dc motor 9
C	capacitors of the switch circuit 5
C_{op}	capacitor in the voltage controller 23
E	bridge voltage of the switch circuit in general 5
E_1	bridge voltage of the master module 29
E_2	bridge voltage of the master module 29
E_{next}	bridge voltage in the next time step 13
f_{act}	frequency of master current to switch slave on/off 41
f_M	frequency of the master current 45
I	inductor current in general 5
I_0	reference current of switch circuit plus hysteresis 40
I_{01}, I_{02}	peaks of slave current with unequal inductances 54
I_A	armature current 9
I_{err}	error of peak current for unequal inductances 54
I_{Master}	inductor current of master module 32
I_{ref}	reference current for the switch circuit 5
I_{Slave}	inductor current of master module 32
I_{out}	output current of switch circuit $I_{Master} + I_{Slave}$ 47
I_ε	Current at the output of the hysteresis circuit 21
ΔI	current error between synchronized and non-synchronized current 35
$\Delta I'$	current error for non-exact synchronization 49
J	moment of inertia 9
L	inductance of the switch circuit in general 5
L_A	armature inductance, airgap- and leakagefields 9
l_A	length of the armature 9
M	motor torque 9
M_a	acceleration torque 9
M_L	load torque 9
N	number of armature windings 9
p	number of polepairs 9
$P_1, P1$	switch signal for the master module 5
$P_5, P5$	switching signal for the slave module 32
R	resistive load 26
R_1	resistance in the voltage controller 23
R_2	resistance in the voltage controller 23
R_3	resistance in the voltage controller 23
R_0	resistor to provide reference current $I_{ref} = \frac{U_b}{R_0}$ 24
R_A	armature resistor 8
r_A	radius of the armature 9
R_{H1}	resistor in the hysteresis comparator cicuit 16
R_{H2}	resistor in the hysteresis comparator cicuit 16
T	time for one cycle of master current 45
T_1	time for rising slope of inductor current 35
T_2	time for falling slope of inductor current 35
t_1, t_2	time errors of the slave module 35
$t1'$	intermediate value to calculate t_1 38
t_3	time error of the slave module for non-exact synchronization 49
t_{act}	time delay to start slave synchronized 43