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Interference Cancellation in a Full duplex System

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<i>Title and subtitle</i> Digital Interference Cancellation in a Full Duplex System (Störningsundertryckning i radio för mobilkommunikation)			
<i>Abstract</i> <p>In a full duplex system as WCDMA a mobile phone transmits and receives at the same time, but at different frequencies. The transmitted signal will cause interference in the receiver which must be suppressed to not get degraded sensitivity in the receiver. This Master Thesis was carried out at Ericsson Mobile Platforms in Lund and the purpose was to examine a method to suppress the interference in the digital domain of a WCDMA transceiver. The method is based on that information from the transmitter is fed forward to the receiver to be able to recreate a resembled replica of the interference and subtract it from the desired signal. Further an adaptive least mean square algorithm is used to estimate correct amount of the interference and to provide a tracking ability for temperature variations. A simulator model was developed in matlab to be able to analyze the interference and design a proper cancellation block between the transmitter and the receiver. This simulator model was designed with complexity reductions that did not affect the study of the phenomena. According to simulations, the LMS algorithm turned out to be a sufficient choice concerning rate of convergence, misadjustment and robustness. The main limitation of the improvement by using a cancellation block, was instead determined by the distortion in the transmitter. The trend today is to achieve lower and lower distortions in the uplink making this method more interesting.</p>			
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Abbreviations

3G	Third Generation
3GPP	Third Generation Partnership Project
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
EVM	Error Vector Magnitude
FBA	First Basic Approach design
FDD	Frequency Division Duplexer
FIR	Finite Impulse Response
HD2	second-order Harmonic Distortion
HD3	third-order Harmonic Distortion
HSDPA	High Speed Downlink Packet Access
HPSK	Hybrid Phase Shift Keying
I	In-phase components
IF	Intermediate Frequency
IIP	Input Intercept Point
IM2	second-order Inter Modulation distortion
IP2	second-order Intercept Point for harmonics
ISI	Inter Symbol Interference
LMS	Least Mean Square
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
NDR	Noise-to-Distortion Ratio
NSC	Normal Simulator Condition
OIP	Output Intercept Point

OSVF	Orthogonal Variable Spreading Factor
PLL	Phase-Locked Loop
PSK	Phase Shift Keying
Q	Quadrature components
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RRC	Root Raised Cosine
RX	Receiver
SAW	Surface Acoustic-Wave
SF	Spreading Factor
SIR	Signal-to-Interference Ratio
SNR	Signal-to-Noise Ratio
TPC	Transmit Power Control
TX	Transmitter
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access
WUD	Weight coefficient Update

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Introduction

1.1 Background

Today's cellular phones work more like multimedia units which can handle calls, email, internet, TV and video-calls. To be able to send and receive such information results in higher demands of the data speed. By using WCDMA (Wideband Code Division Multiple Access) higher speed can be achieved. WCDMA is a full duplex system, a radio system where the mobile phone transmits and receives at the same time. The transmitter and receiver operate at different frequencies, called frequency division duplex. It is important to protect the received signal from the transmitted to not get decreased sensitivity in the receiver. A duplex filter is used to be able to connect the transmitter and receiver to the same antenna. Such a filter does not provide infinite isolation between the TX and RX and a leakage signal from the transmitter will appear at the receiver input. Interference products will arise in the receiver and degrade the performance of the receiver. The solution of today is to use a larger and more complex duplex filter, resulting in more expensive cellular units.

1.2 Purpose

The purpose with this Master Thesis is to examine a new method to suppress the interference, caused by the transmitter signal. The method is based on that the information in the transmitted signal is feed forward to the receiver to be able to recreate and subtract the arised interference. This will be done in the digital domain. The following tasks are considered in this thesis.

- Develop a simulator model of a WCDMA radio transceiver.
- Design an algorithm that suppresses the interference, caused by

the leakage signal from the transmitter, and implement it in the simulator model.

- Verify the interference phenomena on hardware.

1.3 Limitations

When designing the simulator and algorithm there are some limitations to consider. This thesis focuses on the interference products caused by internal signals of the transceiver. No adjacent RF interference signal will be considered. Since the problem is largest in a direct conversion receiver, this is the architecture studied in this thesis. A cancellation algorithm can be designed in a large number of different ways. This thesis will focus on the well known least mean square algorithm to suppress the interference.

1.4 Thesis Outline

Chapter 2 gives an introduction to the WCDMA radio interface describing the basic functions in the uplink and downlink. The structure of a frequency division duplexer (FDD) transceiver is also explained here. In chapter 3 the cause of the interference is described and derived. The simulator model design is presented in chapter 4. Here the structure, block diagram and behavior of the simulator will be discussed. In chapter 5 the design of the cancellation block is described together with a proposed hardware architecture. Furthermore model assumptions and complexity reductions will be presented. Chapter 6 and 7 show and discuss the results, both from simulations and measurements. The conclusions are presented in chapter 7.

Technology Overview

2.1 WCDMA Radio Interface

When the third generation (3G) cellular system was invented, some groups of telecommunication association collaborated and made a system specification of the 3G. This resulted in the 3GPP (Third Generation Partnership Project), which standardized the WCDMA-technology.

WCDMA, the abbreviation of Wideband Code Division Multiple Access, is an air interface for voice and data traffic. The Multiple Access part of WCDMA indicates that the transmission medium is shared by many users. The bandwidth of the earlier generation systems was divided into frequency channels or time slots, which means that the users either send or receive on different frequency channels or in different time slots. In WCDMA every user uses a unique spreading code so they can send and receive at the same time and over the whole bandwidth. To be able to send and receive at the same time, called full duplex, WCDMA uses Frequency Division Duplex (FDD), which means that the transmitter and receiver operates at different frequencies but at the same time. The block diagram of an FDD transceiver and its function is described in section 2.2.

The signal which is sent, either from a cellular unit or a base station, has to be modulated so information can be conveyed. Different modulation technologies are used in the uplink and in the downlink. In the uplink a cellular unit transmits to the base station and in the downlink a base station transmits to a cellular unit. HPSK-modulation is used in the uplink and either 16-QAM, 64-QAM or QPSK are used in the downlink. Since many users are sharing the same bandwidth and uses it at the same time, every user has their unique spreading code. The spreading code multiplied with the user data becomes the spread signal that is transmitted. The spreading code is divided into two coding-operations, channelization and scrambling, where channel-

ization can be explained as the inner encoding and scrambling as the outer. Inner encoding means that the codes separates channels and the outer encoding separates cellular units or base stations.

2.1.1 Uplink: Modulation and Spreading

WCDMA uses a variety of channels depending on the amount of data which is being sent. The basic structure is one channel that handles the data, Dedicated Physical Data Channel (DPDCH), and one channel that handles control information, Dedicated Physical Control Channel (DPCCH). The block diagram of the uplink is shown in figure 2.1.

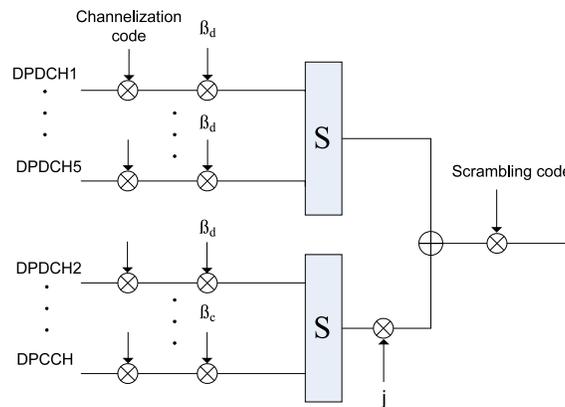


Figure 2.1: Data- and control-channels spread to chip and scrambled

Every channel is multiplied with a channelization code which has a certain chip rate. The data in the channels then spreads out to chip. The spreading factor is the chip rate to data rate ratio. With a higher spreading factor it is easier to recover a signal in the receiver [1].

The channelization codes are known as Orthogonal Variable Spreading Factors (OVSF). These codes are taken from the code tree in figure 2.2 and are related to the spreading factor (SF). When transmitting on more than one channel, two channels can use the same code at the same time. This is not a problem since these channels always will be on different I and Q branches. The function of the channelization codes is to separate data streams from each other and is only used for inner encoding in a transmitter [2]. After the channelization the chip rated signal is weighted with a gain (β). Then the channels are mapped to I and Q branches, summed to a complex signal and scrambled with a complex scrambling code.

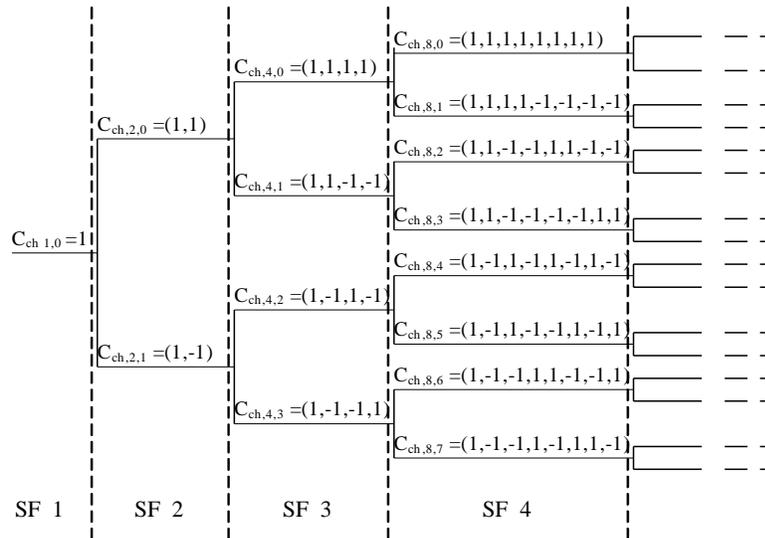


Figure 2.2: OVSF code Tree

If channelization codes are defined as the inner encoding, scrambling codes are defined as the outer encoding. The scrambling code identifies the user and is allocated from the base station. Therefore every scrambling code must be unique in the base station neighborhood [3]. The uplink can be scrambled with either a long or a short code. Both of them have 2^{24} appearances. The scrambling code is a kind of pseudo noise and after the multiplication the signal has the properties of a pseudo noise signal but the scrambling code does not affect the chip rate. If the receiver does not know correct scrambling code it is impossible to recover the signal.

Hybrid Phase Shift Keying (HPSK) is the modulation type that is used in the uplink for WCDMA. HPSK is based of Quadrature Phase Shift Keying (QPSK) which is used in the downlink. The principles of QPSK are for that reason explained here. By using Phase-Shift Keying the phase of a transmitted signal is varied so that information can be conveyed. In 4-PSK, called QPSK, there are four possible phases the carrier wave can have at a specific time. These possible phases are 0, 90, 180 and 270 degrees. Figure 2.3 shows a constellation diagram for QPSK. Every constellation point represents a symbol and the symbol represents two bits of information. That makes the bit rate two bits per symbol. When the QPSK signal get scrambled (complex), the constellation points shifts 45, -45, 135 or -135 degrees. The transitions between the constellation points often goes through zero.

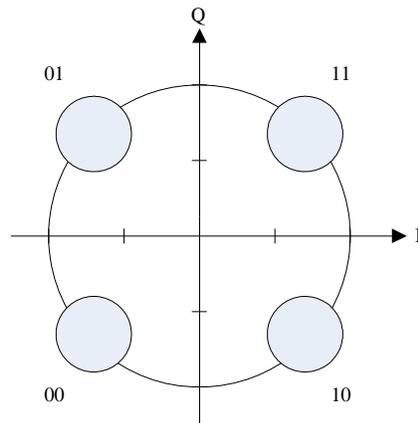


Figure 2.3: The constellation diagram for QPSK (Gray coded).

To get a lower peak-to-average power ratio of the signal, HPSK reduces the number of transitions through zero [4]. This can be done by scrambling the signal with OVSF codes. By scrambling with OVSF codes two consecutive identical constellation points can only be rotated $+45$ or -45 degrees and no zero-crossings will occur. If more than one pair of consecutive constellation points occur some of the transitions might go through zero. This is depicted in figure 2.4. The reason

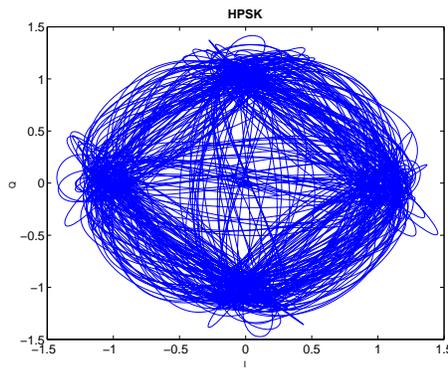


Figure 2.4: Vector diagram of an RRC filtered HPSK signal.

to try to achieve a lower peak-to-average power ratio of the signal, especially in the uplink, is because it increases the lifetime of the cell-phone battery.

2.1.2 Downlink: Modulation and Spreading

Data transmitted from the base station to a cellular unit is called the downlink. The downlink uses more channels than the uplink because it needs channels for pilots, synchronization, etc. The channels are spread to chip and scrambled as shown in figure 2.5. QAM and QPSK

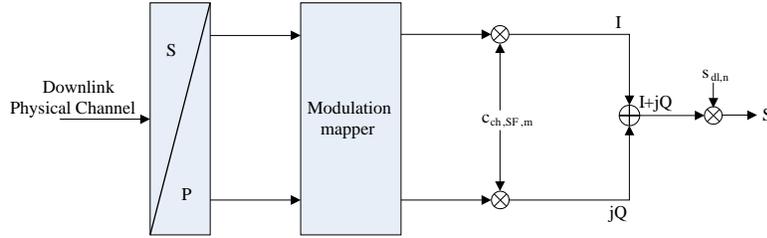


Figure 2.5: Block diagram of the downlink

are the modulation-types used in the downlink. QAM is a method of combining two amplitude modulated signals, with the same carrier wave frequency, into one channel. They are out of phase by 90 degrees and that is why the term quadrature arises. The QAM-signal can be written as in equation 2.1 [5].

$$s(t) = A(t) \cos(2\pi f_c t) + B(t) \sin(2\pi f_c t) \quad (2.1)$$

$A(t)$ is often referred as the in-phase (I) component, $B(t)$ as the quadrature (Q) component and f_c is the carrier frequency. With a digital approach $A(t)$ and $B(t)$ can be observed as a pair of numbers where every unique combination can be interpreted as a symbol. These symbols can then be represented in a constellation diagram where every constellation point is a symbol. The constellation points often have the shape of a square, as in figure 2.6. Since the data often is binary and QAM is square the most common form of signals is 16-QAM, 64-QAM, 128-QAM and 256-QAM. More constellation points contribute to a higher bit rate (bits per symbol). If a higher bit rate is wanted and the mean energy of the constellation remains the same, the constellation points will come closer to each other and are then more exposed to noise and distortion, resulting in a higher bit error rate (BER).

Every channel is split into one I-stream and one Q-stream. Even symbols are mapped to the I-branch and odd symbols are mapped to the Q-branch. The streams are then spread to chip rate by the channelization code. The same code is used for the I- and Q-branch. As in the uplink OVSF-codes are used and they are taken from the

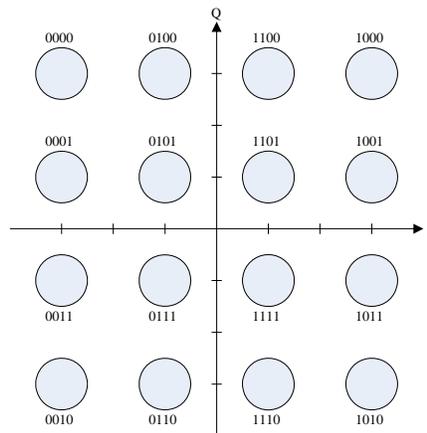


Figure 2.6: The constellation diagram for 16-QAM (Gray coded).

code tree in figure 2.2. After the spreading the two streams are added, resulting in a complex signal. The signal is then scrambled.

The scrambling codes used in the downlink are called gold codes and are similar to the long codes that are used in the uplink. In the downlink a total of $2^{18} - 1$ scrambling codes are used. Since it would be too time-consuming to check a received signal with all the scrambling codes, the codes have been divided into 512 groups where every group has a primary scrambling code. Every primary scrambling code has 15 secondary codes. A cellular unit is allocated one primary scrambling code and the base station basically uses the primary scrambling code to transmit.

2.2 RF and Baseband Design

The structure of an FDD transceiver can be divided into four main blocks, the receiver RF block, the receiver baseband block, the transmitter baseband block and the transmitter RF block. The block diagram of a FDD transceiver is shown in figure 2.7. Since an FDD transceiver transmits and receives at the same time, the function of the duplex filter is to connect the transmitter and receiver to the same antenna. The duplex TX/RX isolation is not infinite and it results in a leakage signal at the receiver input, which is discussed in chapter 3.

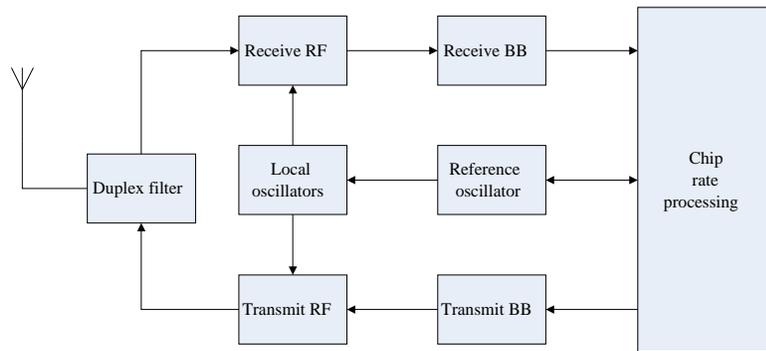


Figure 2.7: Block diagram of a FDD transceiver.

2.2.1 Receiver RF Architecture

The purpose of the receiver RF block is to convert the received signal, which is an RF signal, into a baseband signal. After the received signal has passed the duplex filter, it continues to a low noise amplifier (LNA). The function of the LNA is to recover the signal. An I/Q demodulator is located directly after the LNA. This demodulator contains two mixers and a phase splitter making it possible to recover even negative frequency components. Two independently signal paths (inphase and quadrature) are hence used as depicted in figure 2.8.

The down conversion to base band in a direct conversion receiver is performed by a single mixer pair in one stage. The output of the mixers will have frequency components at the sum and difference frequency. The component at the sum frequency ($2f_{LO}$) is undesired and must be removed by a low pass filter. These analog low pass filters are also used as narrow band filters to attenuate blocking signals before the base band blocks [3].

2.2.2 Receiver Baseband Architecture

In the receiver baseband block an ADC (analog to digital converter) converts the analog baseband signal to a digital signal. A DC-blocker is placed after the ADC to compensate for DC-offset in the receiver. The signal also passes through a chain of decimations with appropriate anti-aliasing filters and a root raised cosine filter (RRC-filter). The RRC-filter forms together with a RRC-filter in the uplink a raised cosine filter. Together they will contribute to a low intersymbol interference (ISI). After the receiver baseband block the signal proceeds for further digital signal processing in the chip rate processing blocks.

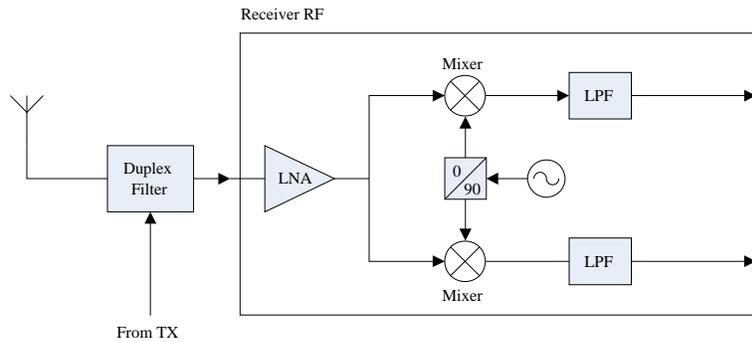


Figure 2.8: Block diagram of the RF Receiver

2.2.3 Transmitter Baseband Architecture

The transmitter baseband block works like the opposite of the receiver baseband block. The signal is here converted from a digital signal into an analog. Before the DAC, the signal is pulse shaped RRC-filtered to limit the occupied bandwidth. It is also possible, at this stage, to compensate for later imperfections in the uplink [3].

2.2.4 Transmitter RF Architecture

The transmitter RF block converts the baseband signals into RF signals in one stage using an I/Q modulator. The main advantage of this direct conversion is its low cost and small size [3]. The modulated RF signal is then amplified and filtered by a band pass filter to reduce the out of band noise. The power amplifier in the transmitter must be designed with high linearity to keep the introduced distortion in the phase and amplitude of the RF signal low. This is a very challenging design task because such a power amplifier consumes much power.

Nonlinearity Effects in a Direct Conversion WCDMA Receiver

In a full duplex system the transmitter and receiver operates simultaneously and in the *third generation mobile communication system*, frequency division duplex (FDD) is used as standard for voice and data communication. To be able to connect the transmitter and receiver to the same antenna, a duplex filter is normally used which in principle is a double bandpass filter. This filter does not provide infinite isolation between the TX and RX paths. The signal from the transmitter will hence leak to the LNA input at the receiver and interference products will, because of nonlinearities, end up in the RX band. Receiver front-ends must therefore be designed to be very linear not to lose sensitivity [6]. The problem with a full duplex transceiver is depicted in figure 3.1.

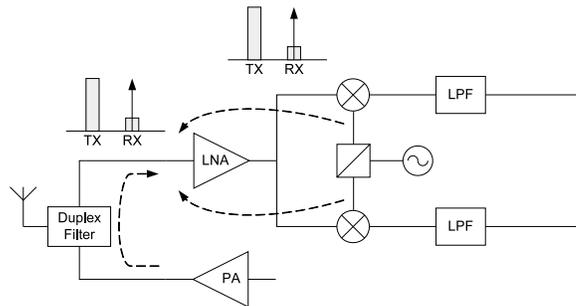


Figure 3.1: A direct conversion receiver and the two dominating leakage signals generated by the transceiver itself.

The magnitude of the leakage signal from the transmitter at the LNA input is dependent of current TX output power and the duplex isolation between the TX and RX paths. Together with the LO leakage signal, nonlinearities in the receiver will produce interference products

in the baseband. These products contain modulated information and can thus not be filtered away.

Next section of this chapter will very briefly describe the basic terminology of distortion and present all necessary equations. Many different mechanisms are responsible for generation of distortion in a zero-IF receiver [7] and the three items in the list below will closely describe four different types of nonlinearity effects.

- Crossmodulation distortion (occurrence at RF)
- Second order distortion (occurrence both at RF and in the base band)
- Self-mixing of TX-leakage signal

The second order distortion contributes with two effects of which one effect occur in the base band and the other one in the RF-parts of the receiver.

All these effects will produce undesired interference at the same frequency as the desired signal and closed-form equations will be derived in this chapter to show similarities. The interconnection or interference coupling between the I- and Q-channel and its influence to the nonlinearity effect will also be described in this chapter. Finally the problem is summarized and similarities between the effects discussed.

3.1 Basic Terminology of Distortion

The behavior of a nonlinear analog block can simply be classified as a weakly or strongly nonlinear behavior. Strongly nonlinear behaviors occur e.g. in an output stage of a switching amplifier, while the weakly nonlinear behavior originate from the transistors curvature in the “linear region”. Weakly distortion can further be classified to arise in a circuit with *memory* or in a *memoryless* circuit. In a circuit with memory the output is not only dependent of the instantaneous input value, but also of previous values of the input signal. This is the case for all analog blocks that include capacitors and inductors.

In a *weakly* nonlinear, *memoryless* amplifier the output signal can be expressed according to the Taylor expansion in equation 3.1 [8].

$$y(t) = a_1x(t) + a_2x^2(t) + a_3x(t)^3 + \dots \quad (3.1)$$

Analog circuits and in particular RF circuits, have memory and the coefficients (a_1, a_2, \dots, a_N) in equation 3.1 can therefore not be considered to be constant over frequency [9]. How much these coefficients

vary depends both on the “memory size” of the amplifier and the bandwidth of the input signal. Even for WCDMA signals, with 3.84 MHz bandwidth, it is a sufficient good approximation to model the nonlinearities in the analog block using the power series approach [8]. If higher accuracy is required numerical simulations or a complete advanced nonlinear analysis using *Volterra series* techniques can be performed for each analog block [10].

Intercept points are of tradition used as a measure of the weakly nonlinearity in RF designs. This results in a measure of distortion where it is not necessary to specify the signal level.

$$IP_{2i} = \frac{a_1}{a_2} \quad (3.2)$$

$$IP_{3i} = \sqrt{\frac{4a_1}{3a_3}} \quad (3.3)$$

The intercept points can be referred to the input (IIP) as well as the output (OIP). The input intercept points are the same as defined above and the requirement of the second order input intercept point is a key specification when designing direct conversion WCDMA receivers [7].

Appendix A contains the frequency response of a two-signal excitation of a weakly linear analog block represented by a Taylor serie of order three. Both harmonic- as well as inter-modulation components are presented in table A.1.

3.2 Crossmodulation Distortion

The first nonlinear effect that will be considered is if one of the input signals to the nonlinear block is a modulated signal. The amplitude modulation will then transfer from one carrier to the other and the effect is therefore called crossmodulation. This occurs in WCDMA transceiver where the TX leakage signal is modulated in both amplitude and phase. The nonlinear block in figure 3.2 contains both the LNA and nonlinearity contributions from the mixer. The mixer is thus split in one part containing nonlinearities and one ideal part only containing the down conversion. The input signal to the nonlinear analog RF block in figure 3.2 contains three signals; a WCDMA modulated leakage signal from the transmitter, leakage from the local oscillators and a desired receiver signal. The desired RX signal is very weak and will thus not activate the nonlinearities in the block. This signal will therefore be neglected in the calculations below. The input signal becomes

$$x(t) = A_{TX}(t) \cos(\omega_{TX}t + \varphi_{TX}(t)) + A_{LO} \cos(\omega_{LO}t + \varphi_{LO}) \quad (3.4)$$

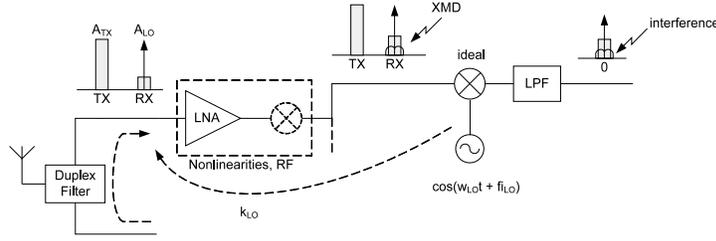


Figure 3.2: Modulated information is moved from one carrier to another and will thus be down converted to baseband. Both the transmitter leakage signal and the LO leakage signal are marked out in the figure.

If the nonlinearity in the RF-block in figure 3.2 is approximated by a third order Taylor expression, with the coefficients $a_{1,RF}$, $a_{2,RF}$, $a_{3,RF}$, the output at LO frequency of the nonlinear block becomes

$$\frac{y_{RF}(t)}{a_{1,RF}} = A_{LO} \left(1 + \frac{1}{IIP_{3i,RF}^2} A_{LO}^2 + \frac{2}{IIP_{3i,RF}^2} \cdot A_{TX}^2(t) \right) \cos(\omega_{LO}t + \varphi_{LO}) \quad (3.5)$$

This expression is related to the input (i.e. divided by $a_{1,RF}$) and is derived by using table A.1 in appendix A (the row marked fundamental frequency) together with the definitions of intercept points. The third term in equation 3.5 contains the modulated TX leakage signal and will therefore become risky and decrease the sensitivity of the receiver. The first and second term will also be down converted to DC but can easily be filtered away.

Crossmodulation arise in the LNA or in the RF-parts of the mixer because of third order distortion (IIP_3) and the interference in the base band, containing the TX leakage signal, is given in equation 3.6.

$$\frac{y_{BB,undesired}(t)}{a_{1,RF}} = \frac{2 \cdot A_{LO}}{IIP_{3i}^2} \cdot A_{TX}^2(t) \quad (3.6)$$

3.3 Second Order Distortion

Another type of nonlinearity phenomena that will arise both in the base band and in the RF stage is second order distortion. Figure 3.3 describes the interference phenomena arising in the base band block and figure 3.4 shows the effect arising in the RF-stage.

The LNA is generally in high gain to be able to detect the weak receiver signal. The TX leakage power can therefore be as high as -10 dBm at the mixer input [6]. As shown in figure 3.3 the mixer is also in

this case split in one ideal part performing the down conversion and one part containing the base band nonlinearities. The input signal to the LNA is the same as in equation 3.4 and the RX signal is neglected as before. Two strong interference signals, expressed in equation 3.7, will consequently be present at the base band block in figure 3.3, where f_d , represent the frequency distance between the LO and TX signal (duplex distance).

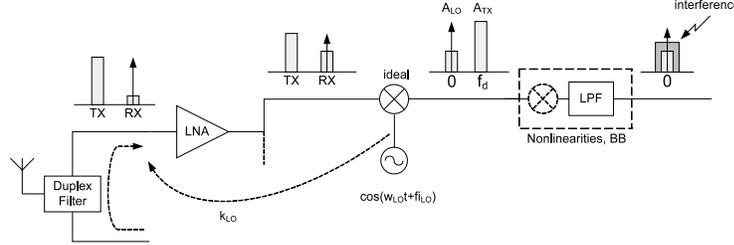


Figure 3.3: If a clean-up SAW filter is not used after the LNA the transmitter leakage signal is still very high at the mixer input causing spurious signals in the base band.

$$x(t) = A_{TX}(t) \cdot \cos(\omega_d t + \varphi_d) + A_{LO} \quad (3.7)$$

Two strong signals to a nonlinear block will, according to table A.1 (appendix A), produce spurious signals at the output of the base band block. These signals can be related to the input of the nonlinear block (i.e. divided by $a_{1, BB}$) as before. The interference can be expressed as in equation 3.8 with the second order intercept point defined in equation 3.2.

The first term cannot easily be filtered away and will thus interfere with the desired RX signal. The second term is also placed at DC but does not contain any modulated information and is therefore easy to remove in the base band.

$$\frac{y_{BB}(t)}{a_{1, BB}} = \frac{1}{2 \cdot IIP_{2i, BB}} \cdot A_{TX}^2(t) + \frac{1}{2 \cdot IIP_{2i, BB}} \cdot A_{LO}^2 \quad (3.8)$$

The undesired signal in the base band, containing the amplitude modulated TX leakage signal, is given in equation 3.9.

$$\frac{y_{BB, undesired}(t)}{a_{1, BB}} = \frac{1}{2 \cdot IIP_{2i, BB}} \cdot A_{TX}^2(t) \quad (3.9)$$

The same effect can also arise in the RF-part of the receiver and leak through the mixer as depicted in figure 3.4. The mixer is, as before,

split into two parts; one part containing the RF nonlinearities of the mixer and one part containing an ideal mixer. If the nonlinear block in figure 3.4 is approximated by a third order Taylor expression, squared components at zero frequency containing the TX leakage signal among others will be generated at the output of the block. These generated

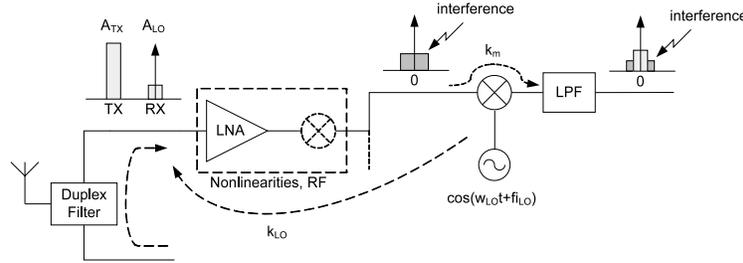


Figure 3.4: The interference placed at DC can leak through the mixer if the isolation is not large enough.

components are found in appendix A (the row marked with DC) and are also shown in equation 3.10, with the intercept points instead of Taylor coefficients. The expression consists of one time constant term that easily can be filtered away in the base band and one term containing the amplitude modulated TX leakage signal and therefore not constant in time.

$$\frac{y_{RF}(t)}{a_1} = \frac{1}{2 \cdot IIP_{2i,RF}} \cdot A_{TX}^2(t) + \frac{1}{2 \cdot IIP_{2i,RF}} \cdot A_{LO}^2 \quad (3.10)$$

The terms in equation 3.10 can, if the isolation in the mixer is not large enough, leak through the mixer and interfere with the desired signal as shown in figure 3.4. If the first term is neglected because of its time constant behavior, the undesired signal in the base band can be expressed as in equation 3.11, with k_m representing the mixer leakage path gain.

$$\frac{y_{BB,undesired}(t)}{a_1} = \frac{k_m}{2IIP_{2i,RF}} \cdot A_{TX}^2(t) \quad (3.11)$$

3.4 Self-Mixing of Transmitter Leakage

The LNA in the receiver is generally in high gain. If a clean-up filter is not used after the LNA the TX leakage signal can still be high at the mixer input. The strong TX leakage signal can leak to the LO-port at the mixer and give rise to self-mixing. The course of events can be studied in figure 3.5. The signal to the mixer input, $u(t)$, is assumed to

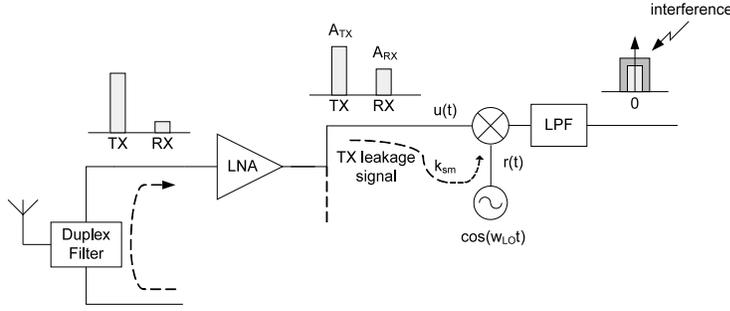


Figure 3.5: A strong TX leakage signal can leak to the LO-port at the mixer and produce interference products in the base band.

only contain the strong transmitter leakage signal as depicted in equation 3.12. In the mixer the signal is multiplied by $r(t)$ in equation 3.13. This signal consists of the LO-signal and some of the TX leakage signal that has leaked into the LO port. The TX leakage signal in $u(t)$ and $r(t)$ respectively are at the same frequency, but with a different phase. This phase difference is represented with $\Delta\varphi_{TX}$. If the isolation between the mixer inputs are bad i.e. leakage factor k_{sm} is large, the interference products due to the self-mixing of the TX-leakage signal becomes significant.

$$u(t) = A_{TX}(t) \cos(\omega_{TX}t) \quad (3.12)$$

$$r(t) = \cos(\omega_{LO}t + \varphi_{LO}) + k_{sm} A_{TX}(t) \cos(\omega_{TX}t + \Delta\varphi_{TX}) \quad (3.13)$$

If the LO magnitude and the mixer gain both are assumed to be unity the interference signal after the low pass filtering can be expressed as in equation 3.14.

$$y_{BB,undesired}(t) = u(t) \cdot r(t) = \frac{k_{sm} \cdot \cos(\Delta\varphi_{TX})}{2} \cdot A_{TX}^2(t) \quad (3.14)$$

3.5 Interference Coupling Between I- and Q-channel

In the previous sections it has been assumed that the leakage signal from the LO is in phase with the LO signal itself. This is usually not the case, but instead the LO signal is coupled back to the LNA input with random phase [11]. Consider figure 3.2 and equation 3.4 again in the crossmodulation section. The WCDMA modulated TX leakage signal will be transferred to a LO leakage signal that is not in phase with the LO signal to the mixer. This will introduce a factor in the interference expressions. The calculations below will illustrate how

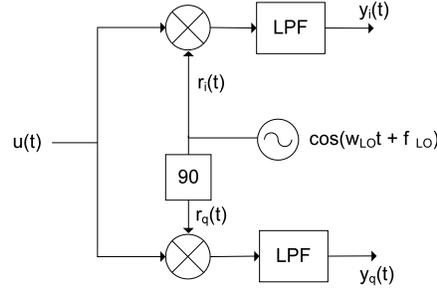


Figure 3.6: I/Q demodulator.

this factor arises and affects the signal. Assume that the input signal to the mixer is at LO frequency but with a phase difference $\Delta\varphi$. Further, assume an error in the phase shifter making $\Delta\varphi_{shift}$ not exactly 90 degrees. The input signals to the mixer pair are expressed below.

$$u(t) = A_{TX}^2(t) \cdot \cos(\omega_{LO}t + \varphi_{LO} + \Delta\varphi) \quad (3.15)$$

$$r_i(t) = \cos(\omega_{LO}t + \varphi_{LO}) \quad (3.16)$$

$$r_q(t) = \cos(\omega_{LO}t + \varphi_{LO} + \Delta\varphi_{shift}) \quad (3.17)$$

The output signal from the mixer, after low pass filtering, becomes in, respectively I and Q channel.

$$y_i(t) = \frac{A_{TX}^2(t)}{2} \cos(\Delta\varphi) \quad (3.18)$$

$$y_q(t) = \frac{A_{TX}^2(t)}{2} \cos(\Delta\varphi - \Delta\varphi_{shift}) \quad (3.19)$$

A LO leakage signal at the LNA input with random phase or an error in the phase shifter will in other words only affect the coefficient in front of the squared TX leakage signal and not the “profile” of the interference.

3.6 Summary of Nonlinearity Effects

In section 3.2 to 3.4, four different nonlinearity effects in a direct conversion receiver front-end with corresponding equations have been described and derived. The effects are generated by the transceivers internal signals, i.e. the transmitter leakage signal and the LO leakage signal and are thus always present during communication. The generated interference signals contain modulated information from the TX leakage signal, at the same frequency as the desired signal, and can

not be filtered away in the base band. These signals are therefore risky because they decrease the sensitivity of the receiver and the jamming effect increases with the square of the TX leakage amplitude. In table 3.1 all effects are summarized together with all derived equations in this chapter. Of course, not all nonlinearity effects in a zero-IF receiver are discussed in this chapter.

Table 3.1: The table contains all derived undesired base band signals occurred by the transceiver's internal leakage signals.

Nonlinearity effect	$\frac{y_{BB,undesired}(t)}{a_{1,x}}$
XMD (RF)	$\frac{2 \cdot A_{LO}}{IIP_{3i,RF}^2} \cdot A_{TX}^2(t)$
2 nd order dist. (RF)	$\frac{k_m}{2 \cdot IIP_{2i,RF}} \cdot A_{TX}^2(t)$
2 nd order dist. (BB)	$\frac{1}{2 \cdot IIP_{2i,BB}} \cdot A_{TX}^2(t)$
Self-mixing (mixer)	$\frac{k_{sm} \cdot \cos(\Delta\varphi_{TX})}{2} \cdot A_{TX}^2(t)$

It has been shown that the derived TX-related effects all have the same profile and can hence be written in a general expression, with an unknown coefficient, according to equation 3.20.

$$y_{BB,undesired}(t) = \text{coeff} \cdot A_{TX}^2(t) = \text{coeff} \cdot (I_{TX}^2(t) + Q_{TX}^2(t)) \quad (3.20)$$

If now both the profile of the interference as well as the transmitter leakage signal itself is known, it should be possible to cancel out the interference. However, the coefficient is still unknown and dependent on dominating effect, temperature, voltage supply and above all is the coefficient unique for each WCDMA transceiver ASIC. The coefficient must therefore in some sense be estimated to optimize the suppression and moreover the coefficients on the I- and Q-channel must be estimated separately.

Simulator Model Design

To be able to evaluate the performance of a cancellation algorithm a mathematical model of the transceiver must be created. This model has to be created with simplifications and assumptions that do not affect the study of the interference phenomena described in chapter 3. The first section of this chapter describes the specified simulator requirements together with chosen design methodology. This is followed by a section describing the structure and accuracy of the implemented simulator environment.

4.1 Simulator Requirements and Design Methodology

For the design and evaluation of a suitable interference cancellation algorithm a simulator model of the transceiver is required. This model can be created in huge number of different ways and with different computer tools. It is therefore important to state the main points of the simulator requirements and lay down the general design methodology at an early stage.

Simulator requirements

- Satisfactory model accuracy. Add only imperfections to the model that are important for the design of the cancellation block.
- Make all imperfections adjustable and possible to disable.
- At least the squared error signal must be calculated to be able to evaluate the performance of the cancellation algorithm.
- It must be possible to simulate over many WCDMA slots with different simulator parameters.
- All simulations should be performed in the base band.

Design Methodology

- Matlab should be used as simulator implementation tool.
- A top-down implementation approach should be used with a top-level structure according to the transceiver block diagram in figure 2.7.
- The I- and Q-channels should, in the model, be represented as a complex number. This gives a better structure and simplifies the implementation process.

Besides the complex simulator specified above, a *conceptual simulator* should be designed where conceptual design ideas quickly can be tried out. This simulator is designed and implemented in the same way (matlab) and with the same structure as the more advanced, but the requirement that it should be possible to simulate over many WCDMA slots with different simulator parameters is not fulfilled for this simulator. New ideas can first be tested in the *conceptual simulator* before they are further implemented and analyzed in the more advanced.

4.2 Simulator Structure and Accuracy

4.2.1 Simulator Block Diagram

Figure 4.1 shows a complete top-level block diagram of the implemented matlab simulator. The block diagram is vertically split into three sections; transceiver, analysis and references. The lower transceiver part contains a model of a WCDMA transceiver with the same block structure as depicted in figure 2.7. In addition, the cancellation block is added in the middle and the transmitter leakage signal is connected directly to the receiver RF block.

The analysis section contains, as specified in the specification, the squared error signal as evaluation option of the cancellation algorithm. To be able to calculate the squared error signal, a reference signal from the upper part of the block diagram is used. This reference signal is passing through exactly the same blocks as the received signal, with the exception that no interference is added and no cancellation block is connected that tries to suppress the interference.

4.2.2 Simulator Behavior

Both the uplink and downlink in WCDMA is transmitting data organized in frames with a duration of 10 ms [3]. With a chip rate of 3.84

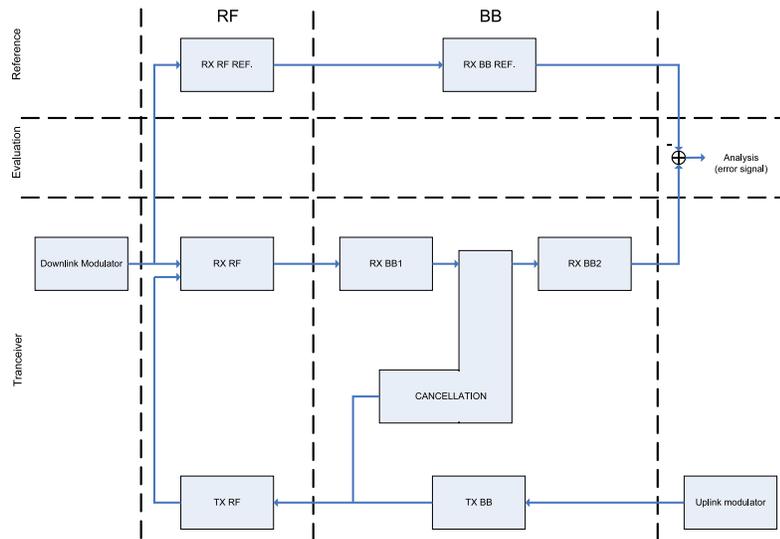


Figure 4.1: A top-level block diagram of the implemented simulator.

Mcps a frame contains 38400 chips. Each frame is divided in 15 slots, or power control periods containing 2560 chips [3]. Power control is a very important aspect in WCDMA to make it possible to distinguish one mobile station (MS) from another. The base station (BS) estimates the received signal-to-interference ratio (SIR) and transmits one TPC command per slot to control the uplink transmission power [12]. Because the output power is changed in every slot, the power of the transmitter leakage signal is also changed in every slot and thus the interference magnitude. As specified in the simulator requirements it is therefore important that it is possible to simulate over many slots with different simulation parameter settings. In HSDPA the power can be changed in a slot.

The simulation time has been quantized in one fifth of a slot or 512 chips, to make it possible to change parameter values even within a slot and the simulator is implemented with a behavior depicted in figure 4.2.

An initial parameter setup sets the general simulation parameters, i.e. oversample rate, chip rate, e.t.c. A simulation over 512 chips is then performed before a new simulation setup can be executed. It is important to make it clear that the simulation parameters must not be changed in every loop. Finally the result vectors are analyzed according to the specified evaluation options.

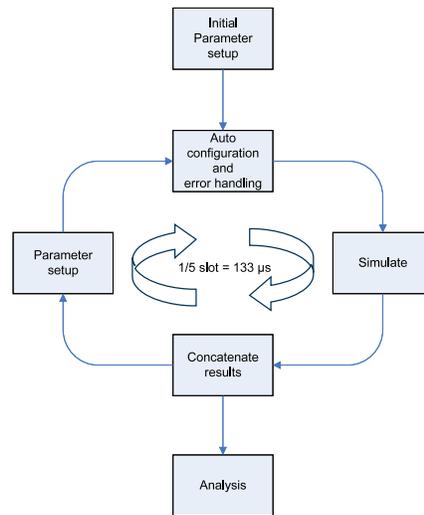


Figure 4.2: The simulator parameters can be changed in every loop (512 chips long).

4.2.3 Model Assumptions and Complexity Reductions

Consider figure 4.1 again, the lower transceiver part consists of eight different blocks. Of these eight blocks, three originates from a WCDMA radio transmitter and four from a direct conversion WCDMA radio receiver. The eighth block is the cancellation block, located between the TX- and RX-chain. The design of this block is completely described in chapter 5 and will therefore not be considered here.

Simulator transmitter chain

The uplink modulator is implemented as a WCDMA modulator with one DPDCH and one DPCCCH channel. A long complex scrambling sequence is generated in the block and used to scramble the data and control message signals. This signal is then upsampled with a specified oversample rate to achieve a larger accuracy in the time domain in the model.

The different blocks in figure 4.1 contain satisfactory mathematical models of effects that arise in the same blocks in a real transceiver. The base band block in the transmitter contains a FIR root raised cosine (RRC) filter with a roll-off factor equal to 0.22. Nyquist RRC filters are used in both the uplink and downlink in WCDMA to enclose the signal bandwidth and at the same time keep the inter symbol interference (ISI) as low as possible [3]. The pulse shape filter is defined in the

3GPP specification [13].

Next block in the block diagram is the RF block. In a real transmitter the message signal is here modulated onto a RF carrier, but this is not done since the implemented simulator should perform all simulations in the base band. There is still one imperfection that originates from the RF block and that not can be dismissed. Most of the distortion in the transmitter chain arises in the power amplifier at maximum output. This distortion will spread the symbols from its constellation points. The error vector magnitude (EVM) is defined in equation 4.1 and figure 4.3, and it is a measure of the difference between the constellation point (z_n) and the measured symbol point (\hat{z}_n).

The trend today is to achieve lower and lower distortion, but it is reasonable to assume at least 5% EVM in the uplink. In this model the TX distortion is modulated as additive white Gaussian Noise (AWGN). This can be considered as a worst case scenario.

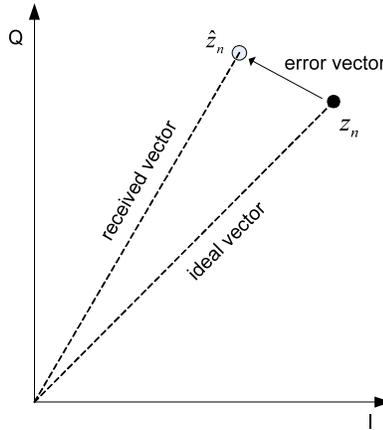


Figure 4.3: The error vector magnitude is used as a measure of the distortion. The solid point is the constellation point and the other one is the received symbol.

$$EVM_{rms} = \sqrt{\frac{\sum_n |\hat{z}_n - z_n|^2}{\sum_n z_n^2}} \quad (4.1)$$

Simulator receiver chain

Consider figure 4.1 and the receiver chain in the middle. This receiver, with all sub blocks, is shown in figure 4.4. The downlink modulator is only generating thermal noise, modeled as AWGN. The interference problem is largest at high TX output power levels. High levels are used

if the mobile phone is far away from the base station and the desired RX signals can thus be assumed to be placed below the thermal noise floor. This complexity reduction will therefore not affect the model accuracy. After the downlink modulator, the signals will pass through a RF block. Input signals to this block are both the downlink signal and the leakage signal from the transmitter chain. The RF block in

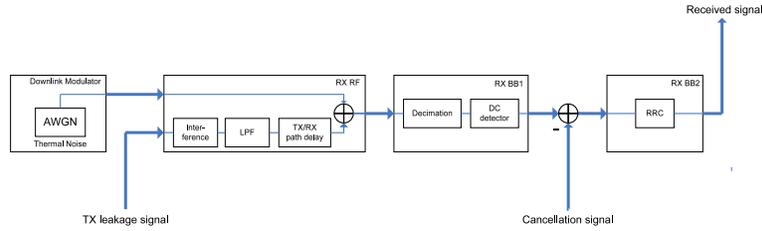


Figure 4.4: Implemented receiver chain in the simulator model.

the receiver contains three different sub blocks. First the interference is created with the TX leakage signal according to the interference expression in equation 4.2. The equation gives the interference in one channel. The coefficients in the I- and Q-channels will be different but are for simplicity both set to one in the simulator model.

$$y_{BB,undesired}(t) = \text{coeff} \cdot (I_{TX}^2(t) + Q_{TX}^2(t)) \quad (4.2)$$

This interference signal arises after the mixers in the receiver and is then enclosed by the analog base band filter. The second sub block in the RF block is thus an analog low pass filter. This filter was here chosen as a fourth-order analog Butter-worth filter with a cut-off frequency of 2.5 MHz. The third sub block will model the delay in the TX/RX path, or more exactly the spreading in delay. It is reasonable to assume that a nominal path delay can be measured from a set of transceiver ASICs. The delay originates from all the analog blocks in both the transmitter and receiver. However, the analog base band filter in the receiver is dominating because of its higher filter order and will therefore also contribute with most of the delay. The designed Butter-worth filter has an initial group delay of approximately 200 ns and it is reasonable to assume a 5% spreading in bandwidth between different ASICs and therefore also in group delay. This results in a 10 ns spreading in the TX/RX path delay.

The base band functions are subdivided in two different blocks with the subtraction of the cancellation signal in between. The first block contains decimation and a DC subtractor. All decimation is modeled to

be performed in one stage. An eighth order Chebyshev Type I low pass filter is located in front of the downsampling unit as an anti-aliasing filter¹. In which order the DC subtractor and RRC filter is placed in a state of the art WCDMA receiver is mathematical equivalent. Since the receiver contain DC components generated in different receiver blocks, it is impossible to distinguish the DC component (caused by the interference) from other DC components. To get rid of the DC problem and consequently make the design of a cancellation block easier, the DC subtractor is located before the RRC filter. The RRC filter is the same filter as in the transmitter chain.

Simulator reference chain

To be able to evaluate the performance of the cancellation block, the received signal (marked in figure 4.3) must be compared with an ideal received signal. The reference receiver chain is located in the reference section in figure 4.1 and contains exactly the same block as the other receiver chain except for the added interference and the subtracted cancellation signal. The error signal can then be calculated as the difference between the reference signal and the received signal, as depicted in figure 4.1.

There is no reason to add imperfections to a model that only will increase the model complexity and not improve the study of a proper cancellation algorithm. Two dominating imperfections in the transceiver have therefore been taking into consideration in this simulator. Besides that, the implemented analog low pass, will contribute with an additional imperfection.

- Transmitter distortion
- TX/RX path delay
- RX LP-filter

¹The *decimate* command in matlab uses this filter as a default anti-aliasing filter.

Cancellation Block Design

The interference problem described in the previous chapters will decrease the sensitivity of the receiver and therefore high demands are put on linearity in RF as well as in base band receiver blocks. The state of the art solution to minimize the transmitter leakage signal is to use a physical larger and steeper duplex filter, which results in higher cost and larger in-band loss.

This chapter will present a solution to suppress the interference, which is based on the knowledge of the interference “profile”. The chapter is subdivided into two main sections. First, the design of a cancellation algorithm is studied and a *first basic approach* solution is presented. Different design options and optimization possibilities will then be discussed. Even if this section just concerns the design of the cancellation block at algorithm level, the fact that the algorithm should be possible to implement in hardware cannot be dismissed. Some design outlines can therefore be determined at an early stage in the design process and will thus point out the direction of the design. The chapter will begin with a brief presentation of adaptive filters in general and define some requirements for convergence and stability. The hardware aspect will be considered in the next section of this chapter and an architecture will be presented and practical considerations concerning implementation in hardware will be discussed, where cost (area), power consumption and performance (speed) are the main issues.

5.1 Algorithm Design

5.1.1 A Typical LMS Application

Adaptive filters are used in many different applications where the statistical environment is not completely known. The filter consists basically of one part performing the filtering of the input signal and one algorithm part whose task is to control the filter coefficients in some efficient

way. The LMS algorithm works by the principle that it minimizes the *mean square* error of the output signal.

Interference cancellation is a typical application for an adaptive filter. Consider the system in figure 5.1 where an adaptive filter is used to cancel out interference in the primary signal and thus improve the systems signal-to-noise ratio. The system consists of a primary signal containing a desired signal and undesired noise together with a reference signal containing a measured copy of the noise. If the noise in the primary signal and the measured noise in the reference signal are correlated it is possible to suppress the interference.

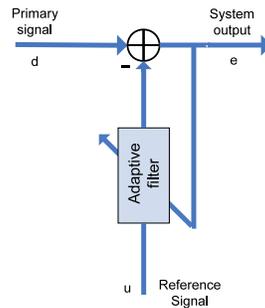


Figure 5.1: The interference cancellation is a typical application for an adaptive filter.

The LMS algorithm starts from a predetermined initial condition and is then iteratively updating the filter tap values, \mathbf{w} , according to equation 5.1 [14]. Both the reference signal and the error signal are used in the updating process and are represented with \mathbf{u} and \mathbf{e} respectively. The algorithm is controlled with a parameter μ which determines the size of the step towards the new coefficient values.

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu \mathbf{u}(n) \mathbf{e}^*(n) \quad (5.1)$$

The main advantage with the LMS algorithm is its simplicity, but it has a relatively slow rate of convergence [14].

It exists a huge number of other adaptive filter algorithms with both faster convergence and better over all performance, but if the rate of convergence for the LMS turn out to be enough it can with advantage be implemented in hardware.

5.1.2 LMS Stability and Steady-state Analysis

Because of the LMS feedback loop it is not guaranteed that the algorithm will converge. If the chosen step-size parameter is too large the

filter coefficients will diverge, and a maximum value of the step-size must therefore be determined when designing with adaptive filters. A complete mathematical analysis of the LMS stability does not exist [14], but instead some rules that can be used in the design process are defined. The condition for convergence is normally expressed as

$$0 < \mu < \frac{2}{\lambda_{max}} \quad (5.2)$$

where λ_{max} is the largest eigenvalue of the input data correlation matrix \mathbf{R} . Because the eigenvalues to the correlations matrices are often not known, the rule of thumb in equation 5.3 can be used instead.

$$0 < \mu < \frac{1}{Mr_u(0)} \quad (5.3)$$

M is the length of the adaptive filter and r_u is the correlation vector for the input signal defined as in equation 5.4 and 5.5. If the input signal power can be estimated, the maximum step-size can also be determined.

$$r_u(k) = E\{u(n)u^*(n-k)\} \quad (5.4)$$

$$r_u(0) = E\{u(n)u^*(n)\} = E\{|u(n)|^2\} \quad (5.5)$$

The stability and rate of convergence are important, but it is not the only design parameter that has to be considered in the design process. Learning curves are a commonly used tool to study the performance of an adaptive filter [14]. The *ensemble-average-square-error* value, defined in equation 5.6, is then plotted versus number of iterations.

$$J(n) = E\{|e(n)|^2\} \quad (5.6)$$

If the step-size parameter is chosen to an appropriate value, $J(n)$ will converge against a constant value for an increasing number of iterations. This “final” value is often represented as $J(\infty)$. The LMS filter coefficients converges against the optimum Wiener solution¹, without reaching the optimum because of the gradient noise. The misadjustment is defined according to equation 5.7 and is hence the ratio of the LMS steady-state value and the mean square value with an optimal wiener filter (J_{min}). The equation is hence a measure of how far the steady-state solution is from the optimal wiener solution.

$$M = \frac{J_{ex}(\infty)}{J_{min}} = \frac{J(\infty) - J_{min}}{J_{min}} \quad (5.7)$$

¹A Wiener filter is an optimum filter in the sense that the mean-squared error signal between the desired output and the filtered output is minimized.

The misadjustment is a proper evaluation parameter of the algorithm performance in steady-state. Furthermore there is a trade-off between fast convergence and small misadjustment and they are both controlled by the step-size parameter. The LMS filter can also be seen to behave as a low-pass filter with a time constant that is inversely proportional to the step-size [14].

5.1.3 A First Basic Approach

It has earlier been declared that an interference in the primary signal can be suppressed by creating a correlated replica of the interference and let an adaptive filter minimize the squared error signal. In chapter 3 the “profile” of the interference in the base band was derived and it was shown that interference in each channel (with different coefficient values) could be expressed as

$$y_{BB,undesired}(t) = \text{coeff} \cdot (I_{TX}^2(t) + Q_{TX}^2(t)) \quad (5.8)$$

Both the inphase and quadrature components in equation 5.8 are known apart from the distortion the leakage signal is exposed for in the uplink power amplifier. The magnitude of the base band interference will depend on current TX/RX operation band (different duplex filters) and vary with the magnitude of the transmitter leakage signal.

The coefficient value in equation 5.8 is on the other hand ASIC and implementation specific and is above all determined of the IP2, IP3 and LO leakage of the receiver. Slowly coefficient variations with temperature and voltage supply are however possible. Both channels in the receiver are exposed for the same interference, but the coefficient values in the channels are usually different.

The first cancellation block design, called “*A first basic approach*”, is divided into two sub blocks; *interference creation block* and *adaptive filter block*. The first sub block tries to create an interference profile that corresponds to the real interference and the task of the second block is, in an adaptive manner, to estimate the coefficient value. This first cancellation design approach puts no demands on implementation costs at all. The only requirement is to create a replica of the base band interference that, at all costs, resembles the real interference as much as possible. A block diagram of the entire cancellation block is shown in figure 5.2, and the functionality of the two subblocks are described subsequently.

Interference creation block

It is not possible to create a replica of the interference that exactly resembles the real interference. The distortion in the transmitter power amplifier, the unknown TX/RX path delay, among others, will expose the TX leakage signal for a difference that in this design approach neither is measured nor estimated.

In figure 5.2 the *interference creation* block is marked with a dashed rectangle and its task is to create a replica of the real base band interference by using the TX data information and the knowledge of the interference profile from chapter 3. The magnitude of the interference will depend on both chosen output power setting in the transmitter and the TX/RX isolation of the duplex filter. Information about the magnitude of the TX leakage signal is very useful for the *interference creation block* to be able to create a similar replica of the interference. It is therefore necessary to estimate the magnitude of the TX leakage signal at the LNA input of the receiver by feed-forward the output power settings and subtract the TX/RX isolation of the duplexer. The leftmost multiplier in figure 5.2 is used to create approximately correct magnitude of the TX leakage signal. Correct magnitude is not possible to get, because a e.g. +3 dB change in software will not exactly result in a +3 dB change in the power amplifier. These differences in the output power are accepted according to the 3GPP specification [13].

The next step is to create the “profile” of the interference. The I- and Q-signals are first individually squared and then added (compare with equation 5.8). Because the interference products in the base band are derived from a squared expression, the spectrum after the mixers in the receiver will be approximately twice the TX-leakage bandwidth, i.e. 3.84 MHz. The analog lowpass filters after the mixers in the receiver (used to remove adjacent channel interferers and blockers) will then enclose the interference to the filter bandwidth.

In this first approach, a digital sampled model of the analog low pass filter will be used to affect the interference in a similar way as the low pass filters in the receiver. The similarities between an analog low-pass filter and its digital equivalence will differ with chosen sample rate. It is in other words easier to create a better sampled model of the analog filter at a higher sample rate. In this design (*first basic approach*) the cancellation block is assumed to work at double chip rate, which is desirable for low power consumption.

Consider figure 5.2 again, the cancellation block is measuring the TX signal directly before the DAC in the transmitter chain and is then creating a replica of the base band interference after the analog low

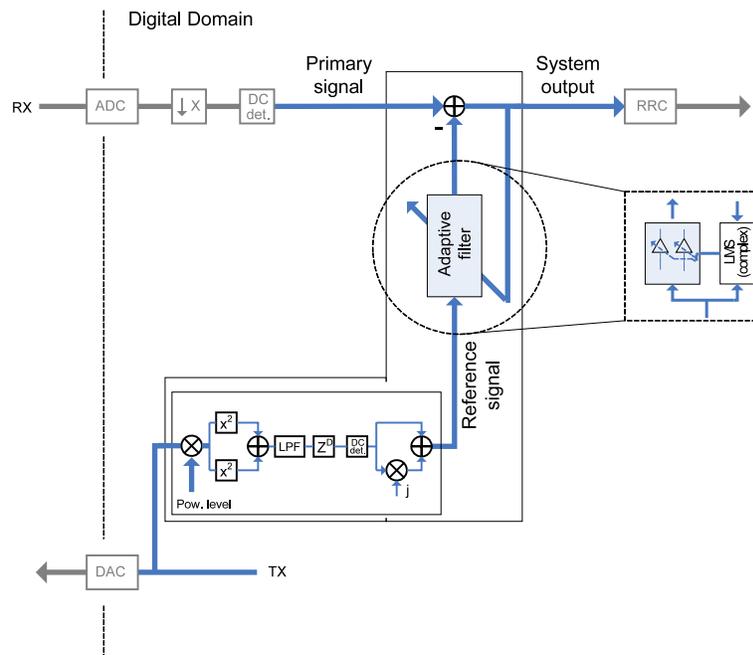


Figure 5.2: The first basic approach of a cancellation block. Thicker lines represent complex numbers.

pass filters, as describe above. It is important to measure the signal as late as possible in the transmitter chain to avoid that the TX-signal is affected after the measuring point.

There are still at least two dominant imperfections (transmitter distortion and TX/RX path delay) that will expose the TX leakage signal for a difference that not exactly can be measured. This distortion in the transmitter power amplifier is in this design neither measured nor estimated. It is however possible to compensate for the TX/RX path delay. The analog low pass filter in the receiver chain is the most dominating factor of this path delay, because of its larger bandwidth, and by doing an equivalent sampled model of the analog low pass filter, the group delay of the analog filter will also be estimated in a good way. The spreading of group delay in the analog low pass filter that originates from a spreading in bandwidth can however not in a simple way be estimated. In this *first design approach*, the LMS algorithm is assumed to take care of the small variations in group delay.

There will also be a dominant delay in the digital blocks in the receiver chain. This delay is exactly known and the cancellation block must compensate for this. In figure 5.2 the compensation of the ana-

log delay is in other words performed by the LPF block, while Z^D is assumed to compensate for delays in the digital domain.

The last block in the *interference creation block* is a DC subtractor, as depicted in figure 5.2. The mixer in a direct conversion receiver will convert the RF signal into base band in one stage and the RX due to imperfections will give an undesired DC component [3]. Also the interference will contain most of its power as DC and it will therefore be confusing for the LMS algorithm to know which part of the DC component that originates from the interference. If the DC component is not removed, the LMS algorithm will converge against a much larger value and not create a good replica of the interference. If the DC is removed before the cancellation chain this problem can be avoided. A DC subtractor is therefore also included in the cancellation chain.

Adaptive filter block

An accurate replica of the interference, except for the coefficient value in equation 5.8, has now been created in the *interference creation block*. To be able to subtract the right amount of the interference the coefficient value must also be estimated. This can be done with a first order LMS adaptive filter. The LMS algorithm will minimize the squared error signal sample for sample and thus converge against the coefficient value. Because the I- and Q-channels necessarily do not have the same coefficient value, the squared error signal must be minimized in the two channels separately and two LMS adaptive filters are needed.

It is not obvious in which bandwidth the LMS algorithm should try to minimize the squared error, i.e. where the feedback should be connected. The interference has a frequency contents from DC up to the cut-off frequency of the analog base band filter in the receiver, which is above the information bandwidth (1.92 MHz). In this *first basic approach* the cancellation block is assumed to work at double chip rate and frequencies up to 3.84 MHz can thus be represented. The optimal solution might be to minimize the squared error signal in a bandwidth where the ratio between the interference power and the thermal noise power is maximal. If this optimal solution should be used, a filter has to be connected in the error feedback loop. This introduces a delay in the loop, putting larger demands on the LMS algorithm concerning robustness and stability.

For simplicity the squared error signal is therefore, in this *first basic approach*, minimized in the double information bandwidth (3.84 MHz). Figure 5.2 shows that the feedback loop is connected directly after the interference subtraction unit.

5.1.4 Design Options and Optimizations

The *interference creation block* described in the previous section contains a number of different components. The sampled model of the analog base band filter in the RX encloses the frequency content of the interference replica and is in the same time compensating for the dominating analog delay in TX/RX path. If this filter is replaced by a block that only compensates for the mean delay in the path, the real interference will contain more high frequency information and this will cause a discrepancy between the real interference and its replica. This discrepancy might be small in comparison to other differences between the paths. Simulations, in later chapters, will show its influence.

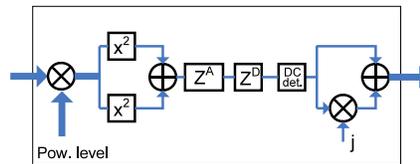


Figure 5.3: The sampled model of the analog base band filter is here removed and replaced by a delay component that only compensates for the mean analog delay.

If it is assumed that the frequency content is equally distributed over the entire filter bandwidth, the mean compensation delay can be chosen as the mean delay marked with a red dashed line in figure 5.4.

The step-size parameter to the LMS algorithm is the only controllable parameter for the entire cancellation block and it is neither sure nor probable that it exists an optimal step-size parameter for all possible situations. A more flexible solution is therefore depicted in figure 5.5 where a RAM memory is used to save different step-size parameters.

In the *first basic approach* presented in the previous section, the LMS initial coefficient value is set to zero. It is therefore probable that a larger step-size must be used in the first slots to quickly converge against the coefficient value, but with a larger amount of gradient distortion. The step-size parameter can then gradually be decreased to minimize the gradient noise. Because the LMS algorithm also offers a tracking behavior, the step-size should not be chosen to small. The coefficient value cannot be considered constant over time. It might be a variation with temperature and power supply, but above all with the error between the actual TX output power and the feed-forward information about the power. This will directly affect the coefficient values in every slot. An output power error like this is always present and the specified error tolerance is different for different power steps [15]. One

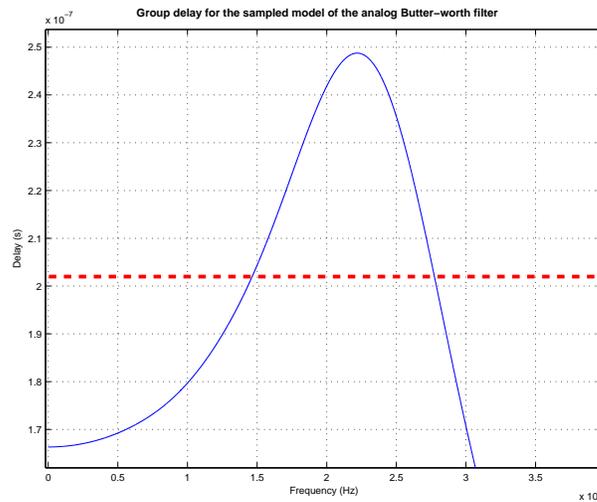


Figure 5.4: The group delay for a digital butter-worth filter with a 2.5 MHz cut-off frequency. The red dashed line marks chosen compensation delay.

solution is therefore to specify different step-sizes for different output power levels as depicted in figure 5.5. This is just a design option and it is not yet established that this is worthwhile.

5.2 Hardware Implementation Proposal

5.2.1 Hardware Architecture

An LMS adaptive filter can generally be divided into one FIR filter block (F-block) performing a general filtering, and one weight coefficient update (WUD) block, that updates the filter coefficients [16]. The tap value in the filter block is updated every iteration. The implementation proposal in figure 5.6 is not optimized in any meaning, but instead it is a direct translation of the design in figure 5.2 into hardware. In this application the F-block consists, as described before, of a filter with only one tap.

5.2.2 Practical Considerations

Before an architecture is implemented in hardware it has to be optimized. The hardware proposal in the previous section is not optimized at all, but more a direct translation of the design into hardware.

It is always a trade-off between cost (area), power consumption and performance (speed). Power reducing can be done at different stages

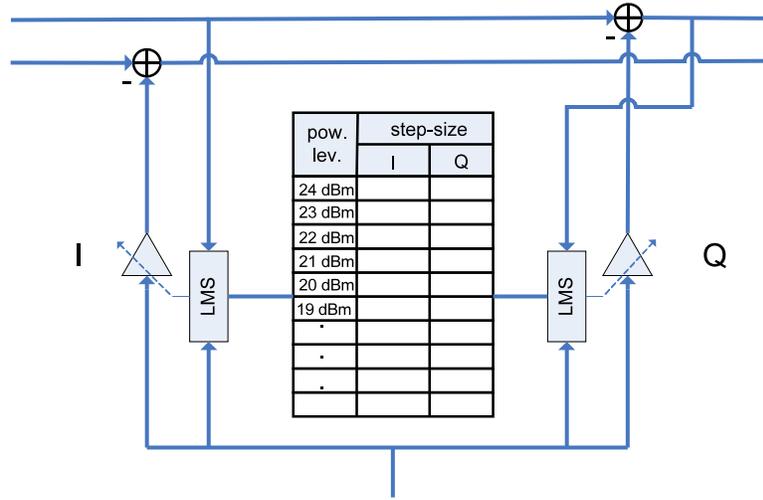


Figure 5.5: Enhanced adaptive filter block with a RAM memory to save step-size parameters.

in the design process [15]. The first step is to optimize the design at algorithmic level, which is maybe the most challenging part. It exists many various options and it is not always obvious which design option that is the best concerning power consumption. At lower levels the design parameters are limited making the optimization problem easier [15].

A trend today is to implement digital as well as analog systems in CMOS technology to benefit from advantage of a lower DC power dissipation. The most power dissipation in a CMOS circuits is consumed during switching and can be expressed as in equation 5.9 [15].

$$P_{switching} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f_{clk} \quad (5.9)$$

where α is the switching activity factor, C_L the load capacitance, V_{DD} the supply voltage and f_{clk} the block clock frequency. In digital CMOS circuits, the switching power dissipation above can be responsible for as much as 90% of the total power consumption [15]. The supply voltage has the largest influence, but is determined by the technology process and cannot easily be reduced. The sample rate (f_{clk}) must however be optimized.

In the *first basic approach* design presented in previous sections, the cancellation block is running at a sample rate that is equal to twice the chip rate. This can be considered as a relatively low sample rate.

The power dissipation can also be optimized by pipelining. If the architecture is pipelined, the critical path is reduced and the capacitance

(C_{charge}) that is charged/uncharged every clock cycle is also reduced [16]. The total capacitance of the system remains the same, but if the capacitance between two delay elements is reduced, the supply voltage to the block can also be reduced.

Another possible way to effectively reduce the power dissipation is to let the cancellation block enter sleep-mode if the distortion is weak and the block does not bring any particularly suppression. This is the case at lower output power levels.

In digital implementations no coefficient values or signal values can be represented with infinite precision. The effect of finite word lengths must therefore also be taken into account. One problem that might occur is that the LMS stop adapting when the $\mu e(n)u(n)$ term in equation 5.1 is smaller than the least significant bit of the tap value that is updated [14]. This phenomenon is called stalling.

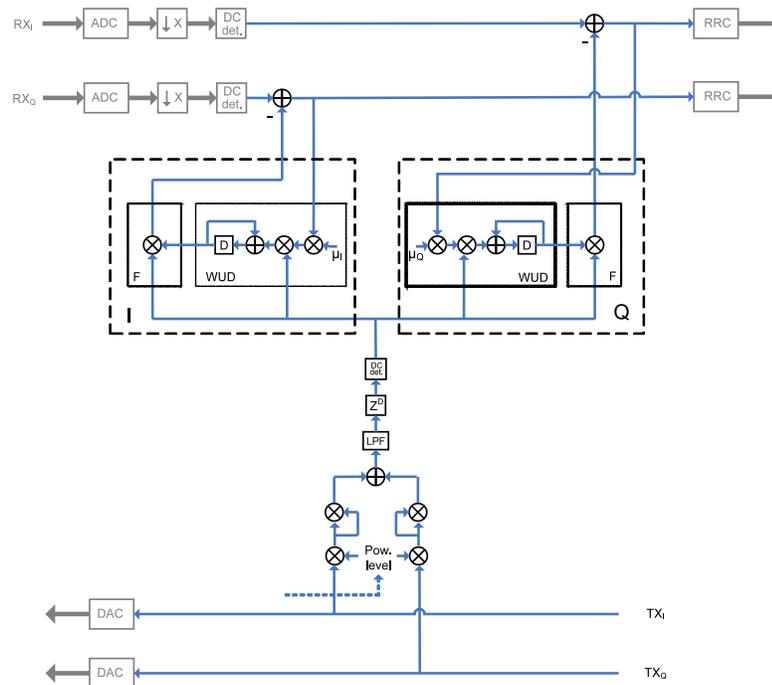


Figure 5.6: A direct translation of the design in figure 5.2 into hardware.

Simulation and Measurement Results

This chapter will present both results from simulations and results from hardware measurements on a WCDMA transceiver ASIC. The simulation results are all produced with the simulator environment described in chapter 4. This chapter includes, among others, simulations over many WCDMA slots with different TX leakage magnitudes. These simulations can be referred as *typical transmission* simulations and will in a good way evaluate the improvement of the system by using the cancellation block.

6.1 Simulation Results

6.1.1 General Simulation Definitions

In chapter 4 the transceiver model with all added imperfections was explained in detail. The points below will again explain some of the most important model considerations to simplify the understanding of figures and plots in this chapter.

- **Downlink test signal**

All simulations are performed without a desired downlink signal. Instead only thermal noise, modeled as AWGN, is applied at the receiver input. This is a correct simplification since scrambled downlink signals are placed below the thermal noise floor in the interval where the TX leakage is a problem, as described in section 4.2.3.

- **Interference test interval**

The *interference power versus the thermal noise power, both measured in the base band*, is in all simulations chosen in the interval -10 to 20 dB. Notice that the -10 dB test case in the simulation results sections hence is referred to a 10 dB *weaker* interference

power compared to the thermal noise power. The power of DC component in the interference is included in the test interval.

- **Power measurements**

The interference and thermal noise power are both measured in the base band as a RRC filtered mean power according to the 3GPP user equipment test specification [13].

- **TX distortion**

The added distortion in the transceiver uplink is modeled as AWGN. The *error vector magnitude* (EVM) is used as a measure of the transmitter distortion. This is explained more in section 4.2.3.

- **Coefficient value** The optimal interference coefficients in the I- and Q-channels are both set fix to 1 in the simulator model. This makes it easier to study the plots since the LMS adaptive coefficients then also should converge against 1.

- **Error signal**

The error signal is defined as the difference between the output signal from the reference receiver chain and the receiver with added interference. The two parallel receiver chains are shown in figure 4.1 and the error signal is also marked out.

- **System NDR**

The system NDR(noise to distortion) is defined as the ratio between the reference receiver output signal (thermal noise) and the error signal defined above.

- **Normal Simulator Condition (NSC)** This condition is referred as a normal condition for the transceiver model with a 5% EVM in the uplink and a TX/RX path delay spreading of 10 ns.

6.1.2 Classification of Simulation Results

The cancellation block was in chapter 5 divided into two sub blocks; *interference creation block* and *adaptive filter block*. It is therefore suitable to evaluate and present the simulation results by first study the two subblocks individually and then evaluate the performance of the entire cancellation block. The following classification of simulation results is therefore used:

- Performance of the interference creation block.

- Performance of the LMS Algorithm block
- Performance of the entire cancellation block from a system point of view

The first two items will more point out different limitations in the two subblocks. How these limitations affect the performance of the cancellation block in the entire system will not be discussed. The third item (and also section) will therefore with system simulations summarize their influences from a system point of view.

6.1.3 Performance of the Interference Creation Block

Spectrum analysis of the interference

To be able to create a replica of the interference that in a good way resembles the real interference, the interference spectrum must be analyzed. The interference spectrum in figure 6.1 (a) contains frequencies all the way from DC to twice the TX leakage signal bandwidth (3.84 MHz). Further, most of the interference power is placed at DC. The base band low pass filter in the receiver affects the interference spectrum and encloses the bandwidth to the filter bandwidth, which is shown in figure 6.1 (b).

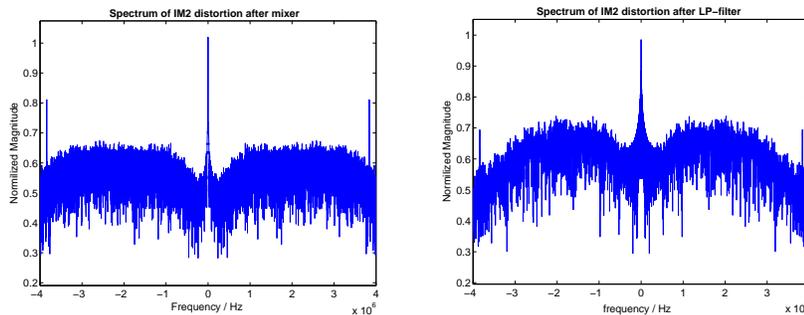


Figure 6.1: (a) Simulated distortion spectrum at the mixer output in the receiver caused by a TX-leakage signal with only one DPDCH channel. (b) Simulated distortion spectrum at the output of the analog base band filter caused by the same TX-leakage signal.

Sampled model of analog base band filter

It was described in the cancellation block design chapter that the *interference creation block* can be implemented in different ways. The first option, that also was used in the *first basic approach design*, was to implement a digital sampled model of the analog base band filter to

enclose the bandwidth of the interference signal and hence affect the interference in the same way as the low pass filter in the receiver.

A sampled model of the filter can be created at different sample rates. In figure 6.2 the frequency response and group delay for a fourth order digital Butter-worth filter, created at different sample rates, can be studied. If a low sample rate is used, i.e. two times the chip rate, there will be a difference in both frequency response and group delay. How this difference in filter frequency response and group delay will af-

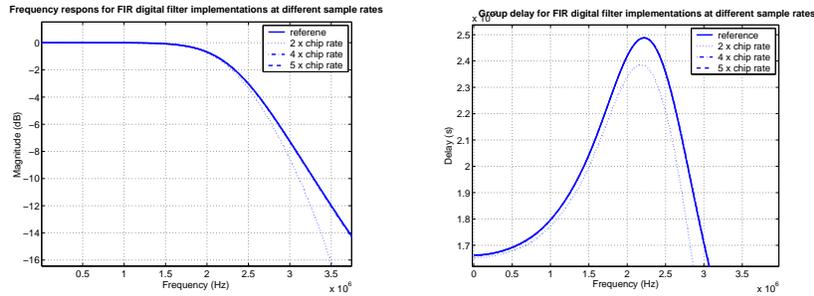


Figure 6.2: (a) Frequency response of a fourth-order Butter-worth lowpass filter. (b) The group delay for the same digital lowpass filter

fect the signal is depicted in figure 6.3 for sample rates of two times the chip rate and four times the chip rate. It can be seen that the created replica of the interference signal, even at low sample rates, overlaps the real interference in a good way. Notice that the difference between the signals is studied without added TX distortion and the observed difference is hence caused by the digital filter implementation only. In comparison to the TX distortion, this difference can be considered to be very small even at low sample rates.

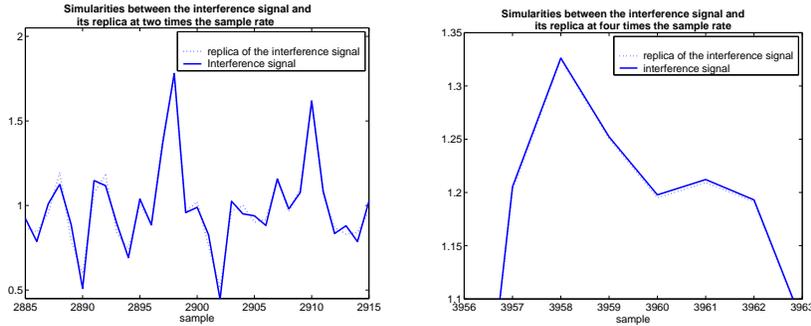


Figure 6.3: (a) Replica of interference signal created at two times the chip rate. (b) Replica of interference signal create at four times chip rate

If the sampled filter model is removed from the cancellation chain and replaced by a block that only adjusts for a mean group delay as described in section 5.1.4, the signals will differ a lot more. Figure 6.4 shows the interference replica, created at twice the chip rate and the real interference, with no added TX distortion. In figure 6.4 (a) the interference replica signal is not adjusted for any delay from the analog base band filter. In figure 6.4 (b) the signal is adjusted with a mean delay in the filter bandwidth as described in section 5.1.4. Hence, the

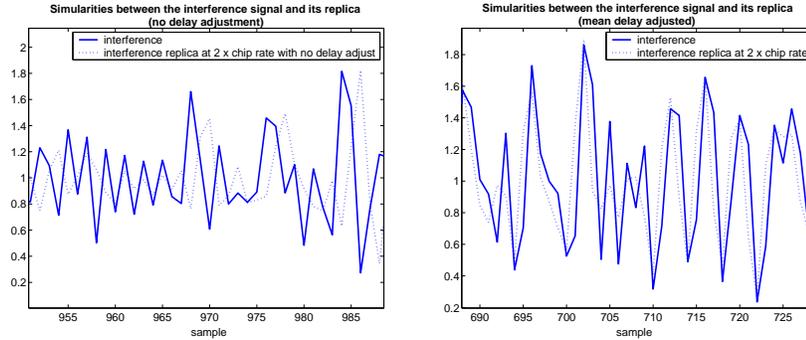


Figure 6.4: (a) Replica of interference without sampled Butter-worth filter in the *interference creation block*. (b) No digital Butter-worth filter in the cancellation chain, but the signal is adjusted with a mean delay.

simplification to substitute the sampled model of the analog base band filter with only a compensation of a mean delay will cause a larger difference between the signals. It can not yet be established if this difference plays an important roll for the LMS algorithm to perform well. This will be examined from a system point of view in section 6.1.5

6.1.4 Performance of the LMS Algorithm

In the previous section simulation results for the performance of the *interference creation block* was presented for two different design options. The influence of the sample rate on the replica of the interference signal was also investigated. In this section the simulation results will focus on the performance of the *adaptive filter block*.

Step-size investigation

The step-size (μ) is the only controllable parameter for the LMS algorithm. For a large step-sizes the LMS algorithm will converge faster but will also be more unstable. There exists a maximal value of the step-size when the LMS algorithm converges, this value can not be exceeded.

Figure 6.5 shows an example of the convergence with a step-size that is chosen close to the maximum value.

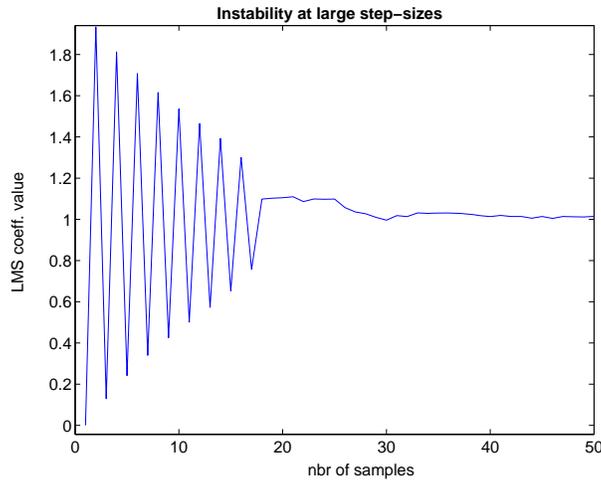


Figure 6.5: Convergence of the LMS-coefficient with a large step-size ($\mu=2$)

Chapter 5 contained a rule of thumb to calculate maximum step-size. In this example the mean power of the tap-input to the LMS algorithm was, in the simulator, calculated to

$$E\{|u(n)|^2\} = 0.086 \quad (6.1)$$

By using equation 5.3 (with $M=1$) the maximum step-size was estimated to 11.6. Actually the LMS algorithm was converging all the way up to μ approximately equal to 20, but with a transient distortion that was not reasonable. For step-sizes over 20 the LMS algorithm (in this example) will not converge. This confirms the assumption that estimation of the maximum step-size with the equations given in chapter 5 is only a coarse estimation. In reality the step-size parameter has to be chosen by a comfortable margin of at least 1/10 of the maximum value.

LMS Misadjustment

The misadjustment, defined in section 5.1.2, is a good measure of how well the LMS algorithm performs in a specific environment. The *ensemble-average-squared value*, i.e. an average value over an ensemble of adaptive filters, is plotted versus number of iterations. This simulation has been performed for three different interference test cases (-10 dB, 0 dB and 10 dB) and are shown in figure 6.6 to 6.8. A reference

level (J_{min}) is also included in the figures, indicating the squared error achieved if the LMS filter uses the optimal wiener coefficient values.

The figures (6.6 to 6.8) show the LMS convergence at start-up, that is, the convergence the very first time the cellular phone begins a data transmission. The cancellation block is, as described in chapter 5, in sleep-mode between two transmissions to reduce power consumption. Next time the cancellation block is enabled, i.e. before the next data transmission, two different design options are possible. The coefficient values for the I- and Q-channels can be saved between two data transmissions and the algorithm start therefore its updating process from this value and not from zero. Another option is to let the algorithm starts from zero every time and hence not implement more complexity in the algorithm. This is a simpler algorithm, with maybe satisfactory rate of convergence.

The principle idea with these three learning curves is to see whether the algorithm has the ability to converge in a single slot at start-up and to investigate its steady-state value. The LMS algorithm works at double chip rate in these simulations and one slot is therefore 5120 iterations.

It can be established that it is possible, in all three test cases, to converge in a single slot at start-up. The achieved misadjustment is however dependent of the interference magnitude and chosen step-size. Misadjustments for different step-sizes and test cases are summarized in table 6.1. These values give just a hint of how well the LMS algorithm performs for different interference magnitudes and step-sizes. With a low magnitude of the interference, the LMS algorithm has difficulties to, in a good way, estimate the coefficient. The misadjustment is therefore also relatively large.

It is not established that the algorithm must converge in one single slot at start-up, but the algorithm have at least the ability.

Table 6.1: Misadjustments, defined in section 5.1.2, for different step-sizes and three different test cases.

Test case	LMS step-size	Misadjustment
-10dB	0.05	63 %
	0.1	144 %
0 dB	0.005	10 %
	0.05	67 %
10 dB	0.0008	1 %
	0.05	73 %

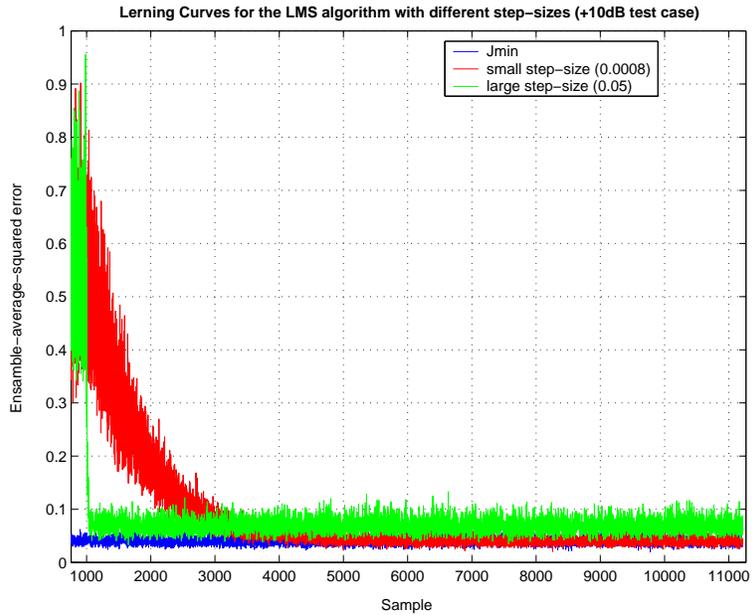


Figure 6.6: +10 dB test case. The algorithm is enabled after 1000 samples. A slot is 5120 iterations long and ends around sample 6000.

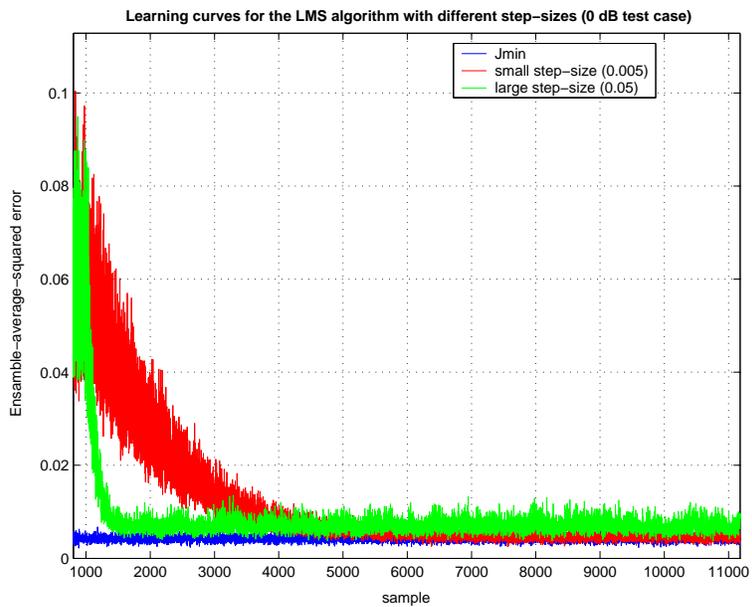


Figure 6.7: 0 dB test case. The algorithm is enabled after 1000 samples. A slot is 5120 iterations long and ends around sample 6000.

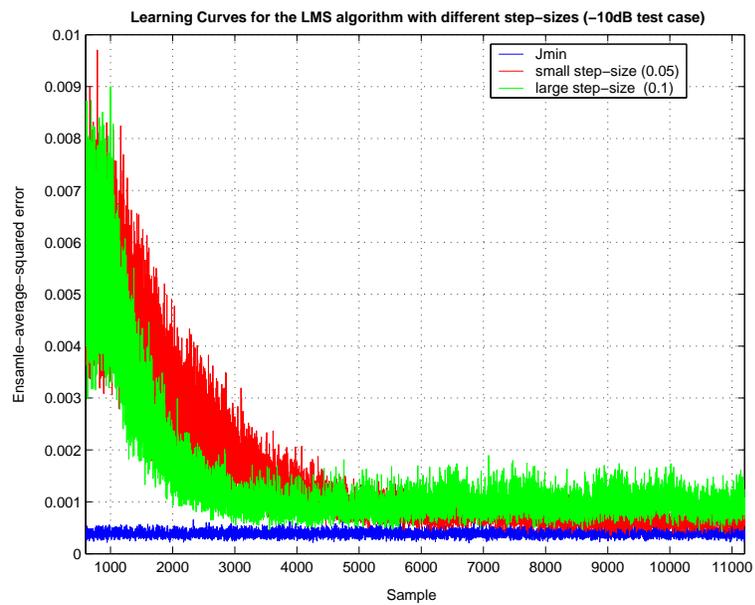


Figure 6.8: -10 dB test case. The algorithm is enabled after 1000 samples. A slot is 5120 iterations long and ends around sample 6000.

6.1.5 Performance of the Cancellation Block (System Simulations)

In the two previous sections, the subblocks in the cancellation chain have been examined individually. This has only indicated the limitations or the capacity of the two subblocks, but no simulations have yet been performed for the entire system.

This section will present two different kinds of system simulations; *a typical transmission scenario* and *evaluation of the system NDR* in the entire interference test interval. The first simulations are not only performed to investigate the ability of the cancellation block to suppress the interference, but also to illustrate the convergence of the LMS coefficients and the suppression of the squared error signal in every slot. This illustration makes it easier to understand that influence the LMS step-size has to the gradient noise and rate of convergence and put it in relation with the WCDMA slot time.

In the second section the system NDR is simulated versus the entire interference test interval. The system NDR is the *noise to distortion* ratio and is defined in section 6.1.1 This will be done for both different transmitter distortions as well as for different TX/RX paths delays to see their impact on the suppression. In section 6.1.3 the differences between the real interference and its replica at different sample rates and for two different design options was studied without telling anything about the impact on the system. These simulations will now also be performed at system level to show if these simplifications and changes concerning sample rate decrease the improvement of the system NDR.

Typical transmission scenario

One way to evaluate the performance of the cancellation block in the complete system is to simulate a realistic transmission scenario. This can be performed by a simulation over many WCDMA slots with different output power levels in every slot. Because the mobile phone change output power level in every slot this can be considered as a *typical transmission scenario*. It is assumed that the mobile phone already has established a connection with the strongest base station, i.e. the mobile phone is synchronized with a base station. The mobile phone can then estimate approximately path attenuation in the uplink if the base station output power is known, by measuring the received signal strength in a control channel [17]. With this information, the mobile phone can estimate necessary output transmission power. A mobile phone can hence be assumed, in the first slot, to send with an arbitrary output power effect less than P_{max} (equal 24 dBm in class 3).

Three ten slots scenarios are simulated with the output power changed in $\pm 1, \pm 2$ or ± 3 dB step and with an initial interference magnitude starting at an arbitrary chosen level in the test interval. The first scenario is a *fixed step-size scenario*, where the LMS algorithm is using a *fixed-step-size* in all slots. The step-size is chosen relatively large to ensure convergence in the first slot. The next approach is to use a much smaller step-size. The LMS algorithm will then not converge in the first slot. The third and last approach is to use different step-sizes in the first and following slots. The default step-size is also in this simulation chosen relatively large (to ensure convergence) and is then decreased in the second slot. The three simulated *ten slot scenarios* are

- A Fix step-size (large)
- B Fix step-size (small)
- C Variable-step size

Except for the step-size parameter, exactly the same settings are used in the three simulations. This includes a 5% added TX distortion and a 10 ns spreading in TX/RX path delay, earlier defined as NSC.

A. Fix large step-size

The simulation over ten WCDMA slots with different output power level and consequently also different interference magnitude is depicted in figure 6.9. It can further be seen in the figure that the cancellation block is turned on in slot 1 and that the LMS algorithm therefore starts its update process from the initial condition (zero). The output power is then randomly increased or decreased in every slot and the LMS algorithm tries to estimate the coefficient value. In this simulation a large step-size (0.05) is used with the advantage of quick convergence in the first slot, but with a large uncertainty in the estimation of the coefficient value.

B. Fix small step-size

Consider now figure 6.10 instead. If a smaller step-size is used the LMS algorithm can perform a better estimation of the coefficient value, but on the other hand is the rate of convergence much lower. The squared error is therefore not optimally suppressed in the first slots.

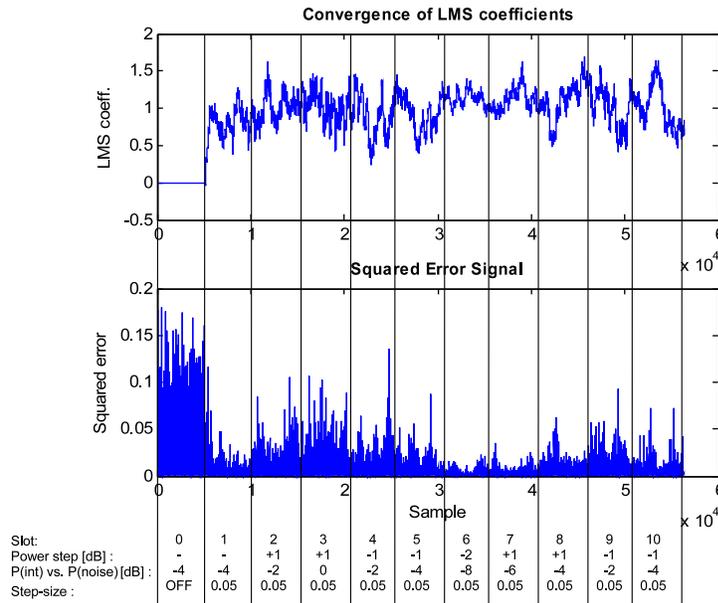


Figure 6.9: A typical data transmission scenario simulated over ten WCDMA slots with a large step-size (0.05).

C. Variable step-size

The optimal solution should be to use a large step-size in the first slot to ensure quick convergence and then decrease the step-size to much smaller value to not suffer from the large gradient noise in the following slots. Figure 6.11 shows the simulated *typical scenario* with two different step-sizes.

These three step-size scenarios have been simulated at two different power level intervals, but with the same power steps between each slot. The two power level intervals are itemed below.

- *Low interference interval:* The interference power versus the thermal noise power is in the interval -10 to 0dB.
- *High interference interval:* The interference power versus the thermal noise power is in the interval 10 to 20dB

Figure 6.12 shows the system NDR improvements during the two different power level intervals. The NDR is here calculated as a mean value in every slot for the three different step-sizes. A reference, simulated with the cancellation algorithm off, is added in the figure. It can be seen, in figure 6.12, that if the ratio between the interference power and the thermal noise is high (i.e. high interference interval) the

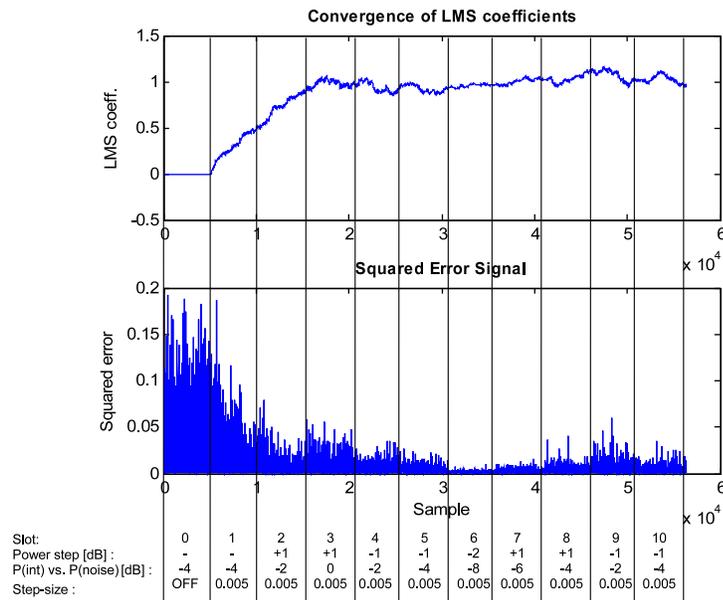


Figure 6.10: A smaller step-size minimize the gradient noise.

step-size do not have the same influence of the system NDR, as if the ratio is low (i.e. low power levels). At low power levels it can be clearly seen that the variable step-size combine the advantages with both the step-sizes. Since a mobile phone will transmit at both a low and a high interference interval, the solution with the variable step-size cannot be dismissed.

Evaluation of improvements in system NDR

Two aspects to further examine, is how the suppression of the interference (or improvement in system NDR) is dependent of different spreading in TX/RX path delay and different distortions in the uplink. These two imperfections are neither estimated nor measured by the cancellation block and will decrease the improvement.

Figure 6.13 - 6.15 shows simulations over 16 WCDMA slots with an interference magnitude starting at -10 dB and ending at +20 dB, i.e. covering the entire interference test interval in steps of 2 dB. Every NDR values are, in the figures, calculated as a mean value in every slot. The figures are only showing the improvement in system NDR after the LMS coefficients have converged, i.e. the suppression of the interference at start-up will not be concerned. Furthermore, a reference line is added to the figures to show the system NDR with a disabled

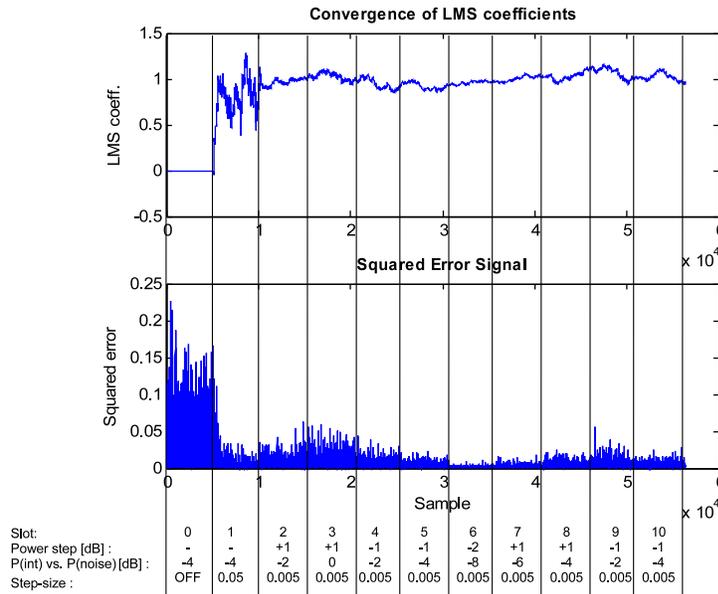


Figure 6.11: By using two different step-sizes it is possible to benefit of both quick convergence and small gradient noise.

cancellation block.

It is shown that the cancellation block can, even at very low interference levels (-10 dB) find the coefficients and provide suppression (or improvement in system NDR). It is reasonable, as described in section 4.2.3, to assume a 10 ns spreading in TX/RX path delay. The 50 ns spreading in delay can therefore be considered as a very large spreading and is more to indicate when the improvement of system NDR has been halved. The same simulations have also been performed for different uplink distortions and are shown in figure 6.14. Increasing distortion in the transmitter chain affect however the interference suppression (or improvement in system NDR) much more in comparison to the spreading in delay and with a very high distortion, the cancellation block will even decrease the NDR level. Anyhow, a 20% distortion in the transmitter chain is not reasonable and according to the 3GPP specification the distortion shall not exceed 17.5% in the uplink [13].

The starting point in the *first basic approach*, designed in chapter 5 was to create a replica of the base band interference that, at all costs, resembles the real interference as much as possible. A sampled model of the analog base band filter was therefore added in the cancellation path. In section 5.1.4, a design option was to remove this block and substitute it with a block that only compensates for a mean delay in

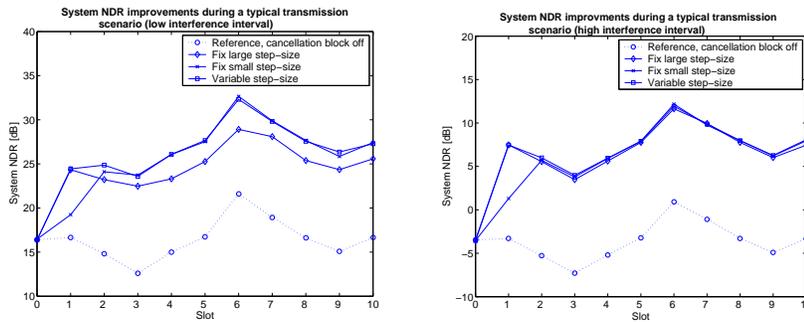


Figure 6.12: The improvement of the system NDR with an implemented cancellation block between the TX and RX chain in the transceiver. (a) Simulations in a the low interference interval. (b) Simulations in the high interference interval.

the filter. A larger difference between the real interference and its replica will then occur. This difference was studied in section 6.1.3 but it was never shown how much the reduction in hardware affected the improvement of the system NDR.

In figure 6.15, both a reference with the cancellation block off as well as a reference line showing the *first basic approach* design (FBA), simulated with a sample rate equal twice the chip rate, are added in the figure.

To increase the sample rate, in the cancellation block, and thus also increase the power dissipation does not improve the performance. It is sufficiently good to create the replica of the interference at twice the chip rate. The two curves in figure 6.15 will overlap each other.

Furthermore is it shown that the cancellation block still improves the system NDR without a sampled model of the analog filter, but no as good as with the sampled model of the filter in the chain. With a low sample rate (two times the chip rate) is it also harder to compensate for a mean filter group delay. Every sample shift in the delay block represents then a much longer time. If a higher sample rate, e.g. four times the chip rate, is used the delay compensation can rather exactly be set to the mean filter delay and the suppression of the interference is therefore also better.

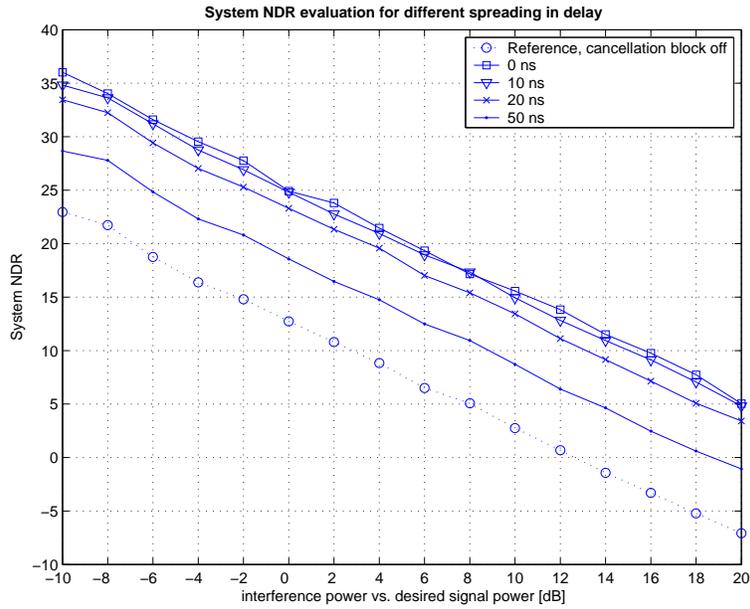


Figure 6.13: The impact of the system NDR with a spread in TX/RX path delay. Simulations are performed over 16 WCDMA slots with a fix 5 % TX distortion.

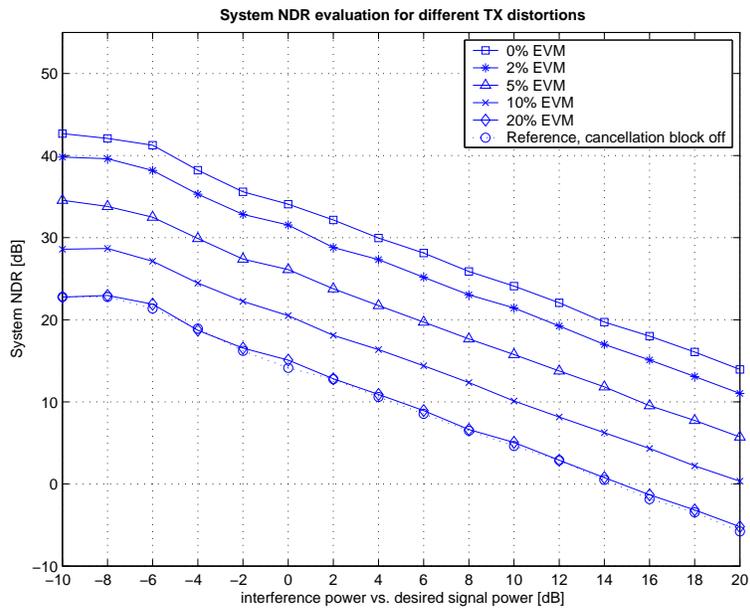


Figure 6.14: The impact of the system NDR with an increasing distortion in the transmitter. Simulations are performed over 16 WCDMA slots with a fix 10 ns TX/RX path delay

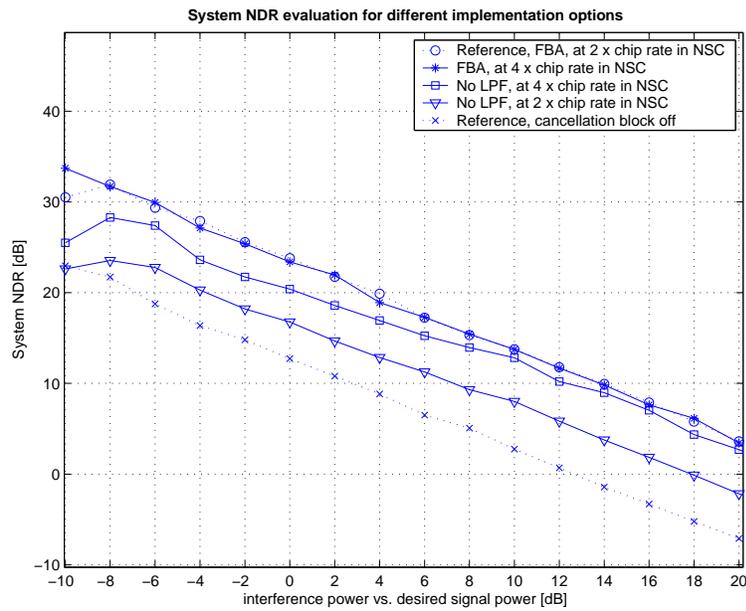


Figure 6.15: Simplifications in the cancellation chain results in decreased improvement. FBA is the abbreviation the first basic approach design and NSC is the abbreviation for normal simulation condition.

6.2 Measurement Results

Hardware measurement have been performed on a WCDMA transceiver ASIC with the purpose to examine the profile of the interference and to verify the functionality of the cancellation block.

The main idea was to recreate a similar environment that the transceiver ASIC is exposed for during data transmission, i.e. expose the receiver in the ASIC for the interference caused by the transceiver itself. The leakage signal from the LO is always present and must therefore not be generated. The TX leakage signal is on the other hand only present during simultaneously transmission and the simplest and also most controllable way to generate this signal is by an external signal generator.

The RF signal is generated with an SMIQ and connected, via a notch filter, to the LNA input of the receiver. The SMIQ is used to convert a base band information signal into RF frequency. The base band signal can be generated internally in the SMIQ or generated in matlab and transmitted to the SMIQ via an AMIQ. An AMIQ is a modulation generator (or I/Q source) which can be controlled by a computer. The measurement setup and all details can be studied in appendix B.

The purpose with this measurement was to examine the interference phenomena in the base band caused by the internal LO leakage and TX leakage signal. The frequency of the TX leakage signal should be set a duplex distance away from the LO frequency and with an amplitude level of approximately -25 dBm. Test conditions, instrument settings and ASIC register settings are further explained in appendix B.

If the linearity performance of the ASIC is sufficiently bad and the TX leakage signal, described above, is connected to the LNA input, an interference signal will arise in the base band. The information signal is a pure 50 kHz sinusoidal with an added DC offset, which will avoid the signal to become negative, and is expressed in equation 6.2 and also shown at the top of figure 6.16.

$$m(t) = 1 + \cos(\omega_m t) \quad (6.2)$$

This signal is modulated onto a RF carrier in the SMIQ and will then become a 100% amplitude modulated signal according to equation 6.3. The frequency of the carrier (ω_c) is set a duplex distance away from the frequency of the receiver LO, i.e. at the TX frequency.

$$s(t) = m(t) \cdot \cos(\omega_c t) = (1 + \cos(\omega_m t)) \cdot \cos(\omega_c t) \quad (6.3)$$

In chapter 3 the theory behind the profile of the base band interference was described and derived. The interference is a squared version of the information signal and with the information signal given in equation 6.2 the interference will contain the frequency components expressed in equation 6.4.

$$y_{BB,undesired}(t) = m^2(t) = (1 + \cos(\omega_m t))^2 = \frac{3}{2} + 2 \cdot \cos(\omega_m t) + \frac{1}{2} \cdot \cos(2\omega_m t) \quad (6.4)$$

The undesired signal contains a DC component, a component at the information frequency and a component at twice the information frequency. In figure 6.16 the interference is shown in the time domain, where the signal in the middle and the signal at the bottom is the base band interference signal in the I- and Q-channel respectively. The oscilloscope was set in average mode to give a clearer picture of the interference. Figure 6.17 is taken from the spectrum analyzer and shows the tone at the information frequency (ω_m).

Consider figure 6.16 again, the interference signal in the middle was sampled and recorded with the digital oscilloscope and plotted in matlab (figure 6.18). A cancellation signal was then created in the simulator, with the cancellation block described in chapter 5. Because of unknown external delays in different instruments etc, the cancellation signal was manually adjusted in time to overlap the real interference. The cancellation signal and how it converges against the optimal value is shown in figure 6.18. The suppression of the base band interference can be studied in figure 6.19. No desired signal was used in these measurements.

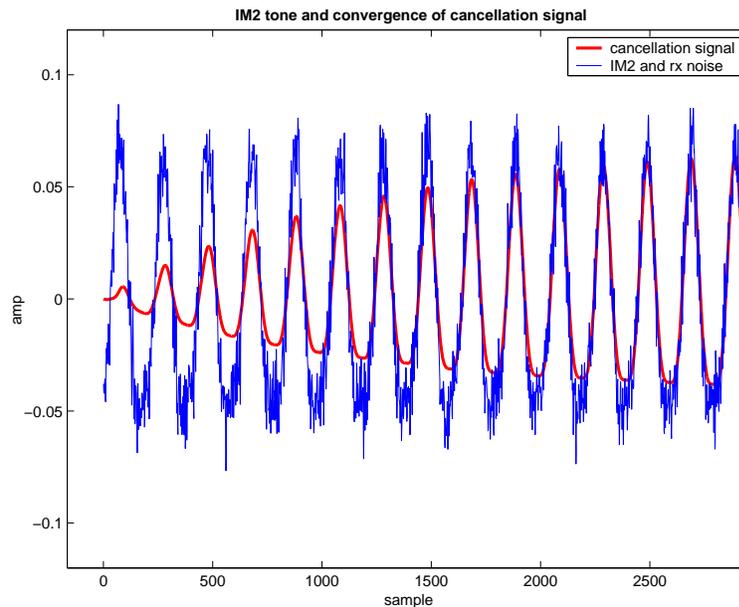


Figure 6.18: The blue signal is the sampled interference signal in the base band. The red one is the cancellation signal created in the simulator. Because the delay in the instruments etc are unknown, the cancellation signal is manually adjusted in time to overlap the real interference signal. Used step-size is 0.0001.

A created simulation model is always a simplification of the reality. No validity check has been possible to do of the implemented matlab model. Instead the interference profile has been verified and the ability of the cancellation block to create a similar replica of the interference. The performance of the cancellation block in a real situation, i.e. with a WCDMA modulated TX leakage signal, has not been examined. It can still be considered that the implemented LMS algorithm converges and that the squared error signal is suppressed.

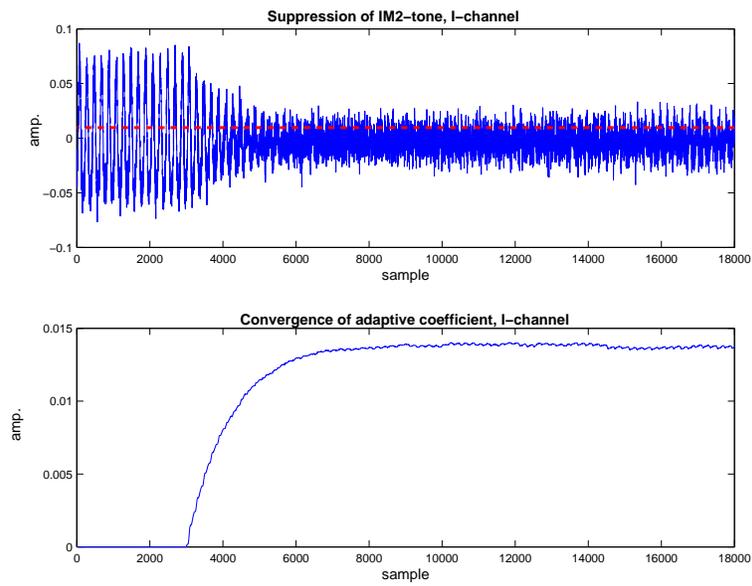


Figure 6.19: The interference signal is gradually suppressed after the cancellation block has been switch on. The red dash dotted line marks the standard derivation of the thermal noise (desired signal). Most of the interference is thus suppressed. Used step-size is 0.0001.

Conclusions and Future Work

7.1 Conclusion

The thesis presents a design of a cancellation algorithm to digitally suppress base band interference in a direct conversion WCDMA receiver. The cancellation block, placed in the digital domain between the transmitter and the receiver, has been designed around the well known adaptive least mean square (LMS) algorithm. It was, however, not in advance established that the LMS algorithm would provide sufficient performance, especially concerning its rate of convergence and steady-state value. If the performance is satisfactory, the LMS can with advantage be implemented in hardware.

Simulations have pointed out that the improvement of the cancellation block is not limited by the choice of the LMS algorithm. Instead, the algorithm provides both sufficiently good rate of convergence and a low misadjustment, with a proper chosen step-size parameter. The algorithm has, according to simulations, the ability to converge to its estimated optimal value in less than a single WCDMA slot. This is true even at start-up if the algorithm starts its convergence from initial values equal zero.

The main limitation in improvement by using a cancellation block is determined by the distortion in the transmitter uplink. This is an imperfection that is neither estimated nor measured by the cancellation block. The task of the cancellation block is to create a replica of the interference that as much as possible resemble the real interference. Simulations have further shown that it is enough to determine a nominal delay between the interference and its created replica and compensate with this delay in the cancellation block. The spreading in delay between different transceiver ASICs will affect the improvement, but not at all as much as the distortion in the uplink.

An implemented cancellation block can use different sample rates,

but there is no gain in creating the replica of the interference at a sample rate higher than two times the chip rate. From power dissipation point of view a sample rate equal twice the chip rate should therefore be used to create the replica of the interference.

Even if the uplink distortion is the dominating imperfection it is still important to carefully choose proper simplifications in the cancellation block. Badly chosen simplifications will directly influence the improvement by using this cancellation block.

7.2 Future Work

Since this Master Thesis just is a first research of a cancellation algorithm at system level, there are still some future works to consider. The step-size is the only controllable parameter for the algorithm and more work is needed concerning step-size optimization. All simulations have been performed in floating-point simulator environment and quantization effects must further be examined. Since the distortion in the transmitter is the main limitation of the improvement, more studies in this area are needed. Another future work is to optimize the cancellation block, i.e. to create a replica of the interference at lower hardware cost.

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Weakly Nonlinear Frequency Components of a Two Signal Excitation

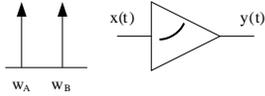


Figure A.1: Two signal excitation of a weakly nonlinear amplifier

Assume the amplifier in figure A.1 to be a weakly nonlinear amplifier, approximated by a third order Taylor serie extension according to equation A.1. Table A.1 contains all frequency components at the output of the amplifier if the input signal is a combination of two sinusoidal signals according to equation A.2.

$$y(t) = k_1 x(t) + k_2 x(t)^2 + k_3 x(t)^3 + \dots \quad (\text{A.1})$$

$$x(t) = A \cos(\omega_A t + \varphi_A) + B \cos(\omega_B + \varphi_B) \quad (\text{A.2})$$

Table A.1: Tones at the output of a weakly nonlinear block.

Frequency, ω	Phase, φ	Factor	Type
0	0	$\frac{1}{2}A^2k_2 + \frac{1}{2}B^2k_2$	DC
$\omega_B - \omega_A$	$\varphi_B - \varphi_A$	ABk_2	IM2
$2\omega_A - \omega_B$	$2\varphi_A - \varphi_B$	$\frac{3}{4}A^2Bk_3$	IM3
ω_A	φ_A	$Ak_1 + \frac{3}{4}A^3k_3 + \frac{3}{2}AB^2k_3$	Fundamental
ω_B	φ_B	$Bk_1 + \frac{3}{4}B^3k_3 + \frac{3}{2}A^2Bk_3$	Fundamental
$2\omega_B - \omega_A$	$2\varphi_B - \varphi_A$	$\frac{3}{4}B^2Ak_3$	IM3
$2\omega_A$	$2\varphi_A$	$\frac{1}{2}A^2k_2$	HD2
$\omega_B + \omega_A$	$\varphi_B + \varphi_A$	ABk_2	IM2
$2\omega_B$	$2\varphi_B$	$\frac{1}{2}B^2k_2$	HD2
$3\omega_A$	$3\varphi_A$	$\frac{1}{4}A^3k_3$	HD3
$2\omega_A + \omega_B$	$2\varphi_A + \varphi_B$	$\frac{3}{4}A^2Bk_3$	IM3
$\omega_A + 2\omega_B$	$\varphi_A + 2\varphi_B$	$\frac{3}{4}B^2Ak_3$	IM3
$3\omega_B$	$3\varphi_B$	$\frac{1}{4}B^3k_3$	HD3

Measurements

B.1 Measurement settings

The measurements were performed on a WCDMA transceiver ASIC with the following settings.

Test condition:

Operating band:	II
Duplex distance:	80MHz
Temperature:	25°C

WCDMA receiver settings:

LO frequency:	1930 MHz
RX PGA:	maximum

Jammer settings (TX leakage):

Jammer carrier frequency:	1850 MHz
Modulated signal frequency:	50 kHz
Power level:	-24dBm

B.2 Measurement setup

The test connection in figure B.1 was used in all measurements. The jammer signal was connected to the LNA input (high band, band II) and the interference was studied at the output of the analog base band filter. Three different instruments were used to examine the interference; a digital oscilloscope, a spectrum analyzer and a vector analyzer. All instruments were synchronized with a 10 MHz reference signal taken from the ASIC via a PLL-card. The registers in the ASIC and the input signal to the AMIQ were both controlled by a computer.

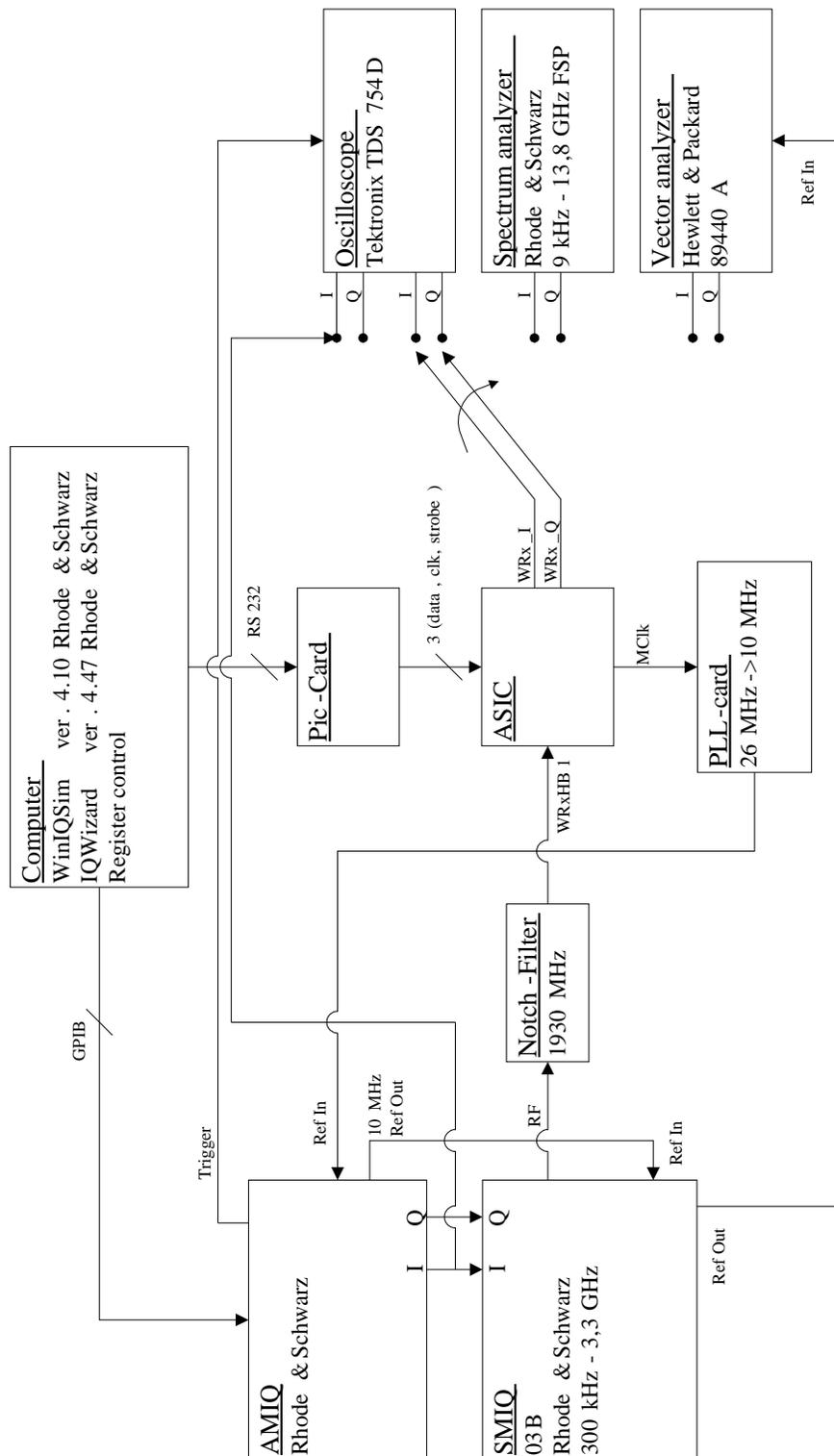


Figure B.1: Block diagram of the measurement setup.