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REJTANG - Industriangepassad Programmeringsenhet

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<i>Abstract</i> <p>As a result of microcomputers becoming less costly, they are often used for quite specialized tasks. In control and measurement applications a few commands are used frequently. This has created a demand from industry of designing their keyboards with big keys for GO, STOP etc. It is not possible to connect such a keyboard directly to a computer i.e. an interface is needed. Rejtang is such an interface, that can be programmed from the computer to give the various keys their functions dynamically during execution.</p>			
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REJTANG:

Industri anpassad
Programmeringsenhet

Examensarbete av
Sverre Palmquist
utfört för
Rejlers Ingenjörbyrå

Handledare: Gustaf Olsson

Abstract:

Som ett resultat av att microdatorerna har sjunkit i pris, används datorerna ofta till väldigt specialicerade uppgifter. Vid styr och mätapplicationer använder man få olika kommandon frekvent. Detta har skapat ett behov från industrin att själv kunna bygga sitt "tangentbord", med stora tangenter/ knappar för t.ex GO, NÖDSTOPP osv. Det är inte möjligt att ansluta ett sådant tangentbord direkt till en dator utan det behövs ett mellanled , ett interface. Rejtang är ett sådant interface, som kan programmeras från datorn för att de olika tangenterna skall få sin funktion. Det är möjligt att omdefiniera funktionen för sitt tangentbord mjukvarumässigt via datorn, och detta kan ske dynamiskt under programmets gång.

As a result of microcomputers becoming less costly, they are often used for quite specialized tasks. In control and measurement applications a few commands are used frequently. This has created a demand from industry of designing their keybords with big keys for GO, STOP etc. It is not possible to connect such a keyboard directly to a computer i.e. an interface is needed. Rejtang is such an interface, that can be programmed from the computer to give the various keys their desired function. It is also possible to redefine their functions dynamically during execution.

Innehållsförteckning:

1	INLEDNING	1
2	KRAVSPECIFIKATION, SYFTE	2
3	FUNKTIONSBESKRIVNING, REALTIDS ASPEKTER	3
	3.1 Funktionsbeskrivning	3
	3.2 Processgraf	4
	3.3 Processbeskrivning	5
	3.4 Monitorer, beskrivning	6
	3.5 Flödesschema huvudloop	7
4	HANDHAVANDE BESKRIVNING	8
	4.1 Allmänt	8
	4.2 Samanfattning	10
	4.3 Exempel	11
5	LITTERATURFÖRTECKNING	13

APPENDIX

A.	Listor och dess uppbyggnad.	
B.	Ingående moduler, samt deras rutiner.	
C.	Programlistor	
	Initsio	1
	Rejinter	7
	Skrstr	12
	Rejinit	15
	Rejhead	19
	Rejcmd	25
	Rejlex	36
	Listor	39
	Rejstruc	46
	Omvandl	51
	Rejdef	55
	Test	58
	Listtest.	61
D.	Länkningsförfarande	

E. Schema hårdvara

F. Datablad ingående komponenter

SN75172 . . .	1
SN75173 . . .	6
SN75176 . . .	11
LM78XX . . .	19
LM78LXX . . .	22
LM317 . . .	28
SN74LS245 . . .	36
SN74LS273 . . .	38
SN74LS06 . . .	41

G. Defaultvärden

Inledning:

I olika styr och reglerprogram har det funnits ett behov av att kunden själv utformar sin programmeringspanel. Då de lite klena standard-tangentborden inte alltid klarar den tunga miljö som kan vara aktuell. Det finns därför ett behov att kunna bygga upp en panel som är specialgjord för sin uppgift.

Vanligtvis används ett mindre PC-system för att sköta en process. När detta är datorns huvudsakliga uppgift, används få kommandon ofta. Ett flertal av Rejlers kunder har därför gjort förfrågningar om en möjlighet att själva bygga sin panel. De kontaktdon som kunderna vill använda går inte att ansluta direkt till datorn, utan kräver ett interface.

Examensarbetet har gått ut på att bygga detta interface samt göra den programmering som är nödvändig. Stommen är en standard enkortsdator (1004-10 från Dataindustrier) som kompletteras med ett framtaget in/ut-kort för anslutning av kontakter. För den seriella kommunikationen mot datorn är ett TTL till RS485 interface framtaget. (se appendix E)

Rejtang är således ett programmerbart interface mot datorn. Det finns möjlighet att fördefiniera 64 st tryck-knappspunkter.

Under utvecklingen av Rejtang byggdes en betydande flexibilitet in i systemet från start, genom att samtliga rutiner är skrivna för största möjliga generalitet. Det finns bl.a ett omfattande paket för listhantering, som ej utnyttjas till fullo för närvarande. Denna inbyggda överkapacitet möjliggör en enkel utbyggnad av programvaran med nya faciliteter.

Syfte:

Att utveckla den erforderliga elektronik och programvara som behövs till en kontrollenhet för en i industri uppbyggd programmerings panel.

Enheten skall innehålla kompletta funktioner för att ansluta ett koordinatsystem av tangenter, (som via seriell kommunikation via datorn), kan programmeras för valfri funktion.

Anslutningen från enhet till yttre kontakter sker genom att kortsluta en punkt mellan två kopplingslistor på TANG, den ena med beteckning A-H och den andra 1-8. Detta ger 64 olika kombinationer. Tex A1, A2, A3, A4 H8.

Dessa olika kontaktpunkter skall kunna programmeras för att ge valfri asciisträng (1 -> 128 st tecken) sänd på en seriell kanal till dator, samt med möjlighet att välja valfri individuell repetitions hastighet.

TANG skall eliminera kontaktstuds inverkan, samt undertrycka yttre störningar.

Via TANG enheten skall även en uppsättning på 8 st utgångar för anslutning av yttre lysdioder, kunna tändas respektive släckas via kommando från dator.

Kravspecifikation:

- digitala ingångar för att avkänna minst 40 st kontaktpunkter
- 8 st digitala utgångar för lysdioder
- unik ascii kod för varje kontaktpunkt
- Om flera kontaktpunkter aktiveras samtidigt skall motsvarande ascii koder sändas direkt efter varandra.
- då en tryckknapp hållits intryckt under en viss tid autorepeteras sändningen av ascii-koden.
- enheten skall kunna ta emot kommandon från datorn via seriekanal för att ändra parametrarna för:
 - vilken ascii kod som genereras för vilken tangent
 - vilka tryckknappar skall kunna auto repetera
 - vilken frekvens för autorepetitionen
 - vilka lysdioder skall vara tända
- elektriska gränssnittet skall vara RS485

Funktionsbeskrivning

Vid uppstart av Rejtang initieras de erforderliga I/O kretsarna på CPU-kortet. Default värden till tangentlistan och timing ställs upp (se appendix G). Tangentlistan är en slags data-area som översätter tangent-koordinaten till teckenkod. Efter denna initiering ställer sig Rejtang i Huvudloopen där den scannar av tangent för tangent genom att lägga ut en rad, och läsa motsvarande kolumn i tangentkoordinat-systemet. När samtliga element i listan har testats ställer sig Huvudloopen och väntar på ett klockavbrott. Testet innehåller t.ex fråga om tangenten är nedtryckt, om den är aktiverad eller om autorepetition skall startas. Detta klockavbrott, som kan ha skett innan varvet är färdigt, tillåter en "varv räknare" att räknas upp. Varvräknarens uppgift är att se till att inga ackumulerade tidsfel uppstår. Denna varvräknare sköter timingen för kontaktstuds osv. Syftet med varvräknaren är att nedtryckning av två eller fler tangenter alltid skall ge samma följd av svar. Klockans funktion är att få timingen oberoende av antalet tangenter som är inlagda i listan.

Om tangentlistan har ändrats börjar varvet om direkt utan att avsluta resterande tangenter. Det element som påbörjats slutförs dock.

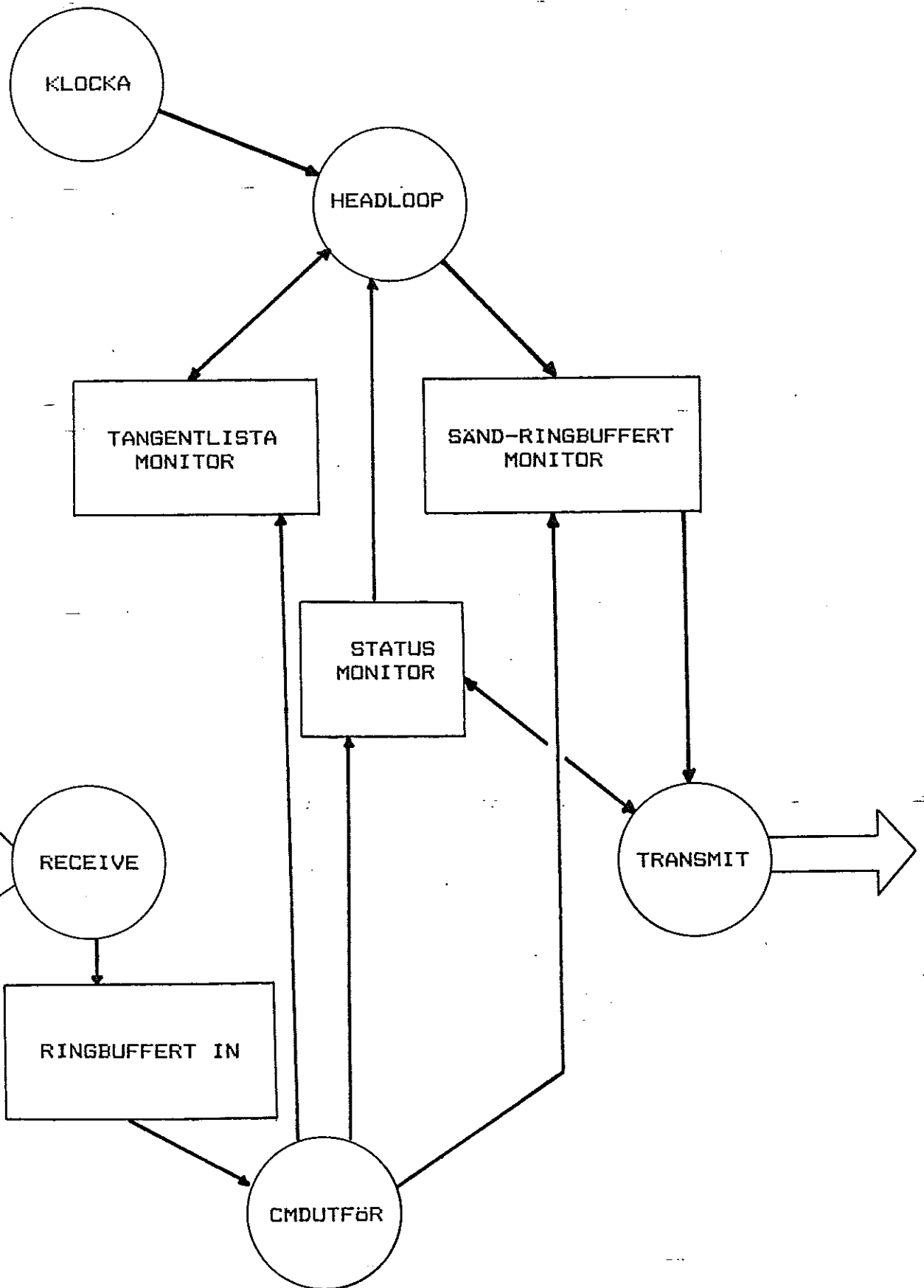
Vid tangentnedtryckning, som varat tillräckligt länge för att motsvarande teckenkod skall skrivas ut, kallar Huvudloopen på en rutin (Skrstr) som arbetar mot en monitor (Sänd-ringbuffert). Informationen i tangentlistan kopieras över till Sänd-ringbufferten. Mot denna monitor arbetar sedan en process (Transmit) som skriver tecknen ett och ett till datorn. Detta sker under ömsesidig uteslutning. De olika specialfallen: buffert full / buffert tom tas om hand i rutinerna. Skulle bufferten vara full ställs anropet att vänta på en händelse för att därefter se om plats finns.

När Rejtang programmeras, uppnås ömsesidig uteslutning genom att varje kommandosträng som sänds till Rejtang, kvitteras med en statusbit. Därefter är Rejtang redo att ta emot ett nytt kommando. Det förutsätts att ingen aktivitet sker mot tangentkoordinaterna under programmeringen från värddatorn.

Om kommandot innebär att en tangent omdefinieras kommer detta att indikeras i en programstatus flagga. Detta medför sedan att Huvudloopen ej hämtar nästa element i listan utan startar från början av listan igen.

För närmare kännedom om dessa förlopp refereras till process-grafen på nästa sida, programlistor samt appendix C.

Processgraf :



Processbeskrivning REJTANG:

Rejtang består av fem processer, vilka är:

Klocka:

En egen process som räknar upp en variabel Time, denna variabel sköter tîmingen för Huvudloopen.

Huvudloop:

Här sker den egentliga tangentbordsavkodningen, med hjälp av en länkad lista *) där all erforderlig information ligger. Huvudloopen talar med en rutin Skrstr som är en monitor till processen Transmit som sänder de tecken som blivit inlagda i monitorn.

*) listan och dess uppbyggnad är beskriven i app. A.

Receive:

En egen process som tar emot ett tecken från den seriella ingången och lägger detta i en ringbuffert. Denna ringbuffert används endast till Receive. Om tecknet är ett avslutningstecken (här valt CHRØ(0)) sker ett hopp till en process Cmdutför (se nedan) som avkodar det kommando som valts, samt utför vad som begärts. Efter varje avslutad kommando sträng svarar Rejtang alltid med en ascii byte mellan 0 -> 9 (se handhavande beskrivning). Detta ger den erforderliga handskakningen. Buffertens storlek är vald till 140 tecken, men ändras enkelt i modulen Rejdef. (app. C)

Transmit:

Fristående process som sänder det som är inlagt i en Sänd-ringbuffert (monitor). Information fylls in till Sänd-ringbufferten via rutinen Skrstr. (se prog.lista) När Sänd-ringbufferten är tom, stängs rutinen av och väntar på en händelse via rutinen Skrstr, som återigen startar Transmit. Om ringbufferten är full vid anropet från Skrstr, inväntas en händelse. Ett nytt försök att lägga in tecken görs, ända till alla tecken är skrivna in till Sänd-ringbufferten.

Cmdutför:

Avkodar den kommando sträng som sänts till Rejtang samt utför det som begärts enligt syntax specificationen. Rejcmd "svarar" alltid med en statusbit *) om hur begärt kommando har utförts. Denna statusbit är en ascii-siffra mellan 0 och 9, 0 motsvarar allt väl och talen 3 till 9 något fel. Rejcmd fyller och ändrar i den länkade lista som Huvudloopen använder.

*) statusbiten beskriven på sid 8.

Monitörer

Rejtang använder sig av fyra stycken monitorer.

Tangentlista, monitor:

Här finns all information om de individuella tangenterna, deras repetitionstid, vilka tecken dom representerar osv. Mot denna monitor arbetar processerna Cmdutför och Huvudloop, Cmdutför lägger in nya definitioner samt ändrar i gamla definitioner. När en ny definition har infogats indikeras detta i en status monitor, se nedan. För att ej få Realtidsproblem med denna monitor, börjar alltid Huvudloopen om från början i Tangentlistan efter att ett element har blivit raderat från monitorn. I annat fall tillåts Huvudloopen att fortsätta med de eventuellt nya värdena.

Status monitor:

Här finns information om lysdiodernas status, (ställes i Cmdutför och läses från Huvudloop). Det finns även information om Sänd-ringbuffert monitorn (se nedan). Monitorn består av två bytes:

- 1) Diodstat som direkt motsvarar tända/ släckta lysdioder.
- 2) Progstat där de ingående bitarna innebär:

bit 0 = 0 -> Ny uppstart
bit 1 = 0 -> Tx interrupt pending avstängd
bit 2 = 0 -> Sänd-ringbuffert är tom
bit 3 ej använd
bit 4 = 1 -> Begärd reset
bit 5 ej använd
bit 6 = 0 -> listan är ändrad
bit 7 ej använd

De fyra lägsta bitvikterna nollställs vid initieringen. De fyra högsta bitarna blir oförändrade vid initiering.

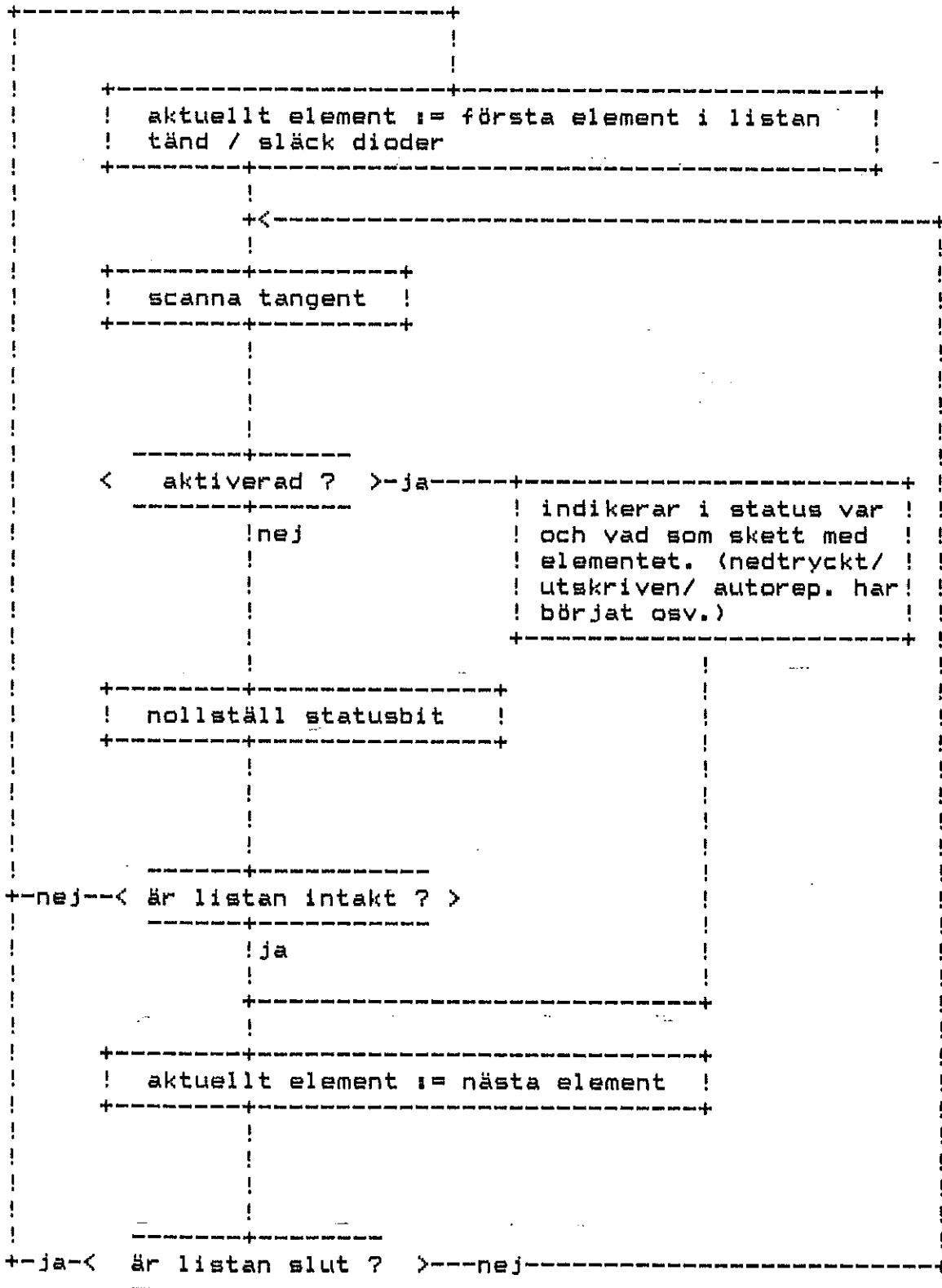
Sänd-ringbuffert monitor:

Monitor där utbufferten till sändrutinen (Transmit) finns. Mot denna monitor jobbar rutinen Skrstr (beskriven i appendix B) och processen Transmit. Skyddad genom ömsesidig uteslutning.

Ringbuffert-in:

Här läggs de indata som kommer via processen Receive. Efter avslutat kommando använder Cmdutför kommandosträngen som finns här. Detta utan att kopiera den till en arbetsarea. Ringbuffert-in skyddas genom handskakning mot värddatorn.

Flödesschema huvudloop



Handhavandebeskrivning:

Programmeringsrutinerna mot Rejtang består av tre delar:

- 1) Kommando för lysdioder
- 2) Modifiering av tangenter
- 3) Generella kommando

Generellt avslutas alla kommandon med ett specialtecken som är det enda som inte kan ingå i tangentbordets teckenuppsättning. Här är det valt till chrØ(0). ChrØ(0) kan alltså ej lämnas från Rejtang. Rejtang svarar alltid med ett tal mellan 0 och 9 efter ett avslutat kommando. Denna siffra skickas över som en byte med ascii värdet för motsvarande siffra. Innebörden av de olika svaren är följande:

Kvittens svar efter avslutat kommando:

kvittens svar

0	ALLT OK
1	- (ej definierad)
2	BEGÄRD RESET

fel meddelande:

3	MINNES BRIST, KOMMANDO EJ UTFÖRT !
4	TANGENT SAKNAS I LISTAN
5	RANGE ERROR ASCII STRÄNG
6	RANGE ERROR TANGENT A1 -> H8
7	RANGE ERROR LYSDIOD 1 -> 8
8	FÖRVÄNTAD SIFFRA UTEBLIVEN
9	OKÄNT KOMMANDO

Svarsalternativ 2 ges endast efter begärd reset, eller eventuellt efter spänningstillslag. Vilket beror på att minnescellernas starttillstånd är slumpmässiga.

För lysdiodernas:

Tänd / Släck diod.

För att tända en diod sänder man en ascii-sträng till Rejtang bestående av "L:" + diodnummer avslutat med en chr(0). På motsvarande vis släcker man med "U:" + diodnummer.

För tangentlistan:

Här finns all information om de individuella tangenternas status.

- 1) lägga in information om en ny definition för tangent.
- 2) ändra information på en redan existerande tangent.
- 3) aktiverad tangent
- 4) deaktiverad tangent

I samtliga fall refereras tangenten med sin koordinatplats, dvs A-H + 1-8. ex A1 .. H8, först anges bokstav och därefter siffra.

Initialvärde vid uppstart.

Vid uppstart av Rejtang har alla kontakt-koordinaterna ett defaultvärde. Det är autorepetition med ca 60 ms intervall samt tecken 0 till 0 för A1 -> H8. (Se appendix G för specifikation.)

Ny definition.

När man lägger till en ny definition raderas den existerande definitionen ur listan samt den nya läggs sist. Detta innebär att efter många omdefinieringar kommer minnet att fyllas. Om detta leder till att minnet blir fullt svarar Rejtang 3, minnesbrist. Vid försök att lägga in ytterligare tangentdefinitioner. För att undvika detta bör man tömma minnet vid nydefiniering av hela tangentbordet. Detta beskrivs i avsnittet om generella kommandon.

Ändra i definition.

Kommandot för att ändra definitionen tillåter att asciisträng samt repetitions hastighet ändras. Ett absolut krav är att asciisträngen ej är längre än den tidigare definierade. I defaultlistan är samtliga tangenters definition inställda på en ascii längd av ett tecken. Skulle den nya strängen vara längre än den som tidigare definierats kommer Rejtang svara med 5, range error ascii.

Aktivera / Deaktivera tangent.

Det finns möjlighet att "stänga av" en tangent temporärt med strängen "D:" + tangentkoordinat. Detta för att vissa alternativ inte alltid skall vara möjliga i alla lägen. För att åter "sätta på" tangenten används "A:" + tangentkoordinat. Dessa kommandon ändrar inget av definitionerna i övrigt.

Generella kommandon:

Initiering av defaultlista.

- 1) "RESET", som används för att nollställa allt i Rejtang. Samt att lägga upp defaultvärdena inkl defaultlistan.

Tömma tangentlista.

- 2) Kommandot "R:" innebär att tangentlistan töms och används för att tömma tangentlistan och tillgodogöra sig minnesutrymmet igen. OBS ! Efter detta kommando töms även defaultvärdena, vilket innebär att inga tangenter finns definierade !

Ändra default tider.

- 3) Kommando för att ändra tiderna för kontaktstuds elimination, och tiden för att autorepetitionen skall starta. Detta används som "T:" + kontaktstuds eliminationstid + start till autorepetitionstid, varje enhet motsvarar ca 0.01 sek Defaulttiderna är "T:2 60" och behöver normalt inte ändras.

Sammanfattning: Kommando till Rejtang

För Lysdioder:

"L:1"+chr(0)	Tänd diod 1
"U:1"+chr(0)	Släck diod 1

För tangentlista:

"F:A1 50 YES"+chr(0)	Definiera tangent A1 med YES och en repetitionstid på ca 500 millisekunder
"C:A1 50 NO"+chr(0)	Omdefiniera tangent A1 till NO.
"D:A1"+chr(0)	Deaktivera tangent A1
"A:A1"+chr(0)	Aktivera tangent A1

Generella kommando:

"RESET"+chr(0)	Töm alla definitioner, återlämna använt minne
"R:"+chr(0)	Tömmer tangentlistan
"T:3 60"+chr(0)	Ändra kontaktsudstiden till ca 3 millisekunder, auto-repetition startar efter 600 millisekunder,

Exempel

L(ight) : 1 -> 8

tänder lysdiod 1 -> 8

ex. "L:5" chrØ(0)

U(nlight) : 0 -> 7

släcker lysdiod 0 -> 7

ex. "U:5" chrØ(0)

F(ill) : koordinat repeat "asciisträng"

Definiera en tangent i tangentlistan

ex "F:A1 12 RUN"+chrØ(0)

=> Om tangent A1 trycks ner sänds "RUN" till datorn

C(hange) : koordinat repeat "asciisträng"

Byter innehåll i existerande lista. OBS
ascii får ej vara längre än vad som tidigare
definierats med F(ill)

ex. "C:A1 12 A"+chrØ(0)

=> Byter RUN mot A i existerande lista.
repeat är det samma som tidigare.

D(eactivate) : koordinat

Stänger av motsvarande tangent utan att
förstöra informationsblocket, vilket innebär
att ingenting händer om motsvarande tangent
trycks ner.

ex "D:A5"+chrØ(0)

A(ktivate) : koordinat

Aktiverar motsvarande tangent (används efter
det att den blivit avstängd via kommandot
deactivate)

ex "A:A5"+chrØ(0)

RESET:

Mjukvarumässig reset för TANG, nollställer
allt som tidigare definierats. Ställer samt-
liga värden till default.

ex. "RESET" chrØ(0)

R:

Tömmer defaultlistan för tangenter, och
återlämnar använt minne. Efter detta komman-
do finns ingen tangent definierad.

ex. "R:"+chrØ(0)

T(iming) kontaktstudselimination & autorepetitions-start

Definierar tidsparametrar.

ex. "T:3 60"+chrØ(0) (se föregående sida)

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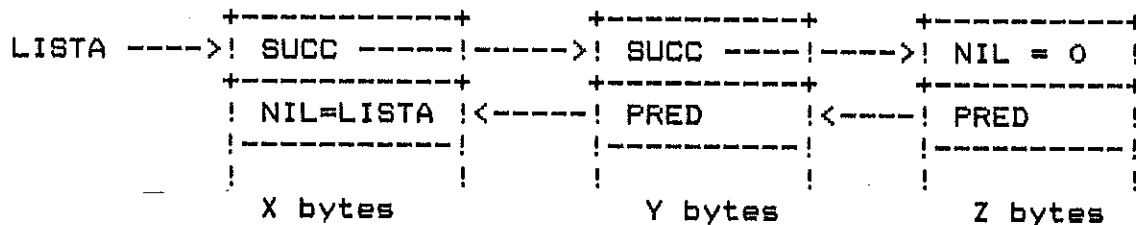
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Listor och dess uppbyggnad i TANG:

Globala variabler är:

BOTRAM
TOPRAM

Start på ledigt ram minne
Slut på ledigt ram minne



Listans uppbyggnad framgår av ovanstående figur. Variabeln LISTA pekar på det första elementet i listan, och de två första byten pekar på nästa element. Listans sista element indikeras av SUCC pekaren = 0. De två efterföljande byten pekar på föregående element. Efter dessa två tvåbytespekare ligger data enligt nedan spec storlekarna X, Y och Z behöver inte vara lika stora, vilket ger dynamisk storlek på varje listelement.

Sista elementet i listan pekar på NIL, vilket är identiskt med att vidarepekaren = 0.

Första elementets PRED pekare pekar på NIL, vilket motsvarar att det pekar på sig själv.

I dokumentationen kommer representationen av ett listelement vara en 16 bitars adress, en pekaren, följt av en punkt samt variabelnamnet. Ex: ett element i en lista heter pek, nästa element i denna lista är pek.succ.

Succ och Pred är de enda fördefinierade variabelerna i liststrukturen, dessa måste ligga först och uppta två bytes var. Om en variabel följs av ett stort L eller H betyder det låg respektive hög byte i en adress. ex: pek.succL & pek.succH

Tangent-listan i TANG:

TANGLIST	ADR:
SUCC	TANGLIST
PRED	TANGLIST+2
STATUS	TANGLIST+4
TG	TANGLIST+5
REPEAT	TANGLIST+6
COUNT	TANGLIST+7
ANT. ASCII	TANGLIST+8
ASCIISTRANG	TANGLIST+6

För att använda listor skapas ett listhuvud vid assemblering-
en genom att reservera två 2 bytes pekare, som skall peka till
NIL. (se appendix C, modul REJDEF)

För att sedan använda denna lista användes de subrutiner som
beskrivs på följande sidor. Ett nytt listhuvud skall ej skapas
dynamiskt, utan endast nya element i redan existerande listor.

Rutiner för listor:

NEW(storlek,pek)

Skapar ett tomt listelement i minnet

IN: BC : storlek (antal bytes, att reservera)
UT: DE : adress till reserverat element, pek
Returnerar carry=1 om minnesbrist

HEAD(pek)

Ger carry=1 om pek pekar på listhuvudet

IN: DE : pek
UT: oförändrat

INLAST(pek,lista) Läger elementet pek sist i listan lista

IN: DE pek
HL lista
UT: oförändrat

LAST(pek)

Hämtar sista element i listan

IN: DE pek
UT: DE sista element

FIRST(pek)

Hämtar första element i listan

IN: DE pek
UT: DE första element

DEL(pek,lista)

Tar bort elementet pek ur listan lista, om pek inte
finns i lista händer ingenting.

IN: DE pek
HL lista
UT: oförändrat

LSUCC(pek)

Hämtar nästa element i listan

IN: DE pek
UT: DE pek.succ carry=0, om pek.succ <> NIL
annars DE oförändrat carry=1

LPRED(pek)

Hämtar föregående element i listan

IN: DE pek
UT: DE pek.pred carry=0, om pek.pred <> NIL
annars DE oförändrat carry=1

Modulbeskrivning:

Programpaketet är uppdelat i 11 st filer, där varje fil har ett modulnamn. Modulnamnet är skrivet med svart stil, och de ingående subrutinerna med understruken stil:

INITSIO

Initierar IO-kretsarna Z80-SIO och Z80-CTC på CPU kortet.

REJINTER

Interruptrutinerna som ingår vid kommunikationen samt den egna processen klocka

RECEIVE: Tar emot enligt tidigare

TRANSMIT: Sänder enligt tidigare

TRANS: Startar processen transmit

KLOCKA: Klockprocess

EXTSTAT: Skall normalt aldrig anropas, felrutin, nollställer felflaggan

SPRXCOND: Skall normalt aldrig anropas, felrutin, nollställer felflaggan

SKRSTR

Talar med sänd-ringbufferten, genom ömsesidig uteslutning.

SKRSTR: lägger in BC (register uppsättning i CPU) tecken till sänd-ringbuffert-monitorn. Från adress som register HL pekar på. Väntar på ledigt utrymme om buffert full.

REJINIT

Initieringsmodul, initierar nödvändiga minnesvariabler samt lägger upp defaultlistan för tangenter

- INITMEM: Initierar minne samt lista
- INDEFALT: Lägger upp defaultlistan, se appendix B, för tangenter.
- RESLISTA: Tömmer tangentlistan

REJLEX

Sköter avkodningen av kommando mot en tabell, tabellen är uppbyggd som kommando, skiljebit+rutin-nummer Returnerar rutinnummer som svar. Om man skall lägga till eller ta bort något kommando görs detta genom att ändra i tabellen enligt programlista.

- REJLEX: Kommandoavkodningsrutin, returnerar reg A=rutin nummer A=0 innebär att rutinen saknas i lista.

REJCMD

Kommando avkodningsrutiner, samt vissa hjälprutiner

- CMDUTFÖR: Kallar på lexscan som avkodar kommando samt utför begärt kommando
- ERRO,.. ERR9: Skriver statusbyte
- SKIPBLANK: Läser förbi blanka i en sträng
- SIFFRA: Returnerar i reg A=tal som HL pekar på eller om det ej är en siffra carry=1
- GRÄNS: Kollar om $1 < A < 9$ om så är fallet returnera carry=0 annars carry=1.
- TANGENT: Packar upp tangent från ex A1 till 1, samt gör en kontroll av riktighet, om tangent inom rätt intervall returneras A= tangentnummer och carry=0 annars carry=1
- BINBIT: Binär till Bit konvertering, in reg A=bitnummer en byte i A med med binummer A satt till 1. ex. in: A=2 ut A=4 (00000100), bit 2=1
- COUNTSTR: Räknar antalet tecken i sträng fram till endbyte, returnerar A = antalet tecken, ändrar ej buffert.

LISTOR

- Listpaket, se separat beskrivning

REJDEF

Innehåller alla minnesvariabler som används i hela REJTANG. Här definieras ringbufferternas storlek.

REJSTRUC

Innehåller strukturen för tangentlistan

READLIST: Packar upp elementet reg. DE pekar på, till minnesvariabler. Detta används vid kommando F:(ill) och C:(hange)

WRITELIST: Packar ner minnesvariabler till element i listan.

FINDTG: Letar i tangentlistan efter tangent-nr som finns i reg A. Returnerar reg DE som pekar på element, vid lyckad sökning, samt carry=0. Fanns ej tangenten returneras carry=1 vilket motsvarar att tangent saknas i listan.

OMVANDLA

Innehåller omvandlingsmoduler

DECBIN: Decimalt till binärt, returnerar A=tal som HL pekar på HL pekar efter anrop på först byte <> från siffra. Siffran måste vara mindre än 255.

BINDEC: Binärt till decimal omvandling, omvandlar register A till decimalt och lägger in detta som tre bytes i buffert. HL pekar på buffert, A innehåller tal att omvandla. Vid retur pekar HL på första lediga byte efter omvandlat tal.

BIN2DEC: Motsvarande BINDEC, men två bytes tal som läggs i DE vid anrop.

Den egentliga huvudloopen. Svarar på eventuell begärd reset och ställer sig därefter i en oändlig loop. Där den går igenom tangentlistan steg för steg, och ställer motsvarande rad låg och avläser kolumn för att se om tangent är nedtryckt. Huvudloopen syncar sig själv varje varv genom att vänta på händelse vilket motsvarar att klockan ökat med ett. Detta för att nedtryckning av två eller fler tangenter skall ge samma följd av ascii tecken beroende på ordningen de trycktes ner. Genom att ha olika repeat kan man uppnå en repetition som består av valfritt antal av det ena samt ett av det andra tecknet som autorepeteras.

- HEADLOOP: Initierar head1, samt svarar vi begärd reset.
- HEAD1: Egentliga huvudloopen, väntar på sync samt går igenom tangentlistan en gång.
- LOOP: Elementloop här går elementen igenom ett och ett, när listan är slut går den upp till Head1
- AKTIVERAD: Hopp hit om tangent är nedtryckt. Kontrollerar om tangenten är aktiverad och därefter om den var nedtryckt förra varvet. Om nedtryckt förra varvet görs hopp till nedtryck. Annars indikeras "nedtryckt förra varvet" i tangentens statusbit.
- NEDTRYCK: Kollar om tangenten är utskriven, i så fall görs ett hopp till ejutskr. Annars kontrolleras om den skall skrivas ut (har det gått tillräckligt med tid för att eliminera kontaktstuds) Därefter indikeras att den är utskriven en gång, under förutsättning att den skrevs ut.
- EJUTSKR: Kollar om autorepetitionen har börjat om så är fallet hopp till autorep. Annars kollas om autorep skall starta. Är repeat = 0 görs ingen autorepetition, är repeat <> 0 kollas om det är tid för att autorepetition skall börja. Då skrivs motsvarande element ut samt det indikeras att autorepetition har startat.
- AUTOREP: Kollar om det är dags för att autorepetera igen.
- CLEAR: Nollställer status för tangent, anropas varje gång en tangent ej är nedtryckt.
- OKEJ: Skriver ut element, via skrstr.
- DIFFTIME:- Returnerar antalet varv "sedan sist"

Modulernas beroendeMODUL INITSIO.ASM

EXTERNA RUTINER
 EXTERNAL INITMEM, HEADLOOP
 EXTERNAL RECEIVE, TRANSMIT, KLOCKA
 EXTERNAL EXTSTAT, SPRXCOND

EXTERNA DATA
 EXTERNAL STACK

GLOBALA PORTADRESSER & KONSTANTER
 GLOBAL SIOADTA, SIOACMD, ENDBYTE, RESET

MODUL REJINTER.ASM

EXTERNA DATA
 EXTERNAL IBPEKIN, IBSTART, IBEND
 EXTERNAL UBPEKUT, UBSTART, UBEND, UBANTAL
 EXTERNAL SIOADTA, SIOACMD
 EXTERNAL TIME, PROGSTAT

EXTERNA KONSTANTER
 EXTERNAL ENDBYTE

EXTERNA RUTINER
 EXTERNAL CMDUTF8R, HEADLOOP

GLOBALA RUTINER
 GLOBAL RECEIVE, TRANSMIT, TRANS, KLOCKA
 GLOBAL EXTSTAT, SPRXCOND

MODUL SKRSTR.ASM

EXTERNA DATA
 EXTERNAL UBPEKIN, UBSTART, UBEND, UBANTAL
 EXTERNAL PROGSTAT

EXTERNA RUTINER
 EXTERNAL TRANS

GLOBALA RUTINER
 GLOBAL SKRSTR

MODUL REJINIT

GLOBALA RUTINER
 GLOBAL INITMEM, RESLISTA

EXTERNA DATA
 EXTERNAL TGLISTA, TGPRED, PEK
 EXTERNAL BOTRAM, STARTRAM
 EXTERNAL UBPEKIN, UBPEKUT, UBSTART, UBANTAL
 EXTERNAL IBPEKIN, IBPEKUT, IBSTART
 EXTERNAL TIME, XSTR, PROGSTAT, DIODSTAT
 EXTERNAL STRANG, TG, STATUS, REPEAT, ANTAL
 EXTERNAL STUDS, AUTOR

EXTERNA RUTINER
 EXTERNAL NEW, INLAST, WRITELIST

MODUL REJHEAD

EXTERNA RUTINER

EXTERNAL HEAD, LSUCC, BINBIT
EXTERNAL SKRSTR, ERR2

EXTERNA DATA

EXTERNAL TGLISTA, PEK
EXTERNAL VARV, TIME, PROGSTAT, DIODSTAT
EXTERNAL STUDS, AUTOR

EXTERNA KONSTANTER

EXTERNAL XSTATUS, XTG, XREPEAT, XCOUNT, XANTAL, XSTR

GLOBALA RUTINER

GLOBAL HEADLOOP

MODUL REJCMD

EXTERNA RUTINER

EXTERNAL LEXSCAN, SKRSTR, DECBIN, BINDEC
EXTERNAL NEW, INLAST, DEL, WRITELIST, READLIST
EXTERNAL SKRORD, FINDTG, LSUCC, LPRED
EXTERNAL LAST, FIRST, REGLISTA, RESET

GLOBALA RUTINER

GLOBAL CMDUTFÖR, BINBIT, ERR2

EXTERNA DATA

EXTERNAL BUFFERT, ENDBYTE, XSTR
EXTERNAL SUCC, PRED, STATUS, TG, REPEAT, COUNT, ANTAL
EXTERNAL TGLISTA, PEK, STRANG, DIODSTAT
EXTERNAL STUDS, AUTOR, PROGSTAT

MODUL REJLEX

GLOBAL RUTINER

GLOBAL LEXSCAN

MODUL LISTOR.ASM

EXTERNA DATA

EXTERNAL BOTRAM

GLOBALA RUTINER

GLOBAL NEW, DEL, INLAST, LSUCC, LPRED
GLOBAL LAST, FIRST, HEAD

MODUL REJSTRUC.ASM

GLOBALA RUTINER

- GLOBAL WRITELIST, READLIST, FINDTG

GLOBALA KONSTANTER

GLOBAL XSUCCL, XSUCCH, XPREDL, XPREDH, XSTATUS, XTG, XREPEAT
GLOBAL XCOUNT, XANTAL, XSTR

EXTERNA DATA

- EXTERNAL SUCC, PRED, STATUS, TG, REPEAT, COUNT, ANTAL
EXTERNAL TGLISTA, STRANG

MODUL OMVANDL.ASM

GLOBALA RUTINER

GLOBAL DECBIN, BINDEC, BIN2DEC

MODUL REJDEF.ASM

GLOBALA DATA

GLOBAL STACK

GLOBAL IBPEKIN, IBPEKUT, IBSTART, IBEND

GLOBAL UBPEKIN, UBPEKUT, UBSTART, UBEND, UBANTAL

GLOBAL BUFFERT

GLOBAL BOTRAM, STARTRAM

GLOBAL SUCC, PRED, STATUS, TG, REPEAT, COUNT, ANTAL, STRANG

GLOBAL TGLISTA, TGPRED

GLOBAL PEK, TIME

GLOBAL VARV, STUDS, AUTOR, PROGSTAT, DIODSTAT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000			1	ZPROB INITSIO.ASM
0000			2	*PAGE 60
			3	;
			4	; EXTERNA RUTINER
			5	EXTERNAL INITMEM, HEADLOOP
			6	EXTERNAL RECEIVE, TRANSMIT, KLOCKA
			7	EXTERNAL EXTSTAT, SPRXCOND
			8	;
			9	;
			10	; EXTERNA DATA
			11	EXTERNAL STACK
			12	;
			13	; GLOBALA PORTADRESSER & KONSTANTER
			14	GLOBAL SIOADTA, SIOACMD, ENDBYTE, RESET
			15	;
			16	;
			17	*****
			18	;
			19	;
			20	;
			21	INIT, INITIERAR SIO SANT SKÖTER AVBROTTSHANTERINGEN
			22	ALL IN OCH UTMÄTNING MOT V24-SNITT
			23	;
			24	;
			25	;
			26	VER DATUM SIGN BESKRIVNING
			27	1.0 850925 SP
			28	;
			29	;
			30	*****
0000			31	;
	0000		32	ENDBYTE EQU 0
			33	;
			34	;
			35	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			36	;
			37	; ***** DEFINITIONER *****
			38	; PORTAR
			39	; *****
0000		0039	40	SIOACMD EQU 57
0000		003B	41	SIOBCMD EQU 59
0000		0038	42	SIOADTA EQU 56
0000		003A	43	SIOBDTA EQU 58
			44	;
0000		0030	45	CTCOCMD EQU 48
0000		0032	46	CTC2CMD EQU 50
0000		0033	47	CTC3CMD EQU 51
			48	; INSTALLNING AV CTC2 FÖR BAUDRATE
			49	; *****
0000		0001	50	BAUD9600 EQU 1
0000		0002	51	BAUD4800 EQU 2
0000		0004	52	BAUD2400 EQU 4
0000		0008	53	BAUD1200 EQU 8
0000		0010	54	BAUD600 EQU 16
0000		0020	55	BAUD300 EQU 32
			56	; INSTALLNINGAR SIO
			57	; *****
			58	; REG 1
			59	; *****
0000		0002	60	ENTXINT EQU 2 ; ENABLE TX INTERRUPT
0000		0004	61	STAFVEKT EQU 4 ; STATUS AFFECT VECTOR
0000		0018	62	INTALLRX EQU 24 ; INTERRUPT ON ALL RX
			63	; REG 3
			64	; *****
0000		0000	65	RX5BIT EQU 0 ; ANTAL DATABITAR MOTTAGNING
0000		0040	66	RX6BIT EQU 64
0000		0080	67	RX7BIT EQU 128
0000		00C0	68	RX8BIT EQU 192
0000		0020	69	AUTOEN EQU 32 ; AUTO ENABLE
0000		0001	70	RXENABLE EQU 1 ; ENABLE RX
			71	; REG 4
			72	; *****
0000		0004	73	STOP1 EQU 4 ; ANTAL STOPBITAR
0000		0008	74	STOP15 EQU 8
0000		000C	75	STOP2 EQU 12
0000		0000	76	NOPARI EQU 0 ; INGEN PARITET
0000		0003	77	JAMNPARI EQU 3 ; JÄMN PARITET, KONTROLL
0000		0001	78	UDDAPARI EQU 1 ; UDDA PARITET, KONTROLL
0000		0000	79	X1 EQU 0 ; SYSTEM KLOCKA DIVIDERAT MED.
0000		0040	80	X16 EQU 64
0000		0080	81	X32 EQU 128
0000		00C0	82	X64 EQU 192
			83	; REG 5
			84	; *****
0000		0000	85	TX5BIT EQU 0 ; ANTAL BITAR SÄNDNING
0000		0040	86	TX6BIT EQU 64
0000		0020	87	TX7BIT EQU 32
0000		0060	88	TX8BIT EQU 96
0000		0080	89	DTRUT EQU 128 ; DTR SIGNAL UT
0000		0002	90	RTSUT EQU 2 ; RTS SIGNAL UT
0000		0008	91	TXENABLE EQU 8 ; ENABLE SÄNDNING
			92	;
			93	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
0000	F3		94	RESET DI	
0001	X 310000		95	LD SP,STACK	
			96	;	
0004	ED5E		97	IN 2	
0006	AF		98	XOR A	
0007	ED47		99	LD I,A	
0009	C32800		100	JP CLR	
			101	;	
000C		0010	102	ORG 010H	
0010	8000		103	INTVEKT DEFW EIRETII	; CHANNEL B
0012	8000		104	DEFW EIRETII	
0014	8000		105	DEFW EIRETII	
0016	8000		106	DEFW EIRETII	
			107	;	
0018	7700		108	DEFW TRANSA	
001A	X 0000		109	DEFW EXTSTAT	; EXTERNAL STATUS
001C	7A00		110	DEFW RECEIWEA	
001E	X 0000		111	DEFW SPRXCOND	; ERROR
			112	;	
0020	8000		113	CTCINT DEFW EIRETII	
0022	8000		114	DEFW EIRETII	
0024	8000		115	DEFW EIRETII	
0026	7D00		116	DEFW KLOCK	
			117	;	
0028		0028	118	CLR EQU *	
0028	0606		119	LD B,6	
002A		002A	120	CLRDAISY EQU *	
002A	C08100		121	CALL RETII	
002D	10FB		122	DJNZ CLRDAISY	
			123	;	
002F	D339		124	OUT SIOACMD,A	; VXLJ REGISTER 0
0031	D33B		125	OUT SIOBCMD,A	
0033	3E18		126	LD A,018H	; RESET CHANNEL
0035	D339		127	OUT SIOACMD,A	
0037	D33B		128	OUT SIOBCMD,A	
			129	;	
0039	0605		130	LD B,5	; VXNTA PA SID
003B		003B	131	DELAYI EQU *	
003B	10FE		132	DJNZ DELAYI	
			133	;	
003D		003D	134	INITSIO EQU *	
003D	216B00		135	LD HL,SIOVEKT	
0040	0608		136	LD B,SIOB-SIOA	
0042		0042	137	ISIOA EQU *	
0042	7E		138	LD A,(HL)	
0043	D339		139	OUT SIOACMD,A	
0045	23		140	INC HL	
0046	10FA		141	DJNZ ISIOA	
0048	0604		142	LD B,SIOSLUT-SIOB	
004A		004A	143	ISIOB EQU *	
004A	7E		144	LD A,(HL)	
004B	D33B		145	OUT SIOBCMD,A	
004D	23		146	INC HL	
004E	10FA		147	DJNZ ISIOB	
			148	;	
			149	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			150	;
			151	;
0050	3E17		152	LD A,23 ; INITERING AV CTC
0052	D332		153	OUT CTC2CMD,A ; =====
0054	3E01		154	LD A,BAUD9600 ; CTC 2 F8R BAUDRATE
0056	D332		155	OUT CTC2CMD,A
			156	;
0058	3E20		157	LD A,CTCINT ; INITERUPTVEKTOR
005A	D330		158	OUT CTC0CMD,A ; TILL CTC 0
			159	;
			160	LD A,0A5H ; CTC3 F8R KLOCKAVBROTT
005C	3EA5		161	OUT CTC3CMD,A ; ENABLE INT, PRESCALL=255
005E	D333		162	LD A,07DH ; TIMEKONSTANT = 125
0060	3E7D		163	OUT CTC3CMD,A
0062	D333		164	;
0064	X CD0000		165	CALL INITHEM
			166	;
0067	FB		167	EI
0068	X C30000		168	JP HEADLOOP
			169	;
			170	;
006B		006B	171	SIOVEKT EQU *
006B		006B	172	SIOA EQU *
006B	0444		173	DEFB 004H,X16+STOP1+NOPARI
006D	011A		174	DEFB 001H,INTALLRX+ENTXINT
006F	0568		175	DEFB 005H,TXBBIT+TXENABLE
0071	03C1		176	DEFB 003H,RXBBIT+RXENABLE
0073		0073	177	SIOB EQU *
0073	0104		178	DEFB 001H,STAFVEKT
0075	0210		179	DEFB 002H,INTVEKT
0077		0077	180	SIOSLUT EQU *
			181	;
			182	;
			183	;
0077		0077	184	TRANSA EQU *
0077	X C30000		185	JP TRANSMIT
			186	;
			187	;
007A		007A	188	RECEIVEA EQU *
007A	X C30000		189	JP RECEIVE
			190	;
			191	;
007D		007D	192	KLOCK EQU *
007D	X C30000		193	JP KLOCKA
			194	;
			195	;
0080		0080	196	EIRETII EQU *
0080	FB		197	EI
0081		0081	198	RETII EQU *
0081	ED4D		199	RETI
			200	;
0083	00 0000		201	END RESET

ERRORS : 0 WARNINGS : 0

ASHZ-4.46 INITSIO.ASM
CROSS REFERENCE LISTING

ERRORS: 0 12:00:00 86-02-24 PAGE 5

SYMBOL	LOCATION	DECL	REFERENCES	-----						
?AUTOEN	0020	69								
?BAUD1200	0008	53								
?BAUD2400	0004	52								
?BAUD300	0020	55								
?BAUD4800	0002	51								
?BAUD600	0010	54								
BAUD9600	0001	50	154							
CLR	0028	118	100							
CLRDaisy	002A	120	122							
CTC0CMD	0030	45	158							
CTC2CMD	0032	46	153	155						
CTC3CMD	0033	47	161	163						
CTCINT	0020	113	157							
DELAY1	003B	131	132							
?DTRUT	0080	89								
EIRETII	0080	196	103	104	105	106	113	114	115	
>ENDBYTE	0000	32	14							
ENTXINT	0002	60	174							
<EXTSTAT	0000	7	109							
<HEADLOOP	0000	5	168							
<INITMEM	0000	5	165							
?INITSIO	003D	134								
INTALLRX	0018	62	174							
INTVEKT	0010	103	179							
ISIOA	0042	137	141							
ISIOB	004A	143	147							
?JAMNPARI	0003	77								
KLOCK	007D	192	116							
<KLOCKA	0000	6	193							
NOPARI	0000	76	173							
<RECEIVE	0000	6	189							
RECEIVEA	007A	188	110							
>RESET	0000	94	14	201						
RETI	0081	198	121							
?RTSUT	0002	90								
?RX5BIT	0000	65								
?RX6BIT	0040	66								
?RX7BIT	0080	67								
RX8BIT	00C0	68	176							
RXENABLE	0001	70	176							
SIOA	006B	172	136							
>SIOACMD	0039	40	14	124	127	139				
>SIOADTA	003B	42	14							
SIOB	0073	177	136	142						
SIOBCMD	003B	41	125	128	145					
?SIOBDTA	003A	43								
SIOSLUT	0077	180	142							
SIOVEKT	006B	171	135							
<SPRXCOND	0000	7	111							
<STACK	0000	11	95							
STAFVEKT	0004	61	178							
STOP1	0004	73	173							
?STOP15	0008	74								
?STOP2	000C	75								
TRANSA	0077	184	108							
<TRANSMIT	0000	6	185							
?TX5BIT	0000	85								
?TX6BIT	0040	86								
?TX7BIT	0020	87								
TX8BIT	0060	88	175							

ASHZ-4.46 INITSIO.ASM

ERRORS: 0 12:00:00 86-02-24 PAGE 6

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES
TXENABLE	0008	91	175
?UDDAPARI	0001	78	
?X1	0000	79	
X16	0040	80	173
?X32	0080	81	
?X64	00C0	82	

```

LOCATION PLC CODE  ARB  LC  SOURCE STATEMENT -----
0000  00          1      ZPROG REJINTER.ASM
0000          2      *PAGE 60
3      ;
4      ;
5      ; EXTERNA DATA
6      EXTERNAL IBPEKIN, IBSTART, IBEND
7      EXTERNAL UBPEKUT, UBSTART, UBEND, UBANTAL
8      EXTERNAL SIDADTA, SIDACMD
9      EXTERNAL TIME, PROBSTAT
10     ;
11     ;
12     ; EXTERNA KONSTANTER
13     EXTERNAL ENDBYTE
14     ;
15     ;
16     ; EXTERNA RUTINER
17     EXTERNAL CMDUTF6R, HEADLOOP
18     ;
19     ;
20     ; GLOBALA RUTINER
21     GLOBAL RECEIVE, TRANSMIT, TRANS, KLOCKA, PUT
22     GLOBAL EXTSTAT, SPRXCOND
23     ;
24     ;
25     ;
26     ; *****
27     ;
28     ; REJINTER, INTERUPTRUTINER
29     ;
30     ; RECEIVE - TERMINAL IN
31     ; TRANSMIT- TERMINAL UT
32     ; KLOCKA - KLOCKA (CTC3)
33     ;
34     ;
35     ; VER  DATUM  SIGN  BESKRIVNING
36     ; 1.0  851117  SP    -
37     ; 1.1  860101  SP    EXTSTAT, SPRXCOND
38     ; 1.2  860113  SP    UBANTAL, ANTAL TECKEN I UTBUFF
39     ; 1.3  860115  SP    SKRSTR, FLYTTAD TILL EGEN MOD.
40     ;
41     ; *****
42     ;
0000  0028  43  RTIP  EQU  02BH  ; RESET TX INT PENDING
0000  0001  44  RI    EQU  001H  ; REGISTER 1
0000  0030  45  ER    EQU  030H  ; ERROR RESET
0000  0010  46  RESI  EQU  010H  ; RESET EXT/STAT INT
47     ;
48     *EJECT

```

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
0000	00	0000	49	RECEIVE EQU *	
0000	F5		50	PUSH AF	; RÄDDA REGISTER
0001	E5		51	PUSH HL	
0002	D5		52	PUSH DE	
			53		
0003	X DB00		54	IN A,(SIDADTA)	; LAS TECKEN
			55		
0005	X ED5B0000		56	LD DE,(IBPEKIN)	; LÄGG TKN I BUFFERT
0009	12		57	LD (DE),A	
			58		
000A	13		59	INC DE	; UPPGRADERA BUFFPTR
000B	X 210000		60	LD HL,IBEND	
000E	A7		61	AND A	
000F	ED52		62	SBC HL,DE	
0011	00 2003		63	JR NZ,BB1	
0013	X 110000		64	LD DE,IBSTART	
0016	X ED530000		65	LD (IBPEKIN),DE	
			66		
001A	X FE00		67	CP ENDBYTE	; COMMANDO STRANG FÄRDIG ?
001C	00 CA2500		68	JP Z,STRREADY	
001F	D1		69	POP DE	
0020	E1		70	POP HL	
0021	F1		71	POP AF	
0022	FB		72	EI	
0023	ED4D		73	RETI	
			74		
0025	00	0025	75	STRREADY EQU *	
			76		
0025	00 CDC400		77	CALL EIRETII	
0028	C5		78	PUSH BC	; RÄDDA RESTEN AV REGISTER
0029	DDE5		79	PUSH IX	
			80		
002B	X 210000		81	LD HL,IBSTART	
002E	X CD0000		82	CALL CHDUTFBR	
			83		
0031	X 210000		84	LD HL,IBSTART	
0034	X 220000		85	LD (IBPEKIN),HL	
			86		
0037	DDE1		87	POP IX	
0039	C1		88	POP BC	
003A	D1		89	POP DE	
003B	E1		90	POP HL	
003C	F1		91	POP AF	
003D	FB		92	EI	
003E	ED4D		93	RETI	
			94		
			95	*EJECT	

ASMZ-4.46 REJINTER.ASM

ERRORS: 0 12:00:00 86-02-24 PAGE 3

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT		
0040	00	0040	96	PUT	EQU *	; SKRIVER TECKEN I A TILL SID
0040	X D300		97	OUT	SIOADTA,A	
0042	X 3A0000		98	LD	A,(PROGSTAT)	
0045	CBCF		99	SET	1,A	; TX.PEND AKTIV
0047	X 320000		100	LD	(PROGSTAT),A	
004A	CB57		101	BIT	2,A	; TRANSMIT BUFFERT EMPTY !
004C	00 CAB600		102	JP	Z,RESTXPEN	
004F	C9		103	RET		
			104			
			105			
0050	00	0050	106	TRANSMIT	EQU *	
0050	00 CDBB00		107	CALL	TRSAVE	
			108			
0053	00	0053	109	TRANS	EQU *	
			110			
0053	X 3A0000		111	LD	A,(PROGSTAT)	
0056	CBCF		112	SET	1,A	; TX.PEND AKTIV
0058	X 320000		113	LD	(PROGSTAT),A	
			114			
005B	X 3A0000		115	LD	A,(UBANTAL)	; FINNS FLER TKN ATT SKRIVA
005E	3D		116	DEC	A	
005F	X 320000		117	LD	(UBANTAL),A	
0062	00 CA7E00		118	JP	Z,BUFFEMPT	
			119			
0065	X ED5B0000		120	LD	DE,(UBPEKUT)	; SKRIV TKN TILL SERIESNÖRE
0069	1A		121	LD	A,(DE)	
006A	X D300		122	OUT	SIOADTA,A	
			123			
006C	13		124	INC	DE	; UPPGRADERA BUFF PTR
006D	X 210000		125	LD	HL,UBEND	
0070	A7		126	AND	A	
0071	ED52		127	SBC	HL,DE	
0073	00 C27900		128	JP	NZ,BB2	
0076	X 110000		129	LD	DE,UBSTART	
0079	X ED530000		130	BB2	LD (UBPEKUT),DE	
007D	C9		131	RET		
			132			
007E	00	007E	133	BUFFEMPT	EQU *	
007E	X 3A0000		134	LD	A,(PROGSTAT)	; BUFFERT TOM
0081	CB97		135	RES	2,A	
0083	X 320000		136	LD	(PROGSTAT),A	
			137			
0086	00	0086	138	RESTXPEN	EQU *	
0086	X 3A0000		139	LD	A,(PROGSTAT)	; TRANSMIT AVSTANGT
0089	CBBF		140	RES	1,A	
008B	X 320000		141	LD	(PROGSTAT),A	
			142			
008E	3E2B		143	LD	A,RTIP	; RESET TX INT PENDING
0090	X D300		144	OUT	SIOACMD,A	
0092	C9		145	RET		
			146			
			147		*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			148	;
0093	00	0093	149	KLOCKA EQU *
0093	F5		150	PUSH AF
0094	X 3A0000		151	LD A,(TIME)
0097	3C		152	INC A
0098	X 320000		153	LD (TIME),A
009B	F1		154	POP AF
009C	FB		155	EI
009D	ED4D		156	RETI
			157	;
			158	;
009F	00	009F	159	SPRXCOND EQU *
009F	F5		160	PUSH AF
00A0	3E01		161	LD A,R1
00A2	X D300		162	OUT SIOACHD,A
00A4	X DB00		163	IN A,SIOACHD
			164	;
00A6	3E30		165	LD A,ER
00AB	X D300		166	OUT SIOACHD,A
00AA	X DB00		167	IN A,SIOADTA
00AC	F1		168	POP AF
00AD	FB		169	EI
00AE	ED4D		170	RETI
			171	;
			172	;
00B0	00	00B0	173	EXTSTAT EQU *
00B0	F5		174	PUSH AF
00B1	X DB00		175	IN A,SIOACHD
			176	;
00B3	3E10		177	LD A,RESI
00B5	X D300		178	OUT SIOACHD,A
00B7	F1		179	POP AF
00B8	FB		180	EI
00B9	ED4D		181	RETI
			182	;
			183	;
00BB	E3		184	TRSAVE EX (SP),HL
00BC	D5		185	PUSH DE
00BD	F5		186	PUSH AF
00BE	00 CDC700		187	CALL GO
00C1	F1		188	POP AF
00C2	D1		189	POP DE
00C3	E1		190	POP HL
00C4	FB		191	EIRETII EI
00C5	ED4D		192	RETI
00C7	E9		193	GO JP (HL)
			194	;
00C8			195	END

ERRORS : 0 WARNINGS : 0

ASMZ-4.46 REJINTER.ASM

ERRORS: 0 12:00:00 86-02-24 PAGE 5

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----						
BB1	0016	65	63							
BB2	0079	130	128							
BUFFEMPT	007E	133	118							
<CHDUTFBR	0000	17	82							
EIRETII	00C4	191	77							
<ENDBYTE	0000	13	67							
ER	0030	45	165							
>EXTSTAT	00B0	173	22							
GO	00C7	193	187							
?HEADLOOP	0000	17								
<IBEND	0000	6	60							
<IBPEKIN	0000	6	56 65 85							
<IBSTART	0000	6	64 81 84							
>KLOCKA	0093	149	21							
<PROGSTAT	0000	9	98 100 111 113 134 136 139 141							
>PUT	0040	96	21							
RI	0001	44	161							
>RECEIVE	0000	49	21							
RESI	0010	46	177							
RESTXPEN	0086	138	102							
RTIP	002B	43	143							
<SIDACMD	0000	8	144 162 163 166 175 178							
<SIDADTA	0000	8	54 97 122 167							
>SPRXCOND	009F	159	22							
STRREADY	0025	75	68							
<TIME	0000	9	151 153							
>TRANS	0053	109	21							
>TRANSMIT	0050	106	21							
TRSAVE	00BB	184	107							
<UBANTAL	0000	7	115 117							
<UBEND	0000	7	125							
<UBPEKUT	0000	7	120 130							
<UBSTART	0000	7	129							

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROG SKRSTR.ASM
0000			2	*PAGE 60
			3	;
			4	;
			5	; EXTERNA DATA
			6	EXTERNAL UBPEKIN, UBSTART, UBEND, UBANTAL
			7	EXTERNAL PROGSTAT
			8	;
			9	; EXTERNA RUTINER
			10	EXTERNAL TRANS
			11	;
			12	;
			13	; GLOBALA RUTINER
			14	GLOBAL SKRSTR
			15	;
			16	;
			17	*****
			18	;
			19	; SKRSTR, MONITOR FÖR TRANSMIT RUTINEN FYLLER BC TECKEN IN I
			20	BUFFERT FRÅN HL
			21	;
			22	;
			23	VER DATUM SIGN BESKRIVNING
			24	1.0 860115 SP EGEN MODUL
			25	;
			26	*****
			27	;
			28	;
			29	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			30	;	
0000	00	0000	31	SKRSTR EQU *	
0000	FB		32	EI	; TILLAT AVBROTT
0001	A7		33	AND A	; DUMMY
0002	F3		34	DI	
			35	;	
0003	X 3A0000		36	LD A,(UBANTAL)	; BUFFERT FULL ?
0006	3C		37	INC A	
0007	X FE00		38	CP UBEND-UBSTART	
0009	00 CA0000		39	JP Z,SKRSTR	; JA
000C	X 320000		40	LD (UBANTAL),A	
			41	;	
000F	X ED5B0000		42	LD DE,(UBPEKIN)	; LXGG IN I BUFFERT
0013	EDA0		43	LDI	
			44	;	
0015	E5		45	PUSH HL	; UPGRADERA BUFFPTR
0016	X 210000		46	LD HL,UBEND	
0019	A7		47	AND A	
001A	ED52		48	SBC HL,DE	
001C	E1		49	POP HL	
001D	00 C22300		50	JP NZ,BBB3	
0020	X 110000		51	LD DE,UBSTART	
0023	X ED530000		52	LD (UBPEKIN),DE	
			53	;	
0027	X 3A0000		54	LD A,(PROGSTAT)	
002A	CB57		55	BIT 2,A	
002C	00 CC3600		56	CALL Z,SKRFIRST	
			57	;	
002F	78		58	LD A,B	
0030	B1		59	OR C	
0031	00 C20000		60	JP NZ,SKRSTR	; JA, SATT ISANG AVBROTT
			61	;	
0034	FB		62	EI	
0035	C9		63	RET	
			64	;	
			65	;	
0036	00	0036	66	SKRFIRST EQU *	
0036	CB07		67	SET 2,A	; TRANSBUFF NOT EMPTY
0038	X 320000		68	LD (PROGSTAT),A	
003B	3E02		69	LD A,2	; I TECKEN + RESET INT.PEND
003D	X 320000		70	LD (UBANTAL),A	
0040	E5		71	PUSH HL	
0041	X CD0000		72	CALL TRANS	
0044	E1		73	POP HL	
0045	C9		74	RET	
			75	;	
			76	;	
0046	-		77	END	

ERRORS : 0 WARNINGS : 0

ASNZ-4.46 SKRSTR.ASM
CROSS REFERENCE LISTING

ERRORS: 0 12:00:00 86-02-24 PAGE 3

SYMBOL	LOCATION	DECL	REFERENCES	-----	
BBB3	0023	52	50		
<PROGSTAT	0000	7	54	68	
SKRFIRST	0036	66	56		
>SKRSTR	0000	31	14	39	60
<TRANS	0000	10	72		
<UBANTAL	0000	6	36	40	70
<UBEND	0000	6	38	46	
<UBPEKIN	0000	6	42	52	
<UBSTART	0000	6	38	51	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROB REJINIT
0000			2	*PAGE 60
			3	;
			4	; GLOBALA RUTINER
			5	GLOBAL INITMEN, RESLISTA
			6	;
			7	; EXTERNA DATA
			8	EXTERNAL TGLISTA, TGPRD, PEK
			9	EXTERNAL BOTRAM, STARTRAM
			10	EXTERNAL UBPEKIN, UBPEKUT, UBSTART, UBANTAL
			11	EXTERNAL IBPEKIN, IBPEKUT, IBSTART
			12	EXTERNAL TIME, XSTR, PROSSTAT, DIDSTAT
			13	EXTERNAL STRANG, TG, STATUS, REPEAT, ANTAL
			14	EXTERNAL STUUS, AUTOR
			15	;
			16	; EXTERNA RUTINER
			17	EXTERNAL NEW, INLAST, WRITELIST
			18	;
			19	*****
			20	;
			21	INITMEN, INITIERAR NODVANDIGA MINNESVARIABLER
			22	;
			23	*****
			24	;
			25	;
0000		0002	26	DEFSTUUS EQU 2 ; 0.02 SEKUNDER
0000		003C	27	DEFAUTOR EQU 60 ; 0.6 SEKUNDER
			28	;
			29	*EJECT

ASHZ-4.46 REJINIT

ERRORS: 0 12:00:00 86-02-24 PAGE 2

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
0000	00	0000	30	RESLISTA EQU *	
0000	210000		31	LD HL,0	
0003	X 220000		32	LD (TGLISTA),HL	
			33	;	
0006	X 210000		34	LD HL,TGLISTA	
0009	X 220000		35	LD (TBPRED),HL	
			36	;	
000C	X 210000		37	LD HL,STARTRAM	
000F	X 220000		38	LD (BOTRAM),HL	
			39	;	
0012	C9		40	RET	
			41	;	
0013	00	0013	42	INITNEM EQU *	
0013	00 CD0000		43	CALL RESLISTA	
			44	;	
0016	X 210000		45	LD HL,IBSTART	
0019	X 220000		46	LD (IBPEKIN),HL	
001C	X 220000		47	LD (IBPEKUT),HL	
			48	;	
001F	X 210000		49	LD HL,UBSTART	
0022	X 220000		50	LD (UBPEKIN),HL	
0025	X 220000		51	LD (UBPEKUT),HL	
			52	;	
0028	00 CD4800		53	CALL INDEFAUL	
			54	;	
0028	AF		55	XOR A	
002C	X 320000		56	LD (TIME),A	; NOLLSTALL KLOCKAN
002F	X 320000		57	LD (UBANTAL),A	; 0 TKN I UTBUFFERT
0032	X 320000		58	LD (DIODSTAT),A	; ALLA DIODER SLACKTA
			59	;	
0035	X 3A0000		60	LD A,(PROBSTAT)	
0038	E6F0		61	AND 11110000B	; NOLLSTALL BIT 0-3
003A	X 320000		62	LD (PROBSTAT),A	
			63	;	
003D	3E02		64	LD A,DEFSTUDS	
003F	X 320000		65	LD (STUDS),A	
0042	3E3C		66	LD A,DEFAUTOR	
0044	X 320000		67	LD (AUTOR),A	
			68	;	
0047	C9		69	RET	
			70	*EJECT	

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT	
			71	;	
004B	00	004B	72	INDEFAUL EQU *	
004B	3E01		73	LD A,1	; AKTIV, 1 TKN.
004A	X 320000		74	LD (STATUS),A	
004D	X 320000		75	LD (ANTAL),A	
			76	;	
0050	3E0A		77	LD A,10	; REPEAT = 10
0052	X 320000		78	LD (REPEAT),A	
			79	;	
0055	X 210000		80	LD HL,PEK	
005B	362F		81	LD (HL),47	; 0,1,...P
			82	;	
005A	0640		83	LD B,64	; 64 TANGENTER.
005C	00	005C	84	LOOP EQU *	
005C	C5		85	PUSH BC	
			86	;	
005D	3E40		87	LD A,64	
005F	90		88	SUB B	
0060	X 320000		89	LD (TB),A	
			90	;	
0063	X 3E00		91	LD A,XSTR	
0065	3C		92	INC A	
0066	4F		93	LD C,A	; ANTAL BYTE'S PER POST
0067	0600		94	LD B,0	
0069	X CD0000		95	CALL NEW	
			96	;	
006C	X 210000		97	LD HL,PEK	
006F	34		98	INC (HL)	
0070	X 220000		99	LD (STRANG),HL	
			100	;	
0073	X CD0000		101	CALL WRITELIST	; PACKA IN POST
0076	X 210000		102	LD HL,TGLISTA	
0079	X CD0000		103	CALL INLAST	; LAGG IN I LISTA
			104	;	
007C	C1		105	POP BC	
007D	00 10DD		106	DJNZ LOOP	
			107	;	
007F	C9		108	RET	
0080			109	END	

ERRORS : 0 WARNINGS : 0

ASHZ-4.46 REJINIT

ERRORS: 0 12:00:00 88-02-24 PAGE 4

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----	
<ANTAL	0000	13	75		
<AUTOR	0000	14	67		
<BOTRAM	0000	9	38		
DEFAUTOR	003C	27	66		
DEFSTUDS	0002	26	64		
<DIDSTAT	0000	12	58		
<IBPEKIN	0000	11	46		
<IBPEKUT	0000	11	47		
<IBSTART	0000	11	45		
INDEFAUL	004B	72	53		
>INITMEM	0013	42	5		
<INLAST	0000	17	103		
LOOP	005C	84	106		
<NEM	0000	17	95		
<PEK	0000	8	80	97	
<PROBSTAT	0000	12	60	62	
<REPEAT	0000	13	78		
>RESLISTA	0000	30	5	43	
<STARTRAM	0000	9	37		
<STATUS	0000	13	74		
<STRANG	0000	13	99		
<STUDS	0000	14	65		
<TB	0000	13	89		
<TBLISTA	0000	8	32	34	102
<TGPRED	0000	8	35		
<TIME	0000	12	56		
<UBANTAL	0000	10	57		
<UBPEKIN	0000	10	50		
<UBPEKUT	0000	10	51		
<UBSTART	0000	10	49		
<WRITELIS	0000	17	101		
<XSTR	0000	12	91		


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LOCATION PLC CODE   ARG   LC   SOURCE STATEMENT -----
0000   00          1       ZPROG REJHEAD
0000          2       *PAGE 60
          3       ;
          4       ; EXTERNA RUTINER
          5       EXTERNAL HEAD, LSUCC, BINBIT
          6       EXTERNAL SKRSTR, ERR2
          7       ;
          8       ; EXTERNA DATA
          9       EXTERNAL TGLISTA,PEK
         10       EXTERNAL VARV,TINE,PROGSTAT, DIOSTAT
         11       EXTERNAL STUUS, AUTOR
         12       ;
         13       ; EXTERNA KONSTANTER
         14       EXTERNAL XSTATUS,XTG,XREPEAT,XCOUNT,XANTAL,XSTR
         15       ;
         16       ; GLOBALA RUTINER
         17       GLOBAL HEADLOOP
         18       ;
         19       ;
         20       ; *****
         21       ;
         22       ;
         23       ;
         24       ;
         25       ;
         26       ; VER   DATUM  SIGN   BESKRIVNING
         27       ; 1.0   850926 SP      -
         28       ; 1.1   860113 SP      LOPEN GENONGAS "PER VARV"
         29       ;
         30       ;
         31       ;
         32       ; *****
         33       ;
         34       ;
         35       ;
         36       ;
         37       *EJECT

```

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT	
			38	;	
0000	00	0000	39	HEADLOOP EQU *	
0000	X 3A0000		40	LD A, (PROBSTAT)	; BEGARD RESET ?
0003	CB67		41	BIT 4,A	
0005	X C40000		42	CALL NZ,ERR2	
0008	CBA7		43	RES 4,A	
000A	X 320000		44	LD (PROBSTAT),A	
			45	;	
000D	00	000D	46	HEADL EQU *	
000D	X 3A0000		47	LD A, (DIODSTAT)	
0010	D300		48	OUT 0,A	
			49	;	
0012	00	0012	50	SYNC EQU *	
0012	X 3A0000		51	LD A, (TIME)	
0015	A7		52	AND A	
0016	00 28FA		53	JR Z,SYNC	
0018	AF		54	XOR A	
0019	X 320000		55	LD (TIME),A	
001C	X 3A0000		56	LD A, (VARV)	
001F	3C		57	INC A	
0020	X 320000		58	LD (VARV),A	
			59	;	
			60	;	
0023	X ED5B0000		61	LD DE, (TGLISTA)	; STARTA MED FÖRSTA ELEMENT
			62	;	
0027	00	0027	63	LOOP EQU *	
			64	;	
0027	X CD0000		65	CALL HEAD	; KR LISTAN TOM ?
002A	00 DA0D00		66	JP C,HEADL	
			67	;	
002D	X ED530000		68	LD (PEK),DE	; 1->8
0031	X DD2A0000		69	LD IX, (PEK)	
0035	X DD7E00		70	LD A, (IX+XT6)	
0038	E607		71	AND 7	
003A	3C		72	INC A	
003B	X CD0000		73	CALL BINBIT	
003E	5F		74	LD E,A	
			75	;	
003F	X DD7E00		76	LD A, (IX+XT6)	; A->H
0042	E638		77	AND 00111000B	
0044	0F		78	RRCA	
0045	0F		79	RRCA	
0046	0F		80	RRCA	
0047	3C		81	INC A	
0048	X CD0000		82	CALL BINBIT	
			83	;	
004B	47		84	LD B,A	
004C	0E02		85	LD C,2	
			86	;	
004E	ED41		87	OUT (C),B	; AKTIVERA RATT RAD
			88	;	
0050	0E00		89	LD C,0	
0052	ED78		90	IN A, (C)	
0054	2F		91	CPL	
0055	A3		92	AND E	; MASKA AV RATT KOLUMN
			93	;	
0056	00 CCDE00		94	CALL Z,CLEAR	
0059	00 C47A00		95	CALL NZ,AKTIVERAD	
			96	;	
005C	X ED5B0000		97	LD DE, (PEK)	

ASM1-4.46 REJHEAD

ERRORS: 0 12:00:00 86-02-24 PAGE 3

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	-----
			98	;	
0060	F3		99	DI	
0061	X 3A0000		100	LD A, (PROBSTAT)	
0064	CB77		101	BIT 6,A	
0066	CBF7		102	SET 6,A	
0068	X 320000		103	LD (PROBSTAT),A	
006B	FB		104	EI	
006C	00 CA0D00		105	JP Z,HEADL	; LISTAN HAR BLIVIT XNDRAD
			106	;	
006F	F3		107	DI	
0070	X CD0000		108	CALL LSUCC	
0073	FB		109	EI	
0074	00 D22700		110	JP NC,LOOP	
0077	00 C30D00		111	JP HEADL	
			112	;	
			113	*EJECT	

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT	
			114	;	
007A	00	007A	115	AKTIVERAD EQU *	
007A	X DDCB0046		116	BIT 0,(IX+XSTATUS)	; AKTIVERAD ?
007E	CB		117	RET Z	
			118	;	
007F	X DDCB004E		119	BIT 1,(IX+XSTATUS)	; NEDTRYCKT FÖRRA GANGEN ?
0083	00 C29100		120	JP NZ,NEDTRYCK	
			121	;	
0086	X 3A0000		122	LD A,(VARV)	
0089	X DD7700		123	LD (IX+XCOUNT),A	
008C	X DDCB00CE		124	SET 1,(IX+XSTATUS)	; INDIKERA NEDTRYCKT FÖRRA VARVET
0090	C9		125	RET	
			126	;	
0091	00	0091	127	NEDTRYCK EQU *	
0091	X DDCB0056		128	BIT 2,(IX+XSTATUS)	; AR DEN UTSKRIVEN EN GANG ?
0095	00 C2AD00		129	JP NZ,EJUTSKR	
			130	;	
0098	00 CDF900		131	CALL DIFFTIME	
			132	;	
009B	X 210000		133	LD HL,STUDS	
009E	BE		134	CP (HL)	
009F	DB		135	RET C	
			136	;	
00A0	X DDCB00D6		137	SET 2,(IX+XSTATUS)	; IDIKERA UTSKRIVEN EN GANG
			138	;	
00A4	X 3A0000		139	LD A,(VARV)	
00A7	X DD7700		140	LD (IX+XCOUNT),A	
00AA	00 C3E800		141	JP OKEJ	
			142	;	
			143	;	
00AD	00	00AD	144	EJUTSKR EQU *	
00AD	X DDCB005E		145	BIT 3,(IX+XSTATUS)	; HAR AUTO-REP BÖRJAT ?
00B1	00 C2CE00		146	JP NZ,AUTOREP	
			147	;	
00B4	AF		148	XOR A	
00B5	X DDB600		149	OR (IX+XREPEAT)	
00B8	CB		150	RET Z	
			151	;	
00B9	00 CDF900		152	CALL DIFFTIME	
00BC	X 210000		153	LD HL,AUTOR	
00BF	BE		154	CP (HL)	
00C0	DB		155	RET C	
			156	;	
00C1	X 3A0000		157	LD A,(VARV)	
00C4	X DD7700		158	LD (IX+XCOUNT),A	
00C7	X DDCB00DE		159	SET 3,(IX+XSTATUS)	; INDIKERA AUTOREPITION HAR BÖRJAT
			160	;	
00CB	00 C3E800		161	JP OKEJ	
			162	;	
00CE	00	00CE	163	AUTOREP EQU *	
00CE	00 CDF900		164	CALL DIFFTIME	
00D1	X DDBE00		165	CP (IX+XREPEAT)	
00D4	DB		166	RET C	
			167	;	
00D5	X 3A0000		168	LD A,(VARV)	
00D8	X DD7700		169	LD (IX+XCOUNT),A	
00DB	00 C3E800		170	JP OKEJ	
			171	;	
			172	*EJECT	

ASMZ-4.46 REJHEAD

ERRORS: 0 12:00:00 86-02-24 PAGE 5

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			173	;
00DE	00	00DE	174	CLEAR EQU * ; T6N STATUS
00DE	X DD7E00		175	LD A,(IX+XSTATUS)
00E1	E601		176	AND 1
00E3	X DD7700		177	LD (IX+XSTATUS),A
00E6	AF		178	XOR A
00E7	C9		179	RET
			180	;
00EB	00	00EB	181	OKEJ EQU * ; SKRIV UT
00EB	X 2A0000		182	LD HL,(PEK)
00EB	X 010000		183	LD BC,XSTR
00EE	09		184	ADD HL,BC
00EF	X DD7E00		185	LD A,(IX+XANTAL)
00F2	4F		186	LD C,A
00F3	0600		187	LD B,0
00F5	X CD0000		188	CALL SKRSTR
00FB	C9		189	RET
			190	;
00F9	00	00F9	191	DIFFTIME EQU *
00F9	X 3A0000		192	LD A,(VARV)
00FC	X DD9600		193	SUB (IX+XCOUNT)
00FF	D0		194	RET NC
0100	C6FF		195	ADD 255
0102	C9		196	RET
			197	;
0103			198	END

ERRORS : 0 WARNINGS : 0

ASHZ-4.46 REJHEAD

ERRORS: 0 12:00:00 86-02-24 PAGE 6

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----						
AKTIVERA	007A	115	95							
<AUTOR	0000	11	153							
AUTOREP	00CE	163	146							
<BINBIT	0000	5	73	82						
CLEAR	00DE	174	94							
DIFFTIME	00F9	191	131	152	164					
<DIDSTAT	0000	10	47							
EJUTSKR	00AD	144	129							
<ERR2	0000	6	42							
<HEAD	0000	5	65							
HEADL	000D	46	66	105	111					
>HEADLOOP	0000	39	17							
LOOP	0027	63	110							
<LSUCC	0000	5	108							
NEDTRYCK	0091	127	120							
OKEJ	00E8	181	141	161	170					
<PEK	0000	9	68	69	97	182				
<PROBSTAT	0000	10	40	44	100	103				
<SKRSTR	0000	6	188							
<STUDS	0000	11	133							
SYNC	0012	50	53							
<TGLISTA	0000	9	61							
<TIME	0000	10	51	55						
<VARV	0000	10	56	58	122	139	157	168	192	
<XANTAL	0000	14	185							
<XCOUNT	0000	14	123	140	158	169	193			
<XREPEAT	0000	14	149	165						
<XSTATUS	0000	14	116	119	124	128	137	145	159	175 177
<XSTR	0000	14	183							
<XTG	0000	14	70	76						

```

LOCATION PLC CODE  ARG  LC  SOURCE STATEMENT -----
0000  00          1      ZPROG REJCMD
0000          2      *PAGE 60
          3      *LIST OFF
          4      |
          5      |
          6      |
          7      |
          8      | EXTERNA RUTINER
          9      EXTERNAL LEXSCAN, SKRSTR, DECBIN, BINDEC
         10      EXTERNAL NEM, INLAST, DEL, WRITELIST, READLIST
         11      EXTERNAL SKRORD, FINDTG, LSUCC, LPRED
         12      EXTERNAL LAST, FIRST, RESLISTA, RESET
         13      |
         14      | GLOBALA RUTINER
         15      GLOBAL CMDUTF8R, BINBIT, ERR2
         16      |
         17      |
         18      | EXTERNA DATA
         19      EXTERNAL BUFFERT, ENDBYTE, XSTR
         20      EXTERNAL SUCC, PRED, STATUS, TG, REPEAT, COUNT, ANTAL
         21      EXTERNAL TGLISTA, PEK, STRANG, DIODSTAT
         22      EXTERNAL STUDB, AUTOR, PROBSTAT
         23      |
         24      |
         25      | *****
         26      |
         27      |
         28      |
         29      |   VER  DATUM  SIGN  BESKRIVNING
         30      |   1.0  850808  SP    -
         31      |   2.0  851012  SP    -
         32      |   2.1  860115  SP    LIGHT, UNLIGHT IMPLEMENTERAT
         33      |
         34      |
         35      |
         36      | *****
         37      |
         38      |
         39      |   ERROCODER:
         40      |       0      ALLT OK
         41      |       1
         42      |       2      BEGARD RESET
         43      |       3      MINNES BRIST, KOMMANDO EJ UTF8RT !
         44      |       4      TANGENT SAKNAS I LISTAN
         45      |       5      RANGE ERROR ASCII STRANG
         46      |       6      RANGE ERROR TANGENT A1 -> H8
         47      |       7      RANGE ERROR LYSDIOD 1 -> 8
         48      |       8      F8RVANTAD SIFFRA UTEBLIVEN
         49      |       9      OKXNT KOMMANDO ....
         50      |
         51      | *EJECT
    
```

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			52	;	
0000	00	0000	53	CMDUTF6R EQU *	
			54	;	
			55	;	
0000	00	0000	56	CMD EQU *	
0000	7E		57	LD A,(HL)	
0001	X CD0000		58	CALL LEXSCAN	; AVKODA KOMMANDO
0004	00 CD8B01		59	CALL SKIPBLANK	; HOPPA ÖVER BLANKA
0007	00 CA5301		60	JP Z,FELCMD	
			61	;	
000A	00	000A	62	CMD1 EQU *	; LIGHT DIOD
000A	FE01		63	CP 1	; == L: ==
000C	00 2017		64	JR NZ,CMD2	
			65	;	
000E	00 CD9701		66	CALL SIFFRA	
0011	00 DA6001		67	JP C,ERR8	
0014	00 CDDC01		68	CALL BINBIT	; 0 < A < 9
0017	00 DA6501		69	JP C,ERR7	
001A	4F		70	LD C,A	
001B	X 3A0000		71	LD A,(DIODSTAT)	
001E	B1		72	OR C	
001F	X 320000		73	LD (DIODSTAT),A	
0022	00 C38801		74	JP ERRO	
			75	;	
			76	;	
0025	00	0025	77	CMD2 EQU *	; UNLIGHT DIOD
0025	FE02		78	CP 2	; == U: ==
0027	00 2018		79	JR NZ,CMD3	
			80	;	
0029	00 CD9701		81	CALL SIFFRA	
002C	00 DA6001		82	JP C,ERR8	
002F	00 CDDC01		83	CALL BINBIT	
0032	00 DA6501		84	JP C,ERR7	
0035	2F		85	CPL	
0036	4F		86	LD C,A	
0037	X 3A0000		87	LD A,(DIODSTAT)	
003A	A1		88	AND C	
003B	X 320000		89	LD (DIODSTAT),A	
003E	00 C38801		90	JP ERRO	
			91	;	
			92	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			93	;	
0041	00	0041	94	CMD3 EQU *	; FILL LISTA
0041	FE03		95	CP 3	; == F: ==
0043	00 205B		96	JR NZ,CMD4	
			97	;	
0045	00 CDBD01		98	CALL TANGENT	; HANTA TANGENT, PACKA UPP
0048	00 DA6A01		99	JP C,ERR6	
0048	X 320000		100	LD (T6),A	
			101	;	
004E	X CD0000		102	CALL FINDTB	; FINNS DET REDAN ?
0051	E5		103	PUSH HL	
0052	X 210000		104	LD HL,TGLISTA	
0055	00 DA5E00		105	JP C,FANNSEJ	
0058	X CD0000		106	CALL DEL	; TA BORT DET !
0058	00 CDAB01		107	CALL INDANDLI	; INDIKERA ANDRAT I LISTAN
005E	00	005E	108	FANNSEJ EQU *	
005E	E1		109	POP HL	
			110	;	
005F	00 C8D01		111	CALL SKIPBLANK	; REPEAT
0062	00 CD9701		112	CALL SIFFRA	
0063	00 DA6001		113	JP C,ERR8	
0068	X 320000		114	LD (REPEAT),A	
			115	;	
0068	23		116	INC HL	
006C	X 220000		117	LD (STRANG),HL	
006F	00 CDE901		118	CALL COUNTSTR	; RAKNA ANTAL TECKEN
0072	X 320000		119	LD (ANTAL),A	
			120	;	
			121	;	
0075	X C600		122	ADD A,XSTR	; FÖREGÅENDE VARIABLER
0077	4F		123	LD C,A	
0078	0600		124	LD B,0	
007A	X FE00		125	CP XSTR	; LEN(ASCII)<> ?
007C	00 CA6F01		126	JP Z,ERR5	
			127	;	
007F	X 3A0000		128	LD A,(PROGSTAT)	; FÖRSTA GANGEN ?, SKALL DEFULT TÄNKA
0082	CB47		129	BIT 0,A	
			130	CALL Z,RELISTA	
0084	CBC7		131	SET 0,A	
0086	X 320000		132	LD (PROGSTAT),A	
			133	;	
0089	X CD0000		134	CALL NEM	
008C	00 BA7901		135	JP C,ERR3	
			136	;	
008F	3E01		137	LD A,1	; AKTIVERA TANGENT
0091	X 320000		138	LD (STATUS),A	
			139	;	
0094	X CD0000		140	CALL WRITELIST	; PACKA IN I POST
0097	X 210000		141	LD HL,TGLISTA	
009A	X CD0000		142	CALL INLAST	; LÄGG POST SIST I LISTA
			143	;	
009D	00 C38B01		144	JP ERRO	
			145	;	
			146	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			147	;	
00A0	00	00A0	148	CMD4 EQU *	; CHANGE LISTA
00A0	FE04		149	CP 4	; ---- C: ----
00A2	00 203A		150	JR NZ,CMD5	
			151	;	
00A4	00 CDBD01		152	CALL TANGENT	; HANTA TANGENT
00A7	00 DA6A01		153	JP C,ERR6	
00AA	X CD0000		154	CALL FINDTG	; FINNS DEN
00AD	00 DA7401		155	JP C,ERR4	; NEJ
			156	;	
00B0	00 CDBD01		157	CALL SKIPBLANK	
00B3	X CD0000		158	CALL READLIST	; PACKA UPP POST
00B6	00 CD9701		159	CALL SIFFRA	
00B9	00 DABF00		160	JP C,NONUMB	; ANDRA EJ REPEAT
00BC	X 320000		161	LD (REPEAT),A	
00BF	00	00BF	162	NONUMB EQU *	
00BF	7E		163	LD A,(HL)	
00C0	X FE00		164	CP ENDBYTE	
00C2	00 CAB800		165	JP Z,READY	
			166	;	
00C5	23		167	INC HL	
00C6	X 220000		168	LD (STRXNB),HL	
00C9	00 CDE901		169	CALL COUNTSTR	
			170	;	
00CC	47		171	LD B,A	; NYSTRXNB KORTARE AN OLDSTRXNB ?
00CD	X 3A0000		172	LD A,(ANTAL)	
00D0	BB		173	CP B	
00D1	00 DA6F01		174	JP C,ERR5	
00D4	78		175	LD A,B	
			176	;	
00D5	X 320000		177	LD (ANTAL),A	
00DB	X CD0000		178	READY CALL WRITELIST	
00DB	00 C38B01		179	JP ERRO	
			180	;	
			181	;	
			182	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
00DE	00	00DE	183	CMD5 EQU *	; DEAKTIVERA TANGENT
00DE	FE05		184	CP 5	; ***** D1 *****
00E0	00 201D		185	JR NZ,CMD6	
			186	;	
00E2	00 CDBD01		187	CALL TANGENT	
00E5	00 DA6A01		188	JP C,ERR6	
00EB	X CD0000		189	CALL FINDTG	
00EB	00 DA7401		190	JP C,ERR4	
00EE	X CD0000		191	CALL READLIST	
00F1	X 3A0000		192	LD A,(STATUS)	
00F4	CBB7		193	RES 0,A	
00F6	X 320000		194	LD (STATUS),A	
00F9	X CD0000		195	CALL WRITELIST	
			196	;	
00FC	00 C38B01		197	JP ERRO	
			198	;	
			199	;	
00FF	00	00FF	200	CMD6 EQU *	; AKTIVERA TANGENT
00FF	FE06		201	CP 6	; ***** A1 *****
0101	00 201D		202	JR NZ,CMD7	
			203	;	
0103	00 CDBD01		204	CALL TANGENT	
0106	00 DA6A01		205	JP C,ERR6	
0109	X CD0000		206	CALL FINDTG	
010C	00 DA7401		207	JP C,ERR4	
010F	X CD0000		208	CALL READLIST	
0112	X 3A0000		209	LD A,(STATUS)	
0115	CBC7		210	SET 0,A	
0117	X 320000		211	LD (STATUS),A	
011A	X CD0000		212	CALL WRITELIST	
			213	;	
011D	00 C38B01		214	JP ERRO	
			215	;	
			216	;	
0120	00	0120	217	CMD7 EQU *	; MJUKVARI6 RESET
0120	FE07		218	CP 7	; ==== RESET ====
0122	00 200B		219	JR NZ,CMD8	
			220	;	
0124	X 3A0000		221	LD A,(PROGSTAT)	
0127	CBE7		222	SET 4,A	
0129	X 320000		223	LD (PROGSTAT),A	
			224	;	
012C	X C30000		225	JP RESET	; RESET
			226	;	
012F	00	012F	227	CMD8 EQU *	; TIDER
012F	FE08		228	CP 8	; = T =
0131	00 2015		229	JR NZ,CMD9	
			230	;	
0133	00 CD9701		231	CALL SIFFRA	
0136	00 DA6001		232	JP C,ERR8	; INGEN SIFFRA
0139	X 320000		233	LD (STUDS),A	
			234	;	
013C	00 CD9701		235	CALL SIFFRA	
013F	00 DA6001		236	JP C,ERR8	; INGEN SIFFRA
0142	X 320000		237	LD (AUTOR),A	
0145	00 C38B01		238	JP ERRO	
			239	;	
			240	;	
0148	00	0148	241	CMD9 EQU *	; T6N DEFAULTLISTAN
0148	FE09		242	CP 9	

ASHZ-4.46 REJCHD

ERRORS: 0 12:00:00 86-02-24 PAGE 6

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
014A	00		243	JP NZ,FELCHD
			244	;
014D	X	CD0000	245	CALL RESLISTA
0150	00	C38801	246	JP ERRO
			247	;
			248	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			249	;
0153	00	0153	250	FELCMD EQU *
0153	3E39		251	LD A,"9" ; OKANT KOMMANDO..
0155	00	0155	252	ERROUT EQU * ; SKRIV UT ERROR A
0155	X 210000		253	LD HL,BUFFERT
0158	77		254	LD (HL),A
0159	010100		255	LD BC,1
015C	X CD0000		256	CALL SKRSTR
015F	C9		257	RET
			258	;
0160	3E38		259	ERRB LD A,"8"
0162	00 C35501		260	JP ERROUT
0165	3E37		261	ERR7 LD A,"7"
0167	00 C35501		262	JP ERROUT
016A	3E36		263	ERR6 LD A,"6"
016C	00 C35501		264	JP ERROUT
016F	3E35		265	ERR5 LD A,"5"
0171	00 C35501		266	JP ERROUT
0174	3E34		267	ERR4 LD A,"4"
0176	00 C35501		268	JP ERROUT
0179	3E33		269	ERR3 LD A,"3"
017B	00 C35501		270	JP ERROUT
017E	3E32		271	ERR2 LD A,"2"
0180	00 C35501		272	JP ERROUT
0183	3E31		273	ERR1 LD A,"1"
0185	00 C35501		274	JP ERROUT
0188	3E30		275	ERRO LD A,"0"
018A	00 C35501		276	JP ERROUT
			277	;
			278	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			279	}	
018D	2B		280	SKIPBLANK DEC HL	
018E	F5		281	PUSH AF	
018F	23		282	SKIPB INC HL	
0190	7E		283	LD A,(HL)	
0191	FE20		284	CP 32	
0193	00 2BFA		285	JR Z,SKIPB	
0195	F1		286	POP AF	
0196	C9		287	RET	
			288	}	
			289	}	
0197	00 -	0197	290	SIFFRA EQU *	; SIFFER KONTROLL, LASER FÖRBI
0197	7E		291	LD A,(HL)	; BLANKA I HL RETURNERAR NC OM OK
0198	FE30		292	CP 48	
019A	DB		293	RET C	
019B	FE3A		294	CP 58	
019D	00 DAA201		295	JP C,OKSIFFRA	
01A0	37		296	SCF	; FEL
01A1	C9		297	RET	
01A2	00 -	01A2	298	OKSIFFRA EQU *	
01A2	X CD0000		299	CALL DECBIN	
01A5	37		300	SCF	; SAKERSTALL NC
01A6	3F		301	CCF	
01A7	C9		302	RET	; OK SIFFRA
			303	}	
			304	}	
01A8	00	01A8	305	INDANDLI EQU *	
01A8	X 3A0000		306	LD A,(PROBSTAT)	
01A8	- CBB7		307	RES 6,A	
01AD	X 320000		308	LD (PROBSTAT),A	
01B0	C9		309	RET	
			310	}	
01B1	00	01B1	311	GRANS EQU *	
01B1	FE09		312	CP 9	
01B3	00 3006		313	JR NC,FELGRANS	
01B5	FE00		314	CP 0	
01B7	00 2802		315	JR Z,FELGRANS	
01B9	A7		316	AND A	
01BA	C9		317	RET	
01BB	37		318	FELGRANS SCF	
01BC	C9		319	RET	
			320	}	
			321	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
			322	;	
01BD	00	01BD	323	TANGENT EQU *	
01BD	7E		324	LD A,(HL)	
01BE	D640		325	SUB 64	
01C0	00 CDB101		326	CALL GRANS	
01C3	00 DADB01		327	JP C,FELT8	
01C6	3D		328	DEC A	; A == (0:7)
01C7	07		329	RLCA	
01C8	07		330	RLCA	
01C9	07		331	RLCA	
01CA	77		332	LD (HL),A	
01CB	23		333	INC HL	
01CC	7E		334	LD A,(HL)	
01CD	D630		335	SUB "0"	; A == (1:8)
01CF	00 CDB101		336	CALL GRANS	
01D2	00 DADB01		337	JP C,FELT8	
01D5	3D		338	DEC A	; A == (0:7)
01D6	2B		339	DEC HL	
01D7	B6		340	OR (HL)	
01D8	23		341	INC HL	
01D9	23		342	INC HL	
01DA	A7		343	AND A	
01DB	00	01DB	344	FELT8 EQU *	
01DB	C9		345	RET	
			346	;	
			347	;	
01DC	00	01DC	348	BINBIT EQU *	; BINART ==> BIT KONVERTERING
01DC	00 CDB101		349	CALL GRANS	
01DF	D8		350	RET C	
01E0	C5		351	PUSH BC	
01E1	47		352	LD B,A	
01E2	AF		353	XOR A	
01E3	37		354	SCF	
01E4	17		355	BBL RLA	
01E5	00 10FD		356	DJNZ BBL	
01E7	C1		357	POP BC	
01E8	C9		358	RET	
			359	;	
			360	;	
01E9	00	01E9	361	COUNTSTR EQU *	; RAKNAR ANTAL TKN I STRANG
01E9	E5		362	PUSH HL	
01EA	C5		363	PUSH BC	
01EB	0E00		364	LD C,0	
01ED	7E		365	CC LD A,(HL)	
01EE	23		366	INC HL	
01EF	X FE00		367	CP ENDBYTE	
01F1	00 2803		368	JR Z,CCUT	
01F3	0C		369	INC C	
01F4	00 18F7		370	JR CC	
01F6	79		371	CCUT LD A,C	
01F7	C1		372	POP BC	
01F8	E1		373	POP HL	
01F9	C9		374	RET	
			375	;	
01FA			376	END	

ERRORS : 0 WARNINGS : 0

ASHZ-4.46 REJCMD

ERRORS: 0 12:00:00 86-02-24 PAGE 10

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----						
<ANTAL	0000	20	119 172 177							
<AUTOR	0000	22	237							
BBL	01E4	355	356							
>BINBIT	01DC	348	15 68 83							
?BINDEC	0000	9								
<BUFFERT	0000	19	253							
CC	01ED	365	370							
CCUT	01F6	371	368							
?CMD	0000	56								
?CMD1	000A	62								
CMD2	0025	77	64							
CMD3	0041	94	79							
CMD4	00A0	148	96							
CMD5	00DE	183	150							
CMD6	00FF	200	185							
CMD7	0120	217	202							
CMD8	012F	227	219							
CMD9	0148	241	229							
>CMDUTF8R	0000	53	15							
?COUNT	0000	20								
COUNTSTR	01E9	361	118 169							
<DECBIN	0000	9	299							
<DEL	0000	10	106							
<DIDSTAT	0000	21	71 73 87 89							
<ENDBYTE	0000	19	164 367							
ERR0	018B	275	74 90 144 179 197 214 238 246							
?ERR1	0183	273								
>ERR2	017E	271	15							
ERR3	0179	269	135							
ERR4	0174	267	155 190 207							
ERR5	016F	265	126 174							
ERR6	016A	263	99 153 188 205							
ERR7	0165	261	69 84							
ERR8	0160	259	67 82 113 232 236							
ERR0UT	0155	252	260 262 264 266 268 270 272 274 276							
FANNSEJ	005E	108	105							
FELCND	0153	250	60 243							
FELGRANS	01BB	318	313 315							
FELT6	01DB	344	327 337							
<FINDT6	0000	11	102 154 189 206							
?FIRST	0000	12								
BRANS	01B1	311	326 336 349							
INDXNDLI	01A8	305	107							
<INLAST	0000	10	142							
?LAST	0000	12								
<LEXSCAN	0000	9	58							
?LPRED	0000	11								
?LSUCC	0000	11								
<NEW	0000	10	134							
NONUMB	00BF	162	160							
OKSIFRA	01A2	298	295							
?PEK	0000	21								
?PPRED	0000	20								
<PROBSTAT	0000	22	128 132 221 223 306 308							
<READLIST	0000	10	158 191 208							
READY	00DB	178	165							
<REPEAT	0000	20	114 161							
<RESET	0000	12	225							
<RESLISTA	0000	12	245							
SIFFRA	0197	290	66 81 112 159 231 235							

ASHZ-4.46 REJCMD

ERRORS: 0 12:00:00 86-02-24 PAGE 11

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----			
SKIPB	018F	282	285				
SKIPBLAN	018D	280	59	111	157		
?SKRORD	0000	11					
<SKRSTR	0000	9	256				
<STATUS	0000	20	138	192	194	209	211
<STRANG	0000	21	117	168			
<STUDS	0000	22	233				
?SUCC	0000	20					
TANGENT	018D	323	98	152	187	204	
<TG	0000	20	100				
<TGLISTA	0000	21	104	141			
<WRITELIS	0000	10	140	178	195	212	
<XSTR	0000	19	122	125			

LOCATION	PLC	CODE	ARG	LC	SOURCE STATEMENT
0000				1	ZPROG REJLEX
				2	GLOBAL LEXSCAN
				3	;
0000				4	*PAGE 60
				5	;
				6	;
				7	*****
				8	;
				9	REILEX, LETAR EFTER STRANG SOM HL PEKAR PA
				10	I TABELL.
				11	;
				12	A INNEHALLER SKILJEBITEN OM OK
				13	A = 0 OM INTE OK.
				14	;
				15	;
				16	VER DATUM SIGN BESKRIVNING
				17	1.0 850615 6P
				18	;
				19	;
				20	*****
				21	;
				22	;
0000	00		0000	23	LEXSCAN EQU *
0000		D5		24	PUSH DE
0001		E5		25	PUSH HL
0002	00	212800		26	LD HL, TABELL
0005		D1		27	LEX1 POP DE ; HANTA STANGSTART
0006		D5		28	PUSH DE
0007		1A		29	LEX2 LD A, (DE)
0008		BE		30	CP (HL)
0009	00	2009		31	JR NZ, NXSTA
0008		13		32	INC DE
000C		23		33	INC HL
000D		7E		34	LD A, (HL)
000E		FE80		35	CP 128
0010	00	3010		36	JR NC, HITTAT
0012	00	18F3		37	JR LEX2
				38	;
0014		23		39	NXSTA INC HL
0015		7E		40	LD A, (HL)
0016		FE80		41	CP 128
0018	00	38FA		42	JR C, NXSTA
001A		FEFF		43	CP 255
001C	00	2803		44	JR Z, FANNSEJ
001E		23		45	INC HL
001F	00	18E4		46	JR LEX1
				47	;
0021		AF		48	FANNSEJ XOR A
0022		E67F		49	HITTAT AND 127
0024		E1		50	POP HL
0025		EB		51	EX DE, HL
0026		D1		52	POP DE
0027		C9		53	RET
				54	;
				55	*EJECT

ASHZ-4.46 REJLEX

ERRORS: 0 12:00:00 86-02-24 PAGE 2

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			56	;
002B	4C3A		57	TABELL DEFN "L1" ; L(IGHT)
002A	81		58	DEFB 128+1
002B	553A		59	DEFN "U1" ; U(NLIGHT) SLACK DIOD
002B	82		60	DEFB 128+2
			61	;
002E	463A		62	DEFN "F1" ; DEFINIERA I LISTA
0030	83		63	DEFB 128+3
			64	;
0031	433A		65	DEFN "C1" ; CHANGE I LISTA
0033	84		66	DEFB 128+4
			67	;
0034	443A		68	DEFN "D1" ; DEAKTIVERA TANGENT
0036	85		69	DEFB 128+5
			70	;
0037	413A		71	DEFN "A1" ; AKTIVERA TANGENT
0039	86		72	DEFB 128+6
			73	;
003A	52455345		74	DEFN "RESET" ; NJUKVARUMSSIG RESET
003F	87		75	DEFB 128+7
			76	;
0040	543A		77	DEFN "T1" ; TIMING KONSTANTER
0042	88		78	DEFB 128+8
			79	;
0043	523A		80	DEFN "R1" ; T&M DEFAULTLISTAN
0045	89		81	DEFB 128+9
			82	;
			83	;
0046	FF		84	DEFB 255 ; AVSLUTNING
			85	;
0047			86	END
ERRORS :	0	WARNINGS :	0	

ASMZ-4.46 REJLEX

ERRORS: 0 12:00:00 86-02-24 PAGE 3

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	
FANNSEJ	0021	48	44	
HITTAT	0022	49	36	
LEX1	0005	27	46	
LEX2	0007	29	37	
>LEXSCAN	0000	23	2	
NXSTA	0014	39	31	42
TABELL	0028	57	26	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROG LISTOR.ASM
0000			2	*PAGE 60
			3	;
			4	;
			5	; EXTERNA DATA
			6	EXTERNAL BOTRAM
			7	;
			8	; GLOBALA RUTINER
			9	GLOBAL NEW, DEL, INLAST, LSUCC, LPRED
			10	GLOBAL LAST, FIRST, HEAD
			11	;
			12	;
			13	;
			14	*****
			15	;
			16	LISTOR, PAKET MED RUTINER FÖR TVAVÄGSLISTOR
			17	FAST I STUKTUREN ÄR ATT ELEMENTET STARTAR MED EN SUCC
			18	PEKARE SOM FÖLJS AV EN PRED PEKARE, GENERELLT ÄR HL
			19	LISTHUVUD OCH DE ELEMNT.
			20	;
			21	;
			22	VER DATUM SIGN BESKRIVNING
			23	1.0 851103 SP -
			24	1.1 851104 SP LSUCC
			25	1.2 860113 SP NEW GER C=1 VID MINNESBRIST
			26	;
			27	;
			28	;
			29	*****
			30	;
			31	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			32	; NEW(STORLEK,PEK), SKAPAR ETT TOMT LISTELEMENT I MINNET
			33	; IN: BC STORLEK PA ELEMENT
			34	; UT: DE ADRESS TILL RESERVERAT ELEMENT, PEK
			35	;
0000	00	0000	36	NEW EQU *
0000	EB		37	EX DE,HL
0001	X 2A0000		38	LD HL,(BOTRAM) ; FÖRSTA LEDIGA BYTE I RAM
			39	;
0004	3600		40	LD (HL),0 ; PEK.SUCC := NIL, PEK.PRED := NIL
0006	23		41	INC HL
0007	3600		42	LD (HL),0
0009	23		43	INC HL
000A	3600		44	LD (HL),0
000C	23		45	INC HL
000D	3600		46	LD (HL),0
000F	2B		47	DEC HL
0010	2B		48	DEC HL
0011	2B		49	DEC HL
			50	;
0012	E5		51	PUSH HL
0013	09		52	ADD HL,BC
0014	00 3803		53	JR C,NEWEXIT
0016	X 220000		54	LD (BOTRAM),HL
0019	00	0019	55	NEWEXIT EQU *
0019	E1		56	POP HL
001A	EB		57	EX DE,HL
001B	C9		58	RET
			59	;
			60	;
			61	; HEAD(PEK), GER C=1 OM DE PEKAR PA LISTHUVUDET
			62	; IN DE : LISTA
			63	; UT: OFÖRÄNDRAT
			64	;
001C	00	001C	65	HEAD EQU *
001C	D5		66	PUSH DE
001D	EB		67	EX DE,HL
001E	23		68	INC HL
001F	23		69	INC HL
0020	7E		70	LD A,(HL)
0021	E3		71	EX (SP),HL
0022	8D		72	CP L ; LISTA.SUCCL = LISTAL ?
0023	E3		73	EX (SP),HL
0024	00 200B		74	JR NZ,NOTEMP
0026	23		75	INC HL
0027	7E		76	LD A,(HL)
0028	E3		77	EX (SP),HL
0029	BC		78	CP H ; LISTA.SUCCH = LISTAH ?
002A	E3		79	EX (SP),HL
002B	00 2004		80	JR NZ,NOTEMP
002D	EB		81	EX DE,HL
002E	D1		82	POP DE
002F	37		83	SCF
0030	C9		84	RET
			85	;
0031	00	0031	86	NOTEMP EQU *
0031	EB		87	EX DE,HL
0032	D1		88	POP DE
0033	A7		89	AND A
0034	C9		90	RET
			91	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			92	;
			93	;
			94	; INLAST(PEK,LISTA), LÄGGER ELEMENTET PEK SIST I LISTAN LISTA
			95	; IN: DE PEK, HL LISTA
			96	; UT: OFÖRÄNDRAT
			97	;
0035	00	0035	98	INLAST EQU *
0035	F5		99	PUSH AF
0036	D5		100	PUSH DE
0037	E5		101	PUSH HL
			102	;
0038	23		103	INC HL
0039	7E		104	LD A,(HL) ; LISTA.NEXT = NIL ?
003A	2B		105	DEC HL
003B	B6		106	OR (HL)
003C	00 2805		107	JR Z,FÖRSTA
			108	;
003E	EB		109	EX DE,HL
003F	00 CD5100		110	CALL LAST ; HÄMTA SISTA ELEMENT I LISTAN
0042	EB		111	EX DE,HL
			112	;
0043	73		113	FÖRSTA LD (HL),E ; SE.NEXT:L := PEK:L
0044	23		114	INC HL
0045	72		115	LD (HL),D ; SE.NEXT:H := PEK:H
0046	2B		116	DEC HL
0047	EB		117	EX DE,HL
0048	23		118	INC HL ; PEK.PRED := "SISTA ELEMENT"
0049	23		119	INC HL
004A	73		120	LD (HL),E ; PEK.PRED:L := SE:L
004B	23		121	INC HL
004C	72		122	LD (HL),D ; PEK.PRED:H := SE:H
			123	;
004D	E1		124	POP HL
004E	D1		125	POP DE
004F	F1		126	POP AF
0050	C9		127	RET
			128	;
			129	;
			130	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			131	;LAST(PEK), HÄMTAR SISTA ELEMENTET I LISTAN
			132	; IN: DE PEKARE
			133	; UT: DE PEKARE TILL SISTA ELEMENT
			134	;
0051	00	0051	135	LAST EQU *
0051	E5		136	PUSH HL
0052	00	0052	137	LALOP EQU *
0052	D5		138	PUSH DE ; PEK
0053	00 CD9B00		139	CALL LSUCC ; PEK := PEK.SUCC
0056	00 3803		140	JR C,LAOK
0058	E1		141	POP HL ; DUMMY, TÖMMER STACK
0059	00 18F7		142	JR LALOP
005B	00	005B	143	LAOK EQU *
005B	00 CD1C00		144	CALL HEAD ; C=1 -> TOM LISTA
005E	D1		145	POP DE ; PEK
005F	E1		146	POP HL
0060	C9		147	RET
			148	;
			149	;
			150	;FIRST(PEK), HÄMTAR FÖRSTA ELEMENTET I LISTAN
			151	; IN: PEK
			152	; UT: PEKARE TILL FÖRSTA ELEMENT
			153	;
0061	00	0061	154	FIRST EQU *
0061	E5		155	PUSH HL
0062	00 CD9B00		156	CALL LSUCC ; UNDVIKA LISTHUVUDET
0065	00	0065	157	FILOP EQU *
0065	D5		158	PUSH DE
0066	00 CD8500		159	CALL LPRED
0069	00 3808		160	JR C,FIOK
006B	00 CD1C00		161	CALL HEAD
006E	00 3803		162	JR C,FIOK
0070	E1		163	POP HL
0071	00 18F2		164	JR FILOP
0073	00	0073	165	FIOK EQU *
0073	00 CD1C00		166	CALL HEAD ; C=1 -> TOM LISTA
0076	D1		167	POP DE
0077	E1		168	POP HL
0078	C9		169	RET
			170	;
			171	+EJECT

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT
			172	;
			173	;
			174	; DEL(PEK), TAR BORT ELEMENTET PEK UR LISTAN
			175	; IN: DE PEK
			176	; UT: OFBRANDRAT
			177	;
0079	00	0079	178	DEL EQU *
			179	;
0079	E5		180	PUSH HL
007A	D5		181	PUSH DE
			182	;
007B	00	C0B500	183	CALL LPRED
007E	EB		184	EX DE,HL ; HL := PEK.PRED
007F	D1		185	POP DE ; DE := PEK
			186	;
0080	1A		187	LD A,(DE) ; PEK.PRED.SUCC := PEK.SUCC
0081	77		188	LD (HL),A
0082	13		189	INC DE
0083	23		190	INC HL
0084	1A		191	LD A,(DE)
0085	77		192	LD (HL),A
0086	1B		193	DEC DE
			194	;
0087	D5		195	PUSH DE
0088	00	C09B00	196	CALL LSUCC
008B	EB		197	EX DE,HL ; HL := PEK.SUCC
008C	D1		198	POP DE ; DE := PEK
			199	;
008D	D5		200	PUSH DE ; PEK.SUCC.PRED := PEK.PRED
008E	13		201	INC DE
008F	13		202	INC DE
0090	23		203	INC HL
0091	23		204	INC HL
0092	1A		205	LD A,(DE)
0093	77		206	LD (HL),A
0094	13		207	INC DE
0095	23		208	INC HL
0096	1A		209	LD A,(DE)
0097	77		210	LD (HL),A
0098	D1		211	POP DE
0099	E1		212	POP HL
009A	C9		213	RET
			214	;
			215	*EJECT

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT	
			216	;	
			217	;LSUCC(PEK), HXMTAR NXSTA ELEMENT I LISTAN	
			218	; IN: DE PEK	
			219	; UT: DE PEK.NEXT C=0, OM PEK.NEXT<>NIL	
			220	; DE OFBRANDRAD, C=1 OM PEK.SUCC=NIL	
			221	;	
009B	00	009B	222	LSUCC EQU *	
009B	F5		223	PUSH AF	
009C	EB		224	EX DE,HL	
			225	;	
009D	7C		226	LD A,H	
009E	B5		227	OR L	; PEK = NIL ?
009F	00 CAB100		228	JP Z,YESNIL	
			229	;	
00A2	23		230	INC HL	; PEK.SUCC = NIL ?
00A3	7E		231	LD A,(HL)	
00A4	2B		232	DEC HL	
00A5	B6		233	OR (HL)	
00A6	00 2B09		234	JR Z,YESNIL	
			235	;	
00A8	23		236	INC HL	
00A9	7E		237	LD A,(HL)	
00AA	2B		238	DEC HL	
00AB	6E		239	LD L,(HL)	
00AC	67		240	LD H,A	
			241	;	
00AD	00	00AD	242	NONIL EQU *	
00AD	EB		243	EX DE,HL	
00AE	F1		244	POP AF	
00AF	A7		245	AND A	; C I= 0
00B0	C9		246	RET	
			247	;	
00B1	00	00B1	248	YESNIL EQU *	
00B1	EB		249	EX DE,HL	
00B2	F1		250	POP AF	
00B3	37		251	SCF	; C I= 1
00B4	C9		252	RET	
			253	;	
			254	;LPRED, HXMTAR FÖREGÅENDE ELEMENT I LISTAN	
			255	; IN: DE PEK	
			256	; UT: DE PEK.SUCC C=0, OM PEK.SUCC<>NIL	
			257	; DE OFBRANDRAD C=1, OM PEK.SUCC=NIL	
			258	;	
00B5	00	00B5	259	LPRED EQU *	
00B5	F5		260	PUSH AF	
			261	;	
00B6	00 CD1C00		262	CALL HEAD	; LISTHUVUDET ?
			263	;	
00B9	EB		264	EX DE,HL	
00BA	00 DAB100		265	JP C,YESNIL	
			266	;	
00BD	23		267	INC HL	
00BE	23		268	INC HL	
00BF	7E		269	LD A,(HL)	
00C0	23		270	INC HL	
00C1	66		271	LD H,(HL)	
00C2	6F		272	LD L,A	
00C3	00 C3AD00		273	JP NONIL	
00C6			274	END	

ASMZ-4.46 LISTOR.ASM

ERRORS: 0 12:00:00 86-02-24 PAGE 7

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----			
<BOTRAM	0000	6	38 54				
>DEL	0079	178	9				
FILOP	0065	157	164				
FIOK	0073	165	160 162				
>FIRST	0061	154	10				
FBRSTA	0043	113	107				
>HEAD	001C	65	10 144	161	166	262	
>INLAST	0035	98	9				
LALOP	0052	137	142				
LACK	005B	143	140				
>LAST	0051	135	10 110				
>LPRED	0085	259	9 159	183			
>LSUCC	009B	222	9 139	156	196		
>NEW	0000	36	9				
NEWEXIT	0019	55	53				
NONIL	00AD	242	273				
NOTEMP	0031	86	74 80				
YESNIL	0081	248	228 234	265			

```

LOCATION PLC CODE  ARG  LC  SOURCE STATEMENT -----
0000  00          1      ZPROG REJSTRUC.ASM
0000          2      *PAGE 60
          3      ;
          4      ;
          5      ; GLOBALA RUTINER
          6      GLOBAL WRITELIST, READLIST, FINDTG
          7      ;
          8      ; GLOBALA KONSTANTER
          9      GLOBAL XSUCCL,XSUCCH,XPREDL,XPREDH,XSTATUS,XTG,XREPEAT
         10      GLOBAL XCOUNT,XANTAL,XSTR
         11      ;
         12      ; EXTERNA DATA
         13      EXTERNAL SUCC, PRED, STATUS, TG, REPEAT, COUNT, ANTAL
         14      EXTERNAL TGLISTA, STRANG
         15      ;
         16      ;
         17      ; *****
         18      ;
         19      ; REJSTRUC, INNEHALLER STRUKTUREN FOR TANGENTLISTAN
         20      ; OCH EN RUTIN WRITELIST, SOM LAGGER IN DATA I DET ELEMENT
         21      ; SOM DE PEKAR TILL. PA MOTSVARANDE VIS LASER READLIST.
         22      ;
         23      ; IN:
         24      ; DE - PEKARE TILL AKTIV ELEMENT
         25      ;
         26      ; MINNESVARIABLER
         27      ; SUCC - VIDAREPEKARE
         28      ; PRED - FÖREGÅENDE PEKARE
         29      ; STATUS
         30      ; TG - KOORDINAT
         31      ; REPEAT
         32      ; COUNT - HJÄLPVARIABLE
         33      ; ANTAL - ANTAL TECKEN I STRANG
         34      ;
         35      ;
         36      ; VER  DATUM  SIGN  BESKRIVNING
         37      ; 1.0  851103  SP      -
         38      ;
         39      ;
         40      ; *****
         41      ;
0000          42      XSUCCL  EQU  0      | +-----+
0000          43      XSUCCH  EQU  1      | !  SUCC  !
0000          44      XPREDL  EQU  2      | +-----+
0000          45      XPREDH  EQU  3      | !  PRED  !
         46      ; | +-----+
0000          47      XSTATUS  EQU  4      | !  STATUS !
         48      ; | +-----+
0000          49      XTG      EQU  5      | !    TG   !
         50      ; | +-----+
0000          51      XREPEAT  EQU  6      | ! REPEAT !
         52      ; | +-----+
0000          53      XCOUNT  EQU  7      | !  COUNT  !
         54      ; | +-----+
0000          55      XANTAL   EQU  8      | !  ANTAL  !
         56      ; | +-----+
0000          57      XSTR     EQU  9      | ! STRANG- !
         58      ; | !  START  !
         59      ; *EJECT
    
```

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT	
0000	00	0000	60	WRITELIST EQU *	
0000	E5		61	PUSH HL	
0001	D5		62	PUSH DE	
0002	DDE3		63	EX (SP),IX	
			64	;	
0004	X 3A0000		65	LD A,(STATUS)	; STATUS
0007	DD7704		66	LD (IX+XSTATUS),A	
			67	;	
000A	X 3A0000		68	LD A,(T6)	; T6
000D	DD7705		69	LD (IX+XT6),A	
			70	;	
0010	X 3A0000		71	LD A,(REPEAT)	; REPEAT
0013	DD7706		72	LD (IX+XREPEAT),A	
			73	;	
0016	X 3A0000		74	LD A,(COUNT)	; COUNT
0019	DD7707		75	LD (IX+XCOUNT),A	
			76	;	
001C	X 3A0000		77	LD A,(ANTAL)	; ANTAL
001F	DD7708		78	LD (IX+XANTAL),A	
0022	0600		79	LD B,0	
0024	4F		80	LD C,A	
			81	;	
0025	210900		82	LD HL,XSTR	; DE PEKAR PA STRANGUTRYNME
0028	19		83	ADD HL,DE	
0029	EB		84	EX DE,HL	
			85	;	
002A	X 2A0000		86	LD HL,(STRANG)	
002D	EDB0		87	LDIR	
			88	;	
002F	DDE3		89	EX (SP),IX	
0031	D1		90	POP DE	
0032	E1		91	POP HL	
0033	C9		92	RET	
			93	;	
			94	*EJECT	

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			95	;
0034	00	0034	96	READLIST EQU *
0034	E5		97	PUSH HL
0035	D5		98	PUSH DE
0036	DDE3		99	EX (SP),IX
			100	;
0038	DD6E00		101	LD L,(IX+XSUCCL) ; SUCC
003B	DD6601		102	LD H,(IX+XSUCCH)
003E	X 220000		103	LD (SUCC),HL
			104	;
0041	DD6E02		105	LD L,(IX+XPREDL) ; PRED
0044	DD6603		106	LD H,(IX+XPREDH)
0047	X 220000		107	LD (PRED),HL
			108	;
004A	DD7E04		109	LD A,(IX+XSTATUS) ; STATUS
004D	X 320000		110	LD (STATUS),A
			111	;
0050	DD7E05		112	LD A,(IX+XT6) ; T6
0053	X 320000		113	LD (T6),A
			114	;
0056	DD7E06		115	LD A,(IX+XREPEAT) ; REPEAT
0059	X 320000		116	LD (REPEAT),A
			117	;
005C	DD7E07		118	LD A,(IX+XCOUNT) ; COUNT
005F	X 320000		119	LD (COUNT),A
			120	;
0062	DD7E08		121	LD A,(IX+XANTAL) ; ANTAL
0065	X 320000		122	LD (ANTAL),A
			123	;
0068	210900		124	LD HL,XSTR
006B	19		125	ADD HL,DE
006C	X 220000		126	LD (STRANG),HL
			127	;
006F	DDE3		128	EX (SP),IX
0071	D1		129	POP DE
0072	E1		130	POP HL
0073	C9		131	RET
			132	;
			133	*EJECT

LOCATION	PLC CODE	ARB	LC	SOURCE STATEMENT
			134	;
			135	; FINDTG, LETAR I TGLISTAN EFTER TANGENT SOM FINNS I A RETURNERAR
			136	; DE SOM PEKARE TILL ELEMENT, C=1 => TG FANNS EJ
			137	;
0074	00	0074	138	FINDTG EQU *
0074	E5		139	PUSH HL
0075	F5		140	PUSH AF
0076	X 2A0000		141	LD HL,(TGLISTA)
			142	;
0079	00	0079	143	FL EQU * ; LISTA = NIL ?
0079	7C		144	LD A,H
007A	B5		145	OR L
007B	00 2B13		146	JR Z,NOTFIND
			147	;
007D	54		148	LD D,H ; PEK I= LISTA
007E	5D		149	LD E,L
			150	;
007F	23		151	INC HL ; LISTA.TG = A ?
0080	23		152	INC HL
0081	23		153	INC HL
0082	23		154	INC HL
0083	23		155	INC HL
0084	F1		156	POP AF
0085	BE		157	CP (HL)
0086	F5		158	PUSH AF
0087	00 2B0B		159	JR Z,FIND
0089	EB		160	EX DE,HL
008A	7E		161	LD A,(HL)
008B	23		162	INC HL
008C	66		163	LD H,(HL)
008D	6F		164	LD L,A
008E	00 1BE9		165	JR FL
			166	;
0090	00	0090	167	NOTFIND EQU *
0090	F1		168	POP AF
0091	E1		169	POP HL
0092	37		170	SCF
0093	C9		171	RET
			172	;
0094	00	0094	173	FIND EQU *
0094	F1		174	POP AF
0095	E1		175	POP HL
0096	A7		176	AND A
0097	C9		177	RET
0098			178	END

ERRORS : 0 WARNINGS : 0

ASMZ-4.46 REJSTRUC.ASM

ERRORS: 0 12:00:00 86-02-24 PAGE 5

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----	
<ANTAL	0000	13	77	122	
<COUNT	0000	13	74	119	
FIND	0094	173	159		
>FINDTB	0074	138	6		
FL	0079	143	165		
NOTFIND	0090	167	146		
<PRED	0000	13	107		
>READLIST	0034	96	6		
<REPEAT	0000	13	71	116	
<STATUS	0000	13	65	110	
<STRANG	0000	14	86	126	
<SUCC	0000	13	103		
<TB	0000	13	68	113	
<TGLISTA	0000	14	141		
>WRITELIS	0000	60	6		
>XANTAL	0008	55	10	78	121
>XCOUNT	0007	53	10	75	118
>XPREDH	0003	45	9	106	
>XPREDL	0002	44	9	105	
>XREPEAT	0006	51	9	72	115
>XSTATUS	0004	47	9	66	109
>XSTR	0009	57	10	82	124
>XSUCCH	0001	43	9	102	
>XSUCCL	0000	42	9	101	
>XTB	0005	49	9	69	112

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROG OMVANDL.ASM
0000			2	*PAGE 60
			3	;
			4	GLOBAL DECBIN,BINDEC, BIN2DEC
			5	;
			6	;
			7	*****
			8	;
			9	OMVANDL, INNEHALLER RUTINER FÖR BINÄRT TILL ASCII OCH ASCII
			10	TILL BINÄRT.
			11	;
			12	;
			13	VER DATUM SIGN BESKRIVNING
			14	1.0 850501 SP -
			15	1.1 851108 SP BIN2DEC
			16	;
			17	;
			18	;
			19	*****
			20	;
			21	;
			22	;
			23	;
			24	DECIMAL TILL BINÄR OMVÄNDNING ;
			25	*****
			26	;
			27	IN HL BUFFERT
			28	UT A TAL
			29	;
			30	HL PEKAR PÅ FÖRSTA BYTE EFTER TALET
			31	;
0000	00	0000	32	DECBIN EQU *
0000	D5		33	PUSH DE
0001	2B		34	DEC HL
0002	1E00		35	LD E,0
			36	;
0004	23		37	DBLOOP INC HL
0005	7E		38	LD A,(HL)
0006	E67F		39	AND 127
0008	D630		40	SUB 48
000A	00 3812		41	JR C,UTDECBIN ; MINDRE ÄN "0"
			42	;
000C	FE0A		43	CP 10
000E	00 300E		44	JR NC,UTDECBIN ; STÖRRE ÄN "9"
			45	;
0010	57		46	LD D,A ; E = 10*E+A
0011	7B		47	LD A,E
0012	CB27		48	SLA A
0014	CB27		49	SLA A
0016	CB27		50	SLA A
0018	83		51	ADD A,E
0019	83		52	ADD A,E
001A	82		53	ADD A,D
001B	5F		54	LD E,A
001C	00 18E6		55	JR DBLOOP
			56	;
001E	7B		57	UTDECBIN LD A,E
001F	D1		58	POP DE
0020	C9		59	RET
			60	;
			61	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			62	
			63	BINAR TILL DECIMAL OMVANDLING
			64	*****
			65	
			66	IN HL BUFFERTPEKARE
			67	IN A TAL ATT OMVANDLA
			68	
			69	HL PEKAR PA FÖRSTA TAL EFTER "A" STRANG
			70	
0021	00	0021	71	BINDEC EQU *
0021	C5		72	PUSH BC
			73	CP 100
			74	JR C,TIOTAL
0022	0664		75	LD B,100
0024	00 CD3600		76	CALL MASK
0027	23		77	INC HL
			78	JR BIN2
			79	TIOTAL CP 10
			80	JR C,ENTAL
			81	BIN2 EQU *
0028	060A		82	LD B,10 ; TIOTAL
002A	00 CD3600		83	CALL MASK
002D	23		84	INC HL
002E	C630		85	ENTAL ADD 48
0030	77		86	LD (HL),A
0031	23		87	INC HL
0032	3620		88	LD (HL),32
0034	C1		89	POP BC
0035	C9		90	RET
			91	
0036	3630		92	MASK LD (HL),48
0038	B8		93	MASKLOOP CP B
0039	00 3001		94	JR NC,B1
003B	C9		95	RET
003C	34		96	B1 INC (HL)
003D	90		97	SUB B
003E	00 18FB		98	JR MASKLOOP
			99	
			100	
			101	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			102	;
			103	;
			104	;
			105	;
			106	;
			107	;
			108	;
			109	;
			110	;
0040	00	0040	111	BIN2DEC EQU *
0040	C5		112	PUSH BC
0041	F5		113	PUSH AF
0042	011027		114	LD BC,10000
0045	00 CD6400		115	CALL EXP
0048	01EB03		116	LD BC,1000
0048	00 CD6400		117	CALL EXP
004E	016400		118	LD BC,100
0051	00 CD6400		119	CALL EXP
0054	010A00		120	LD BC,10
0057	00 CD6400		121	CALL EXP
005A	7B		122	LD A,E
005B	C630		123	ADD 4B
005D	77		124	LD (HL),A
005E	23		125	INC HL
005F	3620		126	LD (HL),*
0061	F1		127	POP AF
0062	C1		128	POP BC
0063	C9		129	RET
			130	;
0064	AF		131	EXP XOR A
0065	EB		132	EX DE,HL
0066	00 ED42	0066	133	EXPL EQU *
0066	00 3803		134	SBC HL,BC
006A	3C		135	JR C,EX00K
006A	00 18F9		136	INC A
006B	00		137	JR EXPL
006D	00	006D	138	EX00K EQU *
006D	09		139	ADD HL,BC
006E	EB		140	EX DE,HL
006F	C630		141	ADD 4B
0071	77		142	LD (HL),A
0072	23		143	INC HL
0073	C9		144	RET
0074			145	END

ERRORS : 0 WARNINGS : 0

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES	-----		
BI	003C	96	94			
>BIN2DEC	0040	111	4			
>BINDEC	0021	71	4			
DBLOOP	-0004	37	55			
>DECBIN	0000	32	4			
?ENTAL	002E	85				
EXOOK	006D	138	135			
EXP	0064	131	115 117 119 121			
EXPL	0066	133	137			
MASK	0036	92	76 83			
MASKLOOP	003B	93	98			
UTDECBIN	001E	57	41 44			

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROG REJDEF.ASM
0000			2	*PAGE 60
			3	;
			4	;
			5	; GLOBALA DATA
			6	GLOBAL STACK
			7	GLOBAL IBPEKIN, IBPEKUT, IBSTART, IBEND
			8	GLOBAL UBPEKIN, UBPEKUT, UBSTART, UBEND, UBANTAL
			9	GLOBAL BUFFERT
			10	GLOBAL BOTRAM, STARTRAM
			11	GLOBAL SUCC,PRED,STATUS, TG, REPEAT, COUNT, ANTAL, STRANG
			12	GLOBAL TGLISTA, TGPRED
			13	GLOBAL PEK,TINE
			14	GLOBAL VARV, STUDS, AUTOR, PROGSTAT, DIODSTAT
			15	;
			16	*****
			17	;
			18	;
			19	VER DATUM SIGN BESKRIVNING
			20	1.0 850926 SP -
			21	;
			22	;
			23	*****
			24	;
			25	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			26	;
			27	;
			28	DEFINITIONER
			29	=====
			30	;
0000			30	DEFS 256 ; STACKDJUP 256 BYTE
0100	00	0100	31	STACK EQU * ; STACK
			32	;
0100	00		33	STUDS DEFB 0 ; KONTAKTSTUDSTID
0101	00		34	AUTOR DEFB 0 ; TID INNAH AUTOREPEAT BBJAR
0102	00		35	TIME DEFB 0
0103	00		36	VARV DEFB 0
0104	00		37	PROGSTAT DEFB 0
0105	00		38	DIDSTAT DEFB 0
			39	;
0106	0000		40	TGLISTA DEFW 0
0108	00 0601		41	TGPRED DEFW TGLISTA
			42	;
010A	0000		43	PEK DEFW 0 ; HJALPPEKARE
010C	0000		44	SUCC DEFW 0 ; VIDAREPEKARE
010E	0000		45	PRED DEFW 0 ; FÖREGAENDE PEKARE
0110	00		46	STATUS DEFB 0
0111	00		47	TG DEFB 0
0112	00		48	REPEAT DEFB 0
0113	00		49	COUNT DEFB 0
0114	00		50	ANTAL DEFB 0
0115	0000		51	STRANG DEFW 0
			52	;
			53	;
0117			54	BUFFERT DEFS 40
			55	;
013F	0000		56	IBPEKIN DEFW 0
0141	0000		57	IBPEKUT DEFW 0
0143			58	IBSTART DEFS 80
0193	00	0193	59	IBEND EQU *
			60	;
0193	00		61	UBANTAL DEFB 0
0194	0000		62	UBPEKIN DEFW 0
0196	0000		63	UBPEKUT DEFW 0
0198			64	UBSTART DEFS 80
01E8	00	01E8	65	UBEND EQU *
			66	;
			67	;
01E8	00 EA01		68	BOTRAM DEFW STARTRAM
01EA	00	01EA	69	STARTRAM EQU *
			70	;
01EA			71	END

ERRORS : 0 WARNINGS : 0

ASHZ-4.46 REJDEF.ASM
 CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES
>ANTAL	0114	50	11
>AUTOR	0101	34	14
>BOTRAM	01EB	68	10
>BUFFERT	0117	54	9
>COUNT	0113	49	11
>DIODSTAT	0105	38	14
>IBEND	0193	59	7
>IBPEKIN	013F	56	7
>IBPEKUT	0141	57	7
>IBSTART	0143	58	7
>PEK	010A	43	13
>PRED	010E	45	11
>PROGSTAT	0104	37	14
>REPEAT	0112	48	11
>STACK	0100	31	6
>STARTRAM	01EA	69	10 68
>STATUS	0110	46	11
>STRANG	0115	51	11
>STUDS	0100	33	14
>SUCC	010C	44	11
>TG	0111	47	11
>TGLISTA	0106	40	12 41
>TGPRED	0108	41	12
>TIME	0102	35	13
>UBANTAL	0193	61	8
>UBEND	01EB	65	8
>UBPEKIN	0194	62	8
>UBPEKUT	0196	63	8
>UBSTART	0198	64	8
>VARV	0103	36	14

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0000	00		1	ZPROG TEST
0000			2	*PAGE 60
			3	;
			4	EXTERNAL BUFFERT,RECEIVE
			5	EXTERNAL HEADLOOP, BINDEC
			6	EXTERNAL INITMEN, KLOCKA
			7	;
			8	GLOBAL SKRSTR, ENDBYTE
			9	GLOBAL SIOADTA,SIOACMD
			10	GLOBAL RESET
			11	;
			12	*****
			13	EGEN TANGENTBORDSRUTIN.
			14	;
			15	FUNGERAR MOT AVBROTT MOT TANGENTBORDET PA MOTSVARANDE
			16	SATT SOM MOT V24 SNITT I ENKORTSDATORN.
			17	;
			18	*****
			19	;
			20	;
0000		0022	21	SIOADTA EQU 34
0000		0023	22	SIOACMD EQU 35
0000		0000	23	ENDBYTE EQU 13 ; CR = SLUT PA CMDSTRANG
0000	00	0000	24	TANG EQU *
			25	;
0000	00	0000	26	RESET EQU *
0000	3E00		27	LD A,0
0002	D301		28	OUT 1,A ; NOLLSTALL ALLA I/O KORT
			29	;
0004	X 210000		30	LD HL,KLOCKA
0007	22D6FF		31	LD (65494),HL
			32	;
000A	X CD0000		33	CALL INITMEN ; INITIERAR VARIABLER MM
			34	;
0000	00 111700		35	LD DE,TANGENT
0010	ED53B4FF		36	LD (65460),DE
			37	;
0014	X C30000		38	JP HEADLOOP
			39	;
0017	00	0017	40	TANGENT EQU *
0017	X C30000		41	JP RECEIVE
			42	;
			43	;
001A	0000		44	STACK DEFB 0,0
			45	;
			46	;
001C	00	001C	47	LASSTR EQU *
001C	010002		48	LD BC,512 ; MAX 512 TECKEN
001F	CD0500		49	CALL 5
0022	C9		50	RET
			51	;
0023	00	0023	52	SKRSTR EQU *
0023	D5		53	PUSH DE
0024	CD0800		54	CALL 11
0027	D1		55	POP DE
0028	C9		56	RET
			57	;
0029	FB		58	EIRETI EI
002A	ED4D		59	RETI
			60	;

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			61	;
002C	00	002C	62	DOS EQU *
002C	213E04		63	LD HL,1086
002F	22B4FF		64	LD (65460),HL
0032	21763A		65	LD HL,14966
0035	22D6FF		66	LD (65494),HL ; KLOCK AVBROTTSRUTIN
0038	F1		67	POP AF
0039	00 CD2900		68	CALL EIRETI
003C	00 ED731A00		69	LD (STACK),SP
0040	00 2A1A00		70	LD HL,(STACK)
0043	00 CD4900		71	CALL SKRORD
0046	C303C1		72	JP 0C103H ; ATERSTART CMDINT
			73	;
0049	00	0049	74	SKRORD EQU *
0049	F5		75	PUSH AF
004A	E5		76	PUSH HL
004B	C5		77	PUSH BC
004C	D5		78	PUSH DE
004D	7C		79	LD A,H
004E	45		80	LD B,L
004F	X 210000		81	LD HL,BUFFERT
0052	X CD0000		82	CALL BINDEC
0055	7B		83	LD A,B
0056	23		84	INC HL
0057	363A		85	LD (HL),*"
0059	X CD0000		86	CALL BINDEC
005C	360D		87	LD (HL),13
005E	23		88	INC HL
005F	360A		89	LD (HL),10
0061	X 210000		90	LD HL,BUFFERT
0064	010900		91	LD BC,9
0067	CD0B00		92	CALL 11
006A	D1		93	POP DE
006B	C1		94	POP BC
006C	E1		95	POP HL
006D	F1		96	PDP AF
006E	C9		97	RET
006F	00 0000		98	END TANG

ERRORS : 0 WARNINGS : 0

CROSS REFERENCE LISTING

SYMBOL	LOCATION	DECL	REFERENCES
<BINDEC	0000	5	82 86
<BUFFERT	0000	4	81 90
?DOS	002C	62	
EIRETI	0029	58	68
>ENDBYTE	000D	23	8
<HEADLOOP	0000	5	38
<INITMEN	0000	6	33
<KLOCKA	0000	6	30
?LASSTR	001C	47	
<RECEIVE	0000	4	41
>RESET	0000	26	10
>SIOACHD	0023	22	9
>SIOADTA	0022	21	9
SKRORD	0049	74	71
>SKRSTR	0023	52	8
STACK	001A	44	69 70
TANG	0000	24	98
TANGENT	0017	40	35

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LOCATION PLC CODE   ARG   LC   SOURCE STATEMENT -----
0000  00           1       ZPRG LISTTEST.ASH
0000           2       *PAGE 60
3       ;
4       ;
5       EXTERNAL BINDEC, BIN2DEC, READLIST
6       EXTERNAL STATUS,TB,REPEAT,SUCC,PRED,ANTAL,STRANG
7       EXTERNAL BUFFERT,TGLISTA,LSUCC, HEAD
8       EXTERNAL SKRSTR
9       ;
10      GLOBAL SKRPOST, SKRLIST
11      ;
12      ;
13      ;
14      ; *****
15      LISTTEST, INNEHALLER SKRLISTA SOM SKRIVER UT HELA LISTAN OCH
16      SKRPOST SOM SKRIVER UT DEN POST DE PEKAR PA
17      ;
18      ;
19      ;
20      VER   DATUM  SIGN   BESKRIVNING
21      1.0   851103  SP     -
22      1.1   851107  SP     KLARAR TOM LISTA OCH LISTHUVUD
23      ;
24      ;
25      ;
26      ; *****
27      ;
28      ;
29      *EJECT

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LOCATION	PLC	CÖDE	ARG	LC	SOURCE STATEMENT
				30	;
				31	; SKRPOST(PEK), SKRIVER UT POSTENS INNEHALL PA SKARMEN
				32	; I FORMEN STATUS,T6,REPEAT SUCC,PRED ANTAL,"STRANG"
				33	; IN: DE PEKARE TILL POST
				34	; UT: OFGRÄNDRAT
				35	;
0000	00		0000	36	SKRPOST EQU *
0000		D5		37	PUSH DE
0001		C5		38	PUSH BC
0002		E5		39	PUSH HL
				40	;
0003		7A		41	LD A,D
0004		B3		42	OR E
0005	00	CAB700		43	JP Z,EMPTY
				44	;
0008	X	CD0000		45	CALL HEAD ; PEKARE = LISTHUVUD ?
0008	00	DAB700		46	JP C,EMPTY
				47	;
000E	X	CD0000		48	CALL READLIST
				49	;
0011	X	210000		50	LD HL,BUFFERT
0014	X	3A0000		51	LD A,(STATUS)
0017	X	CD0000		52	CALL BINDEC
001A		23		53	INC HL
				54	;
001B	X	3A0000		55	LD A,(T6)
001E		E638		56	AND 00111000B
0020		OF		57	RRCA
0021		OF		58	RRCA
0022		OF		59	RRCA
0023		C641		60	ADD 65 ; A:H
0025		77		61	LD (HL),A
0026		23		62	INC HL
0027	X	3A0000		63	LD A,(T6)
002A		E607		64	AND 00000111B
002C		C631		65	ADD 49 ; 1:B
002E		77		66	LD (HL),A
002F		23		67	INC HL
0030		3620		68	LD (HL),"
0032		23		69	INC HL
0033		3620		70	LD (HL),"
0035		23		71	INC HL
				72	;
0036	X	3A0000		73	LD A,(REPEAT)
0039	X	CD0000		74	CALL BINDEC
003C		23		75	INC HL
003D		3620		76	LD (HL),"
003F		23		77	INC HL
0040		3620		78	LD (HL),"
0042		23		79	INC HL
				80	;
0043	X	ED5B0000		81	LD DE,(SUCC)
0047	X	CD0000		82	CALL BIN2DEC
004A		363A		83	LD (HL),";"
004C		23		84	INC HL
				85	;
004D	X	ED5B0000		86	LD DE,(PRED)
0051	X	CD0000		87	CALL BIN2DEC
0054		23		88	INC HL
				89	;

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
0055	3620		90	LD (HL), * *
0057	23		91	INC HL
0058	3620		92	LD (HL), * *
005A	X 3A0000		93	LD A, (ANTAL)
005D	X CD0000		94	CALL @INDEC
0060	23		95	INC HL
			96 ;	
0061	X 210000		97	LD HL, BUFFERT
0064	011F00		98	LD BC, 31
0067	X CD0000		99	CALL SKRSTR
			100 ;	
006A	X 3A0000		101	LD A, (ANTAL)
006D	4F		102	LD C, A
006E	0600		103	LD B, 0
0070	X 2A0000		104	LD HL, (STRANG)
0073	X CD0000		105	CALL SKRSTR
			106 ;	
0076	X 210000		107	LD HL, BUFFERT
0079	360D		108	LD (HL), 13
007B	23		109	INC HL
007C	360A		110	LD (HL), 10
007E	X 210000		111	LD HL, BUFFERT
0081	010200		112	LD BC, 2
0084	X CD0000		113	CALL SKRSTR
			114 ;	
0087	00	0087	115	EMPTY EQU *
0087	E1		116	POP HL
0088	C1		117	POP BC
0089	D1		118	POP DE
008A	C9		119	RET
			120 ;	
			121	*EJECT

LOCATION	PLC CODE	ARG	LC	SOURCE STATEMENT
			122	;
			123	; SKRLIST, SKRIVER UT HELA LISTAN TGLISTA ENLIST FORMAT I SKRPOST
			124	; INGA PARAMETRAR
			125	;
008B	00	008B	126	SKRLIST EQU *
008B	D5		127	PUSH DE
008C	X ED5B0000		128	LD DE,(TGLISTA)
0090	00	0090	129	SKLOOP EQU *
0090	00 CD0000		130	CALL SKRPOST
0093	X CD0000		131	CALL LSUCC
0096	00 30FB		132	JR NC,SKLOOP
0098	D1		133	POP DE
0099	C9		134	RET
			135	;
009A			136	END

ERRORS : 0 WARNINGS : 0

ASN2-4.46 LISTTEST.ASM
CROSS REFERENCE LISTING

ERRORS: 0 12:00:00 86-02-24

SYMBOL	LOCATION	DECL	REFERENCES	-----	
<ANTAL	0000	6	93 101		
<BIN2DEC	0000	5	82 87		
<BINDEC	0000	5	52 74	94	
<BUFFERT	0000	7	50 97	107	111
EMPTY	0087	115	43 46		
<HEAD	0000	7	45		
<LSUCC	0000	7	131		
<PRED	0000	6	86		
<READLIST	0000	5	48		
<REPEAT	0000	6	73		
SKLOOP	0090	129	132		
>SKRLIST	008B	126	10		
>SKRPOST	0000	36	10 130		
<SKRSTR	0000	8	99 105	113	
<STATUS	0000	6	51		
<STRXNG	0000	6	104		
<SUCC	0000	6	81		
<TG	0000	6	55 63		
<TGLISTA	0000	7	128		

Länkingsförfarande

Samtliga program är asemeblerade med Luxors assembler ASMZ, och länkade med motsvarande Estab.

Följande kommandofil har använts vid länkningen av originalversionen:

```
TASK REJPROM
ORG 0
INC INITSIO
INC REJINTER
INC BKRSTR
INC REJINIT
INC REJHEAD
INC REJCMD
INC REJLEX
INC LISTOR
INC REJSTRUC
INC OMVANDL
ORG 57344
INC REJDEF
CHECK
END
```

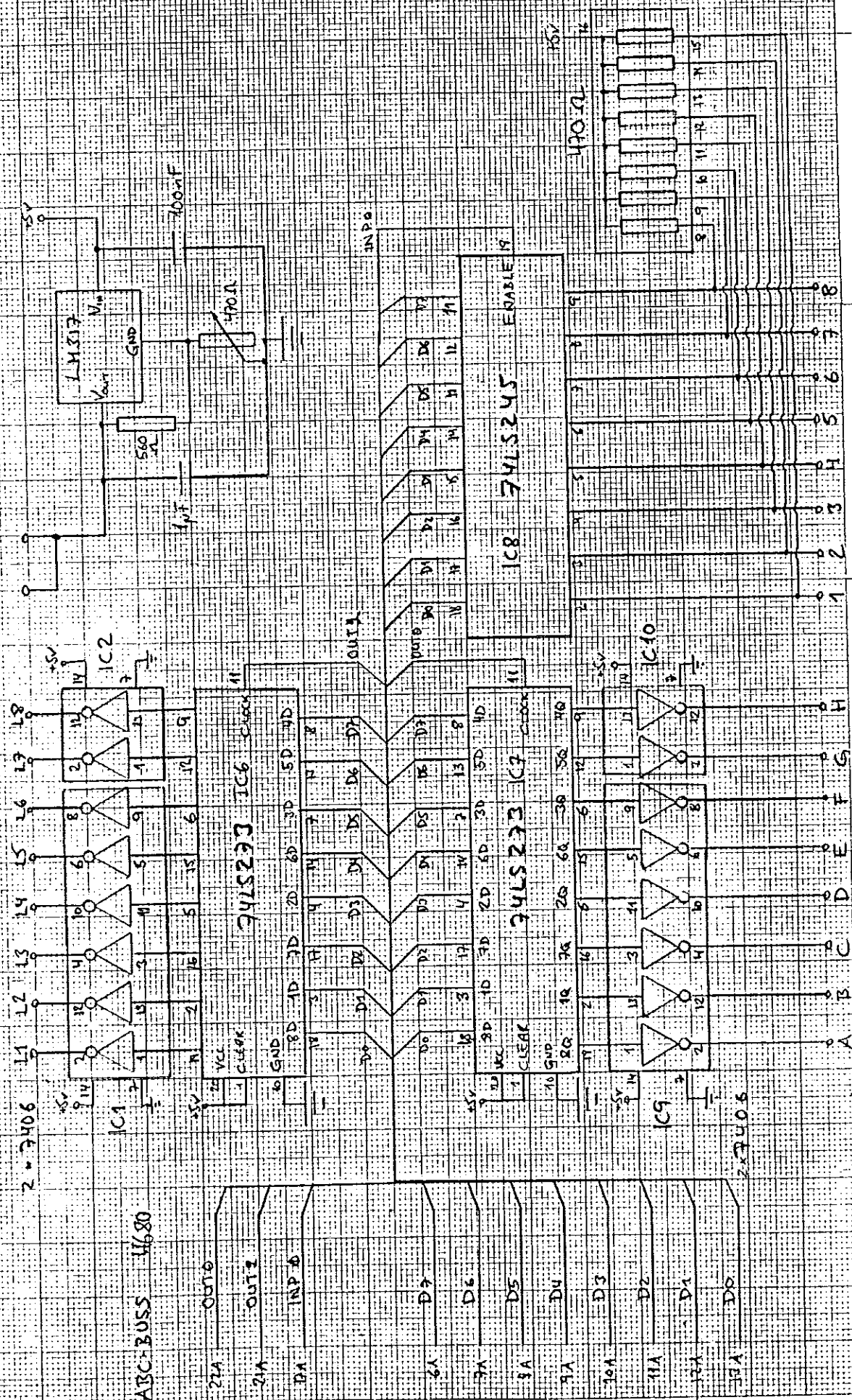
Vilket visar vilka de ingående modulerna är.

För utveckling av programmet har vissa moduler bytts för att simulera enkortsdatorn. Detta möjliggör utvärdering av programmet under körning mot en av Luxors datorer i 800 serien. Den kommando fil som då använts är:

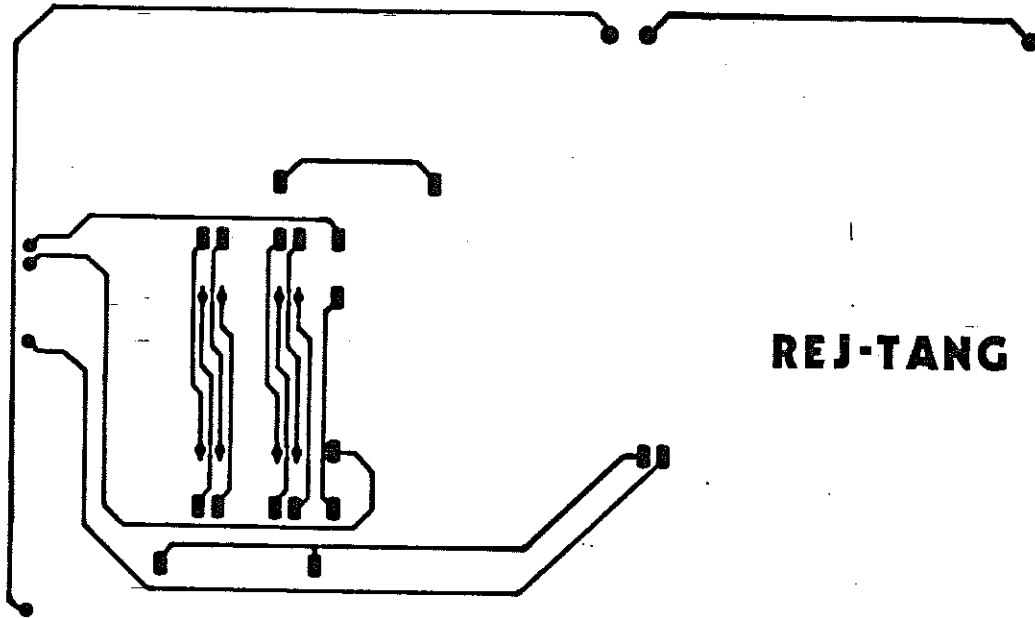
```
TASK REJ
ORG 55000
INC TEST
INC REJINTER
INC LISTTEST
INC REJHEAD
INC REJCMD
INC REJINIT
INC REJLEX
INC LISTOR
INC REJSTRUC
INC OMVANDL
INC REJDEF
CHECK
END
```


I/O - KORT REITANG (DEL 1 (2))

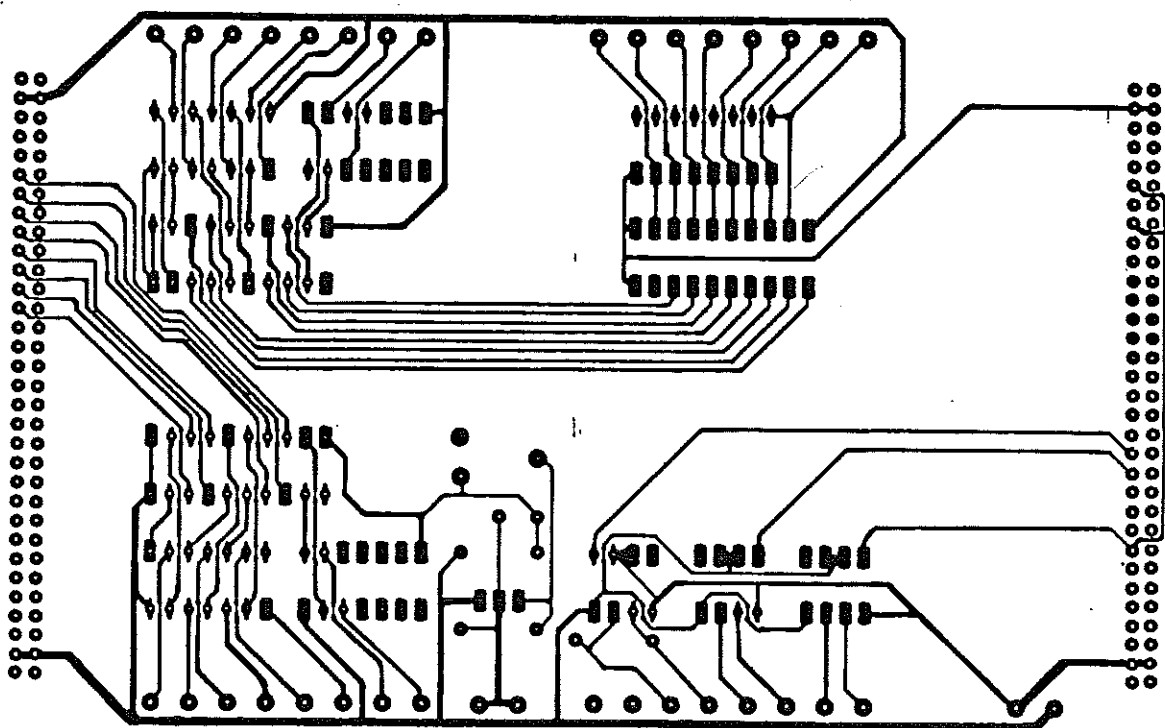
125V → 2.3V



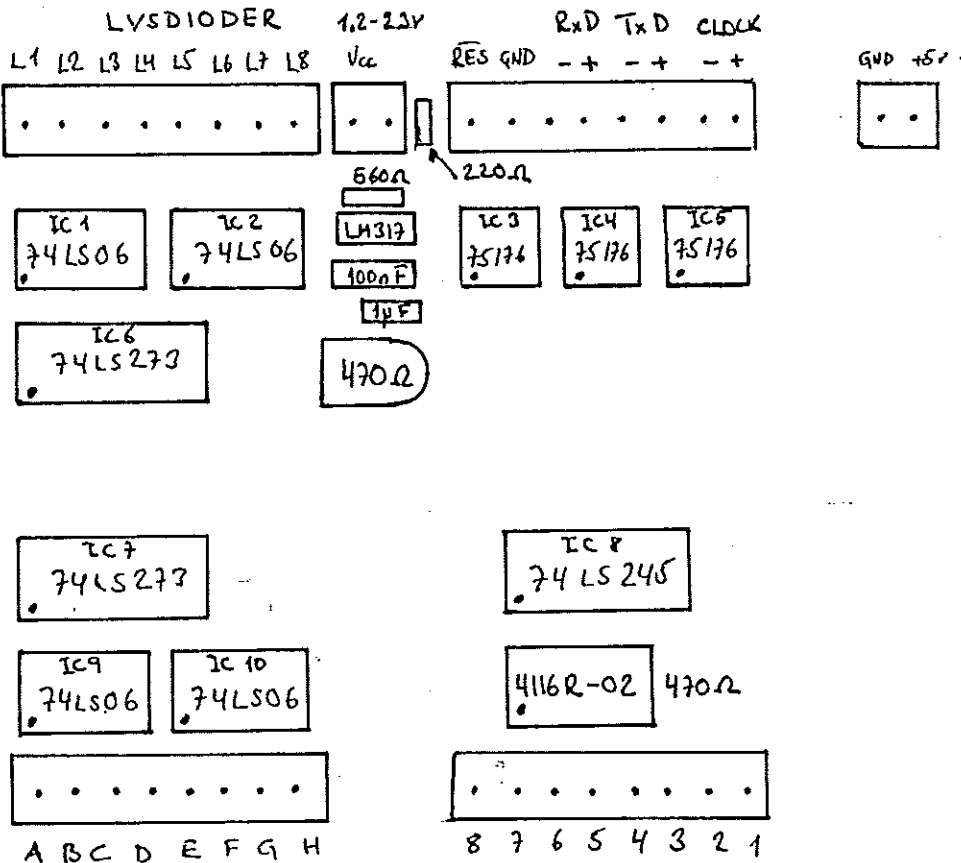
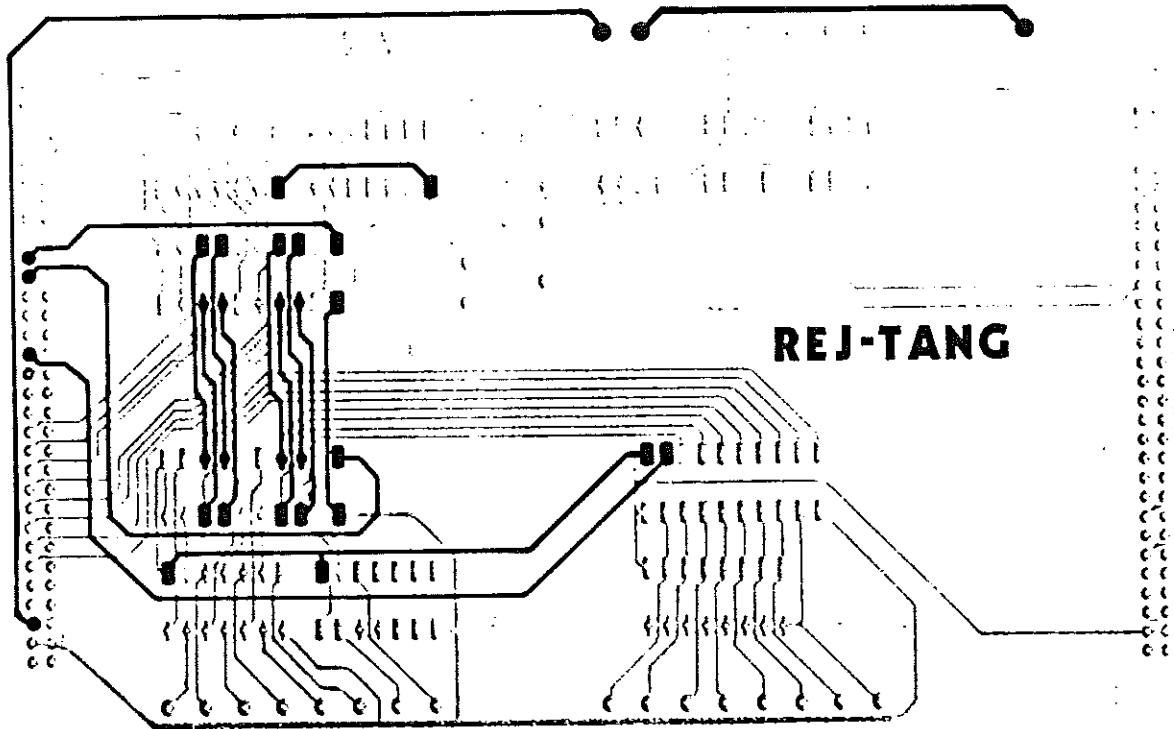
LAYOUT I/O - KORT



REJ-TANG



KOMPONENT PLACERING I/O-KORT

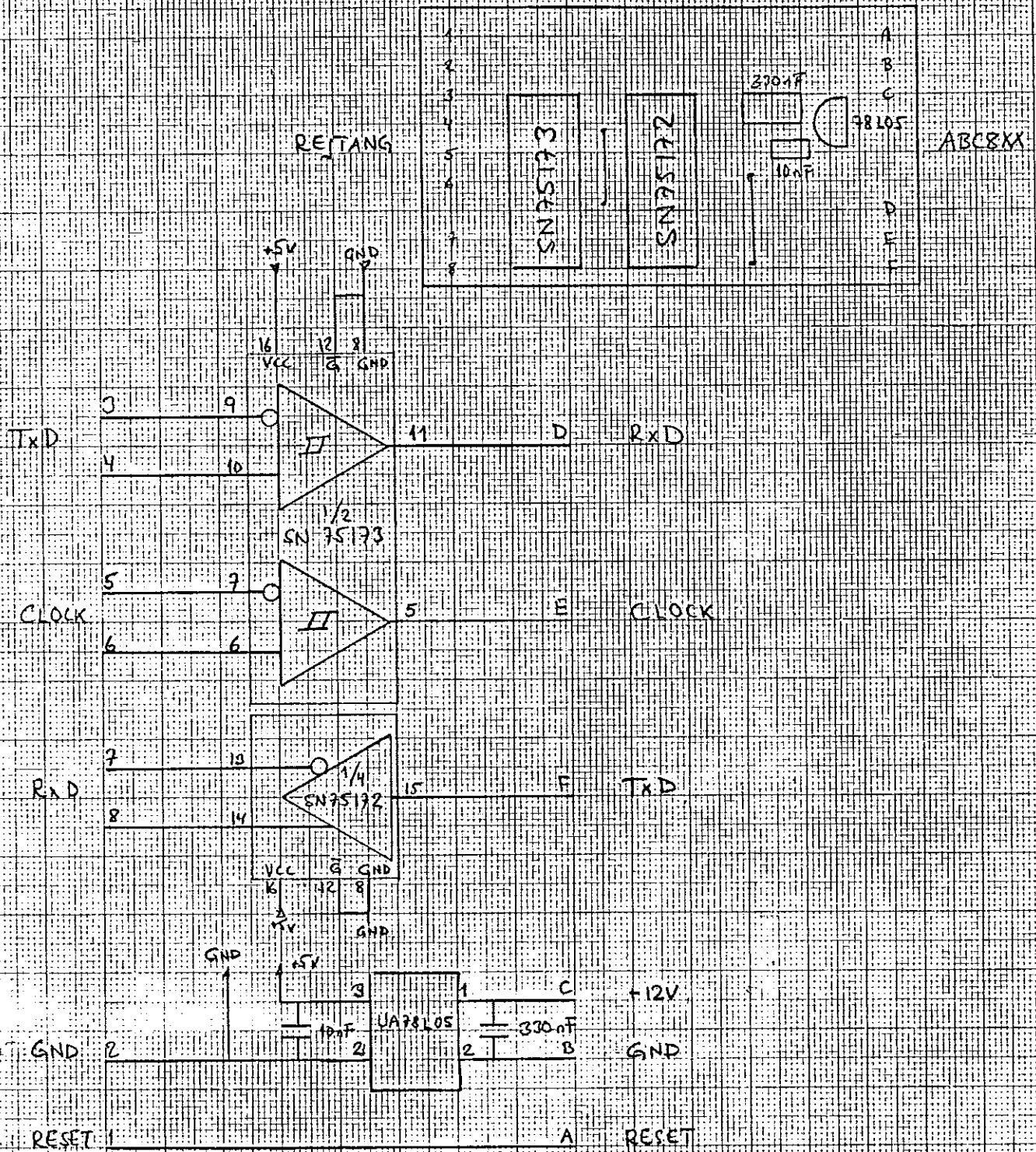


4680
BUSS

"V24"
BUSS

TANGENTER

RS-485 → TTL INTERFACE



ASIXI 11.6

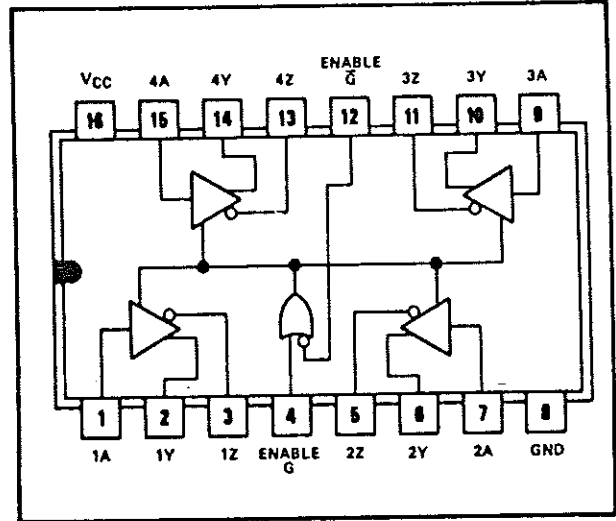
INTERFACE CIRCUITS

TYPE SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12769, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range ... -7 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Functionally Interchangeable With AM26LS31

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = Irrelevant
Z = high Impedance (off)

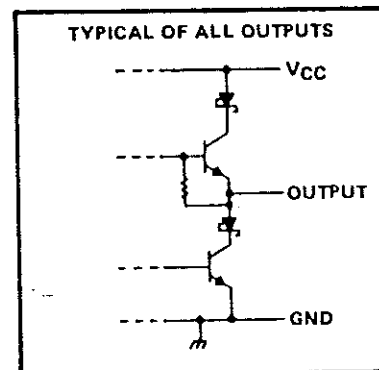
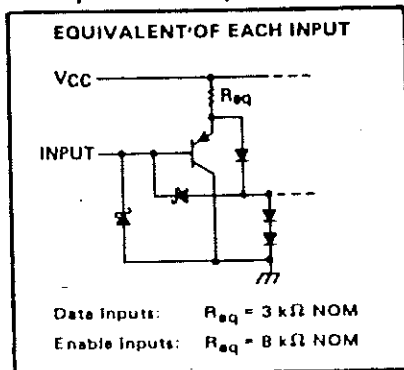
description

The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standard RS-422A and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission-bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



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TYPE SN75172

QUADRUPLE DIFFERENTIAL LINE DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1375 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package	260°C

- NOTES: 1. All voltage values are with respect to the network ground terminal.
 2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75172 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode output voltage, V_{OC}	-7 [†]		12	V
High-level output current, I_{OH}			-60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

[†]The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet with common-mode output voltage only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless other noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT	
V_{IH}	High-level input voltage		2		V	
V_{IL}	Low-level input voltage			0.8	V	
V_{IK}	Input clamp voltage	$I_I = -18$ mA		-1.5	V	
V_{OH}	High-level output voltage	$V_{IH} = 2$ V, $I_{OH} = -33$ mA	$V_{IL} = 0.8$ V,	3.7	V	
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $I_{OL} = 33$ mA	$V_{IL} = 0.8$ V,	1.1	V	
$ V_{OD1} $	Differential output voltage	$I_O = 0$		$2V_{OD2}$	V	
$ V_{OD2} $	Differential output voltage	$R_L = 100 \Omega$, $R_L = 60 \Omega$,	See Figure 1 See Figure 1	2 1.5	V	
$\Delta V_{OD} $	Change in magnitude of differential output voltage [§]	$R_L = 60 \Omega$ or 100Ω , See Figure 1		± 0.2	V	
V_{OC}	Common-mode output voltage [¶]			3	V	
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage [§]			± 0.2	V	
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7$ V to 12 V		± 100	μ A	
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V		± 100	μ A	
I_{IH}	High-level input current	$V_I = 2.7$ V		20	μ A	
I_{IL}	Low-level input current	$V_I = 0.5$ V		-360	μ A	
I_{OS}	Short-circuit output current	$V_O = -7$ V		-180	mA	
		$V_O = V_{CC}$		180		
		$V_O = 12$ V		500		
I_{CC}	Supply current (all drivers)	No load	Outputs enabled	38	60	mA
			Outputs disabled	18	40	

[‡]All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ$ C.

[§] $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

[¶]In EIA Standard RS-422A, V_{OC} , which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

TYPE SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	$R_L = 60\ \Omega$, See Figure 2		35	50	ns
t_{TD}			50	75	ns
t_{PLH}	$R_L = 27\ \Omega$, See Figure 3		16	25	ns
t_{PHL}			44	65	ns
t_{PZH}	$R_L = 110\ \Omega$, See Figure 4		60	80	ns
t_{PZL}	$R_L = 110\ \Omega$, See Figure 5		30	45	ns
t_{PHZ}	$R_L = 110\ \Omega$, See Figure 4		51	75	ns
t_{PLZ}	$R_L = 110\ \Omega$, See Figure 5		18	30	ns

PARAMETER MEASUREMENT INFORMATION

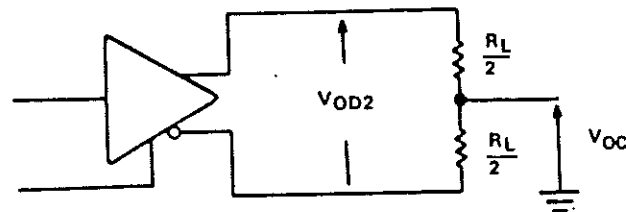
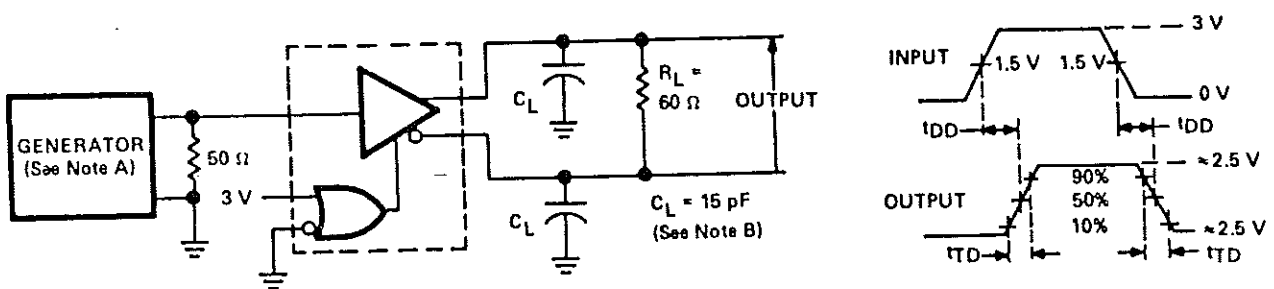


FIGURE 1—DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

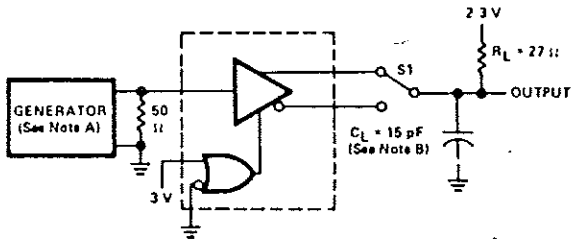
VOLTAGE WAVEFORMS

- NOTES
- A The input pulse is supplied by a generator having the following characteristics $t_r < 5\text{ ns}$, $t_f < 5\text{ ns}$, $\text{PRR} = 1\text{ MHz}$, duty cycle = 50%, $Z_o = 50\ \Omega$
 - B C_L includes probe and stray capacitance.
 - C All diodes are IN916 or IN3064.

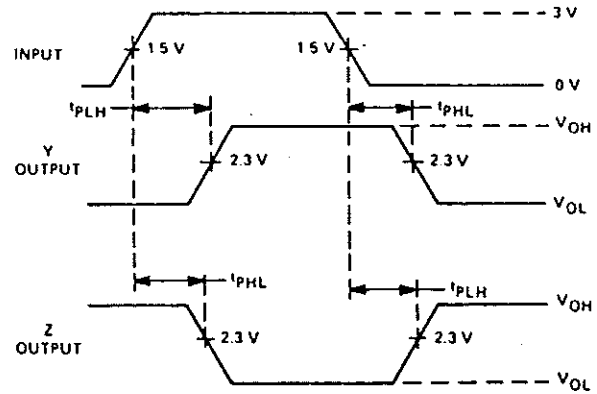
FIGURE 2—DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

TYPE SN75172
 QUADRUPLE DIFFERENTIAL LINE DRIVER

PARAMETER MEASUREMENT INFORMATION

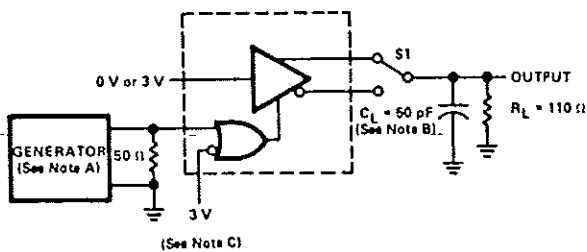


TEST CIRCUIT

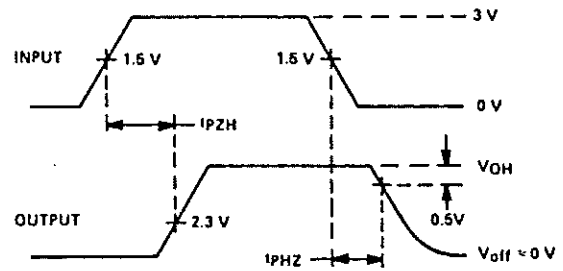


VOLTAGE WAVEFORMS

FIGURE 3—PROPAGATION DELAY TIMES

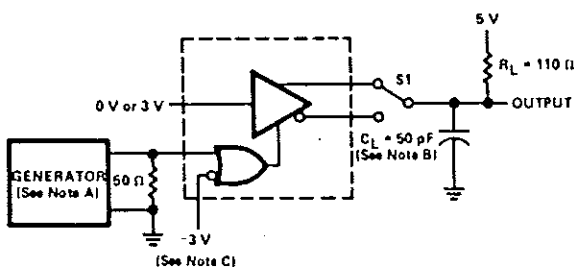


TEST CIRCUIT

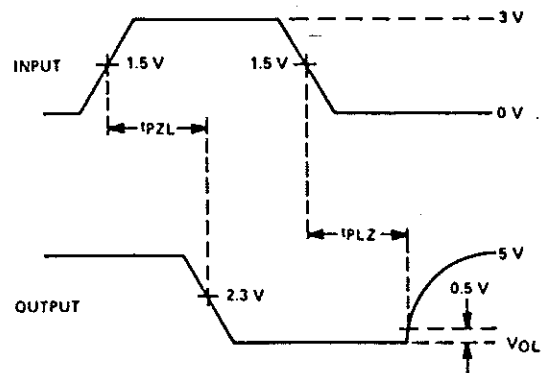


VOLTAGE WAVEFORMS

FIGURE 4— t_{pZH} AND t_{pHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 5— t_{pZL} AND t_{pLZ}

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f < 5$ ns, $t_r < 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} = 50 \Omega$.
 B. C_L include probe and jig capacitance.
 C. To test the active low enable \bar{G} , ground G and apply an inverted waveform to \bar{G} .

TYPE SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

TYPICAL CHARACTERISTICS

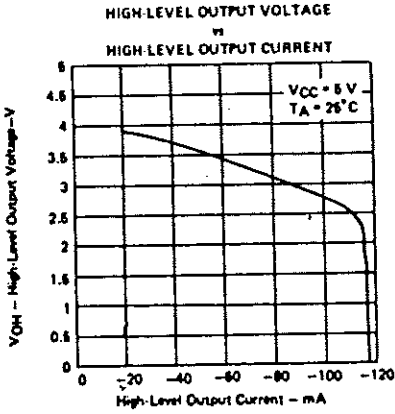


FIGURE 6

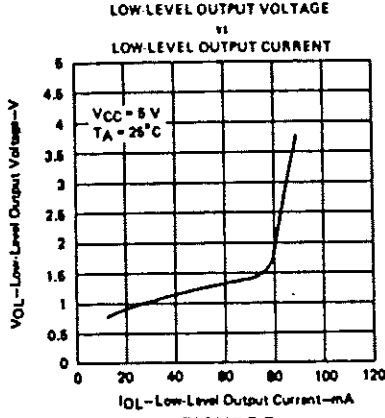


FIGURE 7

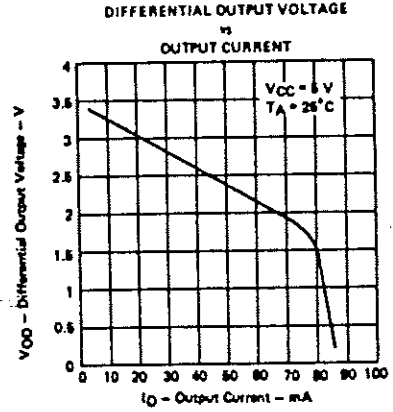


FIGURE 8

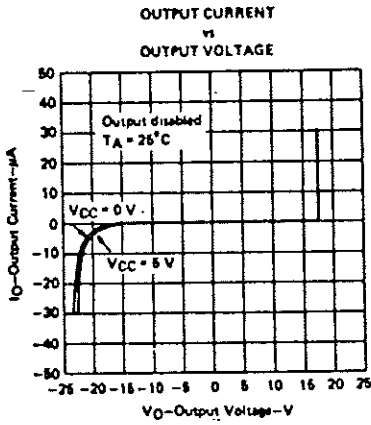


FIGURE 9

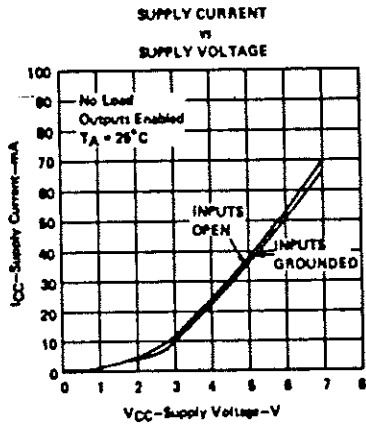


FIGURE 10

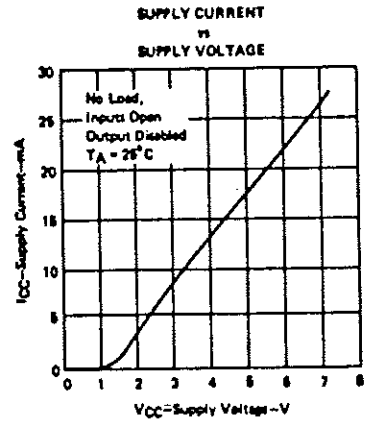
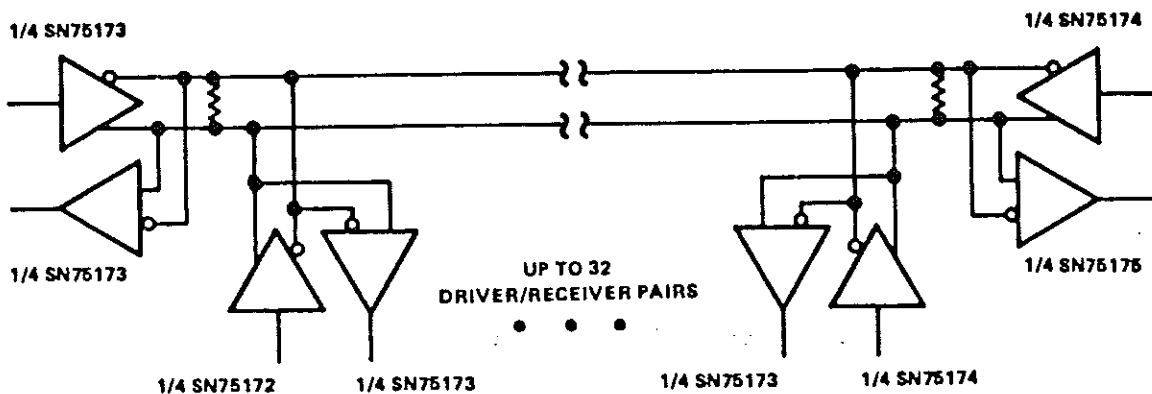


FIGURE 11

5

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 12

INTERFACE CIRCUITS

TYPE SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12770, OCTOBER 1980

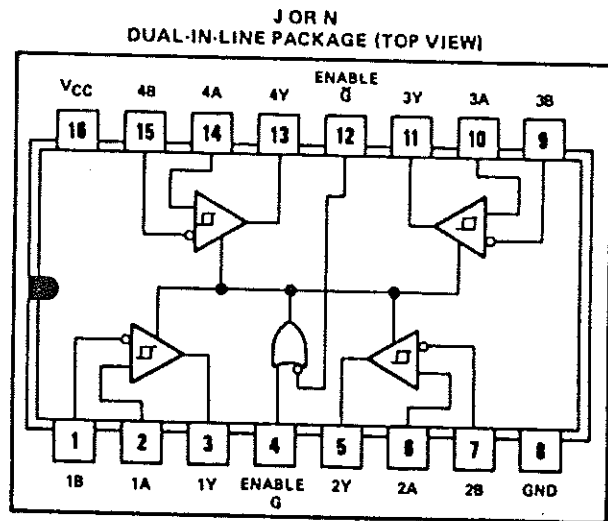
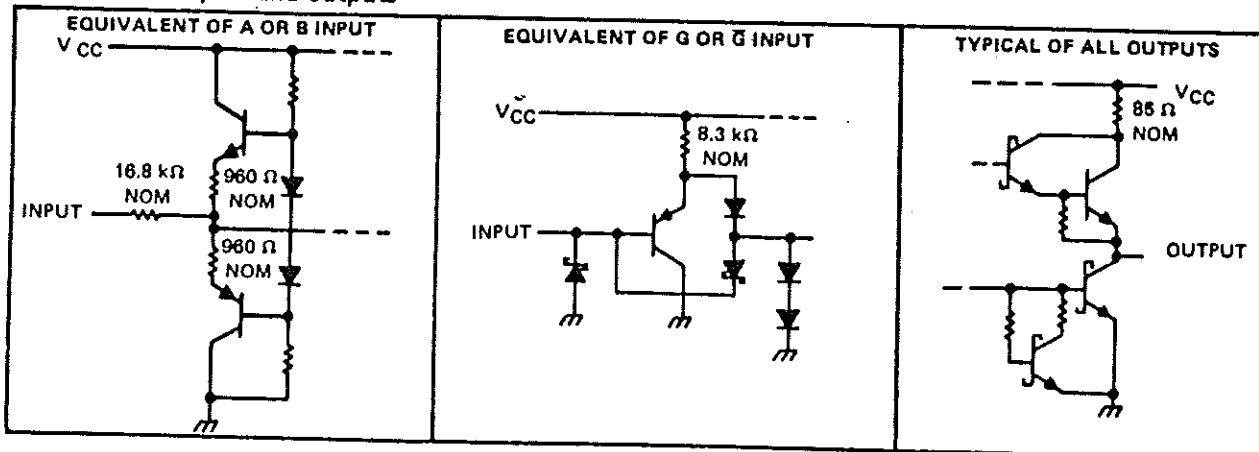
- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11 X.26, and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range ... -12 V to 12 V
- Input Sensitivity ... ± 200 mV
- Input Hysteresis ... 50 mV Typ
- High Input Impedance ... 12 k Ω Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for AM26LS32

description

The SN75173 is a monolithic quadruple differential line receiver with three state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features an active-high enable and an active-low enable common to all four receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 millivolts over a common-mode input voltage range of -12 volts to 12 volts. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN75173 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A - B	ENABLES		OUTPUT Y
	G	G-bar	
$V_{ID} > 0.2$ V	H	X	H
-0.2 V $< V_{ID} < 0.2$ V	X	L	?
$V_{ID} < -0.2$ V	H	X	L
X	X	L	L
	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

TYPE SN75173

QUADRUPLE DIFFERENTIAL LINE RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, A or B inputs	± 25 V
Differential input voltage (see Note 2)	± 25 V
Enable input voltage	7 V
Low-level output current	50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	
J Package	1025 mW
N Package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package	260°C

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75173 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 12	V
Differential input voltage, V_{ID}			± 12	V
High-level output current, I_{OH}			-400	μ A
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{TH} Differential-input high-threshold voltage	$V_O = 2.7$ V, $I_O = -0.4$ mA			0.2	V
V_{TL} Differential-input low-threshold voltage	$V_O = 0.5$ V, $I_O = 16$ mA	-0.2 [‡]			V
$V_{T+} - V_{T-}$ Hysteresis [§]			50		mV
V_{IH} High-level enable input voltage		2			V
V_{IL} Low-level enable input voltage				0.8	V
V_{IK} Enable-input clamp voltage	$I_I = -18$ mA			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -400$ μ A	2.7			V
V_{OL} Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA			0.45	V
				0.5	
I_{OZ} High-impedance-state output current	$V_O = 0.4$ V to 2.4 V			± 20	μ A
I_I Line input current	Other input at 0 V, See Note 4	$V_I = 12$ V		1	mA
		$V_I = -7$ V		-0.8	
I_{IH} High-level enable-input current	$V_{IH} = 2.7$ V			20	μ A
I_{IL} Low-level enable-input current	$V_{IL} = 0.4$ V			-100	μ A
r_I Input resistance		12			k Ω
I_{OS} Short-circuit output current [¶]		-15		-85	mA
I_{CC} Supply current	Outputs disabled			70	mA

[†]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C

[‡]The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} . See Figure 4.

[¶]Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 4: Refer to EIA Standard RS-422A and RS-423A for exact conditions.

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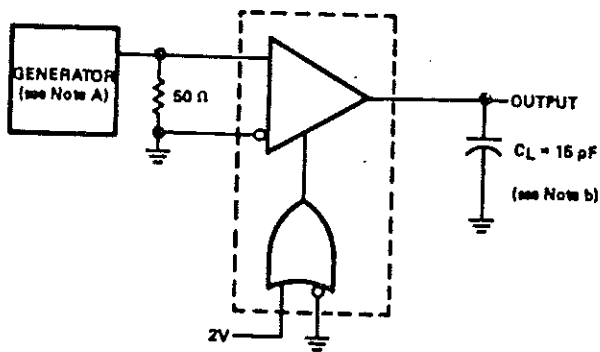
5-183

TYPE SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVER

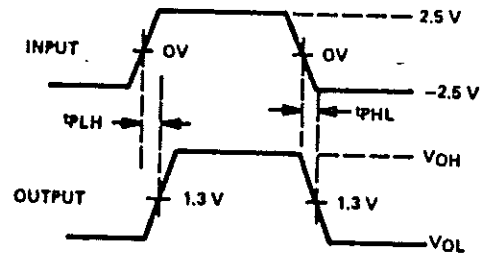
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{ID} = -2.5\text{ V to } 2.5\text{ V}$, $C_L = 15\text{ pF}$,		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1		22	35	ns
t_{PZH}	Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	$C_L = 15\text{ pF}$, See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 5\text{ pF}$, See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 5\text{ pF}$, See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

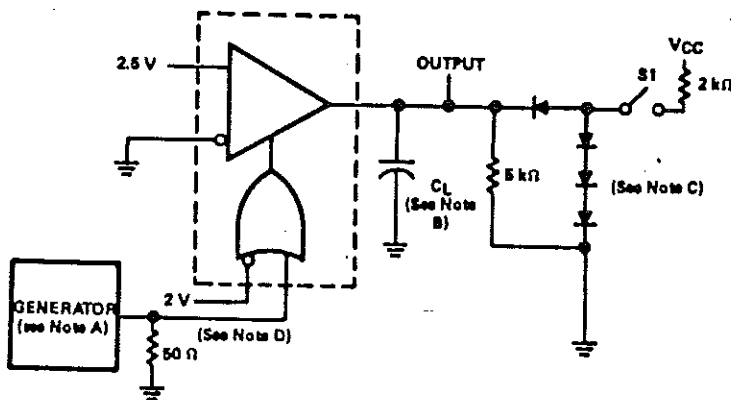


TEST CIRCUIT

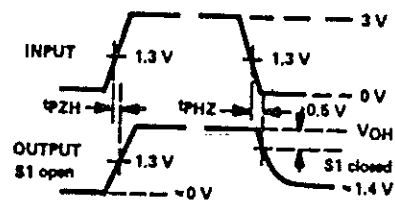


VOLTAGE WAVEFORMS

FIGURE 1 - t_{PLH} , t_{PHL}



TEST CIRCUIT



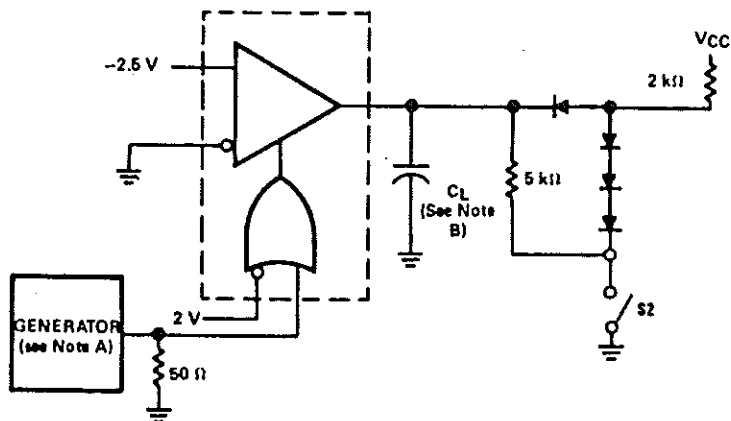
VOLTAGE WAVEFORMS

FIGURE 2 - t_{PHZ} , t_{PZH}

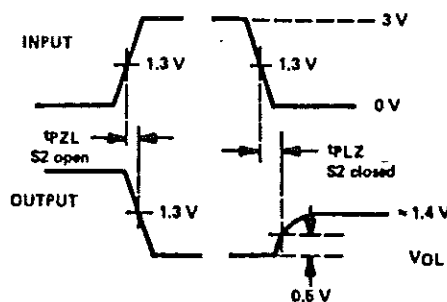
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 5\text{ ns}$, $Z_{out} = 50\ \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are in 916 or equivalent.
- D. To test the active low enable \bar{G} , ground \bar{G} and apply an inverted input waveform to \bar{G} .

TYPE SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVER

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES:**
- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle, = 50%, $t_r = t_f = 6$ ns, $Z_{out} = 50 \Omega$.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are in 916 or equivalent.
 - D. To test the active low enable \bar{G} , ground G and apply an inverted input waveform to \bar{G} .

FIGURE 3 - t_{pZL} , t_{pLZ}

TYPICAL CHARACTERISTICS

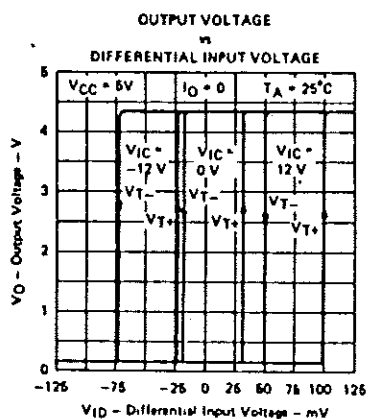


FIGURE 4

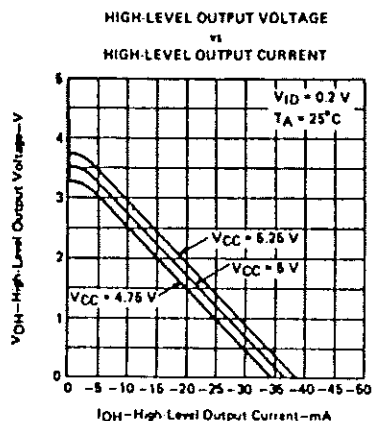


FIGURE 5

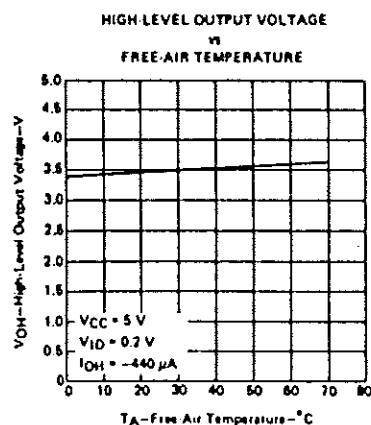


FIGURE 6

TYPE SN75173 QUADRUPLE DIFFERENTIAL LINE RECEIVER

TYPICAL CHARACTERISTICS

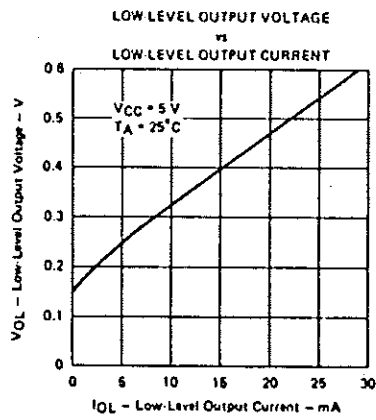


FIGURE 7

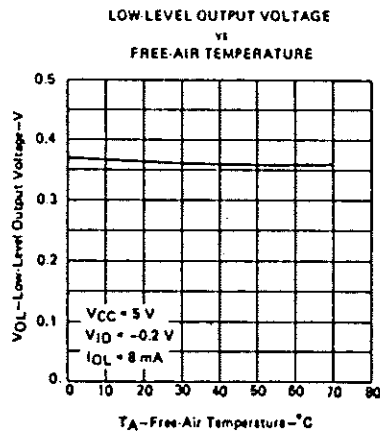


FIGURE 8

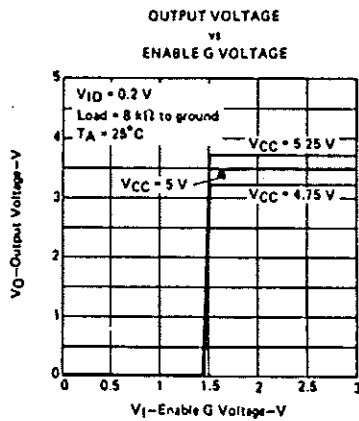


FIGURE 9

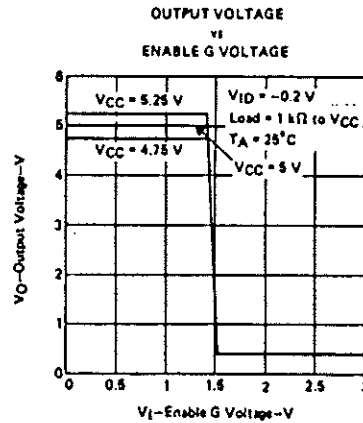
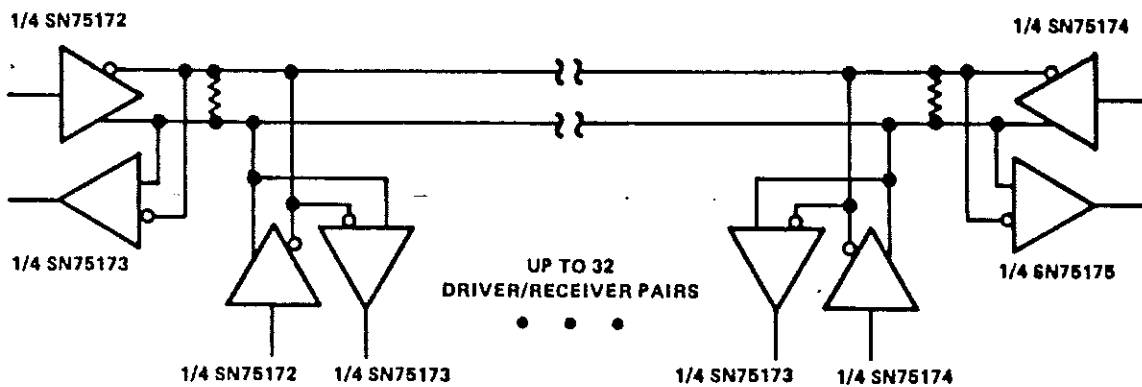


FIGURE 10

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11

INTERFACE CIRCUITS

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

BULLETIN NO. DL-S 12790, OCTOBER 1980

- Bidirectional Transceiver
- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability ... ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance ... $12\text{ k}\Omega$ Min
- Receiver Input Sensitivity ... ± 200 mV
- Receiver Input Hysteresis ... 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

description

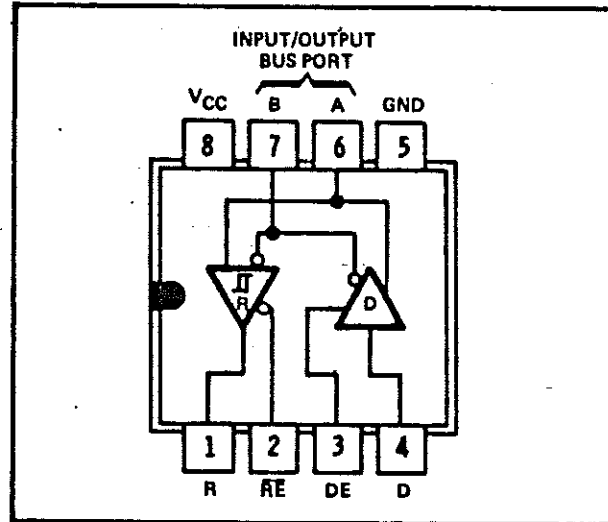
The SN75176 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A, the EIA Subcommittee TR30.1 Draft Standard PN1360, and CCITT Recommendations V.11 and X.27.

The SN75176 combines a three-state differential line driver and a differential-input line receiver both of which operate from a single 5-volt power supply. The driver and receiver have an active enable that can be externally connected to function as a direction control. The driver differential-outputs and the receiver differential-inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$ volts. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 milliamperes of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C . The receiver features a minimum input impedance of $12\text{ k}\Omega$, an input sensitivity of ± 200 millivolts, and a typical input hysteresis of 50 millivolts.

The SN75176 can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A - B	ENABLE RE	OUTPUT R
$V_{ID} > 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} < -0.2\text{ V}$	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

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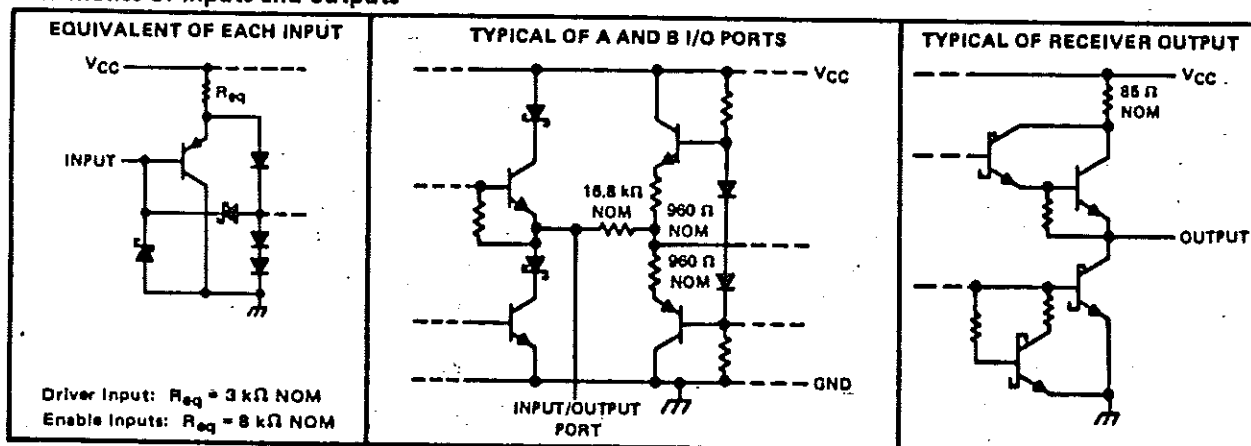
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5-207

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage at any bus terminal	-10 V to 15 V
Enable input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG Package	825 mW
P Package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG Package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P Package	260°C

- NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
 2. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 840 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75176 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}	-7†		12	V
Differential input voltage, V_{ID} (see Note 3)			±12	V
High-level output current, I_{OH}	Driver		-60	mA
	Receiver		-400	μA
Low-level output current, I_{OL}	Driver		60	mA
	Receiver		16	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.8	V
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V
V _{OH}	High-level output voltage	V _{IH} = 2 V, I _{OH} = -33 mA	V _{IL} = 0.8 V,		3.7		V
V _{OL}	Low-level output voltage	V _{IH} = 2 V, I _{OL} = 33 mA	V _{IL} = 0.8 V,		1.1		V
V _{OD1}	Differential output voltage	I _O = 0				2V _{OD2}	V
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 9	2	2.7		V
		R _L = 54 Ω,	See Figure 9	1.5	2.4		V
ΔV _{OD}	Change in magnitude of differential output voltage‡	R _L = 54 Ω or 100 Ω, See Figure 9				±0.2	V
V _{OC}	Common-mode output voltage§					3	V
ΔV _{OC}	Change in magnitude of common-mode output voltage‡					±0.2	V
I _O	Output current	Output disabled, See Note 4	V _O = 12 V			1	mA
			V _O = -7 V			-0.8	
I _{IH}	High-level input current	V _I = 2.4 V				20	μA
I _{IL}	Low-level input current	V _I = 0.4 V				-360	μA
I _{OS}	Short-circuit output current	V _O = -7 V †				-180	mA
		V _O = V _{CC}				180	
		V _O = 12 V				500	
I _{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled				

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ ΔV_{OD} and ΔV_{OC} are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

§ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{DD}	Differential-output delay time	R _L = 60 Ω,	See Figure 11		35	50	ns
t _{TD}	Differential-output transition time				50	75	ns
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 27 Ω,	See Figure 12		16	25	ns
t _{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω,	See Figure 13		60	80	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω,	See Figure 14		30	45	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω,	See Figure 13		51	75	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω,	See Figure 14		18	30	ns

TEXAS INSTRUMENTS
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5-209

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{TH}	Differential-input high-threshold voltage V _O = 2.7 V, I _O = -0.4 mA			0.2	V
V _{TL}	Differential-input low-threshold voltage V _O = 0.5 V, I _O = 8 mA	-0.2‡			V
V _{T+} - V _{T-}	Hysteresis§		50		mV
V _{IH}	High-level enable input voltage		2		V
V _{IL}	Low-level enable input voltage			0.8	V
V _{IK}	Enable-input clamp voltage I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage V _{ID} = 200 mV, I _{OH} = -400 µA, See Figure 10	2.7			V
V _{OL}	Low-level output voltage V _{ID} = -200 mV, See Figure 10	I _{OL} = 8 mA		0.45	V
		I _{OL} = 16 mA		0.5	
I _{OZ}	High-impedance-state output current V _O = 0.4 V to 2.4 V			±20	µA
I _I	Line input current Other input = 0 V, See Note 4	V _I = 12 V		1	mA
		V _I = -7 V		-0.8	
I _{IH}	High-level enable-input current V _{IH} = 2.7 V			20	µA
I _{IL}	Low-level enable-input current V _{IL} = 0.4 V			-100	µA
r _i	Input resistance		12		kΩ
I _{OS}	Short-circuit output current		-15	-85	mA
I _{CC}	Supply current (total package) No load	Outputs enabled		35	mA
		Outputs disabled		30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output V _{ID} = -2.5 V to 2.5 V,		28	35	ns
t _{PHL}	Propagation delay time, high-to-low-level output C _L = 15 pF, See Figure 15		27	35	ns
t _{pZH}	Output enable time to high level C _L = 15 pF, See Figure 16		13	30	ns
t _{pZL}	Output enable time to low level		19	30	ns
t _{PHZ}	Output disable time from high level C _L = 5 pF, See Figure 16		28	35	ns
t _{PLZ}	Output disable time from low level		27	35	ns

TYPICAL CHARACTERISTICS

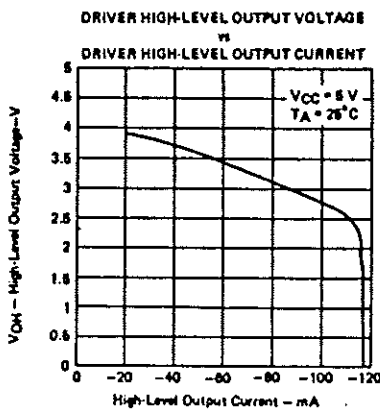


FIGURE 1

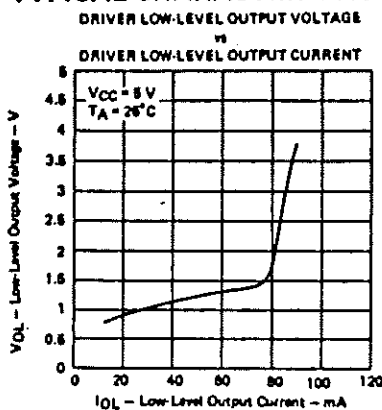


FIGURE 2

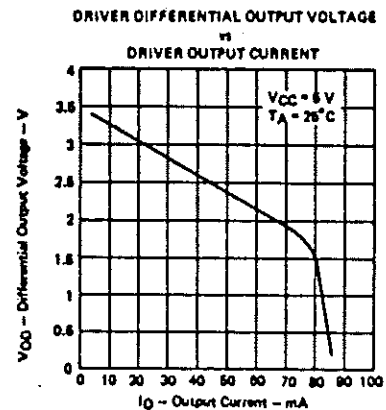


FIGURE 3

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

TYPICAL CHARACTERISTICS

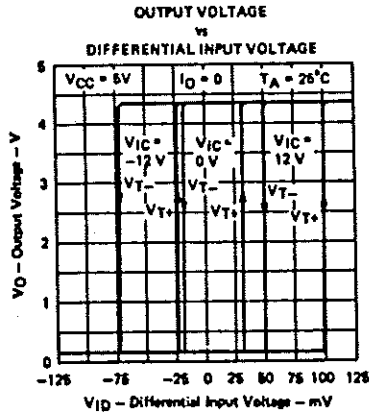


FIGURE 4

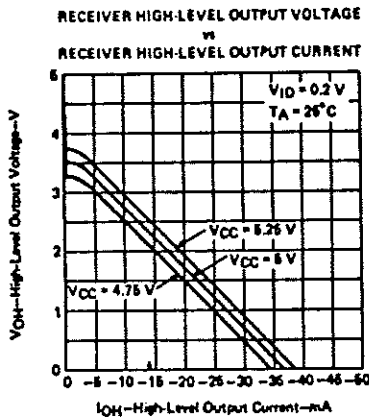


FIGURE 5

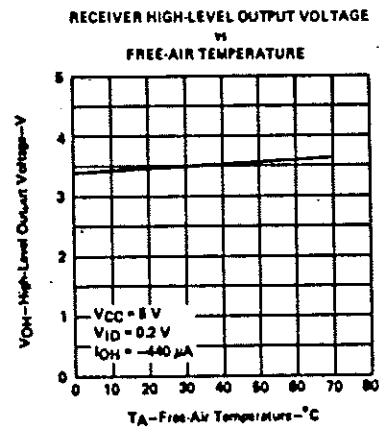


FIGURE 6

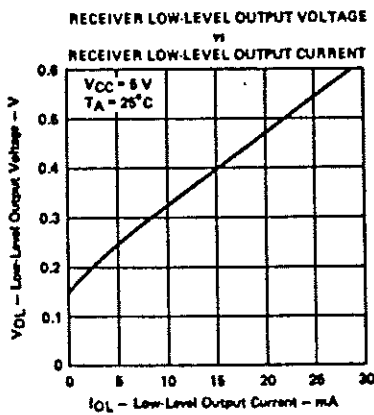


FIGURE 7

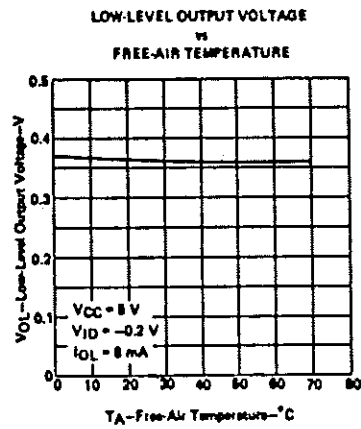


FIGURE 8

5

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

PARAMETER MEASUREMENT INFORMATION

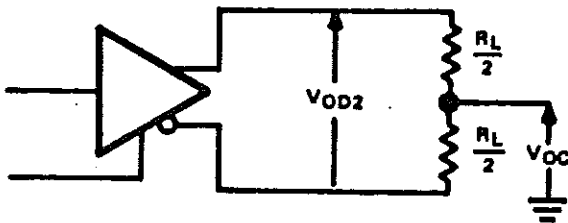


FIGURE 9—DRIVER V_{OD} AND V_{OC}

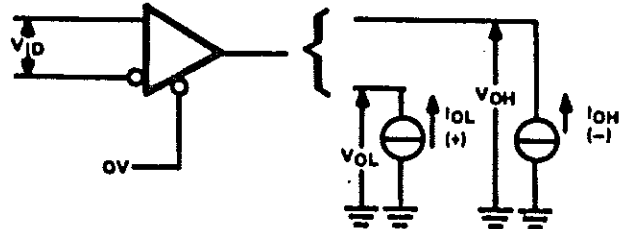
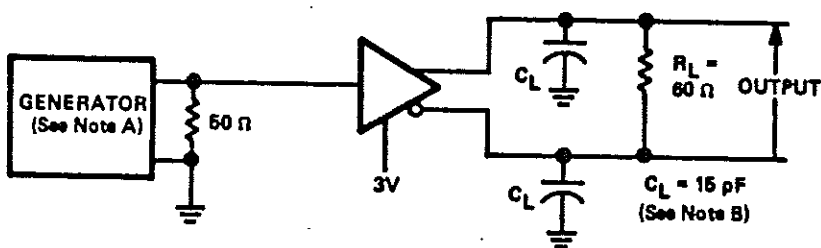
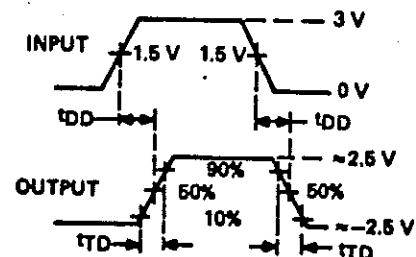


FIGURE 10—RECEIVER V_{OH} AND V_{OL}

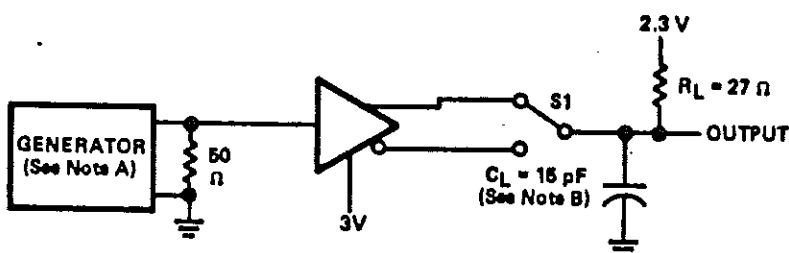


TEST CIRCUIT

FIGURE 11—DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

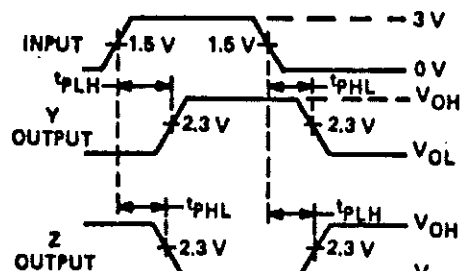


VOLTAGE WAVEFORMS



TEST CIRCUIT

FIGURE 12—DRIVER PROPAGATION TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_{out} = 50 \Omega$.
B. C_L includes probe and jig capacitance.

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

PARAMETER MEASUREMENT INFORMATION

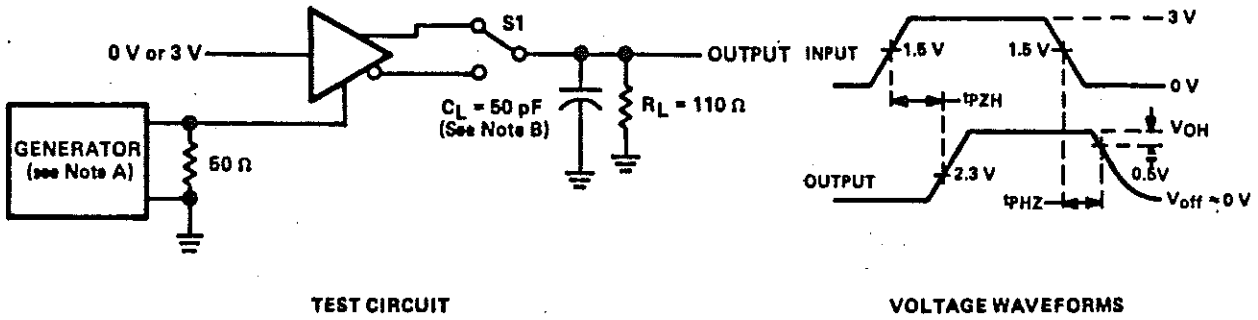


FIGURE 13—DRIVER ENABLE AND DISABLE TIMES

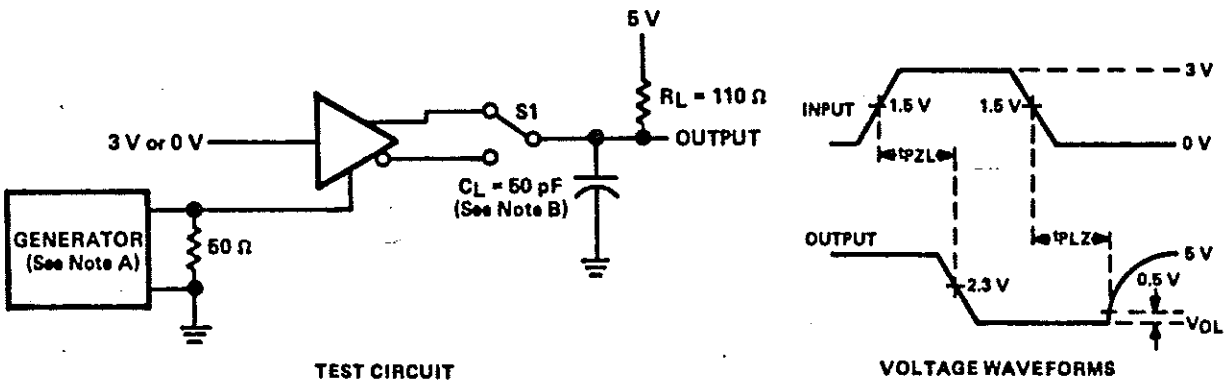


FIGURE 14—DRIVER ENABLE AND DISABLE TIMES

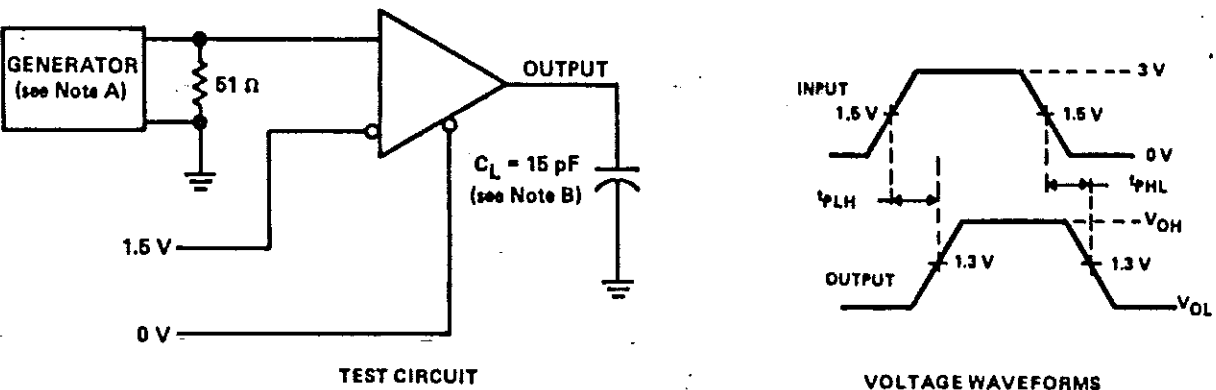


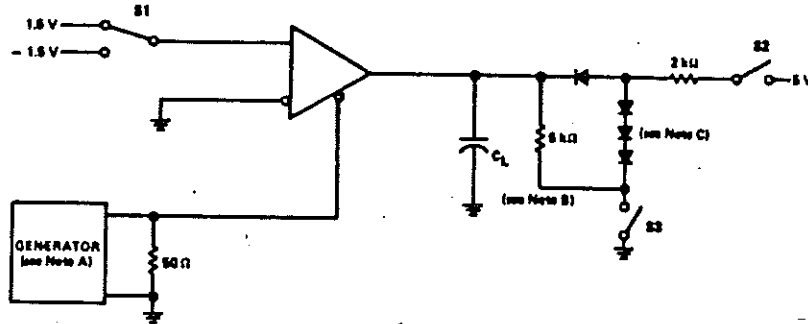
FIGURE 15—RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_{out} = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

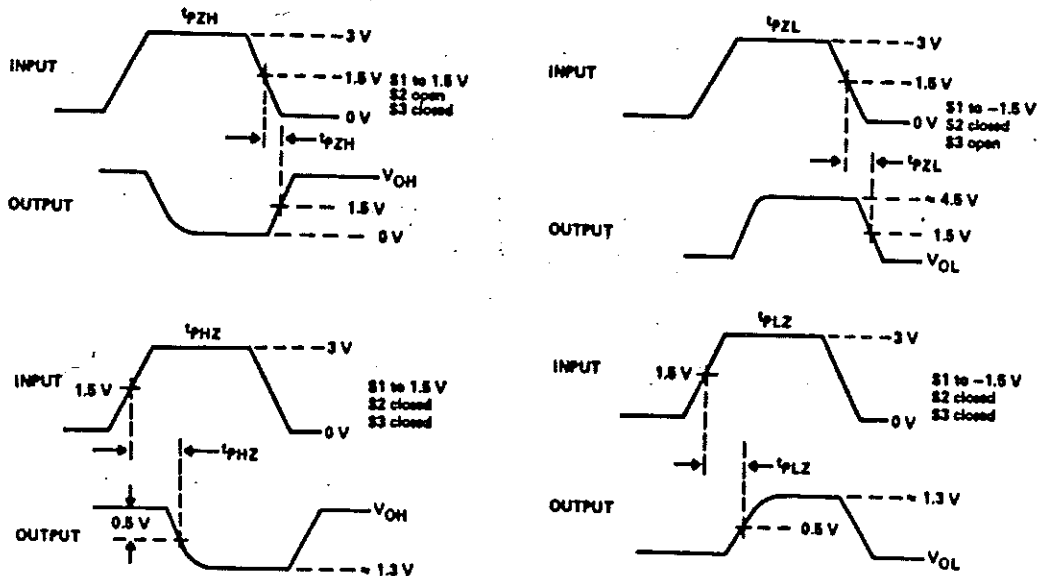
5

TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

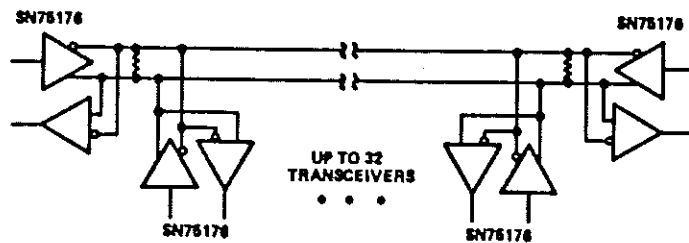


VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
 B. C_L includes probe and stray capacitance.
 C. All diodes are 1N916 or equivalent.

FIGURE 16—RECEIVER ENABLE AND DISABLE TIMES

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stubs lengths off the mainline should be kept as short as possible.

FIGURE 17



Voltage Regulators

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number

of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For applications requiring other voltages, see LM117 data sheet.

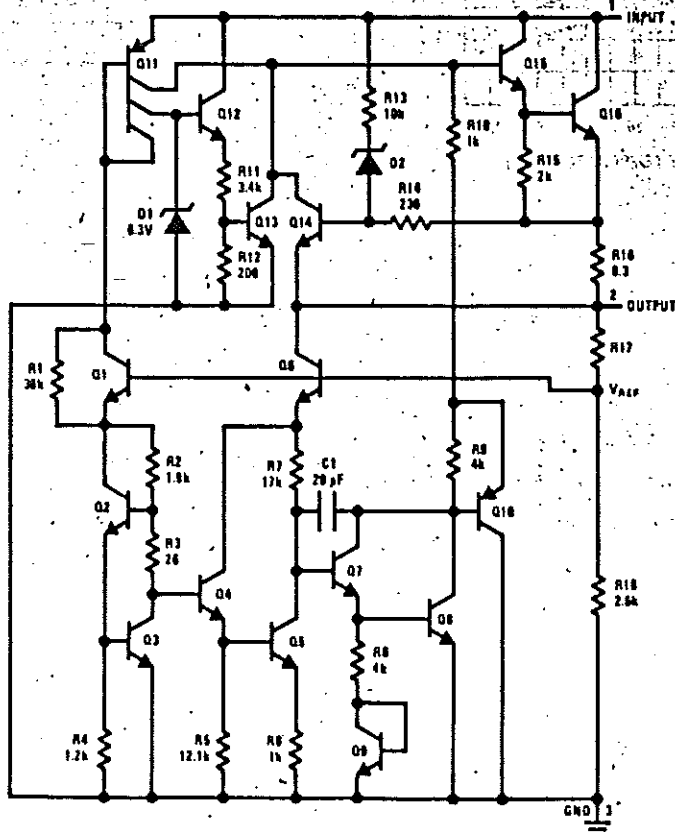
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

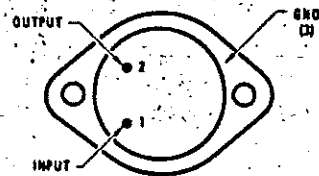
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



Metal Can Package
TO-3 (K)
Aluminum



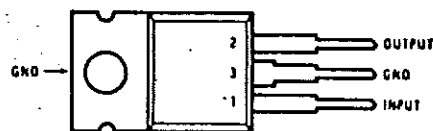
BOTTOM VIEW

Order Numbers:

- LM7805CK
- LM7812CK
- LM7815CK

See NS Package KC02A

Plastic Package
TO-220 (T)



TOP VIEW

Order Numbers:

- LM7805CT
- LM7812CT
- LM7815CT

See NS Package T03B

Absolute Maximum Ratings

Input Voltage ($V_O = 5V, 12V$ and $15V$)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to $+70^\circ\text{C}$
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	125°C
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

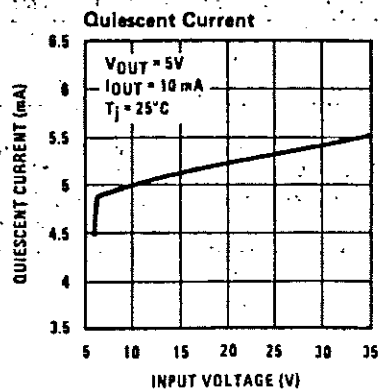
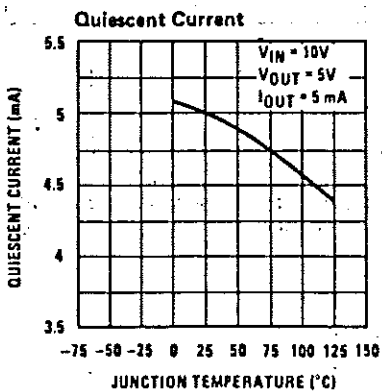
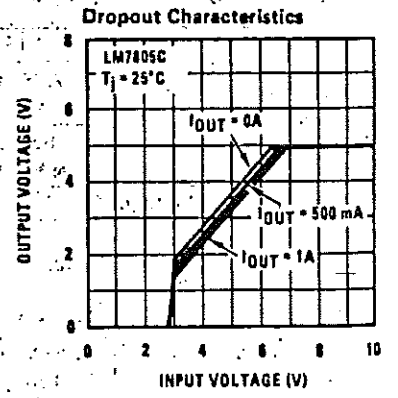
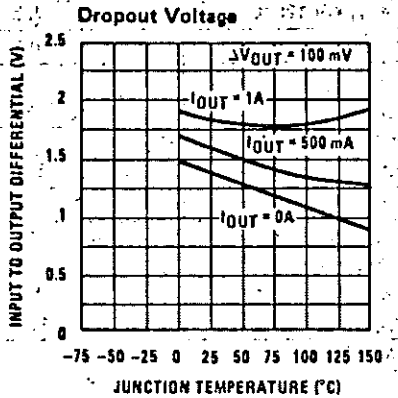
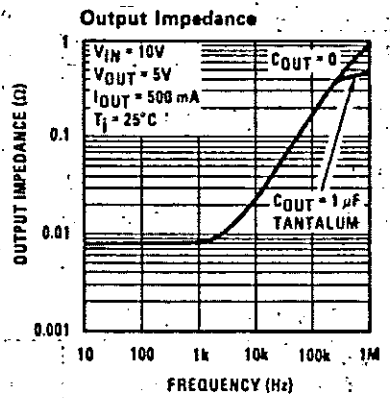
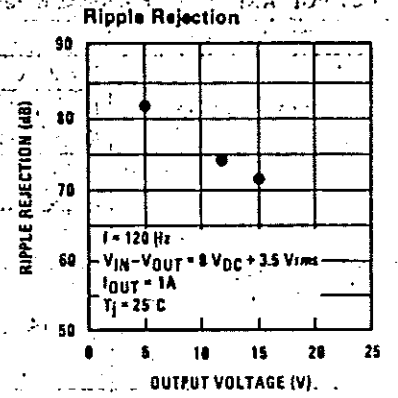
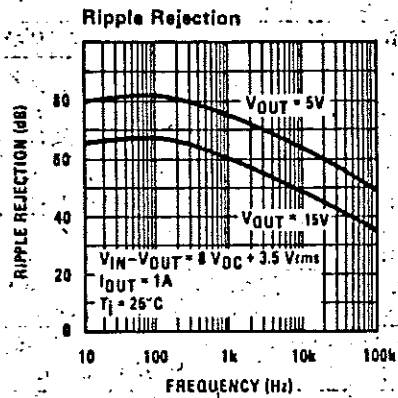
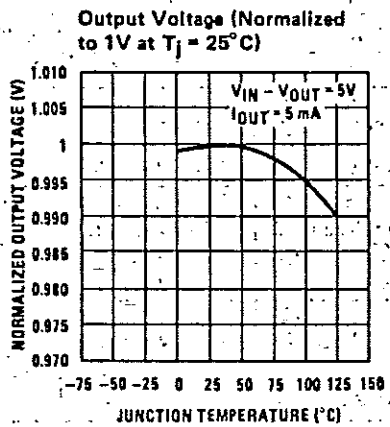
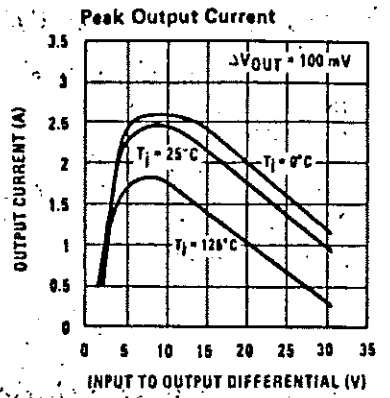
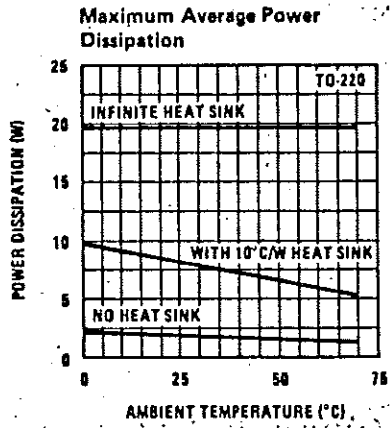
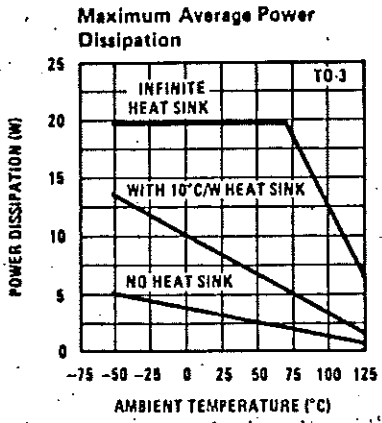
Electrical Characteristics LM78XXC (Note 2) $0^\circ\text{C} < T_J < 125^\circ\text{C}$ unless otherwise noted.

OUTPUT VOLTAGE		5V			12V			15V			UNITS
PARAMETER		10V			19V			23V			
CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_J = 25^\circ\text{C}, 5\text{ mA} < I_O < 1\text{ A}$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
	$P_D \leq 15\text{ W}, 5\text{ mA} < I_O < 1\text{ A}$ $V_{\text{MIN}} < V_{\text{IN}} < V_{\text{MAX}}$	4.75		5.25	11.4		12.6	14.25		15.75	V
Line Regulation	$I_O = 500\text{ mA}$	$T_J = 25^\circ\text{C}$ ΔV_{IN}	3	50	4	120	4	150			mV
		$0^\circ\text{C} < T_J < +125^\circ\text{C}$ ΔV_{IN}		50		120		150			mV
	$I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$ ΔV_{IN}		50		120		150			mV
		$0^\circ\text{C} < T_J < +125^\circ\text{C}$ ΔV_{IN}		25		60		75			mV
Load Regulation	$T_J = 25^\circ\text{C}$ $5\text{ mA} < I_O < 1.5\text{ A}$ $250\text{ mA} < I_O < 750\text{ mA}$		10	50	12	120	12	150			mV
				25		60		75			mV
Quiescent Current	$I_O < 1\text{ A}$			8			8			8	mA
				8.5			8.5			8.5	mA
Quiescent Current Change	$5\text{ mA} < I_O < 1\text{ A}$			0.5			0.5			0.5	mA
	$T_J = 25^\circ\text{C}, I_O < 1\text{ A}$ $V_{\text{MIN}} < V_{\text{IN}} < V_{\text{MAX}}$			1.0			1.0			1.0	mA
	$I_O < 500\text{ mA}, 0^\circ\text{C} < T_J < +125^\circ\text{C}$ $V_{\text{MIN}} < V_{\text{IN}} < V_{\text{MAX}}$			1.0			1.0			1.0	mA
Output Noise Voltage	$T_A = 25^\circ\text{C}, 10\text{ Hz} < f < 100\text{ kHz}$			40			75			90	μV
Ripple Rejection	$f = 120\text{ Hz}$ $I_O < 1\text{ A}, T_J = 25^\circ\text{C}$ or $I_O < 500\text{ mA}$ $0^\circ\text{C} < T_J < +125^\circ\text{C}$ $V_{\text{MIN}} < V_{\text{IN}} < V_{\text{MAX}}$	62	80		55	72		54	70		dB
		62			55			54			dB
Dropout Voltage	$T_J = 25^\circ\text{C}, I_{\text{OUT}} = 1\text{ A}$			2.0			2.0			2.0	V
Output Resistance	$f = 1\text{ kHz}$			8			18			19	$\text{m}\Omega$
Short-Circuit Current	$T_J = 25^\circ\text{C}$			2.1			1.5			1.2	A
Peak Output Current	$T_J = 25^\circ\text{C}$			2.4			2.4			2.4	A
Average TC of V_{OUT}	$0^\circ\text{C} < T_J < +125^\circ\text{C}, I_O = 5\text{ mA}$			0.6			1.5			1.8	$\text{mV}/^\circ\text{C}$
Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ\text{C}, I_O < 1\text{ A}$	7.3			14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically $4^\circ\text{C}/\text{W}$ junction to case and $35^\circ\text{C}/\text{W}$ case to ambient. Thermal resistance of the TO-220 package (T) is typically $4^\circ\text{C}/\text{W}$ junction to case and $50^\circ\text{C}/\text{W}$ case to ambient.

Note 2: All characteristics are measured with capacitor across the input of $0.22\ \mu\text{F}$, and a capacitor across the output of $0.1\ \mu\text{F}$. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_{\text{PW}} \leq 10\text{ ms}$, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics



LM78LXX Series 3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78LXX is available in the metal three lead TO-39 (H) and the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

For applications requiring other voltages, see LM117 data sheet.

Features

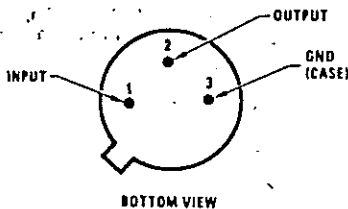
- Output voltage tolerances of $\pm 5\%$ (LM78LXXAC) and $\pm 10\%$ (LM78LXXC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 low profile packages

Voltage Range

LM78L05	5V
LM78L12	12V
LM78L15	15V

Connection Diagrams

Metal Can Package

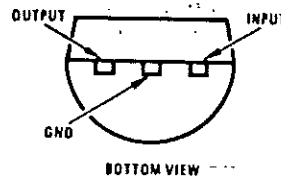


Order Numbers:

LM78L05ACH	LM78L05CH
LM78L12ACH	LM78L12CH
LM78L15ACH	LM78L15CH

See NS Package H03A

Plastic Package



Order Numbers:

LM78L05ACZ	LM78L05CZ
LM78L12ACZ	LM78L12CZ
LM78L15ACZ	LM78L15CZ

See NS Package Z03A

Absolute Maximum Ratings

Input Voltage	$V_O = 5V$	30V
	$V_O = 12V$ and $15V$	35V
Internal Power Dissipation (Note 1)		Internally Limited
Operating Temperature Range		$0^\circ C$ to $+70^\circ C$
Maximum Junction Temperature		$125^\circ C$
Storage Temperature Range		
Metal Can (H Package)		$-65^\circ C$ to $+150^\circ C$
Molded TO-92 (Z Package)		$-55^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 seconds)		$300^\circ C$

LM78LXXAC Electrical Characteristics (Note 2)

$T_J = 0^\circ C$ to $+125^\circ C$, $I_O = 40$ mA, $C_{IN} = 0.33\mu F$, $C_O = 0.1\mu F$ (unless noted)

LM78LXXAC OUTPUT VOLTAGE		5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)		10V			19V			23V			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O Output Voltage (Note 4)	$T_J = 25^\circ C$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
	$1\text{ mA} \leq I_O \leq 70\text{ mA}$	4.75		5.25	11.4		12.6	14.25		15.75	V
	$1\text{ mA} \leq I_O \leq 40\text{ mA}$ and	4.75		5.25	11.4		12.6	14.25		15.75	V
	$V_{MIN} \leq V_{IN} \leq V_{MAX}$			($7 \leq V_{IN} \leq 20$)			($14.5 \leq V_{IN} \leq 27$)			($17.5 \leq V_{IN} \leq 30$)	V
ΔV_O Line Regulation	$T_J = 25^\circ C$		10	54		20	110		25	140	mV
			($8 \leq V_{IN} \leq 20$)		($16 \leq V_{IN} \leq 27$)		($20 \leq V_{IN} \leq 30$)				V
			18	75		30	180		37	250	mV
		($7 \leq V_{IN} \leq 20$)		($14.5 \leq V_{IN} \leq 27$)		($17.5 \leq V_{IN} \leq 30$)				V	
ΔV_O Load Regulation	$T_J = 25^\circ C$, $1\text{ mA} \leq I_O \leq 40\text{ mA}$		5	30		10	50		12	75	mV
	$T_J = 25^\circ C$, $1\text{ mA} \leq I_O \leq 100\text{ mA}$		20	60		30	100		35	150	mV
ΔV_O Long Term Stability			12			24			30		mV/1000 hrs
I_Q Quiescent Current	$T_J = 25^\circ C$		3	5		3	5		3.1	5	mA
	$T_J = 125^\circ C$			4.7			4.7			4.7	mA
ΔI_Q Quiescent Current Change	$1\text{ mA} \leq I_O \leq 40\text{ mA}$			0.1			0.1			0.1	mA
	$V_{MIN} \leq V_{IN} \leq V_{MAX}$			1.0			1.0			1.0	mA
				($8 \leq V_{IN} \leq 20$)			($16 \leq V_{IN} \leq 27$)			($20 \leq V_{IN} \leq 30$)	V
V_n Output Noise Voltage	$T_J = 25^\circ C$, (Note 3) $f = 10\text{ Hz} - 10\text{ kHz}$		40			80			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ Ripple Rejection	$f = 120\text{ Hz}$		47	62		40	54		37	51	dB
			($8 \leq V_{IN} \leq 16$)		($15 \leq V_{IN} \leq 25$)		($18.5 \leq V_{IN} \leq 28.5$)				V
Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ C$		7			14.5			17.5		V

Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is $15^\circ C/W$ junction to case and $140^\circ C/W$ junction to ambient. Thermal resistance of the TO-92 package is $180^\circ C/W$ junction to ambient with $0.4''$ leads from a PC board and $160^\circ C/W$ junction to ambient with $0.125''$ lead length to a PC board.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3: Recommended minimum load capacitance of $0.01\mu F$ to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within $\pm 0.01\% V_O/^\circ C$.

Absolute Maximum Ratings

Output Voltage $V_O = 5V$	30V
$V_O = 12V$ and $15V$	35V
Maximum Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	$0^\circ C$ to $+70^\circ C$
Maximum Junction Temperature	$125^\circ C$
Storage Temperature Range	
Metal Can (H Package)	$-65^\circ C$ to $+150^\circ C$
Molded TO-92	$-55^\circ C$ to $+150^\circ C$
Soldering Temperature (Soldering, 10 seconds)	$300^\circ C$

LM78LXXC Electrical Characteristics (Note 2)

$0^\circ C$ to $+125^\circ C$; $I_O = 40$ mA, $C_{IN} = 0.33\mu F$, $C_O = 0.1\mu F$ (unless noted)

LM78LXXC OUTPUT VOLTAGE		5V			12V			15V			UNITS	
INPUT VOLTAGE (unless otherwise noted)		10V			19V			23V				
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_O Output Voltage (Note 4)	$T_J = 25^\circ C$	4.6	5	5.4	11.1	12	12.9	13.8	15	16.2	V	
	1 mA $\leq I_O \leq 70$ mA or	4.5		5.5			13.2	13.5		16.5	V	
	1 mA $\leq I_O \leq 40$ mA and ΔV_{IN}	(7 $\leq V_{IN} \leq 20$)			(14.5 $\leq V_{IN} \leq 27$)			(18 $\leq V_{IN} \leq 30$)			V	
ΔV_O Line Regulation	$T_J = 25^\circ C$		10	150		20	200		25	250	mV	
			(8 $\leq V_{IN} \leq 20$)			(16 $\leq V_{IN} \leq 27$)			(20 $\leq V_{IN} \leq 30$)			V
			18	200		30	250		30	300	mV	
		(7 $\leq V_{IN} \leq 20$)			(14.5 $\leq V_{IN} \leq 27$)			(18 $\leq V_{IN} \leq 30$)			V	
ΔV_O Load Regulation	$T_J = 25^\circ C, 1$ mA $\leq I_O \leq 40$ mA		5	30		10	50		12	75	mV	
	$T_J = 25^\circ C, 1$ mA $\leq I_O \leq 100$ mA		20	60		30	100		35	150	mV	
ΔV_O Long Term Stability			12			24			30		mV/1000 hrs	
I_Q Quiescent Current	$T_J = 25^\circ C$		3	6		3	6.5		3.1	6.5	mA	
	$T_J = 125^\circ C$			5.5			6			6		
ΔI_Q Quiescent Current Change	$T_J = 25^\circ C, 1$ mA $\leq I_O \leq 40$ mA			0.2			0.2			0.2	mA	
	$T_J = 25^\circ C$			1.5			1.5			1.5	mA	
V_n Output Noise Voltage	$T_J = 25^\circ C$, (Note 3) $f = 10$ Hz – 10 kHz		40			80			90		μV	
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ Ripple Rejection	$f = 125$ Hz		40	60		36	52		33	49	dB	
			(8 $\leq V_{IN} \leq 18$)			(15 $\leq V_{IN} \leq 25$)			(18.5 $\leq V_{IN} \leq 28.5$)			V
Input Voltage Required to Maintain Line Regulation	$T_J = 25^\circ C$		7			14.5			18		V	

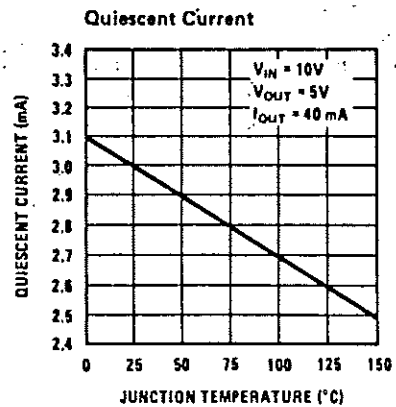
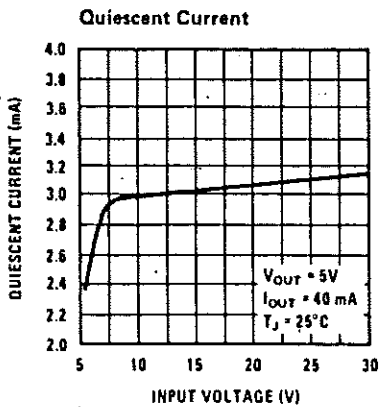
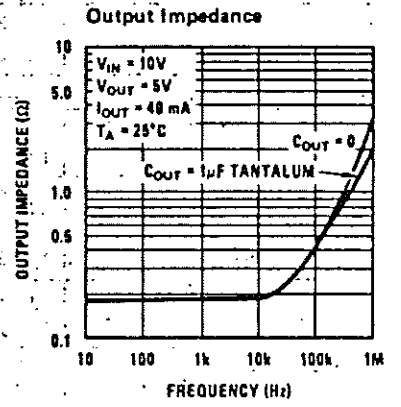
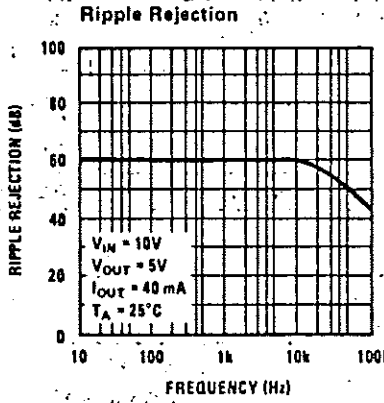
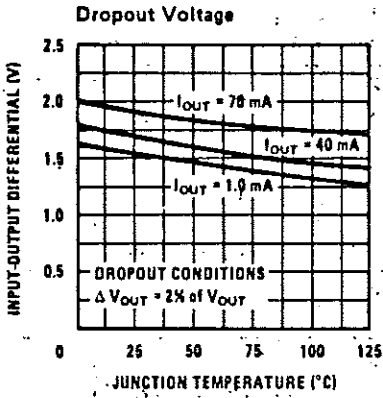
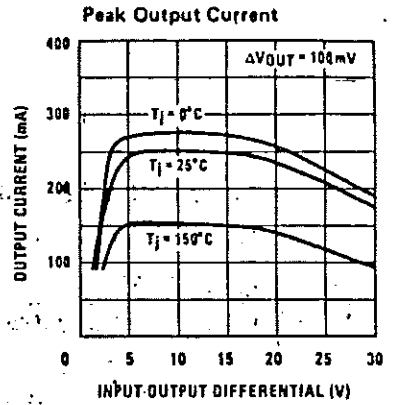
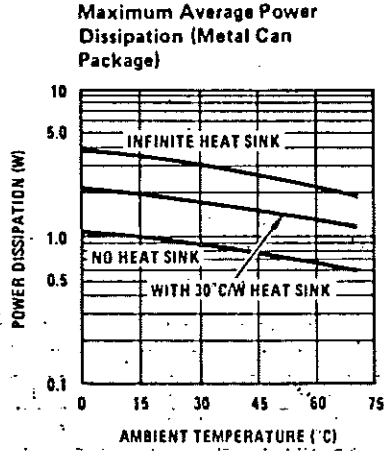
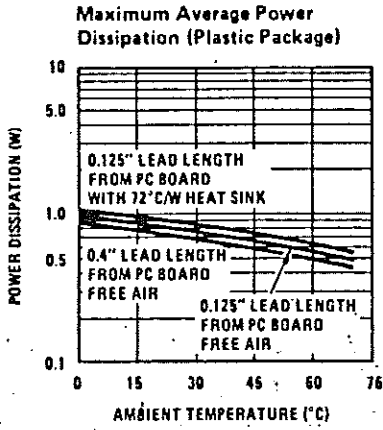
Note 1: Thermal resistance of the Metal Can Package (H) without a heat sink is $15^\circ C/W$ junction to case and $140^\circ C/W$ junction to ambient. Thermal resistance of the TO-92 package is $180^\circ C/W$ junction to ambient with $0.4''$ leads from a PC board and $160^\circ C/W$ junction to ambient with $0.125''$ lead length to a PC board.

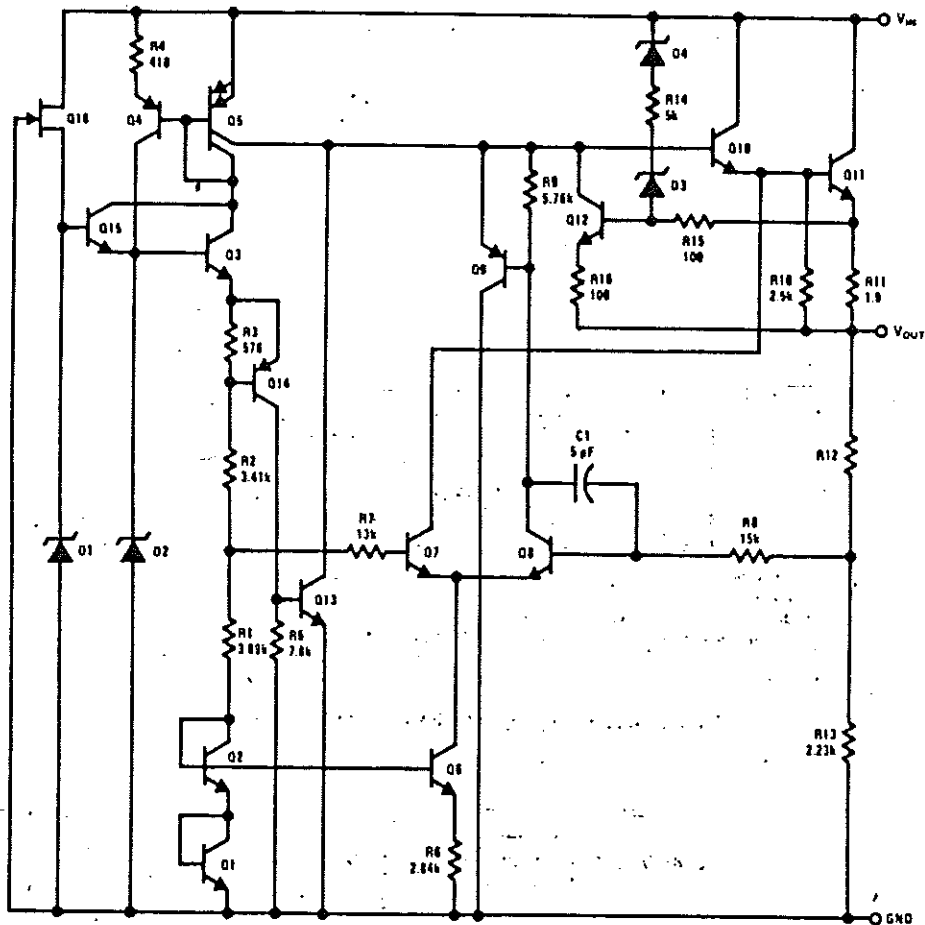
Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3: Recommended minimum load capacitance of $0.01\mu F$ to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within $\pm 0.01\% V_O/^\circ C$.

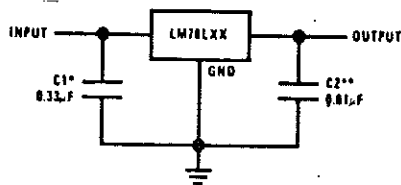
Typical Performance Characteristics





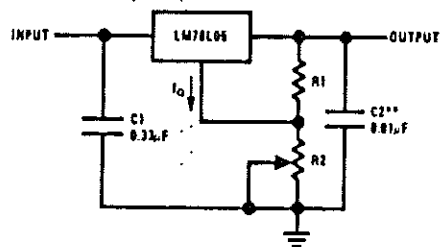
LM78LXX

Typical Applications



*Required if the regulator is located far from the power supply filter.
 **See Note 3 in the electrical characteristics table.

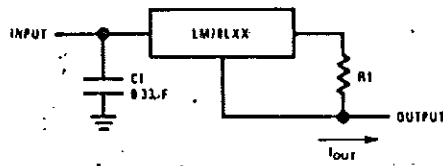
Fixed Output Regulator



$$V_{out} = 5V + (5V/R1 + I_Q) R2$$

$$5V/R1 > 3I_Q, \text{ load regulation } (L_r) = [(R1 + R2)/R1] (L_r \text{ of LM78L05})$$

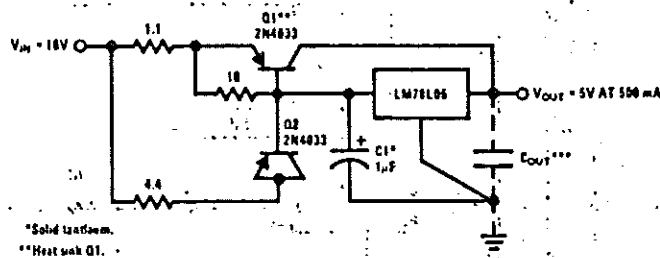
Adjustable Output Regulator



$$I_{out} = (V_{in}/R1) + I_Q$$

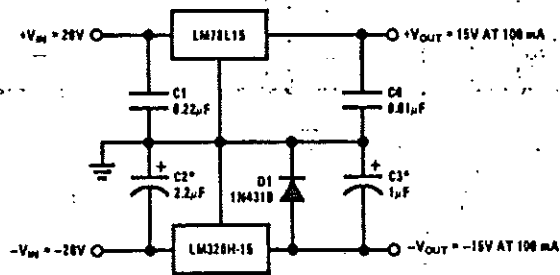
$$I_Q = 1.5 \text{ mA over line and load changes}$$

Current Regulator



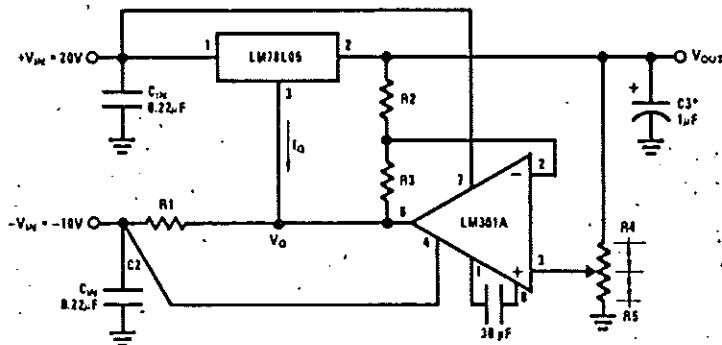
- *Solid tantalum.
- **Heat sink Q1.
- ***Optional: Improve ripple rejection and transient response.
- * Load Regulation: 0.5% @ $I_L \leq 250 \text{ mA}$ pulsed with $I_{out} = 50 \text{ mA}$.

5V, 500 mA Regulator with Short Circuit Protection



*Solid tantalum.

±15V, 100 mA Dual Power Supply



- *Solid tantalum.
- $V_{out} = V_Q + 5V, R1 = (-V_W/I_Q)_{LM78L05}$
- $V_{out} = 5V (R2/R4) \text{ for } (R2 + R3) = (R4 + R5)$
- A 0.5V output will correspond to $(R2/R4) = 0.1, (R2/R4) = 0.0$

Variable Output Regulator 0.5V - 18V

LM117/LM217/LM317 3-Terminal Adjustable Regulator

General Description

The LM117/LM217/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K, LM217K and LM317K are packaged in standard TO-3 transistor packages while the LM117H, LM217H and LM317H are packaged in a solid Kovar base TO-5 transistor package. The LM117 is rated for operation from -55°C to +150°C, the LM217 from -25°C to +150°C and the LM317 from 0°C to +125°C. The LM317T and LM317MP, rated for operation over a 0°C to +125°C range, are available in a TO-220 plastic package and a TO-202 package, respectively.

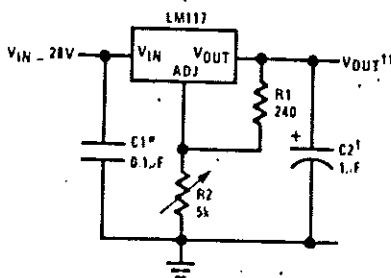
For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

LM117 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM117	TO-3	20W	1.5A
LM217	TO-39	2W	0.5A
LM317	TO-220	15W	1.5A
LM317M	TO-202	7.5W	0.5A

Typical Applications

1.2V-25V Adjustable Regulator

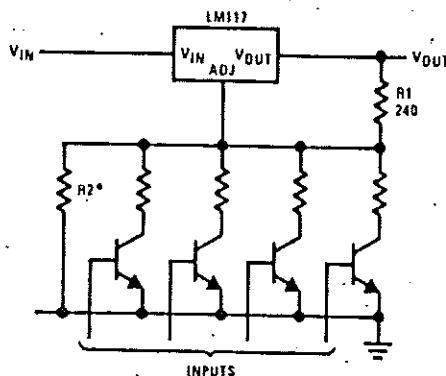


† Optional—improves transient response

* Needed if device is far from filter capacitors

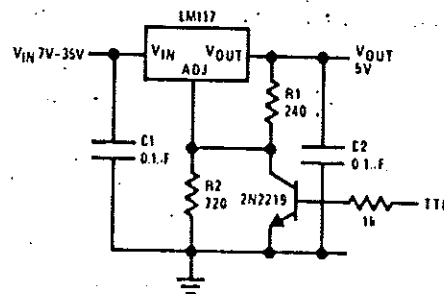
$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1} \right)$$

Digitally Selected Outputs



* Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



* Min output ≈ 1.2V

Absolute Maximum Ratings

Power Dissipation	Internally limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM117	-55°C to +150°C
LM217	-25°C to +150°C
LM317	0°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit 100% All Devices

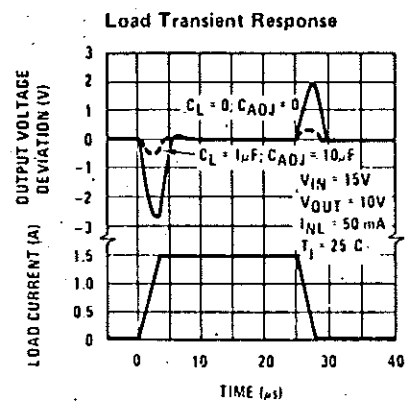
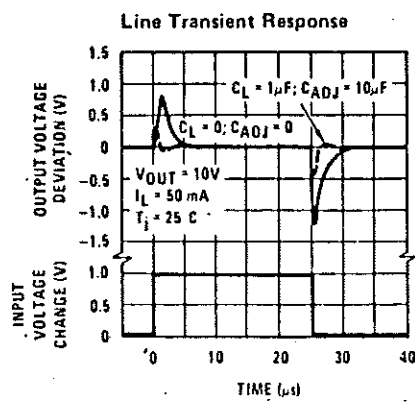
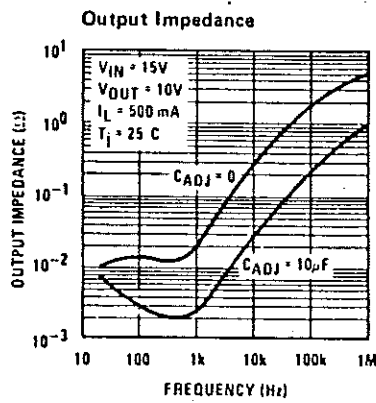
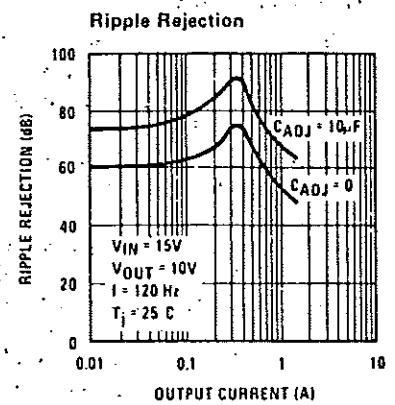
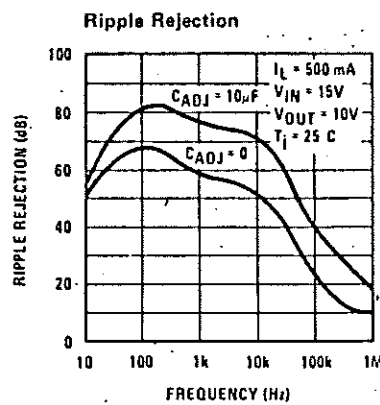
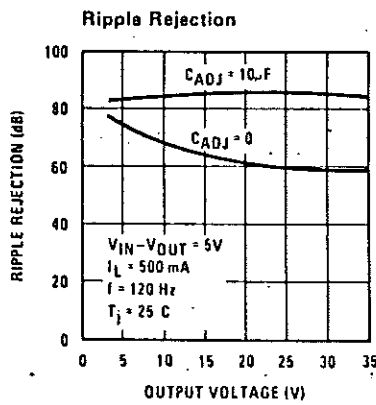
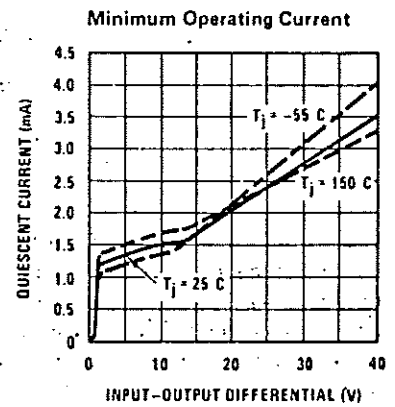
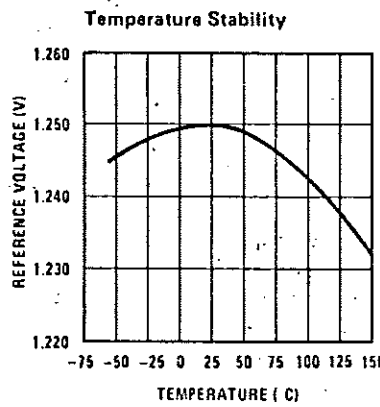
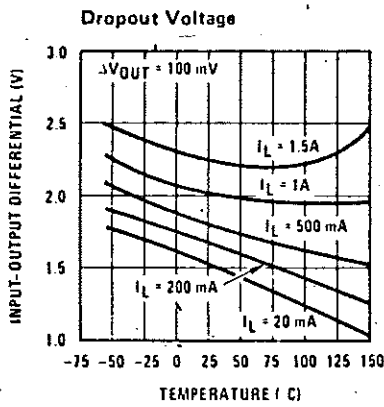
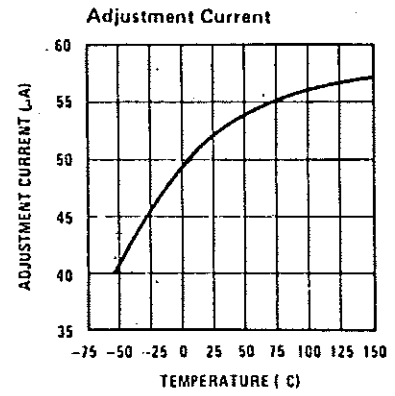
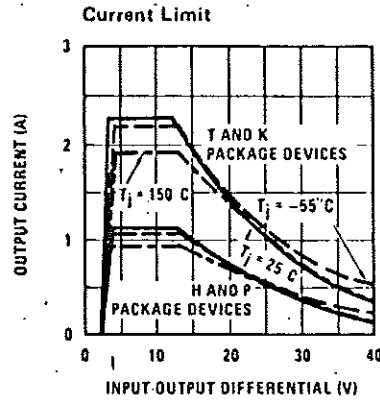
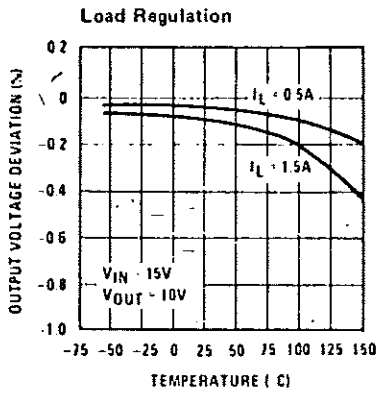
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM117/217			LM317			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25^\circ\text{C}$, $3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$ (Note 2),		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$ $V_{\text{OUT}} \leq 5\text{V}$, (Note 2) $V_{\text{OUT}} \geq 5\text{V}$, (Note 2)		5	15		5	25	mV
			0.1	0.3		0.1	0.5	%
Thermal Regulation	$T_A = 25^\circ\text{C}$, 20 ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\text{mA} \leq I_L \leq I_{\text{MAX}}$ $2.5\text{V} \leq (V_{\text{IN}} - V_{\text{OUT}}) \leq 40\text{V}$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{\text{IN}} - V_{\text{OUT}}) \leq 40\text{V}$, (Note 3) $10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$, $P \leq P_{\text{MAX}}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$, (Note 2) $V_{\text{OUT}} \leq 5\text{V}$ $V_{\text{OUT}} \geq 5\text{V}$		20	50		20	70	mV
			0.3	1		0.3	1.5	%
Temperature Stability	$T_{\text{MIN}} \leq T_j \leq T_{\text{MAX}}$		1			1		%
Minimum Load Current	$V_{\text{IN}} - V_{\text{OUT}} = 40\text{V}$		3.5	5		3.5	10	mA
Current Limit	$V_{\text{IN}} - V_{\text{OUT}} \leq 15\text{V}$ K and T Package		1.5	2.2		1.5	2.2	A
			0.5	0.8		0.5	0.8	A
	$V_{\text{IN}} - V_{\text{OUT}} = 40\text{V}$, $T_j = +25^\circ\text{C}$ K and T Package		0.30	0.4		0.15	0.4	A
			0.15	0.20		0.075	0.20	A
RMS Output Noise, % of V_{OUT}	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{\text{OUT}} = 10\text{V}$, $f = 120\text{Hz}$ $C_{\text{ADJ}} = 10\mu\text{F}$		66			66		dB
			66	80		66	80	dB
Long-Term Stability	$T_A = 125^\circ\text{C}$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	$^\circ\text{C}/\text{W}$
	K Package		2.3	3		2.3	3	$^\circ\text{C}/\text{W}$
	T Package					4		$^\circ\text{C}/\text{W}$
	P Package					12		$^\circ\text{C}/\text{W}$

Note 1: Unless otherwise specified, these specifications apply: $-55^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ for the LM117, $-25^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ for the LM217 and $0^\circ\text{C} \leq T_j \leq +125^\circ\text{C}$ for the LM317; $V_{\text{IN}} - V_{\text{OUT}} = 5\text{V}$ and $I_{\text{OUT}} = 0.1\text{A}$ for the TO-5 and TO-202 packages and $I_{\text{OUT}} = 0.5\text{A}$ for the TO-3 package and TO-220 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-5 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 package and 0.5A for the TO-5 and TO-202 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Selected devices with tightend tolerance reference voltage available.



In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF} , between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2 , giving an output voltage of

$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

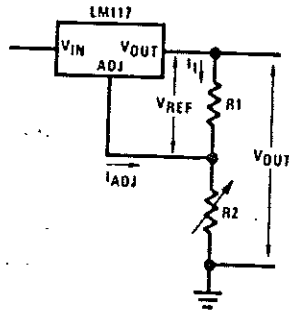


FIGURE 1.

Since the $100\mu\text{A}$ current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A $0.1\mu\text{F}$ disc or $1\mu\text{F}$ solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a $10\mu\text{F}$ bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over $10\mu\text{F}$ do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about $25\mu\text{F}$ in aluminum electrolytic to equal $1\mu\text{F}$ solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, $0.01\mu\text{F}$ disc may seem to work better than a $0.1\mu\text{F}$ disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A $1\mu\text{F}$ solid tantalum (or $25\mu\text{F}$ aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be $0.05\Omega (1 + R_2/R_1)$ or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

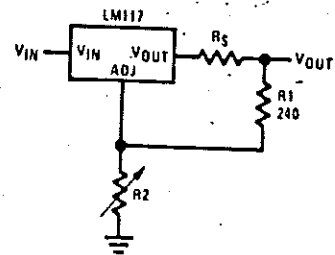


FIGURE 2. Regulator with Line Resistance in Output Load.

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most $10\mu\text{F}$ capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge

Application Hints (Continued)

current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN} . In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of $25\mu\text{F}$ or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge

occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and $10\mu\text{F}$ capacitance. Figure 3 shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

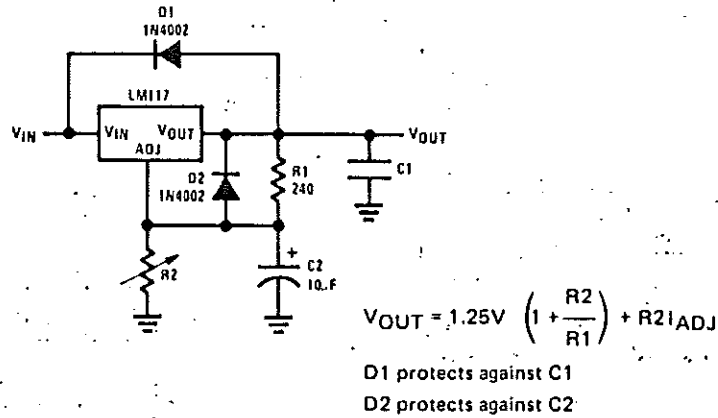
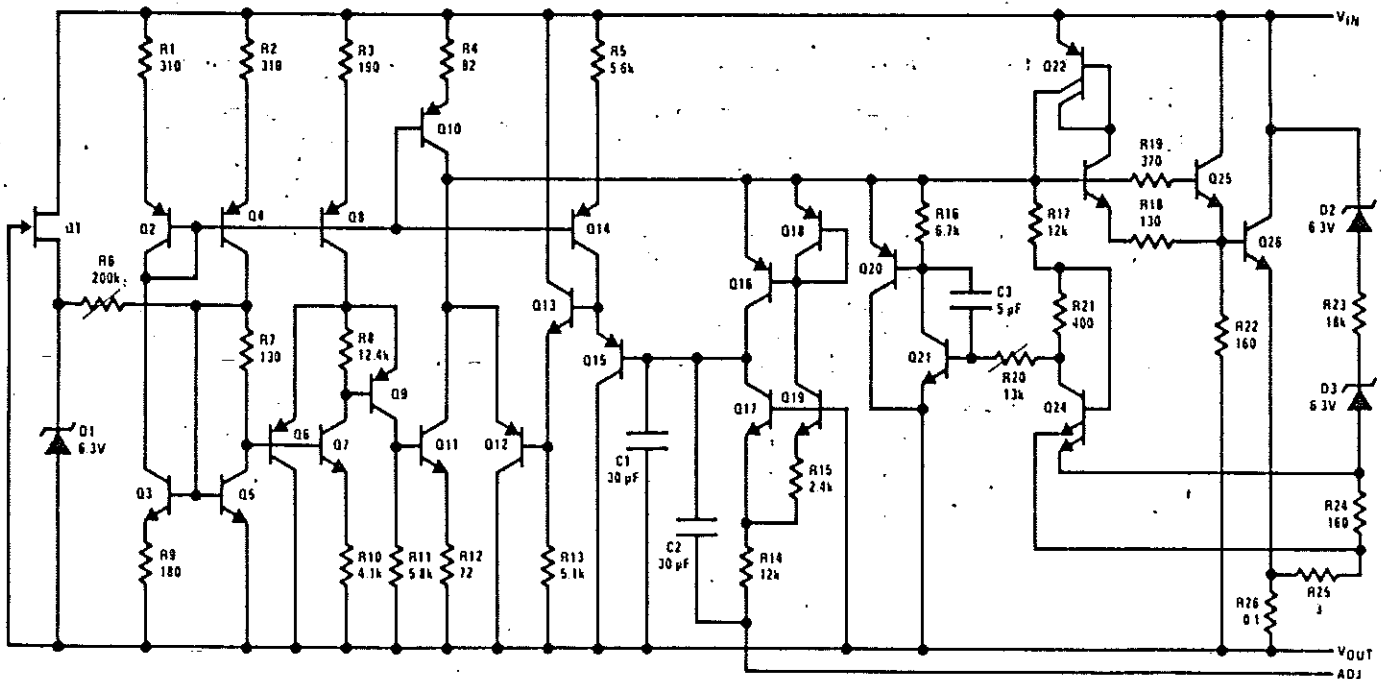


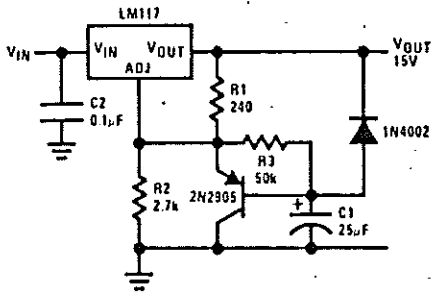
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

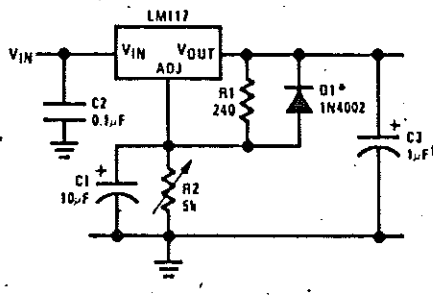


Typical Applications (Continued)

Slow Turn-On 15V Regulator

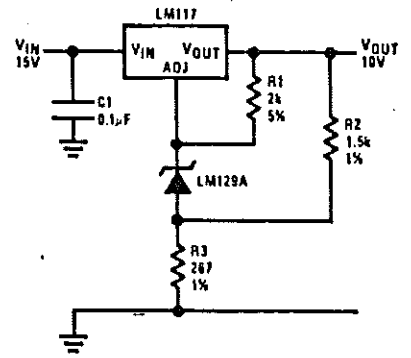


Adjustable Regulator with Improved Ripple Rejection

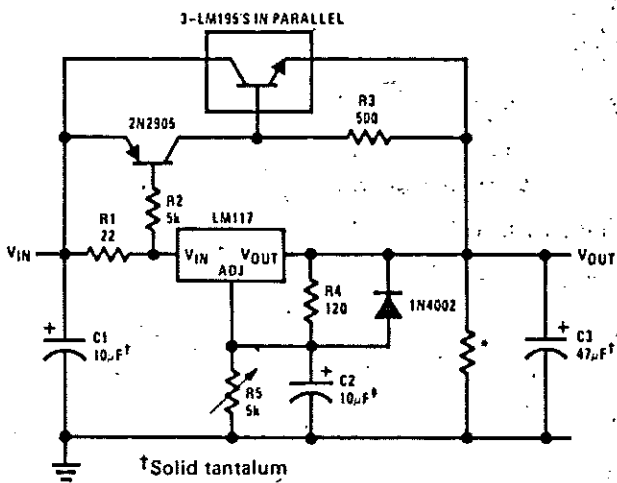


†Solid tantalum
*Discharges C1 if output is shorted to ground

High Stability 10V Regulator

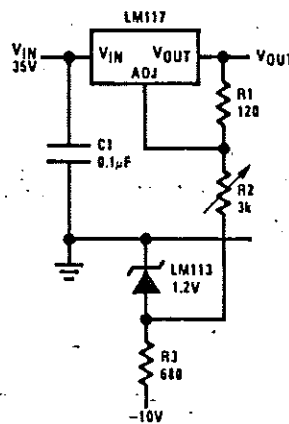


High Current Adjustable Regulator

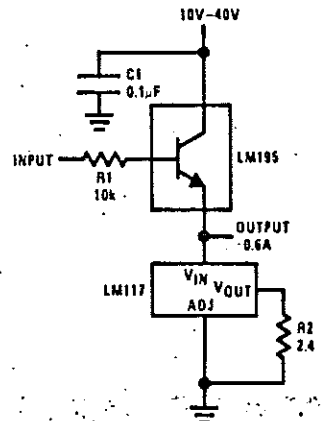


†Solid tantalum
*Minimum load current = 30 mA
‡Optional—improves ripple rejection

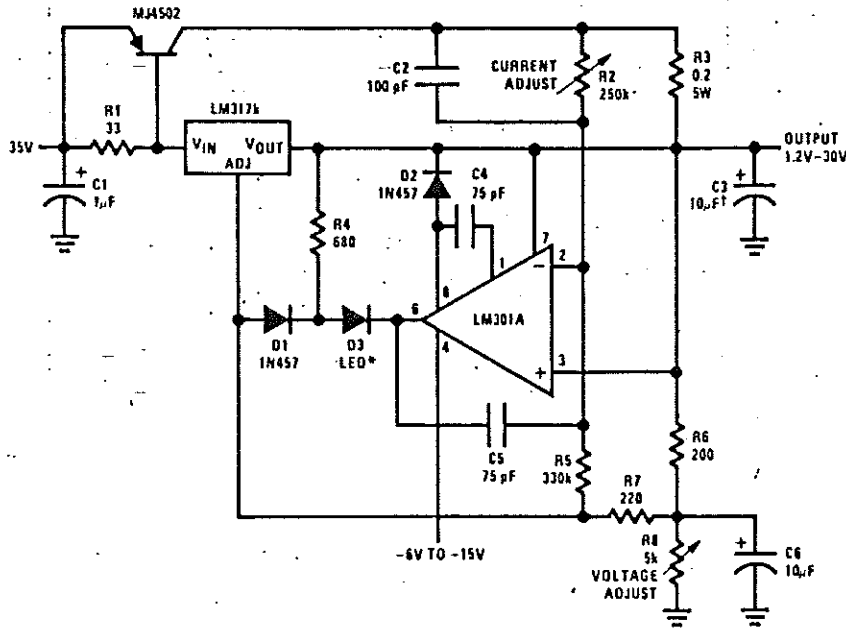
0 to 30V Regulator



Power Follower

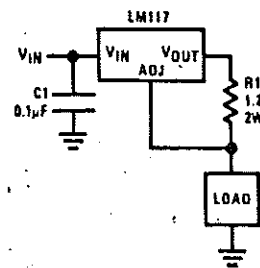


5A Constant Voltage/Constant Current Regulator

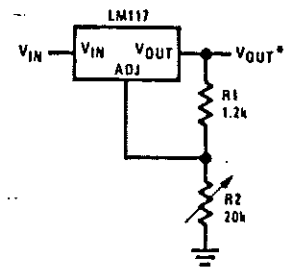


†Solid tantalum
*Lights in constant current mode

1A Current Regulator



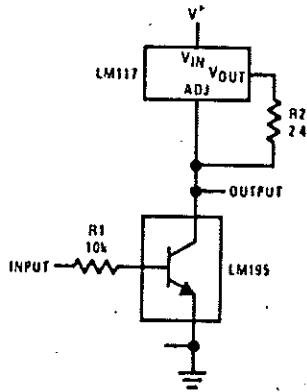
1.2V-20V Regulator with Minimum Program Current



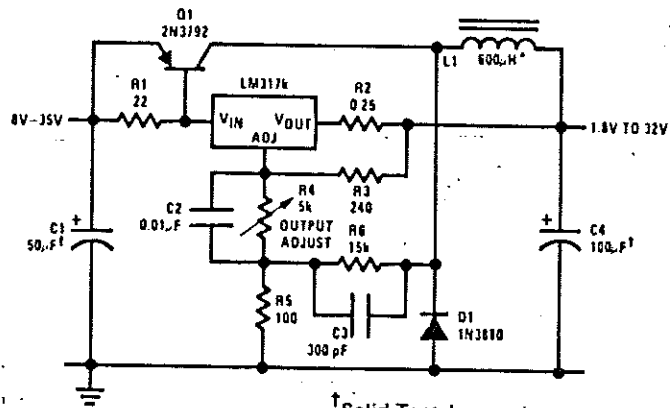
*Minimum load current ≈ 4 mA

Typical Applications (Continued)

High Gain Amplifier

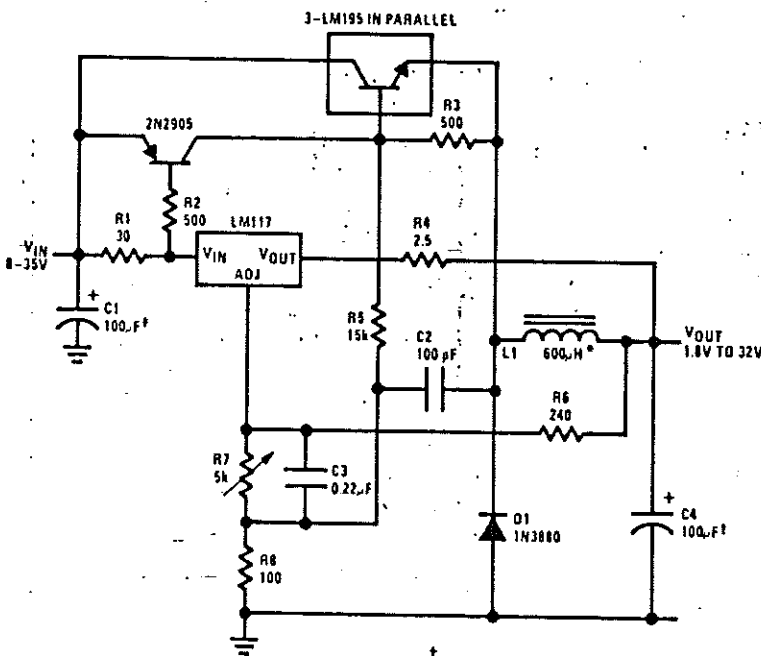


Low Cost 3A Switching Regulator



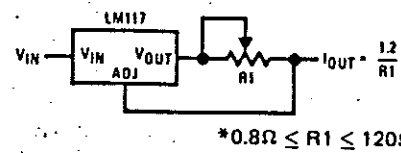
†Solid Tantalum
*Core—Arnold A-254168-2 60 turns

4A Switching Regulator with Overload Protection



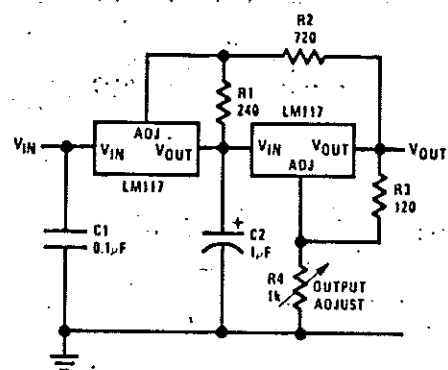
†Solid Tantalum
*Core Arnold A-254168-2 60 turns

Precision Current Limiter

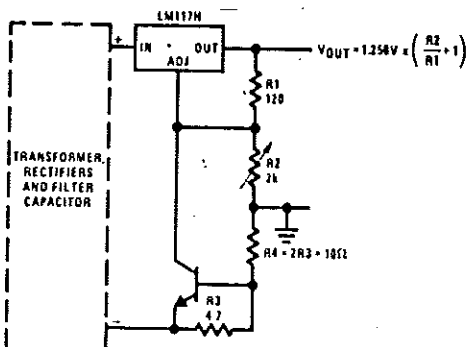


*0.8Ω ≤ R1 ≤ 120Ω

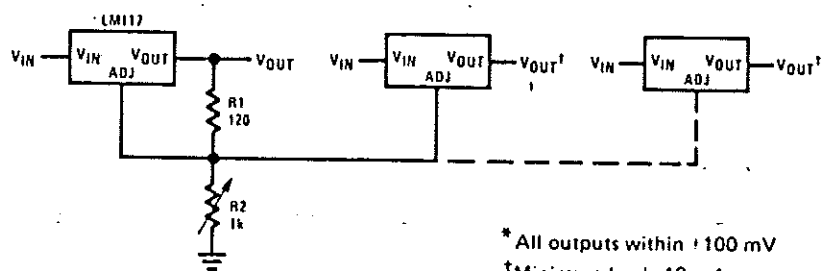
Tracking Preregulator



Adjustable Regulator with Current Limiter



Adjusting Multiple On-Card Regulators with Single Control*

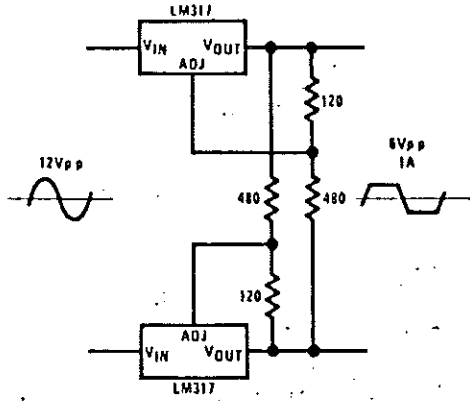


* All outputs within ±100 mV
† Minimum load—10 mA

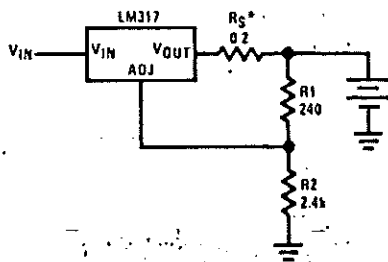
Short circuit current is approximately 600 mV/R3, or 120 mA (compared to LM117H's 1 ampere current limit)
At 50 mA output only 3/4V of drop occurs in R3 and R4

Typical Applications (Continued)

AC Voltage Regulator

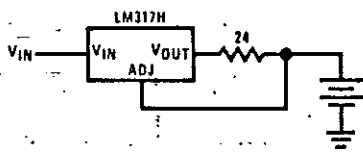


12V Battery Charger

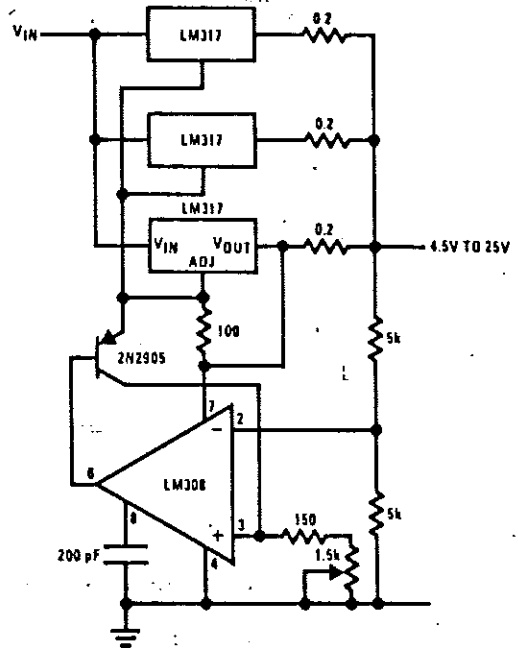


* R_s —sets output impedance of charger $Z_{OUT} = R_s \left(1 + \frac{R_2}{R_1} \right)$
 Use of R_s allows low charging rates with fully charged battery.

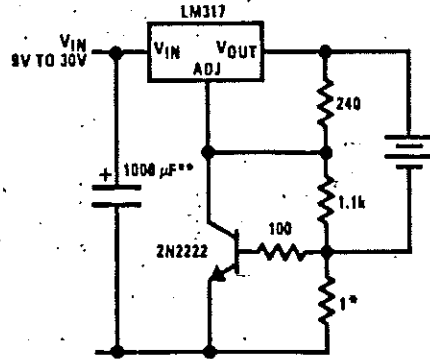
50 mA Constant Current Battery Charger



Adjustable 4A Regulator



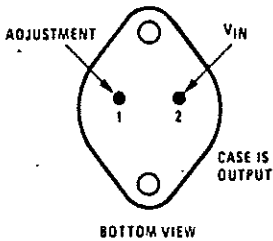
Current Limited 6V Charger



*Sets peak current (0.6A for 1 Ω)
 **1000 μF is recommended to filter out any input transients.

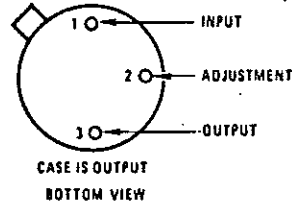
Connection Diagrams

(TO-3 Steel) Metal Can Package



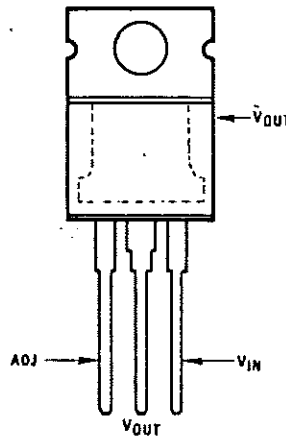
Order Number:
 LM117K STEEL
 LM217K STEEL
 LM317K STEEL
 See NS Package K02A

(TO-39) Metal Can Package



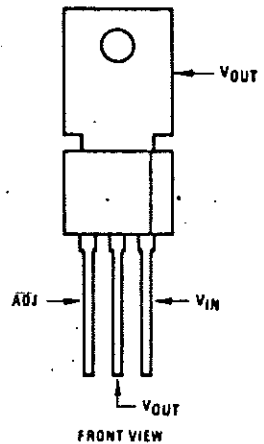
Order Number:
 LM117H
 LM217H
 LM317H
 See NS Package H03A

(TO-220) Plastic Package



Order Number:
 LM317T
 See NS Package T03B

(TO-202) Plastic Package



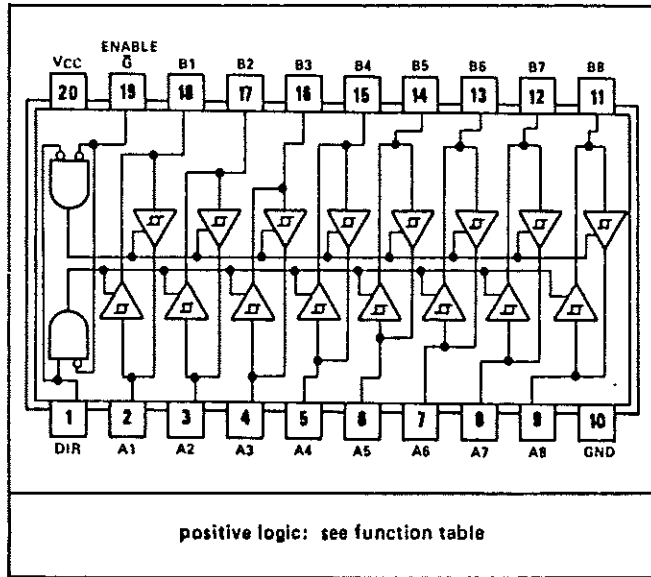
Order Number:
 LM317MP
 See NS Package P03A
 TAB Formed Devices
 LM317MP TB
 See NS Package P03E

TYPES SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612471, OCTOBER 1976

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns
- Typical Enable/Disable Times . . . 17 ns

SN54LS245 . . . J PACKAGE
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



TYPE	I _{OL} (SINK CURRENT)	I _{OH} (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

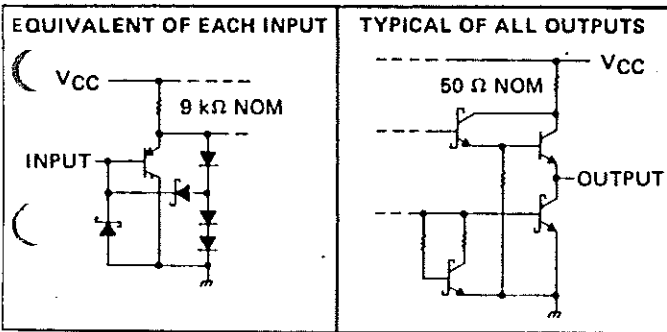
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS245 is characterized for operation from 0°C to 70°C .

schematics of inputs and outputs



FUNCTION TABLE

ENABLE \bar{G}	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS245	-55°C to 125°C
SN74LS245	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

7

DESIGN GOAL

This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

7-349

TYPES SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS245			SN74LS245			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$ $I_{OH} = -3 \text{ mA}$		2.4	3.4		2.4	3.4	V
		$I_{OH} = \text{MAX}$	2		2			
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$ $I_{OL} = 12 \text{ mA}$			0.4			0.4	V
		$I_{OL} = 24 \text{ mA}$					0.5	
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, \bar{G}$ at 2 V			10			10	μA
I_{OZL} Off-state output current, low-level voltage applied				-200			-200	
I_I Input current at maximum input voltage	A or B			0.1			0.1	mA
	Dir or \bar{G}	$V_{CC} = \text{MAX}$		0.1			0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_{IH} = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-0.2			-0.2	mA
I_{OS} Short-circuit output current††	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC} Supply current	Total, outputs high		48	70		48	70	mA
	Total, outputs low	$V_{CC} = \text{MAX},$ Outputs open	62	90		62	90	
	Outputs at Hi-Z		64	95		64	95	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

†† Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}, R_L = 667 \Omega, \text{ See Note 2}$		8	12	ns	
t_{PHL} Propagation delay time, high-to-low-level output			8	12	ns	
t_{pZL} Output enable time to low level				27	40	ns
t_{pZH} Output enable time to high level				25	40	ns
t_{pLZ} Output disable time from low level	$C_L = 5 \text{ pF}, R_L = 667 \Omega, \text{ See Note 2}$		15	25	ns	
t_{pHZ} Output disable time from high level			15	25	ns	

NOTE 2: Load circuit and waveforms are shown on page 3-11.

DESIGN GOAL

This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators

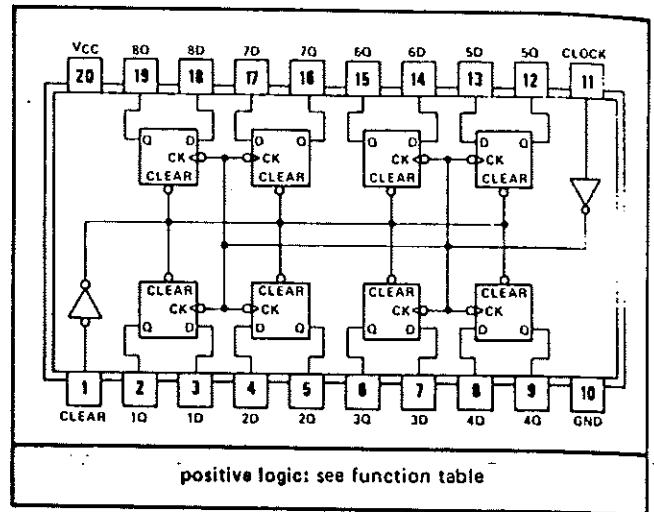
SN54273, SN54LS273 . . . J PACKAGE
SN74273, SN74LS273 . . . J OR N PACKAGE

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

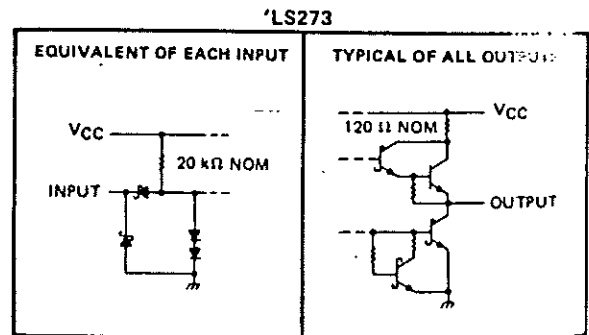
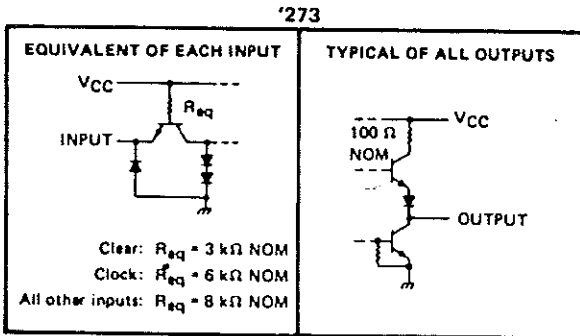


FUNCTION TABLE
(EACH FLIP-FLOP)

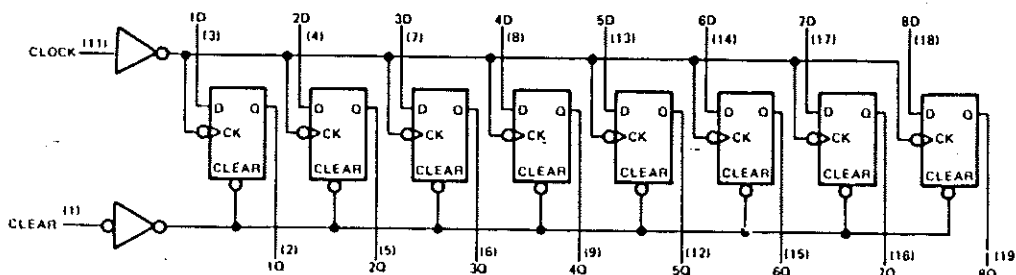
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

See explanation of function tables on page 3-8.

schematics of inputs and output



functional block diagram



TYPES SN54273, SN74273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54273	-55°C to 125°C
SN74273	0°C to 70°C
Storage temperature range	-65°C to 150°C

†E 1: Voltage values are with respect to network ground terminal.

Recommended operating conditions

	SN54273			SN74273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_w	16.5			16.5			ns
Set-up time, t_{su}	Data input			20†			ns
	Clear inactive state			25†			
Data hold time, t_h	5†			5†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

The arrow indicates that the rising edge of the clock pulse is used for reference.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	Clear			80	μ A
	Clock or D			40	
I_{IL} Low-level input current	Clear			-3.2	mA
	Clock or D			-1.6	
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		62	94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 3	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear		18	27		ns
t_{PLH} Propagation delay time, low-to-high-level output from clock		17	27		ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		18	27		ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54LS273, SN74LS273

OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS273	-55°C to 125°C
SN74LS273	0°C to 70°C
Storage temperature range	65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54LS273			SN74LS273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_w	20			20			ns
Set-up time, t_{su}	Data input	20†		20†			ns
	Clear inactive state	25†		25†			ns
Data hold time, t_h	5†			5†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS273		SN74LS273		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V_{IH} High-level input voltage		2			2	V	
V_{IL} Low-level input voltage				0.7		0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5		-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.35	0.5	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			0.1		0.1	mA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = -0.4 \text{ V}$			20		20	μ A
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$			-0.4		-0.4	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	-20	-100	-20	-100	-100	mA
		17	27	17	27	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
 NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 4}$	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

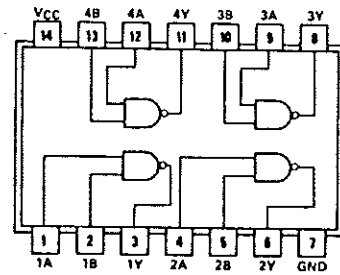
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
 $Y = \overline{AB}$

See page 6-4



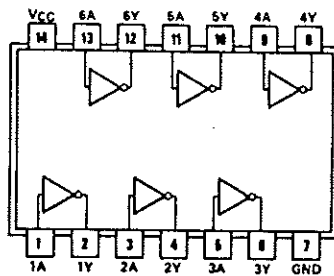
SN5403 (J)	SN7403 (J, N)
SN54L03 (J)	SN74L03 (J, N)
SN54LS03 (J, W)	SN74LS03 (J, N)
SN54S03 (J, W)	SN74S03 (J, N)

HEX INVERTERS

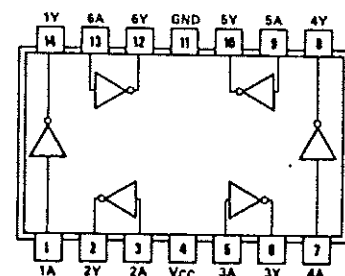
04

positive logic:
 $Y = \overline{A}$

See page 6-2



SN5404 (J)	SN7404 (J, N)
SN54H04 (J)	SN74H04 (J, N)
SN54L04 (J)	SN74L04 (J, N)
SN54LS04 (J, W)	SN74LS04 (J, N)
SN54S04 (J, W)	SN74S04 (J, N)



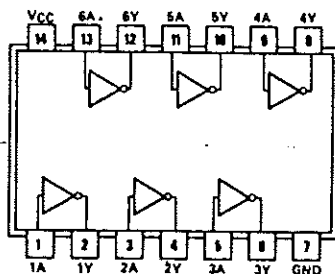
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

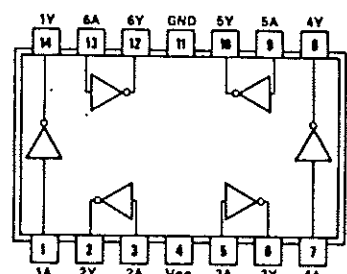
05

positive logic:
 $Y = \overline{A}$

See page 6-4



SN5405 (J)	SN7405 (J, N)
SN54H05 (J)	SN74H05 (J, N)
SN54LS05 (J, W)	SN74LS05 (J, N)
SN54S05 (J, W)	SN74S05 (J, N)



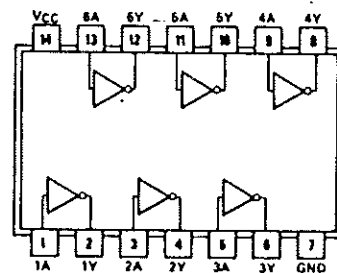
SN5405 (W)
SN54H05 (W)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

06

positive logic:
 $Y = \overline{A}$

See page 6-24



SN5406 (J, W)	SN7406 (J, N)
---------------	---------------

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54' SERIES 74'												UNIT
		'06, '07			'16, '17			'26			'33, '38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, VCC	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V
High-level output voltage, VOH		30												V
Low-level output current, IOL	54 Family 74 Family	30			30			40			16			48 mA
Operating free-air temperature, TA	54 Family 74 Family	-55			-55			-55			-55			125 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54' SERIES 74'												UNIT
			'06, '07			'16, '17			'26			'33, '38			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH} High-level input voltage	1, 2		2												V
V _{IL} Low-level input voltage	1, 2		0.8												V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = -12 mA	-1.5												V
I _{OH} High-level output current	1	V _{CC} = MIN, V _I = Δ	250			250			1000			250			μA
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = Δ	0.4			0.4			0.4			0.4			V
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V	1												1 mA
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V	40												40 μA
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.4 V	-1.6												-1.6 mA
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page												mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Δ The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5V, T_A = 25^\circ C$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		TYP	MAX	TYP	MAX
'06, '16	$C_L = 15 pF, R_L = 110 \Omega$	10	15	15	23
'07, '17		6	10	20	30
'26	$C_L = 15 pF, R_L = 1 k\Omega$	16	24	11	17
'33	$C_L = 50 pF, R_L = 133 \Omega$	10	15	12	18
	$C_L = 150 pF, R_L = 133 \Omega$	15	22	16	24
'38	$C_L = 45 pF, R_L = 133 \Omega$	14	22	11	18

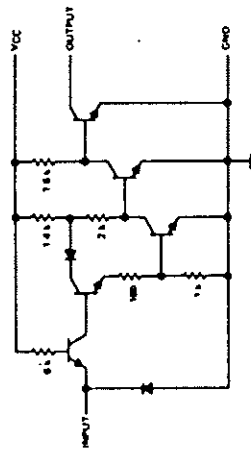
Load circuit and voltage waveforms are shown on page 3-10.

supply current

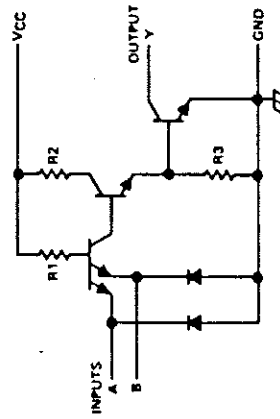
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	TYP	MAX	Total with outputs high	Total with outputs low	Average per gate (50% duty cycle)	TYP
'06, '16	30	48	32	51	5.17	
'07, '17	29	41	21	30	4.17	
'26	4	8	12	22	2.00	
'33	12	21	33	57	5.63	
'38	5	8.5	34	54	4.88	

† Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.

schematics (each gate)

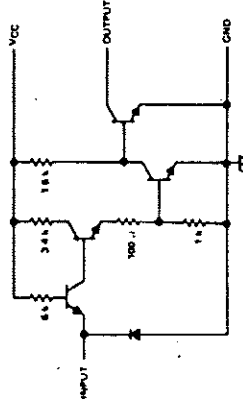


'06, '16 CIRCUITS

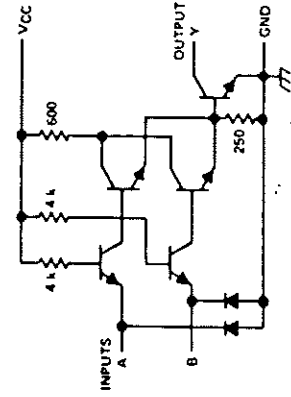


CIRCUITS	R1	R2	R3
'26	4 k Ω	1.6 k Ω	1 k Ω
'38	4 k Ω	600 Ω	400 Ω

'26, '38 CIRCUITS



'07, '17 CIRCUITS



'33 CIRCUITS

Defaultvärden

Defaulttabellen för tangenterna är följande:

	A	B	C	D	E	F	G	H
1	0	B	E	H	P	X	e	h
2	1	9	A	I	Q	Y	a	i
3	2	:	B	J	R	Z	b	j
4	-3	:	C	K	S	A	c	k
5	4	<	D	L	T	b	d	l
6	5	=	E	M	U	A	e	m
7	6	>	F	N	V	Ü	f	n
8	7	?	G	O	W	_	g	o

samtliga repetitionstider är satta till ca 0.1 sek.

Start till autorepetitions början ca 0.6 sek
 Kontaktsudselimination ca 0.02

För att ändra dessa värden, får man gå in i modulen rejinit. (se appendix C)

För den seriella kommunikationen finns som default överföringen 9600 Baud, 1 stopbit, ingen paritet. Värdena för detta samt värdet för klockan (default ca 100 anrop per sek) finns i modulen initsio. För närmare information refereras till de mer utförliga kommentarerna i programlistan. (appendix C, modul initsio.)